A Self-Bias-Flip with Charge Recycle Interface Circuit with No External Energy Reservoir for Piezoelectric Energy Harvesting Array

Li, Zhen; Chen, Zhiyuan; Wang, Jing; Wang, Jiawei; Jiang, Junmin; Du, Sijun; Cheng, Xu; Zeng, Xiaoyang; Han, Jun

DOI
10.1109/TPEL.2023.3286399

Publication date
2023

Document Version
Final published version

Published in
IEEE Transactions on Power Electronics

A Self-Bias-Flip With Charge Recycle Interface Circuit With No External Energy Reservoir for Piezoelectric Energy Harvesting Array

Zhen Li, *Student Member, IEEE*, Zhiyuan Chen, *Member, IEEE*, Jing Wang, Jiawei Wang, Junmin Jiang, *Member, IEEE*, Sijun Du, *Senior Member, IEEE*, Xu Cheng, Xiaoyang Zeng, *Senior Member, IEEE*, and Jun Han, *Member, IEEE*

***Abstract*—This article presents a piezoelectric energy harvesting (PEH) interface circuit using a new self-bias-flip with the charge recycle (SBFR) technique without employing any additional energy reservoir. Traditional designs, including synchronous-switch harvesting on inductor (SSHI), synchronous-switch harvesting on capacitor (SSHC), synchronous electric charge extraction (SECE), etc., require additional capacitors or inductors to reverse the voltage on the PEH at the zero-crossing point. This design innovatively uses the inherent capacitors of the piezoelectric harvesters as the flipping capacitors. In order to improve the extract efficiency of the interface, the zero-crossing state is split into a charge recycle stage and a voltage-flip stage. For a piezoelectric array with 2^n PEHs, a configuration with (n-1) phases in the charge recycle stage is adopted to reduce the loss caused by direct charge neutralization. The charge redistribution loss is reduced by employing (2n+1) phases in the voltage-flip stage. The proposed principle has been implemented with discrete components and is verified by three different prototypes. The measurement results show that a flipping efficiency of 67% is achieved by utilizing SBFR with four PEHs. And the proposed interface can provide up to 5.2x improvement when compared with the full-bridge rectifier (FBR).**

***Index Terms*—Energy harvesting, maximum output power improving rate (MOPIR), multiple input, piezoelectric energy harvester (PEH), self-bias-flip, synchronous-switch harvesting on inductor (SSHI).**

Manuscript received 7 December 2022; revised 5 April 2023; accepted 8 June 2023. Date of publication 15 June 2023; date of current version 28 July 2023. This work was supported in part by the National Natural Science Foundation of China under Grants 62004041 and 62104093, in part by the Major Scientific and Technological Innovation Projects of Shanghai Municipal Education Commission under Grant 2017-01-07-00-07-E00026, and in part by the National Key Research and Development Program of China under Grants 2018YFB2202400 and 2018YFB2202404. Recommended for publication by Associate Editor B. Semail. *(Corresponding author: Zhiyuan Chen.)*

Zhen Li, Zhiyuan Chen, Jing Wang, Jiawei Wang, Xu Cheng, Xiaoyang Zeng, and Jun Han are with the State-Key Laboratory of ASIC and System, Fudan University, Shanghai 201203, China (e-mail: zhenli19@fudan.edu.cn; chen_zy@fudan.edu.cn; 20112020078@fudan.edu.cn; 20112020123@fudan.edu.cn; chengxu@fudan.edu.cn; xyzeng@fudan.edu.cn; junhan@fudan.edu.cn).

Junmin Jiang is with the Department of Electronic and Electrical Engineering, Southern University of Science and Technology, Shenzhen 518055, China (e-mail: jjiangah@connect.ust.hk).

Sijun Du is with the Department of Microelectronics, Delft University of Technology, 2628, CD Delft, Netherlands (e-mail: sijun.du@tudelft.nl).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3286399.

Digital Object Identifier 10.1109/TPEL.2023.3286399

I. Introduction

With the emergence of the Internet-of-Things (IoT) era, sensor nodes are required in almost all fields such as manufacturing, medical care, and security to achieve a better interaction between humans and the environment. The characteristics of sensors include small size, long working life, remote placement [1], and high disassembly cost, which cause power supply difficulties. The emergence of energy harvesting technology is expected to solve this problem [2]. The popular ambient energy sources include solar, thermal, and various vibrations in the environment. Compared to other sources, piezoelectric energy harvesters (PEHs) have the advantages of high energy density [3], easy scalability, and high output voltage [4]. Thus, research projects involving PEH have been a point of interest.

The commonly used PEH adopts a cantilever structure. One end of the beam is fixed to the base, and the free end usually carries a proof mass to adjust the resonance frequency and enhance the output power [5], [6], [7]. The cantilever vibrates under an external kinetic force and converts the deformation into a potential difference based on the piezoelectric effect. However, the output of the PEH is an ac voltage whose amplitude varies with the vibration intensity. Thus, an interface is required to rectify the PEH's output for the dc load. The full-bridge rectifier (FBR) is widely used as an interface for the advantages of simple implementation and stable performance, as shown in Fig. 1(a) [8]. When the PEH electromechanical coupling is relatively weak, the equivalent electrical model of PEH is usually simplified as an inherent capacitance C_P in parallel with the ac current source I_P. In the process of energy harvesting, the polarity of I_P changes periodically, which leads to repeated charging and discharging of C_P resulting in energy loss. In view of this, researchers have proposed three popular solutions: synchronous-switch harvesting on inductor (SSHI) [9], [10], [11], [12], [13], synchronous-switch harvesting on capacitor (SSHC) [14], [15], [16], [17], and synchronous electric charge extraction (SECE) [18], [19], [20], [21], [22], [23].

The principle of SSHI/C technique is shown in Fig. 1(b). At the zero-crossing point, the charge on C_P is flipped to the other side efficiently with the aid of external energy reservoirs, so that the polarity of the C_P's voltage and I_P are always kept in the same direction. The voltage-flip operation makes

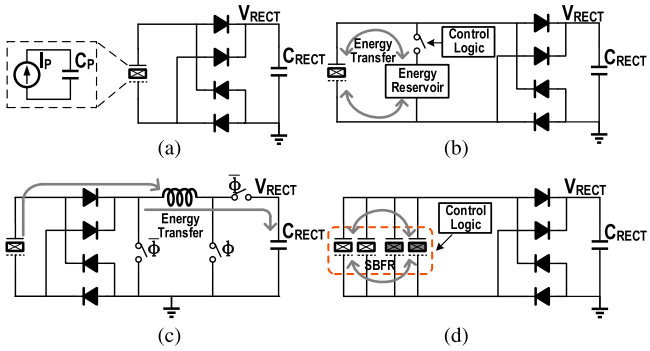


Fig. 1. Structure of the conventional and proposed interface: (a)FBR; (b)SSHI/C; (c)SECE; (d)Proposed SBFR.

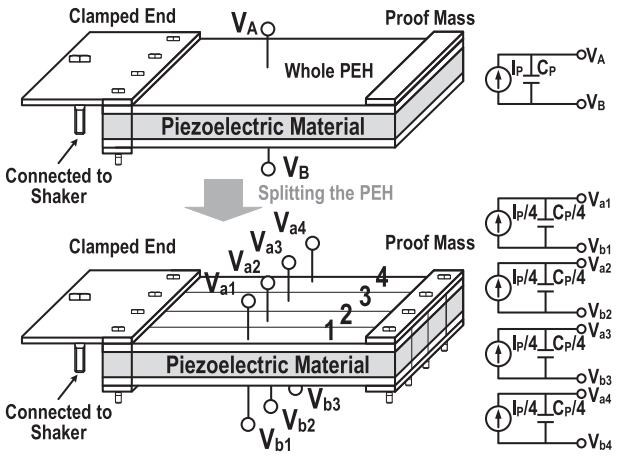


Fig. 2. Splitting the monolithic electrode of a PEH into a 4-input array.

the charge accumulated on the C_P reused, which significantly improves the energy extraction efficiency. The basic structure of SECE is shown in Fig. 1(c). During the nonzero-crossing time, I_P continues to charge C_P. When I_P crosses zero, the harvested energy is first transferred to the inductor by the *LC* loop composed of the inductor and the C_P, and then the inductor and C_{RECT} constitute a new *LC* loop to transfer the energy to the load. Besides, there are various hybrid schemes such as SSHIC, SICE, etc., [24], [25], [26], [27], [28]. All of the above schemes inevitably use the extra energy reservoirs to achieve highly efficient energy extraction. However, employing the passive elements (capacitors and inductors) not only decreases the power density of the system, but also contradicts the trend of miniaturization in the IoT era.

In this article, we attempt to avoid using additional capacitors and inductors for voltage flipping at the cost of array self-flipping. As shown in Fig. 2, the PEH array is implemented by splitting the monolithic electrode of a PEH into several mechanically connected piezoelectric elements, with independent electrical terminals. Two novel techniques, the self-bias-flip (SBF) and the self-bias-flip with charge recycle (SBFR), based on piezoelectric array input are proposed. Different from the traditional piezoelectric energy multiinput systems [29], [30], where each PEH is only used as a power supply, this scheme uses part of the inherent capacitators in the PEH array as the

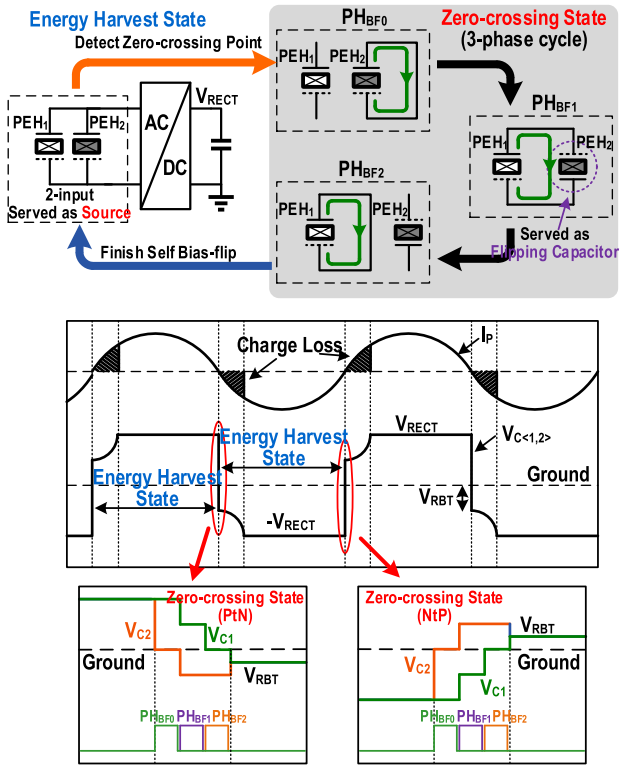


Fig. 3. Operation of the proposed SBF_2 technique.

flipping capacitors during the zero-crossing time of I_P as shown in Fig. 1(d). Three prototypes, the SBF_2, SBF_4, and $SBFR_4$ with 3, 5, and 6 phases, respectively, are implemented using discrete components to validate the effectiveness of our proposed topology. In addition, a general version of a 2^n-input SBFR interface circuit with 3n phases is proposed and analyzed theoretically. Compared to the conventional SSHI, SSHC, and SECE techniques, the proposed interface circuits can extract piezoelectric energy efficiently without the aid of additional passive energy storage elements. The rest of this article is organized as follows. Section II aims at introducing the proposed SBF_2, SBF_4 and $SBFR_4$ as examples and conducts theoretical analysis and simulation verification. Section III derives and summarizes the general topological transformation of SBFR based on 2^n input and provides the trend of performance when the input nodes scale increases. In order to experimentally validate the concept, Section IV carries out the test verification of the proposed SBFR piezoelectric energy harvesting interface. Finally, Section V concludes this article.

II. Proposed SBF and SBFR Technique

A. Proposed SBF Technique Based on 2-Input (SBF_2)

Fig. 3 shows the basic form SBF_2 that utilizes two input PEHs ($PEH_{<1,2>}$) and transforms in 3 phases ($PH_{BF<0,2>}$) during the zero-crossing time of I_P. SBF_2 operates in two states, including energy harvesting state and zero-crossing state. In the energy harvesting state, PEH_1 and PEH_2 are parallel to serve as energy sources and followed by a rectifier to extract power. Under

periodic excitement, the peak values of the equivalent ac current of PEH_1 and PEH_2 are I_{P1} and I_{P2}, respectively. Since the free ends of the two PEHs are tightly fixed on the same mass, their phases and currents are exactly the same (e.g., $I_{P1} = I_{P2} = I_P$). When the current $I_{P\langle 1,2\rangle}$ crosses zero, the interface enters the voltage-flip stage. During this stage, the inherent capacitor of PEH_2 is used as the flipping capacitor, which is filled with gray in Fig. 3. Considering the direction of PEH will change during the bias-flip process, the positive terminal of PEH is represented by a solid line, while the negative terminal of PEH is represented by a dotted line. In order to quantitatively analyze the circuit's performance, the theoretical derivation will be carried out in the following content.

C_P is the inherent capacitance of the whole piezoelectric material, and it is divided into two parts, PEH_1 and PEH_2. In order to obtain the optimal ratio of PEH_1 and PEH_2, it is assumed that the inherent capacitance of $PEH_1(PEH_2)$ is $C_{P1}(C_{P2})$, where $C_{P1} + C_{P2} = C_P$, and $C_{P1} = m \times C_{P2}$. The SBF_2 operates as follows. First, entering the PH_{BF0} phase, the ports of PEH_2 are shorted and the charge is cleared to zero. At this time, the voltages V_{C1} and V_{C2} across the PEH_1 and PEH_2 are

$$V_{C1} = V_{RECT} \quad V_{C2} = 0 \tag{1}$$

where V_{RECT} is the voltage at the output of the rectifier. The inherent capacitance C_{P2} of PEH_2 will act as a flipping capacitor after clearing the charge. The interface circuit enters the PH_{BF1} phase, PEH_1 and PEH_2 are switched to parallel connection, and the charge accumulated on C_{P1} is partially transferred to C_{P2} through charge sharing

$$|V_{C1}| = |V_{C2}| = \frac{C_{P1}}{C_{P1} + C_{P2}} \cdot V_{RECT}. \tag{2}$$

When completing the charge sharing, it enters PH_{BF2} phase to clear the residual charge on C_{P1}, resulting in

$$V_{C1} = 0 \quad |V_{C2}| = \frac{C_{P1}}{C_{P1} + C_{P2}} \cdot V_{RECT}. \tag{3}$$

After finishing the voltage-flip, the interface returns to the energy harvest state, and PEH_1 and PEH_2 are connected in parallel again. The voltage polarities of V_{C1}/V_{C2} and I_P turn to identical. The rebuilt voltage V_{RBT} is equal to

$$|V_{RBT}| = \frac{C_{P1} \cdot C_{P2}}{(C_{P1} + C_{P2})^2} \cdot V_{RECT}. \tag{4}$$

Based on the rebuilt voltage, the charge loss $Q_{0.5lost}$ during the entire flipping process is

$$Q_{0.5lost} = \frac{(C_{P1} + C_{P2})^2 - C_{P1} \cdot C_{P2}}{C_{P1} + C_{P2}} \cdot V_{RECT}. \tag{5}$$

Meanwhile, the total charge $Q_{0.5cy}$ generated by $PEH_{<1,2>}$ in each half cycle is

$$Q_{0.5cy} = 2 \cdot (C_{P1} + C_{P2}) \cdot V_P \tag{6}$$

where V_P is the peak of $PEH_{1/2}$ open circuit voltage

$$V_P = \frac{I_P}{\omega_P \times C_P} \tag{7}$$

where $\omega_P = 2\pi f_P$ and f_P is the frequency with which the PEH is excited. The output power P_{RECT} during one period can be expressed as follows:

$$P_{RECT} = (Q_{0.5cy} - Q_{0.5lost}) \cdot V_{RECT} \cdot 2f_P \tag{8}$$

substitute (5)–(7) into (8), the P_{RECT} can be calculated as

$$P_{RECT} = [2 \cdot C_P \cdot V_P - \frac{(m+1)^2 - (m+1) + 1}{(m+1)^2} \cdot C_P \cdot V_{RECT}] \cdot V_{RECT} \cdot 2f_P. \tag{9}$$

Substituting $k = m + 1$ into (9)

$$P_{RECT} = [2 \cdot V_P - \frac{k^2 - k + 1}{k^2} \cdot V_{RECT}] \cdot V_{RECT} \cdot C_P \cdot 2f_P. \tag{10}$$

By differentiating (10) with respect to V_{RECT} and equating the result to zero, the PEH voltage at maximum power point for SBF_2 can be obtained as

$$V_{RECT} = \frac{k^2}{(k^2 - k + 1)} \cdot V_P. \tag{11}$$

By substituting (11) into (10), we can obtain the maximum power of the SBF_2 as

$$P_{RECT,MAX} = \frac{2 \cdot k^2}{k^2 - k + 1} \cdot V_P^2 \cdot C_P \cdot f_P. \tag{12}$$

Maximum output power improving rate (MOPIR) is commonly used for performance evaluation when analyzing piezoelectric interface circuits, which is defined as the ratio of the maximum extract power of the interface to the FBR maximum output at the same vibration level [2] (e.g., MOPIR=$P_{RECT,MAX}$/$P_{FBR,MAX}$)

$$P_{FBR,MAX} = C_P \times V_P^2 \times f_P. \tag{13}$$

Hence, the MOPIR is equal to

$$MOPIR = \frac{2 \cdot k^2}{k^2 - k + 1} \quad (k > 1). \tag{14}$$

According to formula (14), we draw the curve of MOPIR with respect to k under SBF_2 in Fig. 4. With the increase of k, MOPIR gradually increases and reaches the peak value of 2.66x when $C_{P1} = C_{P2}$. However, when $C_{P1} < C_{P2}$, the MOPIR gradually decreases due to charge clearing in the PH_{BF0} phase. In contrast, if $C_{P1} > C_{P2}$, the residual charge in PH_{BF2} will reduce energy efficiency significantly. Hence, in the following analysis and implementation, the input used as flipping capacitors accounts for half of the total inputs in order to obtain the maximum MOPIR.

B. Proposed SBF Technique Based on 4-Input (SBF_4)

The previous discussion shows that SBF_2 can improve the MOPIR by 33% compared with switch only rectifier (SOR) [2]. However, there are only three phases in SBF_2, which result in large charge redistribution loss so as to limit the improvement of MOPIR. In order to reduce the charge redistribution loss, it is necessary to split PEH into more units to extend the phase

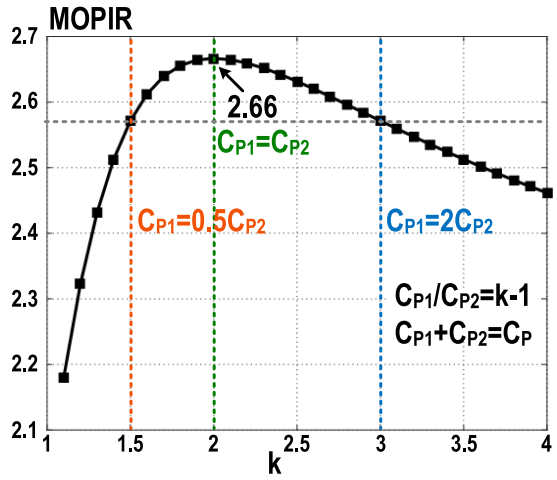


Fig. 4. Relationship between MOPIR and C_{P1}/C_{P2} in SBF_2.

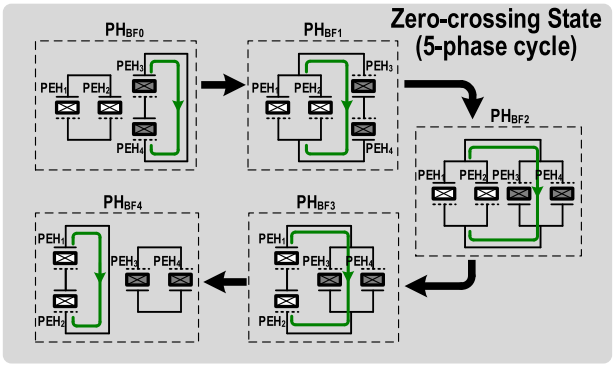


Fig. 5. Zero-crossing state of the proposed SBF_4.

number during the voltage-flip stage. More phases aim to reduce voltage difference before charge sharing so as to obtain a higher MOPIR. Fig. 5 shows the SBF_4 that utilizes four input PEHs ($PEH_{<1,4>}$) and transforms in five phases ($PH_{BF<0,4>}$) during the zero-crossing time of I_P. The equivalent ac current of $PEH_{<1,4>}$ in this structure are exactly the same by default, and their respective inherent capacitors $C_{P<1,4>}$ are also equal (e.g., $C_{P1} = C_{P2} = C_{P3} = C_{P4} = 0.25C_P$). Accomplishing the voltage-flip, the rebuilt voltage is

$$V_{RBT} = \frac{9}{25} \cdot V_{RECT}. \tag{15}$$

Similar to (11) and (12), we can calculate the maximum output when $V_{RECT} = \frac{25}{16} \cdot V_P$

$$P_{RECT,MAX} = \frac{25}{8} \cdot V_P^2 \cdot C_P \cdot f_P. \tag{16}$$

According to (13) and (16), the MOPIR is equal to 3.12x, which is about 17.3% higher than SBF_2. It shows that dividing the PEH into more input units to increase the phase number in voltage-flip stage is helpful to reduce charge redistribution loss. As a result, the MOPIR will be improved significantly.

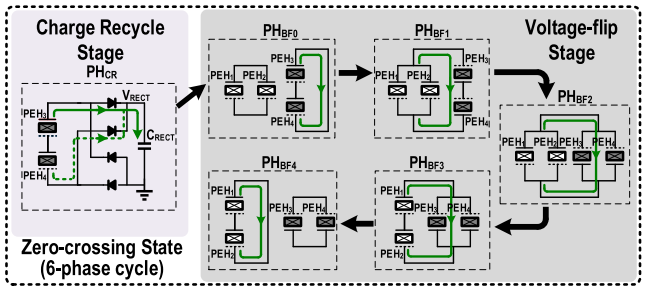


Fig. 6. Zero-crossing state of the $SBFR_4$.

C. Proposed SBFR Technique Based on 4-Input ($SBFR_4$)

Increasing the flipping phases can reduce the charge redistribution loss but is incapable of decreasing the energy waste caused by charge clearing in the PH_{BF0} phase. In order to effectively take advantage of the charge on $PEH_{<3,4>}$ to improve MOPIR, $SBFR_4$ is proposed to further improve harvesting efficiency from SBF_4. Fig. 6 shows the $SBFR_4$ that utilizes four input PEHs ($PEH_{<1,4>}$) and transforms in six phases (PH_{CR}, $PH_{BF<0,4>}$) during the zero-crossing time of I_P. The difference between $SBFR_4$ and SBF_4 lies in the charge recycle stage in the zero-crossing state. SBF_4 discards all charges on the $PEH_{<3,4>}$ in order to employ it as a flipping capacitor. This operation leads to 50% charge of input being wasted. However, the $SBFR_4$ divides the zero-crossing state into two stages: charge recycle stage and voltage-flip stage. The inherent capacitors of gray filled $PEH_{<3,4>}$ are used as the flipping capacitors. In the charge recycle stage, through connecting $PEH_{<3,4>}$ in series, half of the charge on $PEH_{<3,4>}$ can be output to C_{RECT} so as to reduce the waste due to charge clearing. The operation of $SBFR_4$ is as follows. When I_P crosses zero, the interface first enters the PH_{CR} phase. During PH_{CR} phase, $PEH_{<3,4>}$ are connected in series to transfer power to the load. The contribution of PH_{CR} phase to the average power transferred to C_{RECT} over a time period of vibration can be expressed as

$$\begin{aligned} P_{RECT,CR} &= C_{SERI} \cdot (2 \cdot V_{RECT} - V_{RECT}) \cdot V_{RECT} \cdot 2f_P \\ &= \frac{1}{8} \cdot C_P \cdot V_{RECT}^2 \cdot 2f_P \end{aligned} \tag{17}$$

where C_{SERI} is the series capacitance of C_{P3} and C_{P4}. The voltage-flip process of $SBFR_4$ from PH_{BF0} to PH_{BF4} is the same as SBF_4 and the output power $P_{RECT,VF}$ during this period is

$$P_{RECT,VF} = \left[2 \cdot C_P \cdot V_P - \frac{16}{25} \cdot C_P \cdot V_{RECT}\right] \cdot V_{RECT} \cdot 2f_P. \tag{18}$$

By summing (17) and (18), we can calculate that the total output P_{RECT} of one $SBFR_4$ cycle is

$$P_{RECT} = C_P \cdot f_P \cdot \left[4 \cdot V_P \cdot V_{RECT} - \frac{103}{100} \cdot V_{RECT}^2\right]. \tag{19}$$

Similar to (11) and (12), when $V_{RECT} = \frac{200}{103} \cdot V_P$, P_{RECT} attains the maximum power $P_{RECT,MAX}$

$$P_{RECT,MAX} = \frac{400}{103} \cdot V_P^2 \cdot C_P \cdot f_P. \tag{20}$$

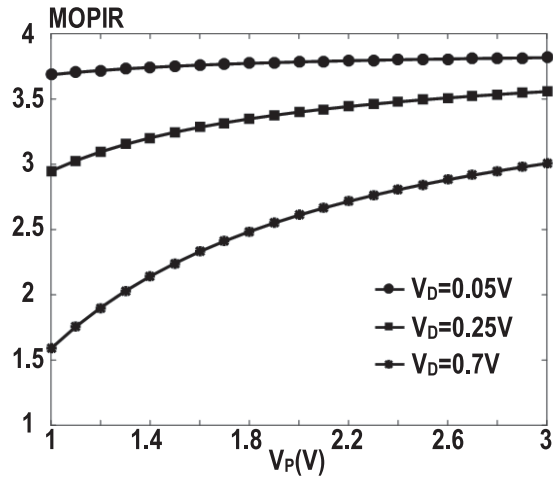


Fig. 7. Relationship between the MOPIR and V_P for $V_D = 0.05$ V, 0.25 V, and 0.7 V of $SBFR_4$.

The calculation shows that without the aid of extra energy reservoirs, the output power enhancement of $SBFR_4$ can reach up to 3.88x, which is 46% higher than that of the SBF_2, and 24% improvement over SBF_4. In the above calculations, the diodes are assumed to be ideal devices. But the influence of diode's forward voltage V_D cannot be ignored. When considering V_D, the total output power $P_{RECT,PRAC}$ of one $SBFR_4$ cycle is

$$P_{RECT,PRAC} = C_P \cdot f_P \cdot \left[\left(4 \cdot V_P - \frac{206}{100} \cdot V_D \cdot V_{RECT} - \frac{103}{100} \cdot V_{RECT}^2\right)\right]. \quad (21)$$

According to (13) and (21), the MOPIR is derived to be

$$MOPIR = \frac{\left[\left(4 \cdot V_P - \frac{206}{100} \cdot V_D\right) \cdot \left(\frac{200}{103} \cdot V_P - V_D\right)\right]}{V_P^2} - \frac{\frac{103}{100} \cdot \left(\frac{200}{103} \cdot V_P - V_D\right)^2}{V_P^2}. \quad (22)$$

As can be seen from the formula (22), MOPIR is related to both V_P and V_D, where V_P is proportional to the vibration level, and V_D is related to the type of diode. When employing active diodes, V_D can be limited within 100 mV; and the V_D of Schottky diodes are usually about 0.25 V. If using standard diodes, the classical value of V_D is about 0.7 V. The above mentioned three typical values of V_D are selected for scanning, and the trend of MOPIR is shown in Fig. 7. It can be seen that the actual value of MOPIR approaches the theoretical maximum value in the case of larger excitation intensity and smaller V_D.

In order to verify the above calculation results, we simulated $SBFR_4$ with the Cadence Virtuoso software. In the simulation, the frequency of I_P is 200 Hz, $C_{P\langle 1,4\rangle} = 22$ nF and $V_P = 2$ V, and the diodes employ the ideal model with threshold equal to 0 V. Fig. 8 depicts the waveforms of the voltages across $PEH_{1/2}(PEH_{3/4})$ during operation and the zoomed-in view of the zero-crossing state waveform. With the arrival of the zero-crossing time, the circuit first enters the PH_{CR} phase, half of the

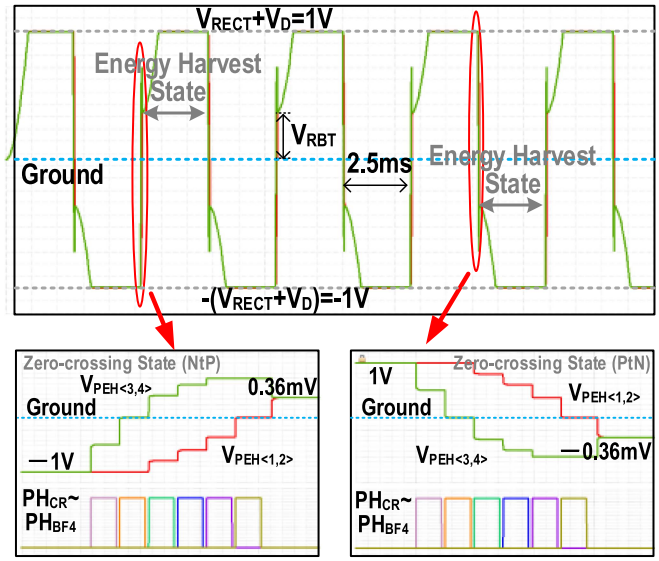


Fig. 8. Simulation waveforms of the $SBFR_4$.

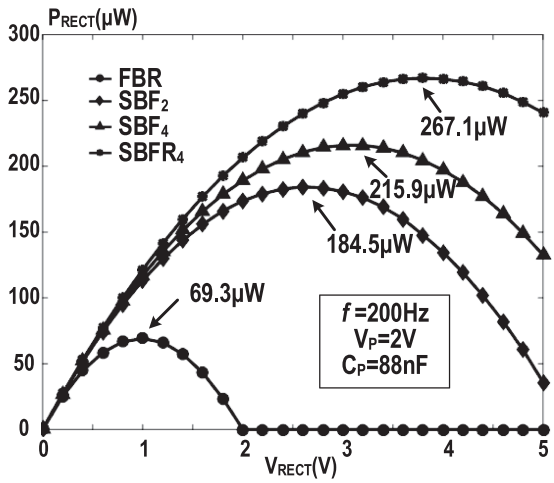


Fig. 9. Simulation results of P_{RECT} versus V_{RECT} for the structure of SBF_2, SBF_4, $SBFR_4$, and FBR.

charge on $PEH_{\langle 3,4\rangle}$ is transferred to the C_{RECT}, and the value of $V_{PEH<3,4>}$ are simultaneously reduced to $0.5V_{RECT}$. Then the interface turns into the voltage-flip stage. In PH_{BF0}, the charge on $PEH_{\langle 3,4\rangle}$ is first cleared, and then the absolute value of the voltage on $C_{P<3,4>}$ gradually increases due to charge transfer. Meanwhile, the absolute voltage on $C_{P<1,2>}$ is progressively reduced due to charge sharing and is cleared at the PH_{BF4} phase. When the interface circuit returns to the energy harvest state again, the rebuilt voltage is $0.36V_{RECT}$. The simulation results are consistent with the theoretical calculations, which verify the feasibility of the scheme.

Fig. 9 shows the simulated P_{OUT} comparison among an ideal FBR and the three interface circuits mentioned above. Note that the piezoelectric devices considered for simulation have different structures, depending on the number of elements with independent electrical terminals needed, but the resonance frequency and the total amount of piezoelectric material are the

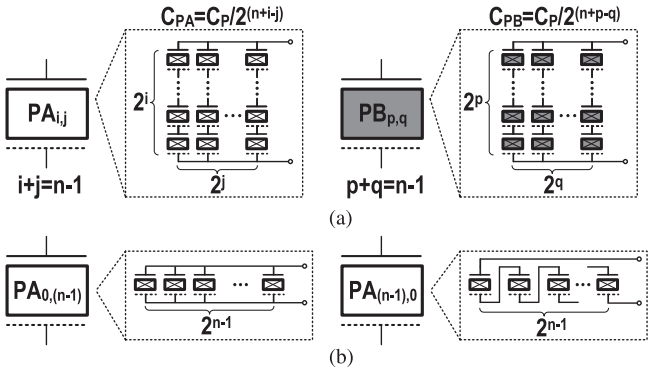


Fig. 10. In the proposed SBFR$_z$. (a) Structure of 2^n-input array. (b) Connection examples for PA$_{i,j}$.

same. The maximum output power of the SBF $_2$ is 184.5 μW, and the corresponding MOPIR is about 2.66x. Employing the SBFR $_4$ can improve the maximum power up to 267.1 μW, which achieves a MOPIR of 3.88x compared with ideal FBR. The theoretical output power of SBFR $_4$ is 1.94 times that of SSH_ SW technique. Compared with the SBF$_2$, the SBFR$_4$ has a substantial improvement in MOPIR of about 46%.

III. Proposed SBFR Interface Based on 2^n-Input (SBFR$_z$)

Through the above analysis, it can be discovered that the piezoelectric material of the same area can be split into more PEH units equally to increase the number of phases during the zero-crossing state, thereby decreasing the loss and improving the flipping efficiency. SBFR$_4$ can be extended to SBFR$_z$, where z is the number of PEHs, which can be expressed as $z = 2^n$. By simply using z reconfigurable PEHs, $3n$ phases can be achieved in the zero crossing state, where $n-1$ phases are in the charge recycle stage and $2n+1$ phases are in the voltage-flip stage.

Fig. 10 shows the grouping diagram of the array with the connection examples, where PEHs in the piezoelectric array are divided into two groups. The equivalent intrinsic capacitance of the total piezoelectric material is assumed to be C_P, which is split into 2^n piezoelectric units. The first 2^{n-1} units are served as energy sources and can be configured as required. When they form an array of 2^i rows $\times$ 2^j columns, which is named as PA$_{i,j}$, and the equivalent capacitance of the array is $\frac{1}{2^{(n+i-j)}} \cdot C_P$, where i+j=n-1. The rest 2^{n-1} units are filled with gray, which are employed as flipping capacitors in the zero-crossing state. Similarly, when they form an array of 2^p rows and 2^q columns, it is named as PB$_{p,q}$. At this time, the equivalent capacitance of the array is $\frac{1}{2^{(n+p-q)}} \cdot C_P$, where p+q=n-1.

Fig. 11 shows the operation process of SBFR$_z$, with two operating states including energy harvesting and zero-crossing. In energy harvest state, all units are configured in parallel as ac sources and followed by a rectifier to extract power. The entire zero-crossing state can be divided into two stages: charge recycle and voltage-flip. In the charge recycle stage, the PA is disconnected from the system, while the PB is connected to the FBR followed by the C_{RECT}, and the charges stored on it are transferred to C_{RECT} in steps. In PH$_{\mathrm{CR1}}$ phase, p=1, q=n-2. At this time, the voltage across PB$_{1,(n-2)}$ is $2V_{RECT}$. The charge on it is shared to the C_{RECT} through FBR, and the equivalent output power P_{CR1} is

$$P_{CR1} = (1/2)^3 \times C_P \times (V_{RECT})^2 \times 2f_P. \quad (23)$$

In the PH$_{\mathrm{CR2}}$ phase, p=2, the voltage across PB rises to $2V_{RECT}$ again and transfers the energy of P_{CR2} to C_{RECT}, where P_{CR2} is equal to

$$P_{CR2} = (1/2)^5 \times C_P \times (V_{RECT})^2 \times 2f_P. \quad (24)$$

Generally, in the phase of PH$_{\mathrm{CR}}$(n-1), the PB outputs power of $P_{CR(n-1)}$ to the C_{RECT} is

$$P_{CR(n-1)} = (1/2)^{2n-1} \times C_P \times (V_{RECT})^2 \times 2f_P. \quad (25)$$

After the charge recycle stage, most of the charges accumulated on the PB have been transferred to C_{RECT}. Then, the interface circuit enters the voltage-flip stage. In the PH$_{\mathrm{BF0}}$ stage, the residual charge on the PB is first cleared. The subsequent phases can be divided into two parts.

1) In the phase of PH$_{\mathrm{BF<1,n>}}$, PA$_{0,(n-1)}$ keeps the same structure, and the units in PB are gradually converted from series to parallel for reducing the sharing loss due to the voltage difference.
2) In the phase of PH$_{\mathrm{BF<(n+1),(2n-1)>}}$, PB$_{0,(n-1)}$ remains unchanged, while the units in the PA are switched from parallel to series step by step, so as to transfer as much charge as possible to PB. Finally, in phase PH$_{\mathrm{BF(2n)}}$, the residual charge on the PA is cleared. After completing the voltage-flip, the interface circuit returns to the energy harvest state. At this time, 2^n-inputs are back to parallel combination, and the phase of rebuilt voltage V_{RBT} is consist with I_P.

The blue curve in the Fig. 12(a) shows the flipping efficiency with respect to the PEH number (z). As expected, the flipping efficiency improves as z increases. The orange curve in Fig. 12(a) represents the normalized total charge transferred from PB to C_{RECT}. When z is less than 4, the interface is unable to establish the charge recycle stage. As z increases, more of the charge on PB is transferred to C_{RECT}. Fig. 12(b) depicts the relationship between the MOPIR and the PEH number. Compared with SBFR$_2$, the MOPIR of SBFR$_4$ is greatly improved by 45.9%, which is mainly due to the utilization of the charge stored on the PB. The output power can be improved by increasing z, but the improvement flattens as z becomes larger. As z increases, the associated increase in the circuit complexity can lead to a higher switching loss that limits the achievable MOPIR.

IV. Circuit Implementation and Test Analysis

To validate the concept, this section describes the circuit implementation and the measured performance of SBF and SBFR circuits.

A. Setup and Characterization

Fig. 13(a) shows the test bench schematic of the proposed SBFR $_4$. The 4 PEH-input based interface is selected to design

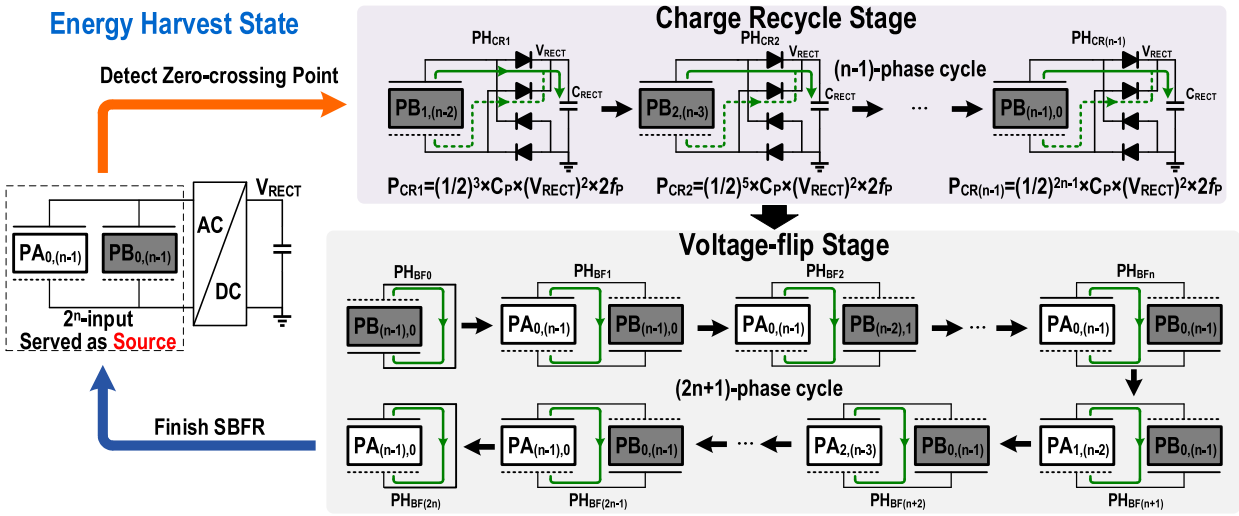


Fig. 11. Structure transformation of 2^n-input array in zero-crossing state of the proposed SBFR_z.

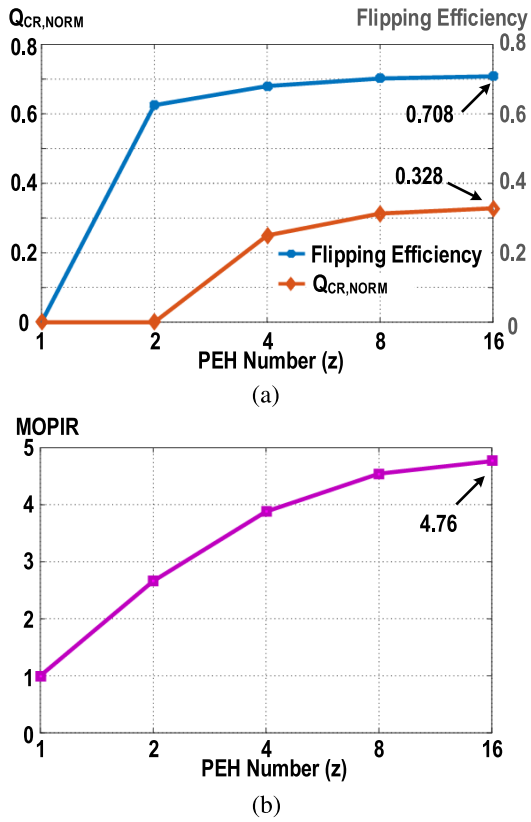


Fig. 12. Performance calculation with input nodes of 1, 2, 4, 8, and 16 of SBFR_z. (a) Flipping efficiency versus PEH number; (b) MOPIR versus PEH number.

the PCB circuit, so as to balance the harvesting efficiency and circuit complexity. PEHs adopt the type of PPA-1021, and FBR consists of 4 Schottky diodes, the typical forward voltage of which is 0.25 V. The PCB circuit uses discrete analog switches to form a switch array for topology transformation. Fig. 14(a) shows the circuit implementation of SBF_2 using eight switches. Table I tabulates the control phases of each switch. If z is greater than 4, routing and implementation of the array become more complex. Therefore, ASIC designs are more suitable for achieving the required performance. In this case, the switches can be implemented using transmission gates to ensure the switch conductance at different source voltages during reconfigurations, with active body biasing to reduce the switch ON-resistance [14], as shown in Fig. 14(b). If an ASIC chip is used to control the PEH array, the structure of the control circuit is similar to the circuit in [17], and the power consumption of the control circuit is estimated to be about 3.8 μW.

TABLE I
CONTROL PHASES OF EACH SWITCH IN SBF_2

	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
EH State	on	on	on	on	off	off	off	off
PH_{BF0}	off	off	off	off	on	off	off	off
PH_{BF1}	off	off	off	off	off	on	on	off
PH_{BF2}	off	off	off	off	off	off	off	on

The combination of the switch array is determined by the control signals PS_{OPERA}, PS_{CR}, and $\text{PS}_{\text{BF}\langle 0,4\rangle}$, whose waveforms are shown in Fig. 13(b). The pulse widths of PS_{CR} and $\text{PS}_{\text{BF}\langle 0,4\rangle}$ are set to 10 μs to ensure the charge is transferred sufficiently. The interval between adjacent pulses is 500 ns to avoid overlapping. The duration t_{ZC} of the zero-crossing state is 42.5 μs. Hence, when $f_P = 100$ Hz, the zero-crossing state only occupies 0.85% of the whole period. Note that we can change the interface structure by altering the output of FPGA. Specifically, if the PS_{CR} signal is set to zero, the rest control signal can realize the SBF_4. Similarly, if the PS_{CR}, PS_{BF1}, and PS_{BF3} signals are set to zero simultaneously, SBF_2 can be implemented. The proposed technique is verified with the discrete components. The types of devices and the development board used in the experiment are shown in Table II.

The entire experimental setup is shown in Fig. 15. The 4 PEHs are tightly mounted on the shaker (KDJ-50), which receives periodic excitations from a function generator together with

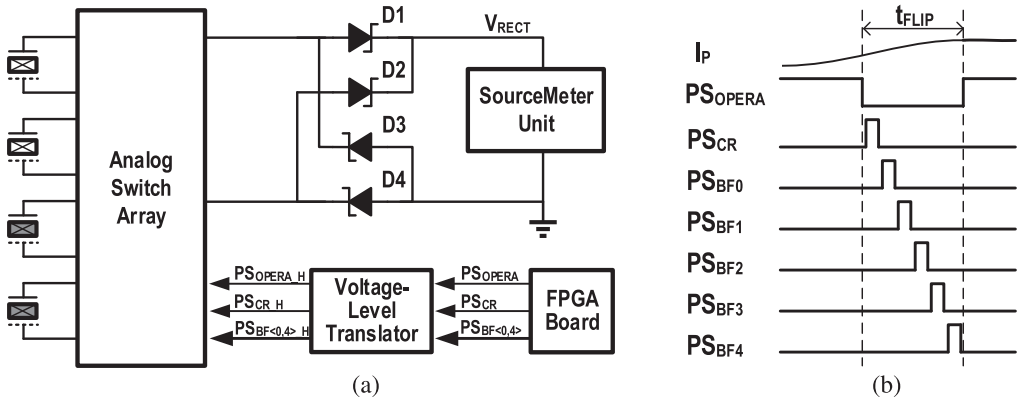


Fig. 13. Principle of the test. (a) Test bench schematic. (b) Control signal.

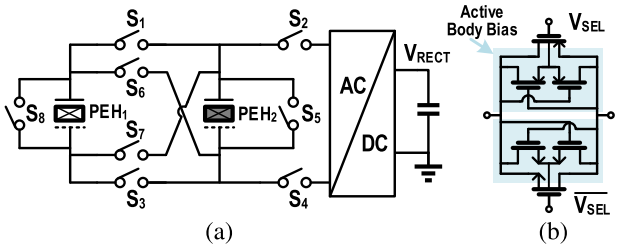


Fig. 14. Circuit implementation of SBF_2. (a) Structure of the switch array. (b) Transmission gate with active body bias.

TABLE II
COMPONENT TYPE

Component	Type
PEH	PPA-1021
Analog Switch	TS5A3167DBVR
Schottky Diode	BAT54T1G
FPGA Board	DE2-115
Voltage-level Translator	SN74LVC8T245DGVR

a power amplifier (KD5708). The details of the 4-node PEH array and designed PCB circuit are shown in Fig. 15(b) and 15(c), respectively. The source meter unit (Keithley 2614B) is employed as the load of the rectifier, which can adjust the output voltage while measuring the output current.

B. Experimental Results

The influence of the C_P value on the flipping efficiency is tested based on the SBF $_2$ scheme. In order to reduce the influence of V_D, the open-circuit voltage is adjusted to 3 V. Fig. 16 shows that when $C_P = 88$ nF, the theoretical maximum output power of the ideal FBR is only 79 μW, while the measured value can be increased to 208 μW with the operation of SBF_2, and the corresponding MOPIR is 2.63x. However, when $C_P = 44$ nF, the MOPIR decreases to 2.49x. According to (14), the MOPIR of both should theoretically equal to 2.66x. However, due to the relatively fixed power losses of switch leakage current and parasitic capacitance, these nonideal factors have a greater impact at low power. Therefore, when C_P is 44 nF, the deviation between MOPIR and the theoretical value is greater.

Fig. 17 shows the measurement results of the impact of C_{P1}/C_{P2} on P_{OUT}. As shown in Fig. 15, we utilized four PEHs in the test. If three of them are connected in parallel to form C_{P1}, then they will form C_{P1}/C_{P2} (3:1) with the remaining one. Similarly, we can obtain 1:1 and 1:3 by grouping without changing the total PEH number. The highest power occurs when C_{P1}: C_{P2} is 1:1, while the P_{OUT} of the ratio 1:3 and 3:1 are approximately equal and relatively small, which are consistent with the theoretical analysis results in Fig. 4.

Fig. 18 depicts the measured voltage across $PEH_{\langle 1,2\rangle}$ and $PEH_{\langle 3,4\rangle}$, where V_{RECT} is set to 1 V. When the voltage across the PEH exceeds 1.25 V, the PEH outputs power to the load. The zoomed-in view of the waveform in zero-crossing state shows the difference between the voltage waveforms of $V_{PEH<1,2>}$ and $V_{PEH<3,4>}$. The value of V_{RBT} is about 34.5% of the $V_{PEH<1,2>}$ before flipping, while the flipping efficiency reaches 67%.

The measured results of the rectifier output power (P_{RECT}) versus V_{RECT} are shown in Fig. 19. Note that FBR($V_D = 0$) on Figs. 19 and 20 is the ideal calculated result of P_{FBR}. For a fair comparison, we use the following formula [2] to calculate P_{FBR} when V_D is zero to avoid changes in V_D at different power levels

$$P_{FBR} = 4 \cdot C_P \cdot (V_P - V_{RECT}) \cdot V_{RECT} \cdot f_P. \quad (26)$$

When $V_{RECT} = 4.4$ V, the P_{RECT} of SBFR $_4$ reaches the maximum value of 281 μW with the V_P of 3 V. Compared with the output power of FBR formed by the Schottky diodes ($V_D = 0.25$ V), the corresponding MOPIR reaches 5.2x. Without PH $_{\mathrm{CR}}$, the measured P_{RECT} of SBF_4 drops to 239 μW when V_P is 3 V, and the corresponding MOPIR is decreased to 3.02x, which indicates that the PH_{CR} phase makes significant contribution to the performance improvement.

Fig. 20 shows the measured maximum output power of SBF_2, SBF_4, and $SBFR_4$ with respect to V_P, respectively. As the vibration level increases, the impact of nonideal factors such as diode forward voltage and transistor resistance decreases. The MOPIR of $SBFR_4$ gradually increases from 2.4x to 3.56x, approaching the ideal value of 3.88x. Note that with the presence of the V_{th} of the CMOS switches, the conduction loss at low input will significantly increase, thereby reducing the efficiency of harvesting. Fig. 21 shows the measured effect of zero-crossing

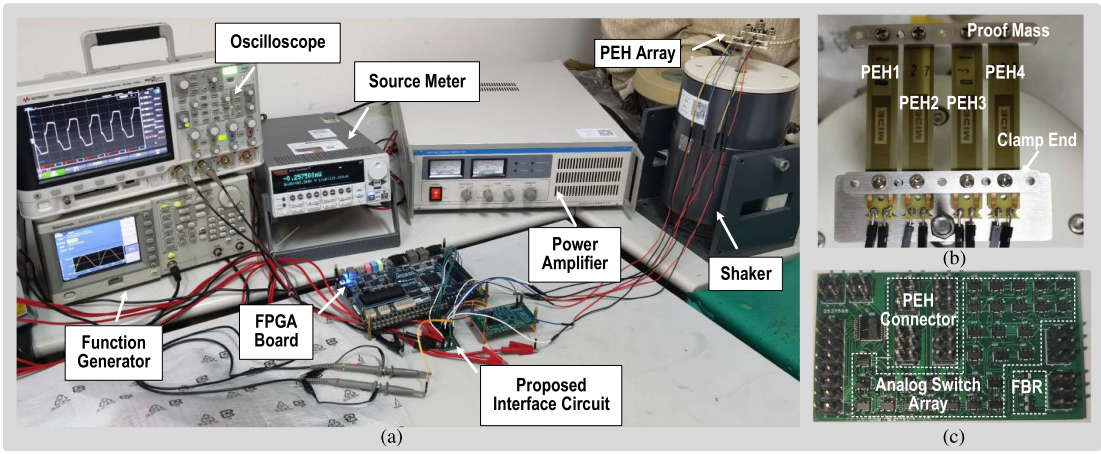


Fig. 15. Experimental setup. (a) Overview. (b) 4-input PEH array. (c) PCB circuit.

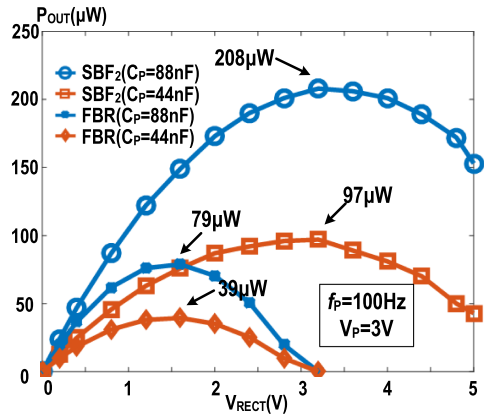


Fig. 16. Measured effect of C_P area on harvested power with SBF_2 and FBR.

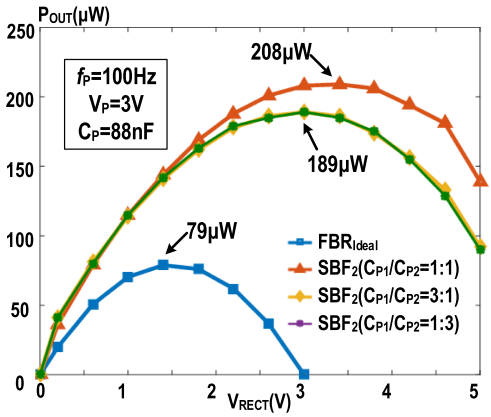


Fig. 17. Measured influence of area ratio on harvested power with SBF_2 and FBR.

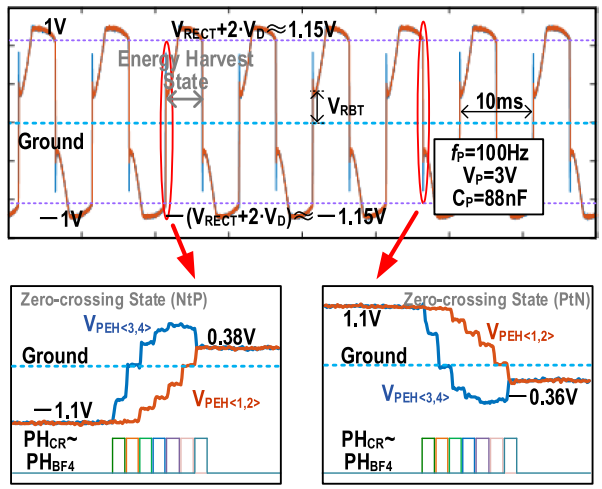


Fig. 18. Measured waveform of the V_{PEH} with $SBFR_4$.

deviation. When there is no deviation, the corresponding MOPIR is 3.56x. However, when the zero-crossing point deviates from 10%, the MOPIR decreases to 3.19x, which decreases by about 10.4%.

The performance of $SBFR_4$ compared with the state-of-the-art is presented in Table III. The "Normalized Volume" (including IC and all OFF chip components) is an estimate of each state-of-the-art interface circuit. The IC chips are assumed to occupy 10 mm^3. Each OFF-chip capacitor or resistor is assumed to occupy 0.75 mm^3. The unit volume for a highly compact inductor is assumed to be 100 mm^3/mH [16]. Compared to other techniques, this work has much less volume and achieves a greater FoM by avoiding the use of OFF-chip component (except for load capacitors). It is especially suitable to be cointegrated with a custom micro-electromechanical systems (MEMS) piezoelectric transducer with its electrode layer equally split into multiple regions [17]. If employing MEMS to realize $SBFR_4$, the volume of 4-node PEH array is about 28 mm^3 [17]. The total volume can be limited to about 40 mm^3, which can be used in the volume strict application. The maximum output power of a cubic centimeter sized PEH can attains to a few milliwatt, and the power consumption of the control circuit is about tens of microwatts [15]. When scales to MEMS PEH, the maximum output power is limited to hundreds of microwatts due to the small size of the piezoelectric material, and the power consumption of the control circuit can optimize to about a few microwatts [17]. The low cost, ultracompact solution with a measured high MOPIR reveals the proposed technique as a

TABLE III
PERFORMANCE COMPARISON

	This Work	[10]	[11]	[15]	[17]	[19]
Technique	**SBFR**	S-SSHI	P-SSHI	SPFCR	SE-SSHC	MI-SECE
Transducer	**MIDE PPA-1021**	MIDE PPA-1014	MIDE PPA-1001	MIDE PPA-1021	Customer MEMS	MIDE PPA-1014
No. of Inputs	**4**	2	3	1	4	2
Key Component	**None**	An Inductor (2.3mH)	An Inductor (10mH)	4 Capacitors (272nF)	8 Capacitors (4nF on Chip)	An Inductor (1mH)
MOPIR	**3.56x**	3.7x	4.8x	3.7x∼6.2x	2.57x∼5.89x	3.6x
Max. Voltage Flipping Efficiency	**0.67**	N/A	0.9	0.84	0.65	N/A
Piezoelectric Capacitor	**88nF (22nF each)**	82nF (41nF each)	300nF (100nF each)	22nF	1.94nF	82nF (41nF each)
Normalized Volume (V^{**}_{NOR})	**1**	24	101	1.3	1	11
FoM^{++}	**3.56**	0.15	0.05	2.84∼4.77	2.57∼5.89	0.33
Output Power	**281μW**	120μW	187μW	64μW	186μW	135μW
Operating Freq	**100Hz**	19Hz	100Hz	200Hz	219Hz	20Hz

$^{**}V_{NOR} = SystemVolume/ChipVolume$
$^{++}FoM = MOPIR/V_{NOR}$

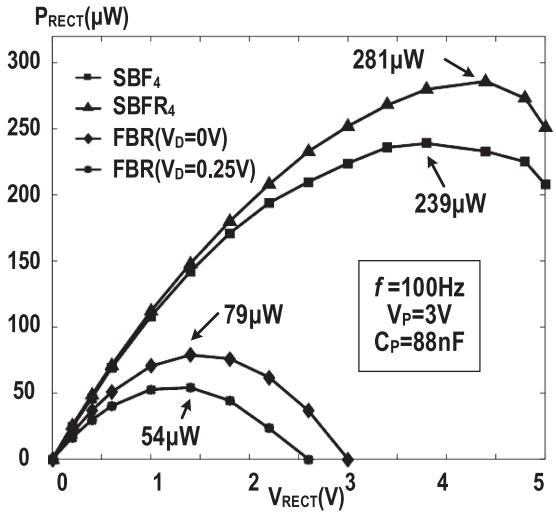


Fig. 19. Measured harvested power versus V_{RECT} with SBF_4, $SBFR_4$, and FBR.

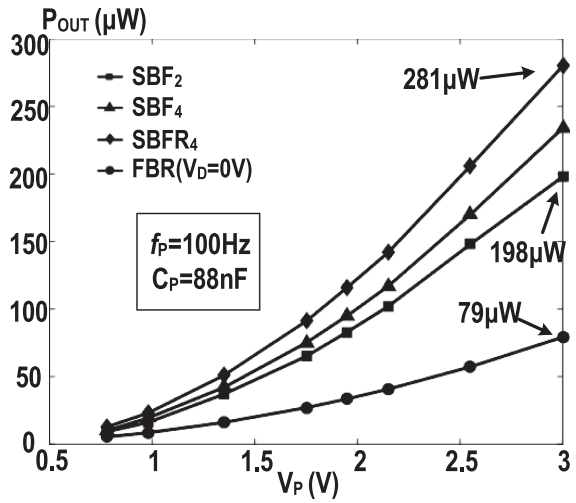


Fig. 20. Measured harvested power versus V_P with SBF_2, SBF_4, $SBFR_4$, and FBR.

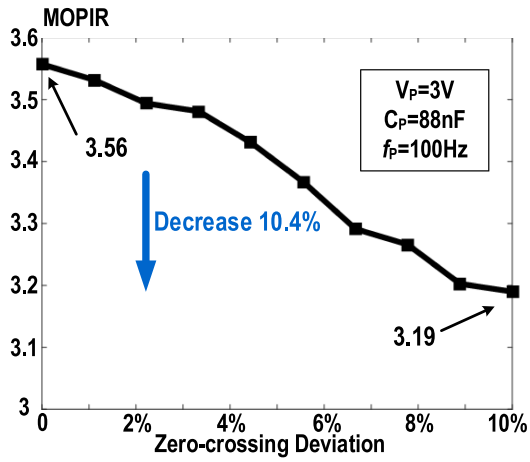


Fig. 21. Measured relationship between the zero-crossing offset and the MOPIR of $SBFR_4$.

promising solution for piezoelectric energy harvesting applications, especially for deep-tissue implant implementations such as implantable micro-oxygen generator (IMOG) [31] or gastric seed [32].

V. CONCLUSION

This article proposes a self-bias-flip with charge recycle interface circuit with no external energy reservoir (except for load capacitors). The theoretical analysis is carried out beginning with the SBF_2, and the design method of SBF_4 and $SBFR_4$ is gradually deduced. The generalized SBFR topology based on 2^n-input by employing the inherent capacitors as flipping capacitors are also illustrated. Except for theoretical analysis, the three prototypes are verified by discrete components. The test results indicate that $SBFR_4$ can achieve a 67% flipping efficiency and the MOPIR can reach up to 5.2x. The scheme conforms to the trend of miniaturization of interfaces in the IoT era, and provides a new design method for piezoelectric harvest systems.

REFERENCES

[1] H. Uluşan, A. Muhtaroğlu, and H. Külah, "A sub-500 μW interface electronics for bionic ears," *IEEE Access*, vol. 7, pp. 132140–132152, 2019.

[2] Y. K. Ramadass and A. P. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 189–204, Jan. 2010.

[3] Y. Manoli, "Energy harvesting – from devices to systems," in *Proc. Proc. Eur. Conf. Solid-State Circuits*, 2010, pp. 27–36.

[4] S. Roundy and P. K. Wright, "A piezoelectric vibration based generator for wireless electronics," *Smart Mater. Struct.*, vol. 13, no. 5, 2004, Art. no. 1131.

[5] G. Tang, B. Yang, J.-Q. Liu, B. Xu, H.-Y. Zhu, and C.-S. Yang, "Development of high performance piezoelectric d33 mode MEMS vibration energy harvester based on PMN-PT single crystal thick film," *Sensors Actuators A: Phys.*, vol. 205, pp. 150–155, 2014.

[6] M. Han, Q. Yuan, X. Sun, and H. Zhang, "Design and fabrication of integrated magnetic MEMS energy harvester for low frequency applications," *J. Microelectromech. Syst.*, vol. 23, no. 1, pp. 204–212, 2014.

[7] N. Rezaei-Hosseinabadi, A. Tabesh, and R. Dehghani, "A topology and design optimization method for wideband piezoelectric wind energy harvesters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2165–2173, Apr. 2016.

[8] G. Ottman, H. Hofmann, A. Bhatt, and G. Lesieutre, "Adaptive piezoelectric energy harvesting circuit for wireless remote power supply," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 669–676, Sep. 2002.

[9] D. Guyomar, A. Badel, E. Lefeuvre, and C. Richard, "Toward energy harvesting using active materials and conversion improvement by nonlinear processing," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 52, no. 4, pp. 584–595, Apr. 2005.

[10] Z. Chen, Y. Xia, G. Shi, X. Wang, H. Xia, and Y. Ye, "Self-powered multi-input serial SSHI interface circuit with arbitrary phase difference for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9183–9192, Aug. 2021.

[11] Z. Long, P. Li, X. Wang, B. Wang, H. S.-H. Chung, and Z. Yang, "A self-powered P-SSHI array interface for piezoelectric energy harvesters with arbitrary phase difference," *IEEE Trans. Ind. Electron.*, vol. 69, no. 9, pp. 9155–9164, Sep. 2022.

[12] S. Chamanian, B. Çıftcı, A. Muhtaroğlu, and H. Külah, "A self-powered and area efficient SSHI rectifier for piezoelectric harvesters," *IEEE Access*, vol. 9, pp. 117703–117713, 2021.

[13] S. Javvaji, V. Singhal, V. Menezes, R. Chauhan, and S. Pavan, "Analysis and design of a multi-step bias-flip rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2590–2600, Sep. 2019.

[14] Z. Chen, M.-K. Law, P.-I. Mak, W.-H. Ki, and R. P. Martins, "Fully integrated inductor-less flipping-capacitor rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3168–3180, Dec. 2017.

[15] Z. Chen, M.-K. Law, P.-I. Mak, X. Zeng, and R. P. Martins, "Piezoelectric energy-harvesting interface using split-phase flipping-capacitor rectifier with capacitor reuse for input power adaptation," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2106–2117, Aug. 2020.

[16] S. Du and A. A. Seshia, "An inductorless bias-flip rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2746–2757, Oct. 2017.

[17] S. Du, Y. Jia, C. Zhao, G. A. J. Amaratunga, and A. A. Seshia, "A fully integrated split-electrode SSHC rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1733–1743, Jun. 2019.

[18] E. Lefeuvre, A. Badel, C. Richard, and D. Guyomar, "Piezoelectric energy harvesting device optimization by synchronous electric charge extraction," *J. Intell. Mater. Syst. Struct.*, vol. 16, no. 10, pp. 865–876, 2005.

[19] X. Wang et al., "Multi-input SECE based on buck structure for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3638–3642, Apr. 2021.

[20] L. Teng, J. Liang, and Z. Chen, "Multiple charge extractions with bias-flip interface circuit for piezoelectric energy harvesting," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2020, pp. 1–5.

[21] D. Kwon and G. A. Rincón-Mora, "A single-inductor 0.35μm CMOS energy-investing piezoelectric harvester," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2277–2291, Oct. 2014.

[22] Z. Long et al., "Self-powered SSDCI array interface for multiple piezoelectric energy harvesters," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9093–9104, Aug. 2021.

[23] T. Hehn et al., "A fully autonomous integrated interface circuit for piezoelectric harvesters," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2185–2198, Sep. 2012.

[24] B. Çiftci, S. Chamanian, A. Koyuncuoğlu, A. Muhtaroğlu, and H. Külah, "A low-profile autonomous interface circuit for piezoelectric micro-power generators," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 68, no. 4, pp. 1458–1471, Apr. 2021.

[25] H. Xia et al., "A self-powered S-SSHI and SECE hybrid rectifier for PE energy harvesters: Analysis and experiment," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1680–1692, Feb. 2021.

[26] S. Li, X. Liu, and B. H. Calhoun, "A 32nA fully autonomous multi-input single-inductor multi-output energy-harvesting and power-management platform with 1.2×105 dynamic range, integrated MPPT, and multi-modal cold start-up," in *Proc. IEEE Int. Solid- State Circuits Conf.*, 2022, vol. 65, pp. 1–3.

[27] M. Lallart, W.-J. Wu, Y. Hsieh, and L. Yan, "Synchronous inversion and charge extraction (SICE): A hybrid switching interface for efficient vibrational energy harvesting," *Smart Mater. Struct.*, vol. 26, no. 11, Oct. 2017, Art. no. 115012.

[28] A. Morel, G. Pillonnet, P. Gasnier, E. Lefeuvre, and A. Badel, "Frequency tuning of piezoelectric energy harvesters thanks to a short-circuit synchronous electric charge extraction," *Smart Mater. Struct.*, vol. 28, no. 2, Dec. 2018, Art. no. 025009.

[29] Z. Li et al., "An energy harvesting system with reconfigurable piezoelectric energy harvester array for IoT applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2020, pp. 1–5.

[30] H. Xia et al., "Self-powered dual-inductor MI-PSSHI-VDR interface circuit for multi-PZTs energy harvesting," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 3753–3762, Apr. 2022.

[31] T. Maleki, N. Cao, S. H. Song, C. Kao, S.-C. Ko, and B. Ziaie, "An ultrasonically powered implantable micro-oxygen generator (IMOG)," *IEEE Trans. Biomed. Eng.*, vol. 58, no. 11, pp. 3104–3111, Nov. 2011.

[32] M. Meng, P. Graybill, R. L. Ramos, A. Javan-Khoshkholgh, A. Farajidavar, and M. Kiani, "An ultrasonically powered wireless system for in vivo gastric slow-wave recording," in *Proc. 41st Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, 2019, pp. 7064–7067.

Zhen Li (Student Member, IEEE) received the B.S. degree from the Anhui University, Hefei, China, in 2016, the M.E. degree from the Ningbo University, Ningbo, China, in 2019, and he is currently working toward the Ph.D. degree with the State Key Laboratory of Integrated Chips and Systems and School of Microelectronics, Fudan University, Shanghai, China, all in electronics engineering.

His current research interests include piezoelectric energy harvesting systems and power management IC.

Zhiyuan Chen (Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in electronics engineering from the University of Macau (UM), Macao, China, in 2011, 2013, and 2018, respectively.

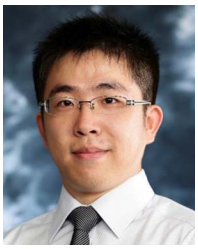
Since 2018, he has been with the School of Microelectronics, Fudan University, Shanghai, China, as a Postdoctoral Researcher, where he is currently an Associate Professor. His research interests include ac–dc rectifiers, dc–dc converters, and energy harvesting systems.

Jing Wang received the B.S. degree in microelectronics from Xidian University, Xi'an, China, in 2020. She is currently working toward the Ph.D. degree in electronics engineering with Fudan University, Shanghai, China.

Her research interests include ultralow power management systems and piezoelectric energy harvesting systems.

Jiawei Wang received the M.S. degree in integrated circuit engineering from Ningbo University, Zhejiang, China, in 2017. He is currently working toward the Eng.D. degree in electrical information engineering with Fudan University, Shanghai, China.

His current research interests include analog and mixed-signal circuit design.



Junmin Jiang (Member, IEEE) received the B.Eng. degree in electronic and information engineering from Zhejiang University, Hangzhou, China, in 2011, and the Ph.D. degree in electronic and computer engineering from The Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2017.

He was a Visiting Scholar with the State Key Laboratory of AMSV, University of Macau, Zhuhai, Macau, in 2015, and was a Postdoctoral Fellow with HKUST, in 2017. He was an Analog Design Engineer with Kilby Labs Silicon Valley, Texas Instruments, Santa Clara, CA, USA, from 2018 to 2021. In 2021, he joined the Southern University of Science and Technology (SUSTech), Shenzhen, China, where he is currently an Associate Professor. His current research interests include power management IC design, especially in switched-mode power converter design.

Sijun Du (Senior Member, IEEE) received the B.Eng. degree in electrical engineering from Sorbonne University, Paris, France, in 2011, the M.Sc. degree in electrical and electronics engineering from Imperial College, London, U.K., in 2012, and the Ph.D. degree in engineering from the University of Cambridge, Cambridge, U.K., in 2018.

He worked with the Laboratory LIP6, Sorbonne University, Paris, France, and then worked as a Digital IC Engineer in Shanghai, China, between 2012 and 2014. He was a Postdoctoral Researcher with the Berkeley Wireless Research Center (BWRC), Department of Electrical Engineering and Computer Sciences (EECS), University of California, Berkeley, CA, USA, between 2018 and 2020. In 2020, he joined the Department of Microelectronics, Delft University of Technology (TU Delft), Delft, The Netherlands, where he is currently an Assistant Professor. His current research interest includes power management integrated circuit designs.

Xu Cheng received the B.S. and M.S. degrees in electronics engineering from Fudan University, Shanghai, China, in 1999 and 2002, respectively, and Ph.D. degree from the University College Cork, Cork, Ireland, in 2007.

From 2007 to 2009, he was with Cypress Semiconductor Ireland. In 2009, he joined Fudan University, where he is currently an Associate Professor. His current research interests include energy-efficient analog mixed-signal design and analog CAD.

Xiaoyang Zeng (Senior Member, IEEE) received the B.S. degree from Xiangtan University, Xiangtan, China, in 1992, and the Ph.D. degree from Changchun Institute of Optics, Fine Mechanics, and Physics, Chinese Academy of Sciences, Changchun, China, in 2001.

From 2001 to 2003, he was a Postdoctoral Researcher with Fudan University, Shanghai, China. Then, he joined the State Key Lab of Integrated Chips and Systems, Fudan University, as an Associate Professor, where he is currently a Full Professor and the Director. His research interests include high performance-energy efficient SoC for information security and artificial intelligence applications, etc., and VLSI implementation of digital signal processing and communication systems.

Jun Han (Member, IEEE) received the B.S. degree from Xidian University, Shanxi, China, in 2000, and the Ph.D. degree in microelectronics from Fudan University, Shanghai, China, in 2006.

He joined Fudan University as an Assistant Professor in July 2006, where he is currently a Full Professor with the State Key Laboratory of Integrated Chips and Systems. His current research interests include domain-specific processors and systems for digital signal processing, machine learning, and human–computer interaction.