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Integration Technologies for Smart Catheters

Li, J.

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INTEGRATION TECHNOLOGIES FOR SMART CATHETERS

Integration Technologies for Smart Catheters

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. dr. ir. T.H.J.J. van der Hagen,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op
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Jian LI

Master of Science in Electrical Engineering
Delft University of Technology, Delft, The Netherland,
geboren te Hebei, China.

Dit proefschrift is goedgekeurd door de

promotor: prof. dr. R. Dekker
promotor: prof. dr. P. French

Samenstelling promotiecommissie:

Rector Magnificus,	voorzitter
Prof. dr. R. Dekker,	Delft University of Technology, promotor
Prof. dr. P. French,	Delft University of Technology, promotor

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Dr. ir. G. Pandraud,	Ommatidia LIDAR, The Netherlands
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Dr. ir. V. Henneken,	Philps Research, The Netherlands

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1

Introduction

1

1.1. SMART CATHETERS

1.1.1. APPLICATION FIELD: HEART DISEASE DIAGNOSIS AND TREATMENT

HEART disease is a general term that refers to several types of heart conditions, such as cardiovascular diseases (CVDs), atrial fibrillation (AF), and valvular heart disease (VHD). As the most common heart disease, CVDs are the leading cause of death each year, taking around 17.9 million lives, an estimated 32% of all deaths worldwide [1]. CVDs are a group of disorders concerning the blood vessels of the heart. Important behavioral risk factors for CVDs are unhealthy diet, lack of exercise, use of tobacco, and abuse of alcohol [2]. The most common CVD, coronary artery disease, is shown in Figure 1.1(a). It starts with accumulating atherosclerotic plaque inside the coronary artery of the heart, which reduces the oxygen-rich blood supply to the heart muscles. As the plaque accumulates over the years, signs of heart attack such as angina, shortness of breath, or nausea eventually occur. Immediate emergency medical care is crucial in this case.

Cardiac catheterization with smart catheters is an invasive procedure that can effectively diagnose and treat coronary artery disease[3]. A smart catheter normally has a long, narrow, flexible tube with a smart tip at the proximal end of the catheter. The smart tip of the catheter is equipped with different sensors or actuators. For diagnosis, the smart catheter is inserted through an artery in the groin or arm, advanced all the way through the body, reaching the coronary artery of the heart. Blood pressure, blood flow, and ultrasound images of the coronary artery can be acquired with smart catheters, such as fractional flow reserve (FFR) and intravascular ultrasound (IVUS) catheters, for high-accuracy diagnosis[4, 5].

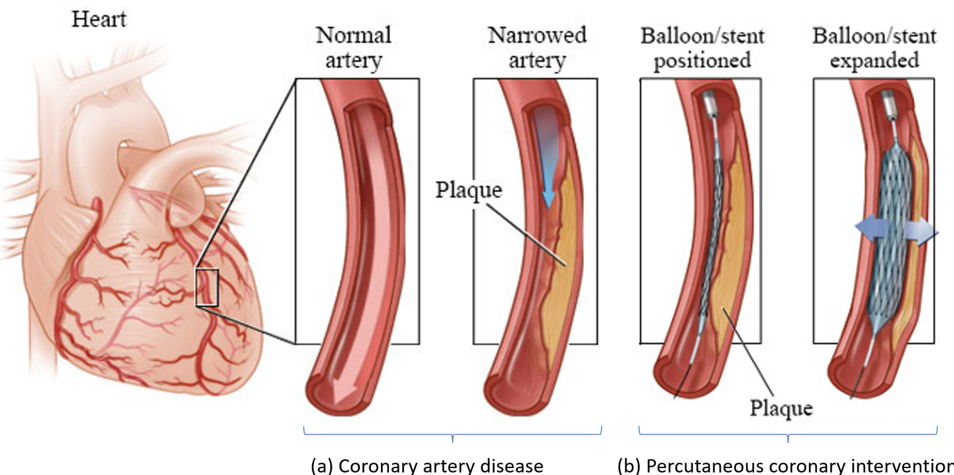

Figure 1.1: Coronary artery disease and percutaneous coronary intervention (PCI) [6]

Percutaneous coronary intervention (PCI), also known as balloon angioplasty, is a mature interventional procedure to treat coronary artery disease with catheters. As shown in Figure 1.1(b), the catheter has a small balloon and a stent at the tip of the catheter. A stent is a small, metal mesh tube that can be expanded to support the inside of the blood

vessel like a scaffold. The balloon catheter with the stent is inserted through the artery until the narrow coronary artery is reached. Once in place, the balloon is inflated to press the plaque against the artery wall, widening the diameter of the artery opening. The stent is expanded simultaneously and holds the artery open permanently after the balloon is deflated and removed. As a result of the intervention, the blood flow to the heart is resumed [7].

1.1.2. CARDIAC CATHETERIZATION CATEGORIES

Figure 1.2 presents the complete spectrum of smart catheter applications. The function of the smart tip and the dimension of the catheter depends on the catheter application. Fractional flow reserve (FFR) is a coronary catheterization technique that uses a presseure sensor on the tip of a guidewire. It measures the pressure difference across the coronary artery blockage to locate the plaque blockages distributed in the coronary artery. With a diameter of only 360 µm, FFR is easy to steer and can reach very narrowed coronary arteries. Intravascular ultrasound (IVUS) is an ultrasound imaging technique to inspect the coronary artery. The ultrasound transducers at the catheter tip allow an in-depth scan from inside the artery into the surrounding tissues. It can provide more detailed information on the plaque blockages, such as density and vulnerability[8, 9]. More about IVUS catheters will be presented in the coming section as a showcase.

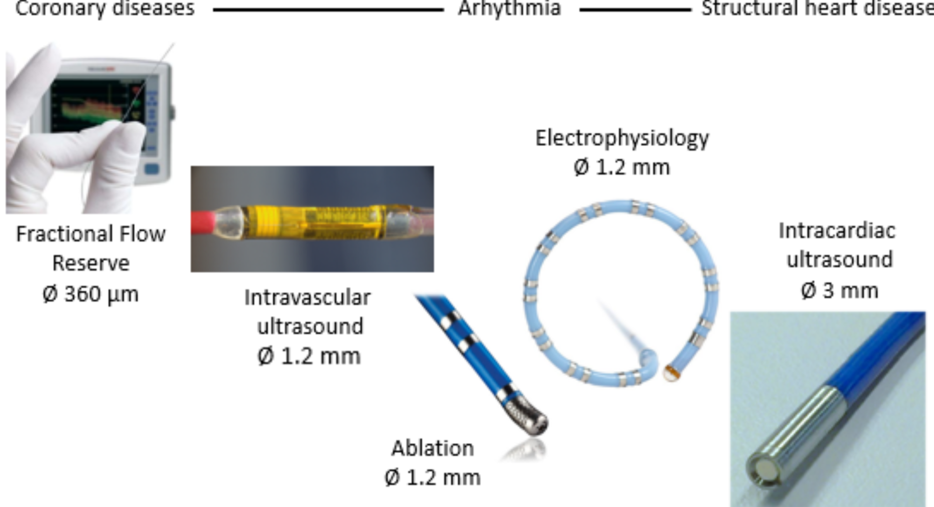

Figure 1.2: A complete spectrum of smart catheter applications, from coronary disease, arrhthmia to structural heart diseases, with various functions and dimensions.[10]

Arrhythmia is a heart rhythm disorder caused by disturbances in the electrical conduction of the heart [11]. Catheters for arrhythmia treatment include ablation catheters and circular mapping catheters for electrophysiology (EP). The circular mapping catheter has platinum electrodes on its tip and can perform EP studies to identify the location that causes the abnormal rhythm. The ablation catheter, using either heat generated by RF

or extreme cold, creates scar tissues in the heart to isolate areas that cause the arrhythmia[12, 13].

Intracardiac echocardiography (ICE) is a unique imaging technique that enables high resolution, high frame rate, and real-time visualization of cardiac structures[14, 15, 16]. Figure 1.2 shows a forward-looking ICE catheter with ultrasound transducers integrated at the catheter tip. The ICE catheter can detect structural heart diseases, recognize procedural complications, and precisely in-situ monitor and guide intervention procedures, such as catheter ablation or valve placement[17]. It is expected that the application of the ICE catheters will continue to evolve to increase its resolution and frame rate for 2D and 3D imaging and consolidate its role in the treatment of structural heart disease.

1.1.3. THE MARKET SIZE OF SMART CATHETERIZATION

According to the latest research from Allied Market Research, the global market size for smart catheterization was valued at USD 22.7 billion in 2021 and is expected to reach USD 49.5 billion by 2031, at a compound annual growth rate (CAGR) of 8.1% from 2022 to 2031 [18]. The growth of the global catheter market is mainly driven by the rising case numbers of cardiovascular diseases that demand minimal invasive surgery, which mainly include ultrasound imaging pressure and fore sensing, and device steering and tracking:

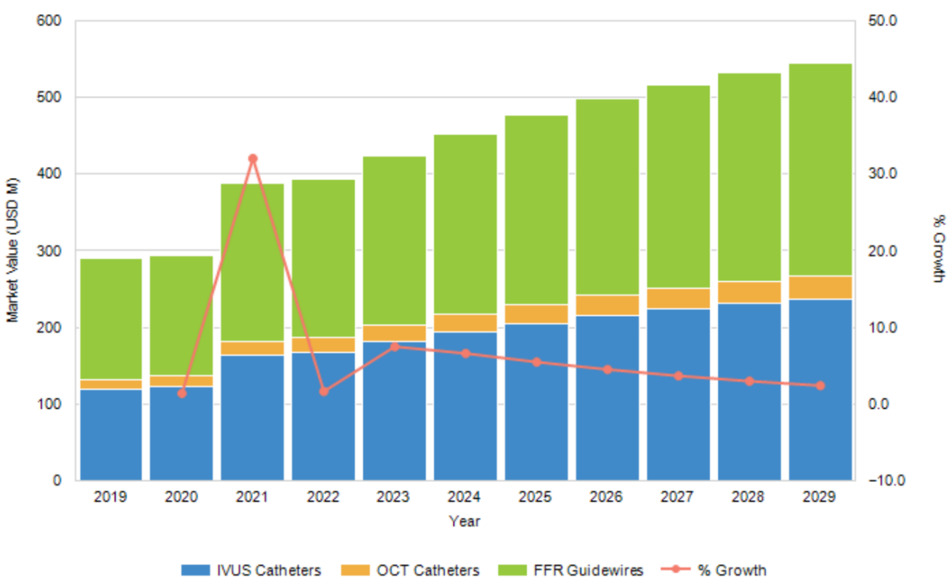

Figure 1.3: The US market for smart catheters used in the treatment of cardiovascular disease, 2019-2029.[19]

- The US market size for in-body imaging and sensing, including IVUS, OCT catheters, and FFR guidewires, has reached USD 390 million in 2021, with a strong potential to grow to USD 530 million in 2029, as shown in Figure 1.3.

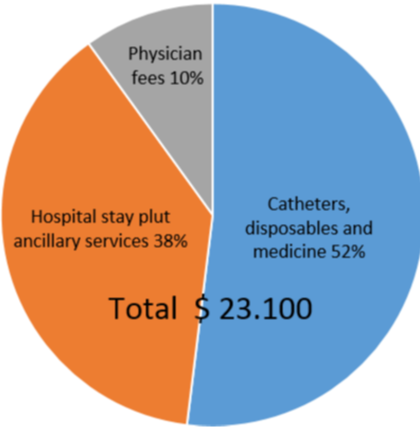

Figure 1.4: Cost composition of a typical PCI surgery

- Pressure and force sensing play an important role in catheter ablation to monitor the ablation depth and locate the ablation point. The expected 300,000 arrhythmia ablation procedures generate USD 525 million in potential catheter revenue annually[20].
- Device steering and tracking are mostly used in arrhythmia ablation. The European market alone amounts to USD 315 million at a growth of 10% CAGR[20]. When the technology matures, it will also find application in other catheterization procedures.
- Figure 1.4 shows a cost breakdown of a typical PCI surgery worth USD 23,100 per operation. The majority of the cost is contributed by catheters, disposables, and medicine [21]. Reducing the cost of catheters and disposables with advanced technologies can therefore contribute to a reduction in the cost of healthcare.

1.1.4. CATHETER TIP INTEGRATION: STATE OF THE ART

Essential and life-saving as these smart catheters are, they are without exception manufactured with outdated technologies. Although the first smart catheters were introduced in the early 1980s, there have been very few hardware technology innovations in the past decades, while users keep demanding catheters with better functionality, smaller dimensions, easier to operate, and at a lower price. The main reason for the lack of innovation is that these various catheters are manufactured with technological “point solutions”. Each point solution is optimum for solving individual specified problems or demonstrating certain functions. The lack of open platform technology hampers the solution sharings between the catheter applications. As a result, these point solutions cannot generate enough production volume and profit to support continuous innovation.

One of the most challenging procedures of smart catheter manufacturing is catheter tip integration. The tip consists of multiple submillimeter functional components, such as application-specific integrated circuits (ASICs), ultrasound transducers, pressure sen-

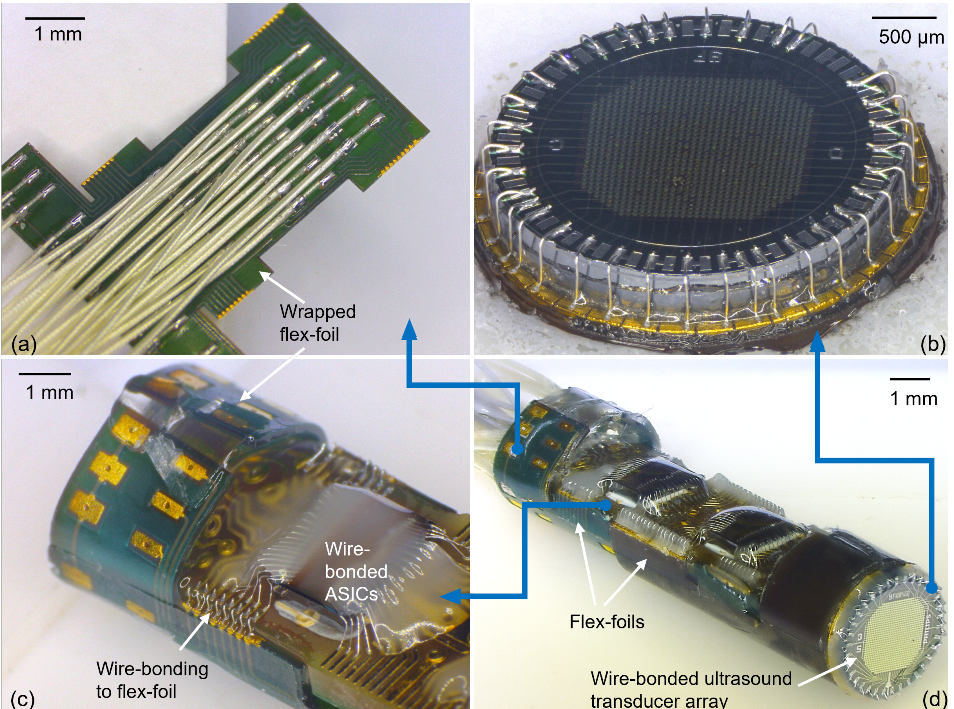

Figure 1.5: Forward-looking ICE catheter tip integrated with state-of-the-art flex-foil and wire-bonding assembly technologies. (a) Data transmission cables soldered to flex-foil. (b) A ultrasound transducer module wire-bonded to the substrate from its edge. (c) Challenging wire-bonding process to connect wrapped flex-foil to the ASIC chip from its edge. (d) A forward-looking ICE catheter tip assembled with conventional technologies[22]

sors, and passive components. Figure 1.5 depicts a forward-looking ICE catheter tip with a diameter of 3 mm manufactured with state-of-the-art assembly technologies. As shown in Figure 1.5a and c, some components are interconnected using standard flex-foil technology, which contains no functionality other than electrical connections. The flex-foil, which normally has a thickness of 40 μm, is too rigid to fold into an arbitrary shape to fit in smaller catheter tips. Other interconnections of components or modules are realized by wire-bond technology. Wire bonding in a catheter tip often has to be performed on nonstandard surfaces or limited bond areas, such as on the edge of the flex-foil or 90-degree corners, as in Figure 1.5b and c. Complex customized machine settings and special tools are necessary for these challenging wire-bond processes. In both integration methods, the component assembly process requires extensive manual tuning to achieve an acceptable yield, which is not robust, time-consuming, and costly. Moreover, each specifically developed assembly process is a "point solution" that cannot be applied for the manufacturing of other types of catheters. Therefore, introducing a scalable open platform technology for catheter tip integration is necessary to improve smart catheter performance and manufacturing at a lower cost. The open platform technol-

ogy will also allow for guiding the development of new generations of catheter products through well-defined and commonly accepted roadmaps.

1.2. THE FLEX-TO-RIGID (F2R) PLATFORM

1.2.1. BEYOND THE STATE OF THE ART

Flex-to-Rigid (F2R) is an interconnect platform designed for heterogeneous integration of electronic components in extremely small form factors, specifically suitable for smart catheter tip integration[23, 24]. It consists of multiple tiny thin silicon islands connected by extremely thin flexible interconnects. Various functional modules or components can be fabricated or assembled onto the thin silicon islands. Figure 1.6 presents a forward and side-looking ICE catheter demonstrator fabricated with the F2R technology platform. After the microfabrication, the device is suspended in a silicon frame using polymer tabs, as shown in Figure 1.6a. The device has thin silicon islands onto which ultrasound transducers are fabricated and a silicon island with bond pads. These silicon islands are connected by flexible interconnects with a thickness of less than 10 um. The device is released from the silicon frame by breaking the polymer tabs and mounted onto a 2-mm diameter catheter tip (Figure 1.6b, c).

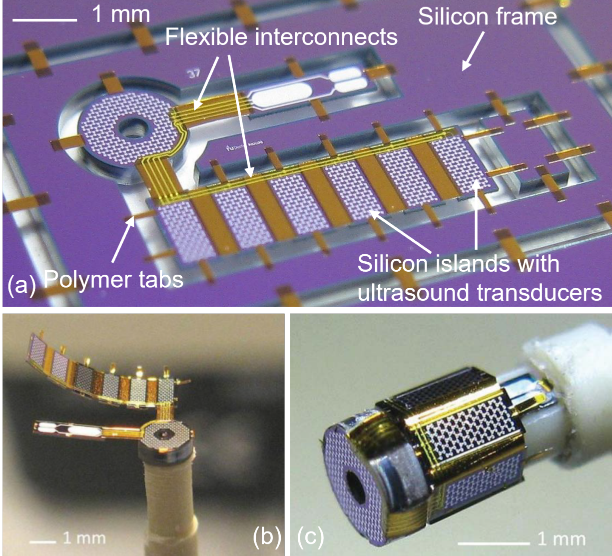

Figure 1.6: Forward and side-looking ICE catheter demo fabricated with the Flex-to-Rigid (F2R) technology platform. (a) the fabricated device is attached to the silicon frame with polymer tabs. (b) Mounting of the device released from the silicon frame. (c) Device mounted onto a 2-mm catheter tip.[25]

Comparing the two examples in Figure 1.5 and Figure 1.6, although the F2R platform might look similar to flex-foil technology at a glance, the F2R platform allows for aggressive dimensional scaling. F2R is based on IC-compatible microfabrication, which allows micron-precision pattern definitions, high-density wiring, and small-pitch bond

pads. At the same time, micro-fabricated devices, such as ultrasound transducers, sensors, and passive components, can be integrated onto the F2R thin silicon islands along with the F2R fabrication without the need for further assembly. The most special feature of F2R is that its semi-flexible structures can be easily bent, rolled, and folded into various configurations thanks to the flexible interconnects. The flexible interconnects in F2R are polymer-metal-polymer sandwiched structures with a thickness of less than 10 µm. The materials and the structure of the flexible interconnects enable a bending radius of 10 µm without failure[26]. This makes it possible to wrap the F2R structures around the catheter shaft, fold the electronics inside the catheter, and mount transducers on the tip of the catheter.

1.2.2. STANDARD F2R PROCESS

Flex-to-Rigid is based on standard micro-fabrication technology. It consists of three main technical stages, as shown in Figure 1.7. The standard F2R process is performed on a silicon-on-insulator (SOI) substrate with a device layer thickness of 40 µm, a buried-oxide (BOX) thickness of 500 nm, and a handle substrate of 380 µm. The thickness of the device layer is the final thickness of the F2R silicon islands and can be adjusted accordingly.

The first stage, as in Figure 1.7a, is the buried trench process, which is the core of the entire F2R concept. A plasma-enhanced chemical vapor deposition (PCVD) oxide is patterned into an oxide mesh mask that consists of sub-micron holes, as shown in Figure 1.8a-b. The customized silicon deep reactive etching process etches through the oxide mesh mask and merges into buried trenches in the SOI device layer, landing on the BOX layer. After the trench etching process, the oxide mesh mask is closed by depositing a second thick PECVD oxide layer, forming an oxide membrane, as shown in Figure 1.8c. In the SEM cross-section image of the closed oxide membrane Figure 1.8d, the original shape of the oxide mesh mask and the closing oxide can be clearly identified. The buried trenches define the outline of the F2R silicon islands. The oxide membrane closes the buried trench from the top to keep the wafer surface planar, allowing for further follow-up processing.

Following the buried trench process, the next critical stage is the device & interconnect fabrication, as depicted in Figure 1.7b. Depending on the application or design, ultrasound transducers, sensors, bond pads, or other passive components are fabricated on top of the wafer or embedded in the SOI device layer. The sandwich-structured flexible interconnects consist of an aluminum trace encapsulated by two polyimide layers, connecting the electrical components.

The last critical stage is releasing the F2R structures from the SOI handle layer, as shown in Figure 1.7c. After the buried trench process, the SOI device layer is already separated but still held in place by the SOI handle wafer. The silicon islands with the fabricated components and the flexible interconnects are released from the silicon wafer by removing the handle wafer that holds the thin silicon islands with a deep reactive ion etch (DRIE) from the backside of the wafer. The F2R structures are still attached to the silicon frame by the polymer tabs after the releasing process for ease of handling during fabrication. The polymer tabs can be dissected by laser to release the F2R structures from the silicon frame for further assembly steps.

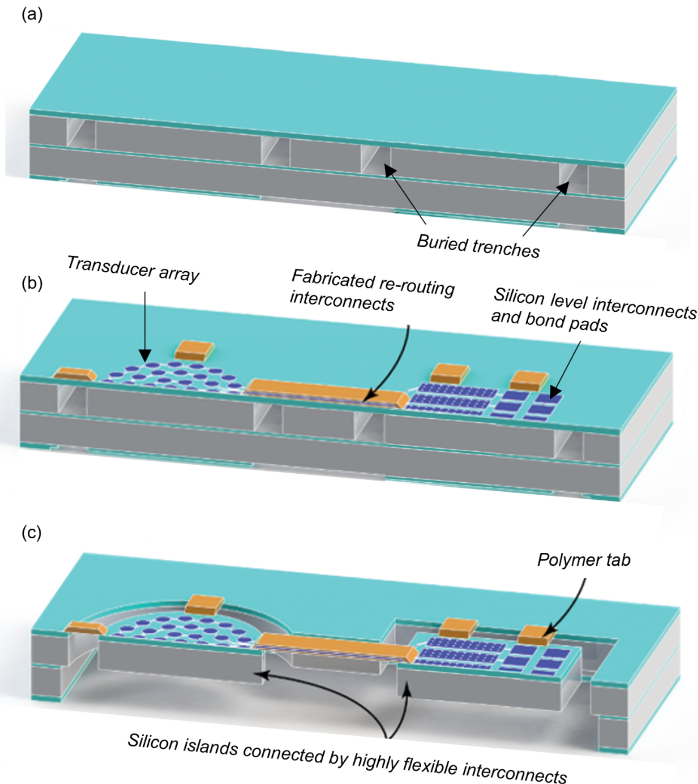

Figure 1.7: Three critical stages in the standard F2R process (thickness not drawn to scale). (a) Define outline of silicon islands in the device layer with buried trench process. (b) Fabricate devices, bond pads and flexible interconnects. (c) Release F2R structures by dry etching SOI handle layer from the backside of the wafer. [27]

1.2.3. F2R CHALLENGES

The buried trench process is one of the key process steps of the F2R technology. However, the buried trench process also brings many challenges to the F2R process. The lithography process for the oxide mesh mask is the first challenge. The mesh mask consists of sub-micron holes on a micron pitch. The critical dimensions of the oxide mesh mask are very sensitive to deviations in lithography, such as variations in humidity, photoresist thickness, and exposure focus or dose, resulting in a small process window. The next challenge is the trench etching process. The dry etching process etches the silicon substrate through the small holes on the oxide mesh mask. It starts with an isotropic etching to merge all the small holes into one trench and continues etching the trench, landing on the SOI BOX layer[29]. The limited in-outlet of the oxide mesh mask makes it extra difficult to merge the trench etching and maintain the etching profile.

Apart from these process challenges, the oxide membrane of the buried trenches naturally suffers from stress issues. Although the layer stresses of the oxide mesh mask and the PECVD closing oxide have been well-tuned to approach the zero-stress level, the ox-

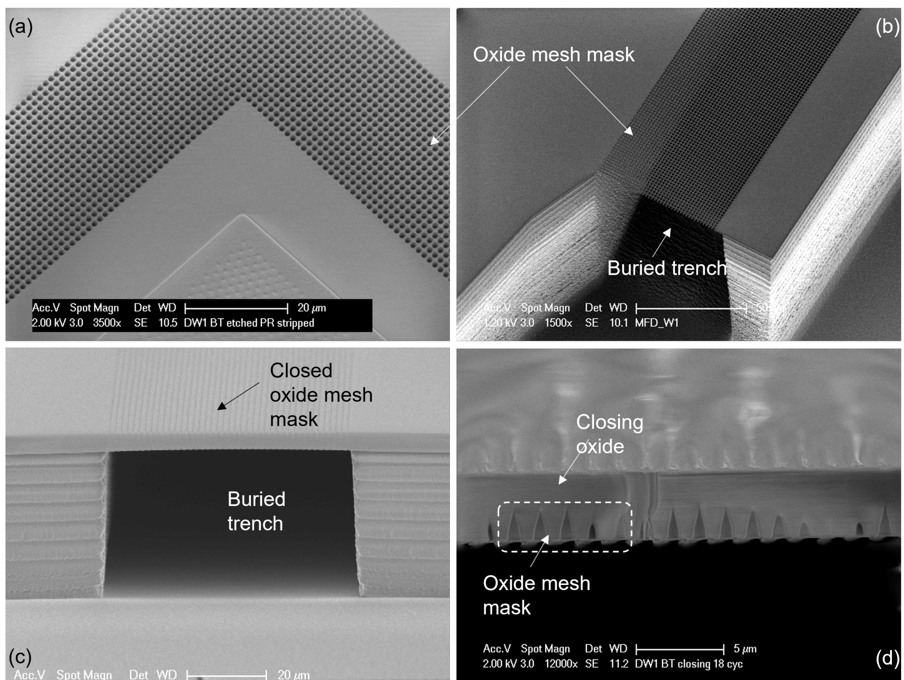

Figure 1.8: F2R buried trench process. (a-b) PECVD oxide is etched into oxide mesh mask first, then buried trenches are etched into silicon using the oxide mesh mask with DRIE process. (c) Cross-section of a buried trench closed by depositing a thick PECVD oxide layer on top of the mesh mask. (d) Cross-section of the closed membrane. [28, 29]

ide membrane is still very fragile when it exceeds certain dimensions (Figure 1.9a) or contains sharp corners. Moreover, the follow-up processes can also damage the oxide membrane. The high-stress thin films deposited on top of the oxide membrane can lead to bulging, buckling, or broken membranes. Certain processing conditions, such as high chamber pressure, high humidity, or high temperature, can also cause broken membranes, as shown in Figure 1.9b.

The F2R buried trench process is very delicate and requires extensive process development and monitoring, adding considerably to the costs of the F2R technology platform. A more robust, compatible, and low-cost process is therefore highly preferred.

1.3. THE IVUS CATHETER

The IVUS catheter is one of the most advanced smart catheter products on the market today. IVUS stands for Intravascular Ultrasound. It is used to make radial ultrasound cross-section images of the target coronary arteries. The IVUS catheter is used for the treatment of coronary artery disease with angioplasty surgery. As shown in Figure 1.10a, the IVUS catheter is an “over the wire device” that is shifted over a 360 µm diameter guidewire inserted into the artery, reaching the point of intervention. It can detect the nature and consistency of the blockage plaque inside the coronary artery, as shown in

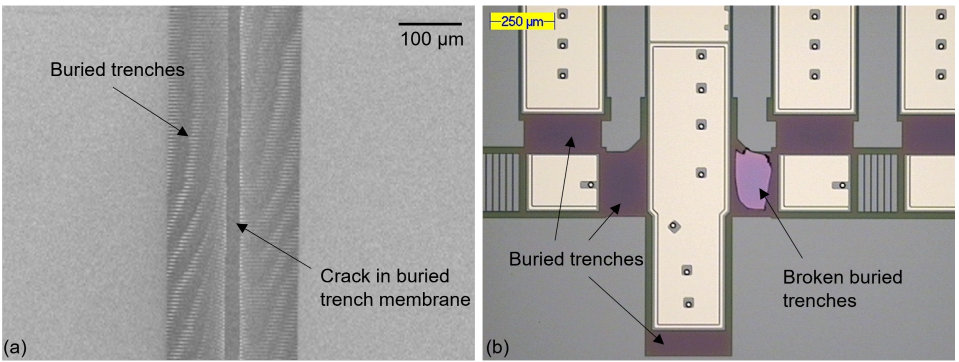

Figure 1.9: Broken buried trenches during the F2R process. (a) broken oxide membrane because of large dimension (200 µm wide). (b) Broken buried trenches during follow-up processes. [30]

Figure 1.10b. A healthy artery has a large opening in the middle of the ultrasound cross-section image, whereas the diseased artery is significantly narrowed down because of the plaque. The information about the blockage plaque, such as its shape, diameter, and length, finally helps to correctly place the stent inside the artery.

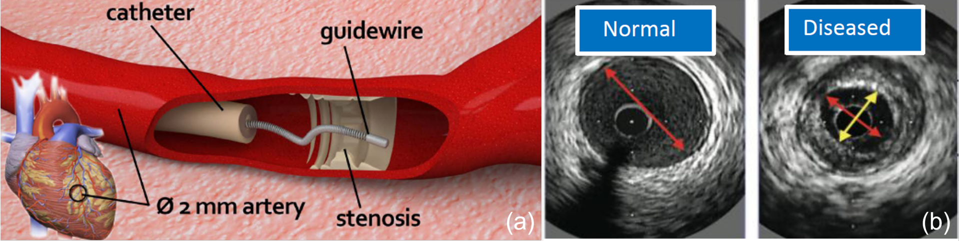

Figure 1.10: IVUS catheterization in a coronary artery. (a) A guidewire is inserted along the artery, reaching the point of intervention, and the IVUS catheter is shifted over the guidewire [reference]. (b) IVUS ultrasound cross-section image of a healthy coronary artery and a diseased artery. [31]

1.3.1. STATE-OF-THE-ART

Figure 1.11 depicts the smart tip of the Eagle Eye Platinum intravascular ultrasound catheter from Philips Volcano, the dominant product in the electronically scanned IVUS imaging catheter market. The outer diameter of this smart tip is 1.2 mm with a rigid length of approximately 9 mm. The ultrasound transducer consists of 64 piezo ceramic elements with a width of 55 µm and a length of 1 mm. This circular piezoelectric ultrasound array is first soldered onto a flex foil as one piece of piezoelectric ceramic material and then mechanically diced into 64 separate elements according to the required length, width, and thickness[10]. This ultrasound array integration process is challenging, time-consuming, and therefore expensive. As a result, scaling to high volumes is difficult.

The Eagle Eye catheter tip has five radially placed ASICs, mainly containing analog functions such as signal conditioning and multiplexing. The ASICs control each ultra-

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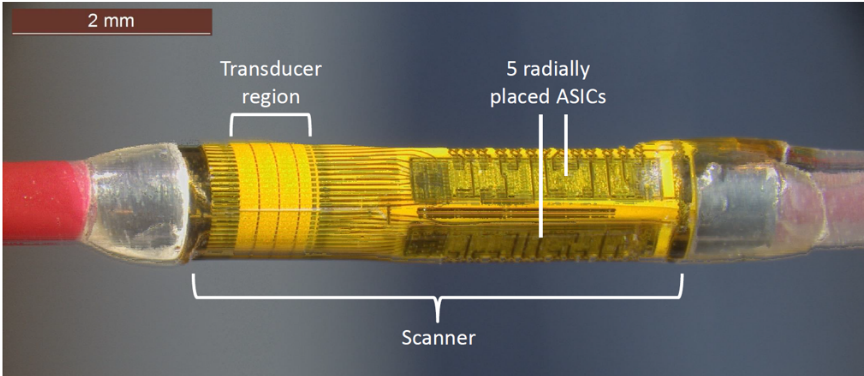

Figure 1.11: Smart tip of the Eagle Eye Platunum intravascular ultrasound catheter from Philips Volcano [32]

sound transducer element and drive them in transmit and receive mode. Using an optimized multiplexing, the number of electrical wires from the tip of the catheter to the proximal end can be reduced to 7[10]. These wires are manually soldered to the catheter tip, which is also time-consuming and expensive. Moreover, integrating the transducer array, ASICs, and wire connections with flex foil results in a rigid length of around 9 mm, which hampers the catheter tip from maneuvering freely in the narrow coronary arteries, one of the major drawbacks of this product.

The Eagle Eye Platinum IVUS catheter is an analog device based on technologies developed 15 years ago. New open platform technologies developed for the next generation of smart catheters will make it easier to integrate, smaller in dimension, better in imaging quality, and cheaper to produce.

1.3.2. AN F2R-BASED IVUS CATHETER

Figure 1.12 shows the first F2R-based IVUS catheter tip developed in the European project "INCITE" . This project demonstrated for the first time the integration of capacitive micromachined ultrasonic transducers (CMUTs) in an IVUS catheter in combination with the Flex-to-Rigid technology platform.

CMUTs resemble small "drums" that consist of two electrodes separated by a small vacuum gap, as shown in Figure 1.13. When an AC signal superimposed a DC bias is applied, the membranes of the "drums" vibrate and generate ultrasound. Conversely in the receive mode, the incoming ultrasound impinges on the CMUT membranes, causing voltage variances, and generating electrical signals. The CMUT fabrication process is also IC fabrication compatible and, therefore, can be smoothly integrated into the F2R platform. CMUTs are fabricated on the F2R silicon islands and attached to the silicon frame (Figure 1.13a). After being released from the silicon frame, the F2R structures are mounted on the catheter metal form, and the 96 CMUT ultrasound transducers are wrapped around the metal form (Figure 1.13b-d). Compared with the state-of-the-art Philips Eagle Eye IVUS catheter, the F2R-based IVUS catheter offers:

INCITE is part of the European Union's Horizon 2020 Research and Innovation Programme on the Topic CE-SPIRE-04-2019 - Efficient integrated downstream processes (Grant Agreement number 870023).

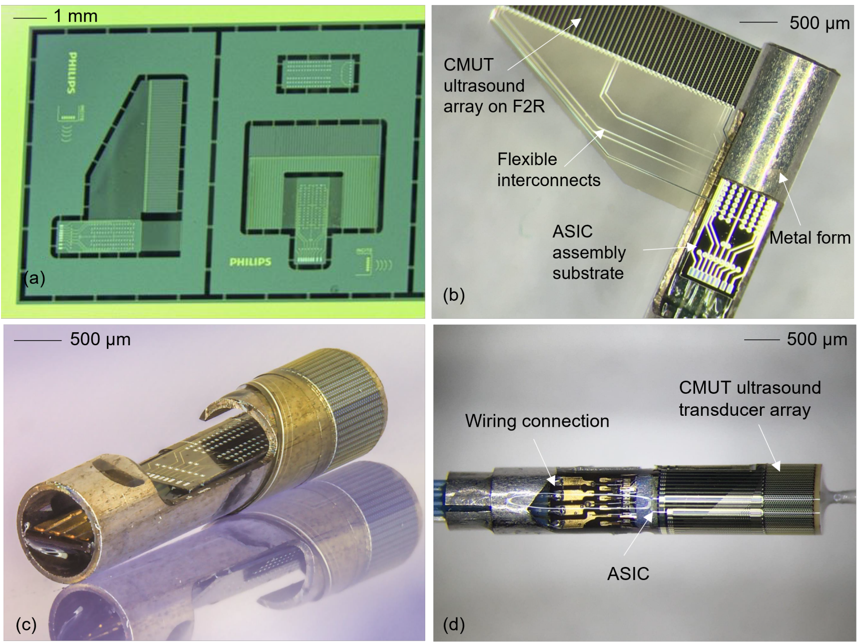

Figure 1.12: F2R-based IVUS catheter tip with CMUT ultrasound transducer demonstrated in the "INCITE" project. (a) Fabricated F2R-based catheter tip with CMUT transducers in silicon frame. (b) Device released from the silicon frame and mounted in a 1 mm diameter metal form. (c) 96 CMUT ultrasound transducers wrapped around the metal form. (d) Assembled and encapsulated catheter tip with ASICs and wire connections. [33]

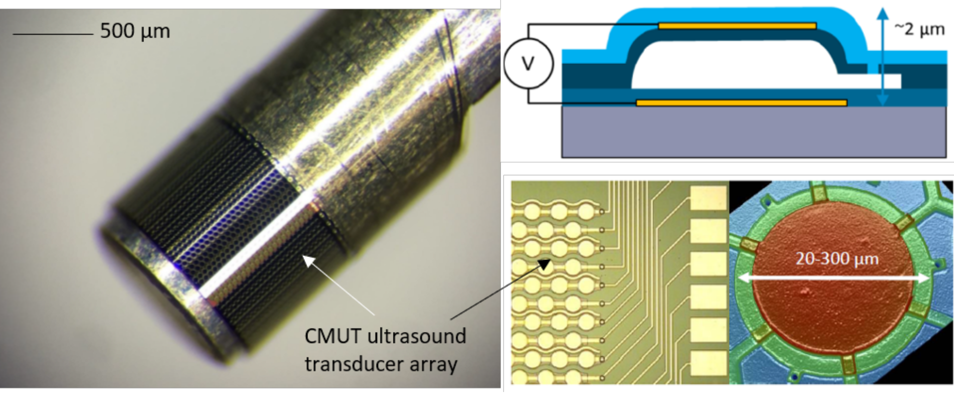

Figure 1.13: Capacitive micromachined ultrasonic transducers (CMUTs) fabricated on the F2R platform. [34]

- The straightforward integration of CMUTs in the F2R platform allows for a flexible design and reduces the need for time-consuming, challenging, and costly manual assembly steps.

- Higher-resolution imaging because of the increased number of ultrasound transducers (96 compared to 64).
- A smaller diameter (1 mm compared to 1.2 mm) and a shorter rigid length (6 mm instead of 9 mm), thanks to the higher interconnect densities and ultra-flexible feature of the F2R platform.

1.4. SCOPE AND OUTLINE OF THIS THESIS

1.4.1. SCOPE OF THE THESIS

The work presented in this thesis is part of the ECSEL-funded European project "A pilot line for the next generation of smart catheters and implants (POSITION-II)," [1]. The POSITION-II project connects 45 partners from academia and industry located in 12 different countries in Europe, aiming to realize innovations in smart catheters and implants by introducing open technology platforms, such as Flex-to-Rigid, for miniaturization, in-tip AD conversion, wireless communication, MEMS transducer technology, and encapsulation [35]. These open platforms, available to different users for multiple applications, allow manufacturers to improve the smart catheter performance at a lower cost. Moreover, the open-platform approach enables the fast development of new smart minimally invasive instruments.

The goal of this thesis work was to design and develop new advanced technology modules and process steps that further enhance the F2R technology platform. In the first part of the thesis, a submillimeter optical data link module is designed, fabricated, and tested that allows for data rates up to 25.8 Gb/s for future digitized smart catheter products. Next, a process module was developed that allows for the integration of high-density trench capacitors in F2R, eliminating the need for additional discrete passive components. Finally, a cavity-BOX process module was developed, which is a robust alternative for the delicate buried trench process in F2R.

1.4.2. OUTLINE OF THE THESIS

The first part of the thesis comprises Chapter 2 and Chapter 3, focusing on the optical data link module (ODLM). **Chapter 2** starts by introducing the need for optical data transmission in digital smart catheters and the fiber-optic fundamentals. Different ODLM designs for a digital IVUS catheter are developed. The chapter also presents the ODLM fabrication details and results. Some key process optimizations during the device fabrication are discussed.

Chapter 3 includes the assembly and characterization of the ODLM. The fabricated ODLM was assembled into two forms: stand-alone ODLM and ODLM with a customized laser driver. The stand-alone ODLM was used to test the maximum optical data rate, and the other assembly form was fabricated for final integration in the smart catheter tip. Both assembly forms were characterized by eye diagrams. The ODLM with a customized laser driver was also integrated in a digital ICE catheter system in a lab-setup format, demonstrating the functionality of the ODLM. The chapter ends with a discussion of the ODLM from its industrialization perspective.

[1] grant no: Ecsel-783132-Position-II-2017-IA

The second part of the thesis starts in **Chapter 4**, which introduces the high-density embedded decoupling trench capacitors in the F2R platform. First, a stable trench capacitor process was developed, compatible with the F2R platform fabrication. Key processes such as trench closing and high-aspect-ratio DRIE process development are discussed. Next, F2R-based cantilevers with embedded trench capacitors were simulated with FEA modeling and fabricated to study the stress introduced in the trench capacitor integration.

In **the final section** of this thesis, the advanced cavity-BOX SOI substrate is introduced to simplify the standard F2R process. An F2R-based deep brain stimulation (DBS) probe demonstrator [2] was produced with the cavity-BOX SOI instead of the standard F2R process as a proof of concept. To enable the industrialization of the cavity-BOX SOI, the overlay-matching between the cavity-BOX structures and the device layer patterns on the SOI substrate is studied. Experiments were performed to align the lithographical compatibility between the foundry and the SOI manufacturer.

Finally, **Chapter 6** contains the conclusions and future research recommendations.

[2] Deep brain stimulation (DBS) prob is an advance neurostimulation implat. An F2R-based DBS prob is under development in the European project InForMed (grant no: 2014-2-662155) lead by TU Delft

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2

Optical Data Link Module (Part 1)

Parts of this chapter have been published in [1, 2, 3]

2.1. BACKGROUND

2.1.1. FROM ANALOG TO DIGITAL CATHETERS

As introduced in the previous chapter, smart catheters on the market vary in function and dimensions. However, they are all, without exception, analog devices. Most imaging catheters have transducers or sensors integrated at the distal tip of the device. A collection of coaxial or twisted pair cables connects the distal tip through the catheter to the interface connector at the proximal end of the catheter. Some more advanced imaging catheters, such as the Philips Eagle Eye Intra Vascular Ultrasound (IVUS) catheter, have embedded ASICs at the smart tip of the catheter for signal control or pre-conditioning. The collection of high-frequency wires transmits the analog signals generated by the transducers or ASICs to the proximal end of the catheter for data analysis or image processing (Figure 2.1).

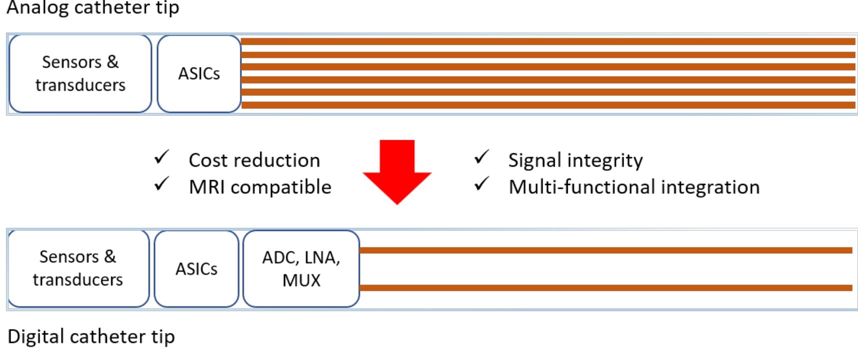

Figure 2.1: Digitization of smart catheters

The next generation of catheters is expected to have digitization at the tip of the catheters. Integrating modules, such as analog to digital converter (ADC), low noise amplifier (LNA), and multiplexer, the smart digital catheters bring the following benefits:

- *Signal integrity*
  The most crucial reason to digitize the analog catheter is to improve the signal integrity. The analog signals generated at the distal tip of the device need to be transmitted through the catheter to the proximal end of the catheter by high-frequency wires. Distortion of the signal transmission can be caused by the impedance of the transmission cables, interference from other electronics in the catheter lab, and a noisy connecting interface at the proximal end of the catheter. Digitization of the catheter ensures reliable and robust transmission of the generated digital signals, which directly impacts the output data and image quality.

- *Cost reduction*
  For advanced imaging catheters that require multiple signal channels, the number of cables that need to be integrated into the tip of the catheter is even larger. It is often underestimated how expensive it is to assemble a smart catheter, especially a smart

catheter with a dimension scale of only a few millimeters. Most cables have to be manually connected because of their small form factor. In fact, the cost to connect a large number of cables and assemble the catheter tip can easily amount up to 80% of the total catheter cost[4]. Digitization of the catheter tip will enable the serialization of the input & output channels, significantly reducing the number of cables needed in the catheter. As a result, the assembly cost will be reduced.

- *Multifunctional integration*
  The diameter of most catheters is on a scale of a few millimeters. All the transducers, sensors, ASICs, and cables have to fit inside the limited space of the catheter tip. Due to the digitization of the catheter tip, the large number of cables can be reduced. Hence, more space will be available in the catheter to integrate other functional modules, such as force sensors, pressure sensors, or temperature sensors [5, 6, 7, 8]. Moreover, digitizing the signals will enable the possibility of optical data transmission from the catheter tip to the proximal end.

- *MRI-compatible smart catheters*
  It is expected that better diagnostic or treatment can be achieved if smart catheters can work in combination with MRI[9, 10, 11]. However, traditional analog catheters with electrically conductive cables can not be used in the strong pulsating magnetic field of an MRI. M. van der Mark and M. Pekar have developed a technology to optically power smart catheter circuits and transmit data simultaneously with one single optical fiber With optical fibers replacing conventional electrical cables[12, 13], smart catheters can be used in combination with MRI in the future. This is only possible after the digitization of the catheters.

2.1.2. FROM ELECTRICAL TO OPTICAL DATA TRANSMISSIONS

To further understand the data transmission inside a digitized smart catheter, a digital IVUS catheter is presented here as a case study[14]. Figure 2.2 shows the data transmission schematics in a single-channel digital IVUS catheter. There are 96 ultrasound transducers integrated on the catheter tip. The ultrasound pulse signal is generated by the proximal backend PC and transmitted through a twisted-pair cable to the channel-selection module. The channel-selection module activates one of the ultrasound transducers to emit an ultrasound signal to the surrounding tissue. In the meantime, the adjacent ultrasound transducer is switched to the receiving mode. The adjacent ultrasound transducer receives the reflected ultrasound signal from the surrounding tissue and then transmit it to the signal processing integrated circuits (IC). These contain a low noise amplifier (LNA), an analog-to-digital converter (ADC), a coding circuit, and other pre-process modules. The signal processing IC converts the received analog ultrasound signal into a coded digital signal and then transmits it back to the backend PC through an output transmission cable. The output data rate for such a single-channel digital IVUS catheter can be roughly calculated with some estimated reasonable specifications. The working frequency of the ultrasound transducers is 40 MHz. Assuming the ADC sample frequency is 100 MHz (according to Nyquist–Shannon sampling theorem) and the ADC resolution is 10 bit, the ADC generates a data rate of 1 Gb/s. With a coding redundancy of around 20%, the final data rate needed should be at least 1.2 Gb/s (Eq. 2.1). This is

the minimum data rate requirement for a digital smart catheter and the starting point of this thesis work.

$$Data\,rate = Sample\,frequency \times Resolution \times (1 + Coding\,Redundancy) \quad (2.1)$$

A data rate of 1.2 Gb/s is already reaching the limit of copper transmission cables. To further increase image quality and frame rate in the future, the digital catheter can activate multiple emitting and receiving ultrasound transducers simultaneously. As a result, each receiving ultrasound transducer will require an ADC for signal processing and generating data at a rate of 1.2 Gb/s. After serialization, the total data rate of the multi-channel digital IVUS catheter will be 1.2 × N (number of receiving transducers) Gb/s. The high data rate is a design challenge for conventional high-frequency transmission cables, as it adds to extra design complexity and cost. Optical fibers, however, have a natural advantage in providing high-speed data transmission.

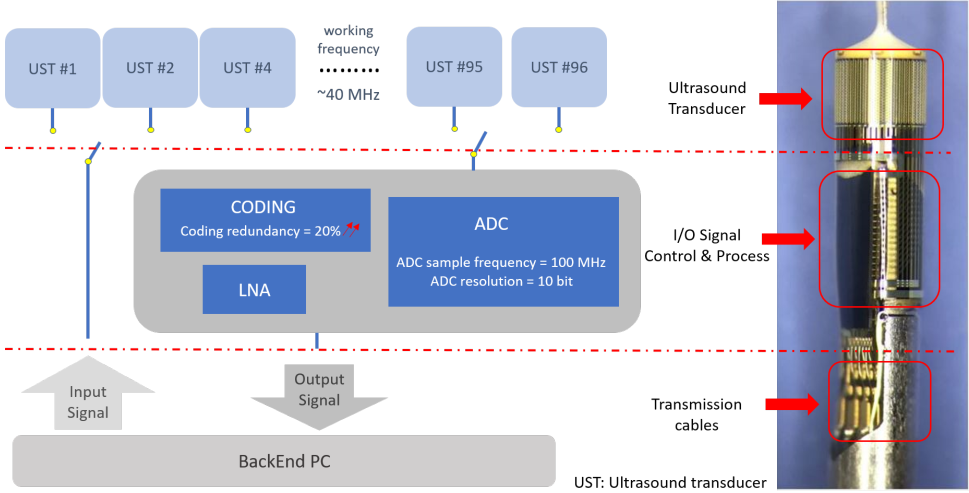

Figure 2.2: Data transmission in a single-channel digital IVUS catheter

2.1.3. FIBER-OPTIC FUNDAMENTALS

The history of fiber optics in communication can be traced back to the 1960s. After decades of development, it is now widely used to transmit voice, video, or data through various systems and networks with various functionalities[15]. Optical signals propagate through optical fibers and enable high-speed data transmission of data from a few Gb/s up to a few Tb/s per fiber, with very low signal loss (generally less than 0.4 dB per km for single mode fibers)[16, 17, 18]. This excellent data transmission capacity has brought enormous changes in the telecommunication field, with the rapidly developing internet as a good example. The application of fiber-optics has a few advantages over conventional copper high-frequency cables:

- Extremely high bandwidth that allows for Gb/s level data rates;
- Low power loss;
- Resistance to electromagnetic interference, hence MRI compatible;
- Lightweight and small in dimension.

Unlike coaxial or twisted-pair cables that can be directly connected to a PCB board, the optical data transmission system usually consists of three main modules: optical transmitter, optical fiber, and optical receiver (Figure 2.3). The optical transmitter converts the electrical input signal into the optical form; the optical signal is transmitted through the optical fiber, reaching the optical receiver; the optical receiver converts the optical signal back to an electrical output.

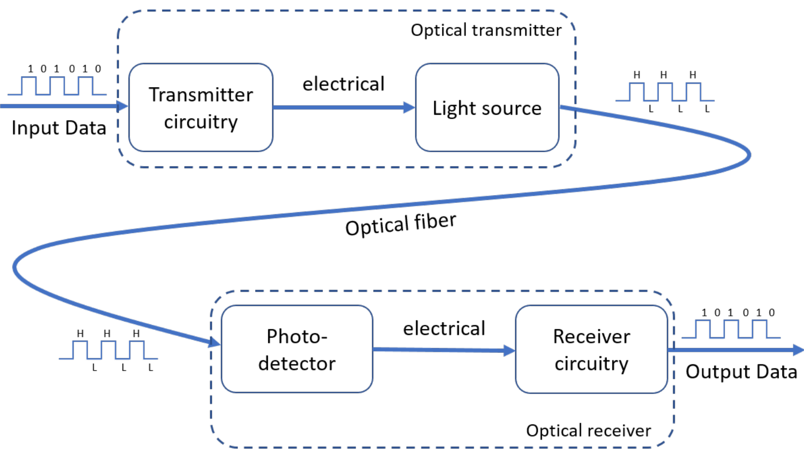

Figure 2.3: Basic composition of an optical data transmission system[19]

OPTICAL TRANSMITTER & RECEIVER

The optical transmitter consists of the transmitter circuit and a light source. The transmitter circuitry normally contains a voltage or current modulation circuit, which powers and modulates the light source. The light source is normally a semiconductor such as a LED or a laser. To transmit optical signals, the light source is modulated by switching it on and off, or in most cases, the light source remains on and is modulated in intensity. The data rate of the optical transmitter is defined by the modulation speed of both the transmitter circuit as well as the light source. The electrical connections between the light source and transmitter circuit, such as the fiber coupling, also play an important role in the achievable maximum data rate.

The most used light sources for data communication are listed in Table 2.1. Although an LED is cheaper compared to a laser, the laser has great advantages in the fiber-optic domain. Lasers have a faster modulation response, which allows for higher data rates. The laser beam divergence is smaller compared to an LED, making the fiber coupling

more efficient. An LED, in addition, often must compensate for the bad beam divergence with a higher power, which leads to higher power consumption. The most used laser diodes are edge-emitting lasers (EELs) and vertical-cavity surface-emitting lasers (VCSELs). The EELs emit light from the side, and the VCSELs emit light perpendicular to the surface of the chip. Both VCSELs as well as EELs have been well established in the optical-electrical field. Due to fabrication limitations, EELs can only be characterized at the end of the manufacturing phase, lowering their production yield and resulting in higher costs [20]. Because of their elliptical beam shape and larger beam angle, EELs often require extra optical components, such as a back facet monitor, to couple them to optical fibers with high alignment accuracies. Moreover, EELs, in general, have higher electrical power consumption as well. Contrary to EELs, VCSELs allow testing along the fabrication process, which lowers the cost. VCSELs also provide excellent beam quality and lower power consumption, making them more suitable for fiber coupling and system integration.

Table 2.1: Comparison of VCSEL, EEL, and LED[21, 22, 23, 24]

Parameter	VCSEL	EEL	LED
Beam Shape	Circle	Elliptical	Circle
Beam angle	< 20°	~ 40°	~ 120°
Wavelength	850-1550 nm	850-1550 nm	400-1300 nm
Wavelength drift	0.06nm/°C	0.3nm/°C	0.3nm/°C
Spectral Width	< 1 nm	~ 2 nm	20-30 nm
Modulation freq.	40 GHz or more	26.5 GHz or more	Hundreds of MHz
Electrical Power	< 20 mW	~ 60 mW	~ 60 mW
Optical Power	~ 5 mW	~ 10 mW	~ 1 mW
Cost	Low	High	Low

The optical receiver is the inverse device of the optical transmitter and comprises a photodetector and receiver circuitry[25]. The photodetector, mostly made of III-V semiconductor materials, converts the received optical signal into an electrical signal. The receiver circuit pre-amplifies the signal, filters, and processes it. The response time of the photodetector and the receiver circuit is as important as it is for the optical transmitter. Furthermore, the noise generated in the receiver is another important factor since it determines the lowest signal level that can be detected.

OPTICAL FIBER

A schematic cross-section of an optical fiber is shown in Figure 2.4. Most of the fiber core is made of glass, with a diameter ranging from a few micrometers to 62.5 µm[16]. A cladding material with a lower refractive index surrounds the core. The light is confined in the core by the phenomenon of total internal reflection, which ensures that the optical fiber acts as a waveguide for optical data transmission. Different combinations of core and cladding materials define the characteristics of optical fibers, such as mode

numbers, dispersion, polarization, and transmission loss. A buffer coating is applied to protect the fiber from moisture and damage. The entire fiber is finally encased in a jacket, usually a colored thick polymer that provides the last layer of protection and adds strength to the fiber.

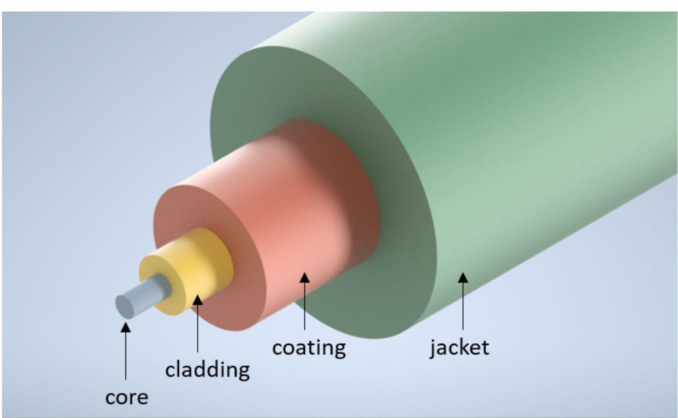

Figure 2.4: Cross-section of an optical fiber

Optical fibers can be classified into multi-mode and single-mode fibers depending on the core diameter. Multi-mode fibers have large core diameters of 50 to 62.5 µm, which allows transmitting multiple light modes and simplifies the fiber coupling. However, the large core diameter results in high modal dispersion losses during optical transmission, limiting the transmission distance to 200-500 m. On the other hand, single-mode fibers have only 5 to 10 µm core diameters, which significantly suppresses modal dispersion, allowing for optical data transmission up to a few kilometers[26].

Losses in optical fibers can be categorized into different types. The main intrinsic losses in an optical fiber are absorption, dispersion, and scattering loss, depending on the material of the optical fiber and its structural defects. The extrinsic losses are mostly from splicing between the fibers, fiber-laser connections, and bending loss. For multi-mode fibers, the fiber loss is up to 3.5 dB/km, and the fiber loss for single-mode fibers can be below 0.4 dB/km[27].

FIBER COUPLING

There are various ways to realize fiber coupling configurations. The fiber coupling mostly uses a pigtail fiber, which has one side of fiber striped and cleaved, and the other side fitted into a standard fiber connector (e.g., LC, FC). For high-accuracy alignment, the cleaved side of the fiber is aligned to a laser that is switched on. The other side of the fiber is connected to an optical power meter, which gives feedback during the alignment of the cleaved side until the best alignment position is found. This alignment method is called active alignment. Compared to active alignment, which uses optical feedback to adjust the alignment position, passive alignment relies on optical interposers to guarantee a good alignment. Hsiao et al. reported a silicon optical bench (SiOB) for a compact passive alignment of a 4-channel × 2.5 Gb/s optical interconnect module, as shown

in Figure 2.5 . The SiOB is a patterned and etched silicon substrate that acts as an assembly platform for the integration of lasers, photodetectors, micro-reflectors, fibers, and other optical or electrical components. The reported SiOB contains silicon V-shape grooves and 45-degree micro-reflectors. The optical fibers can be fixated in the V-shape grooves and orientated with respect to the micro-reflectors. The electrical contact layout of the lasers is based on the calculated relative position between the fibers, micro-reflectors, and lasers. Therefore, all the components are passively self-aligned by design after the assembly. Although active alignment can achieve higher alignment accuracy, its assembly scheme is rather complex. Passive alignment with optical interposers and multi-mode fibers can provide reliable optical connection and simplified integration for short-distance optical data communication applications, such as data centers[28], optical interconnects[29], and smart catheters.

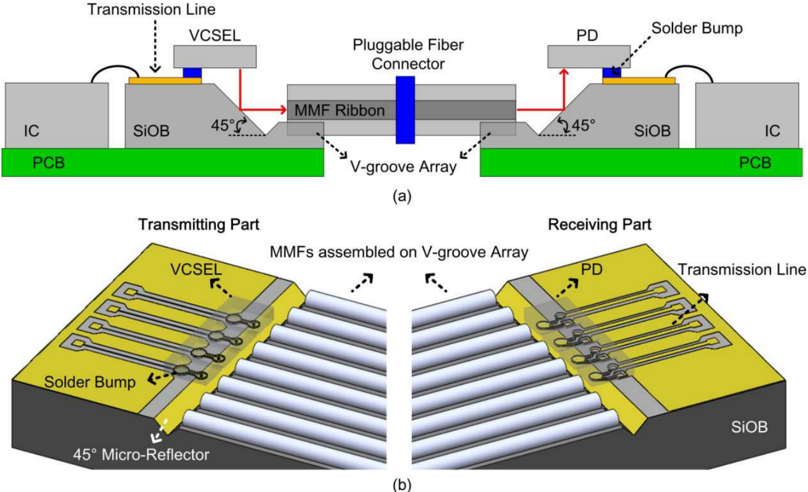

Figure 2.5: Schematic diagrams of the proposed optical interconnect module based on the SiOBs. (a) Side-view drawing. (b) top-view drawing.[30]

2.1.4. OPTICAL LINK IN IVUS: DESIGN REQUIREMENTS

The main challenge for all smart catheters is the limited available space at the distal catheter tip. In 2012, Fandrey et al. reported on a small optical link that fits in a catheter with a diameter of 2.33 mm[31]. However, the extremely small scale of the IVUS catheter requires further miniaturization. As shown in Figure 2.6, the distal tip of the IVUS catheter has a cylindrical outer diameter of 1 mm and a rigid length of approximately 8 mm. There is a guidewire lumen at the center of this cylindrical shape with a diameter of 500 µm. With this lumen, the IVUS catheter runs over the guidewire and is led to the location of the intervention. The only available space in the IVUS catheter is the narrow gap of around 200-300 µm in between the outer wall of the catheter and the guidewire lumen. Just as the other electronic components, power wires, and transmission cables, the Optical Data Link Module (ODLM), should also fit within this gap.

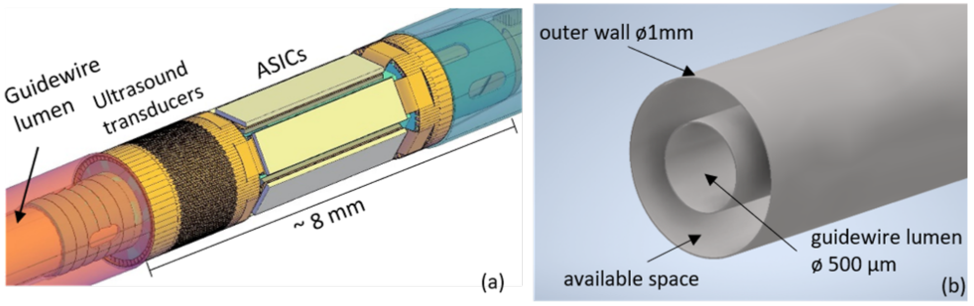

Figure 2.6: Schematic drawing of the digital IVUS tip. (a) 3D modeling[32]; (b) Cross-section view of the catheter tip, showing limited space for functional integration

In addition, integrating an optical link into such an IVUS catheter raises assembly challenges. The IVUS catheter smart tip is an advanced micro-electromechanical (MEMS) system consisting of multifunctional integrated stand-alone components, including an ultrasound transducer array fabricated on an F2R flexible substrate, application-specific integrated circuits (ASICs), and other passive devices. In the final integration step, these components are all manufactured separately and assembled onto a thin, flexible PCB. This 40 µm-thick flexible PCB with all the components wraps around the central lumen, making the most use out of the limited available space in the catheter tip. The optical link should be mass-producible and must be a stand-alone device to align with the overall standard catheter assembly protocol.

Finally, it is also important to take into account the coupling of the VCSEL to the fiber. In the case of the IVUS catheter, the data communication distance is slightly longer than the catheter length, approximately two to three meters. Therefore, the optical signal loss is less affected by signal attenuation and dispersion due to the short transfer distance but is more affected by the alignment accuracy of the fiber to the laser. The fiber coupling must be reliable enough to survive multiple bending during the catheter surgery procedure. Moreover, the alignment between the optical fiber and the optical source must be well guaranteed. A precise self-alignment feature in the optical interposer is highly preferred to minimize assembly complexities.

Based on the specifications and issues stated above, several design requirements for an optical interposer for the digital IVUS catheter are summarized below:

- Fit in the gap of 200-300 µm in the IVUS catheter;
- To be assembled to a flex-PCB as a stand-alone component;
- Provide a reliable connection and proper fiber alignment, preferably by self-alignment;
- Mass producible.

2.1.5. GOAL STATEMENT & CHAPTER GUIDANCE

The trend towards better image quality is driving the development of smart catheters from analog to digital processing and from electrical to optical data communication.

The goal of this work was to design and fabricate an Optical Data Link Module (ODLM) that fits inside the limited space in the digital IVUS catheter tip and provides a data rate of at least 1.2 Gb/s. As introduced in the previous chapter, the F2R technology has great advantages in miniaturized system integration. Furthermore, F2R has been well established in the cleanroom of Philips MMD for smart catheter production. Therefore, we chose to build our ODLM based on the F2R technology. This ODLM also fits in other smart catheters for optical data communications.

The ODLM description is split into two chapters in this thesis. In this chapter, we first discuss the designs of the ODLM. Next, the detailed F2R-based ODLM process flow and the fabricated ODLM device will be presented. Finally, some process optimization is discussed. The ODLM assembly and characterization parts will continue in the next chapter.

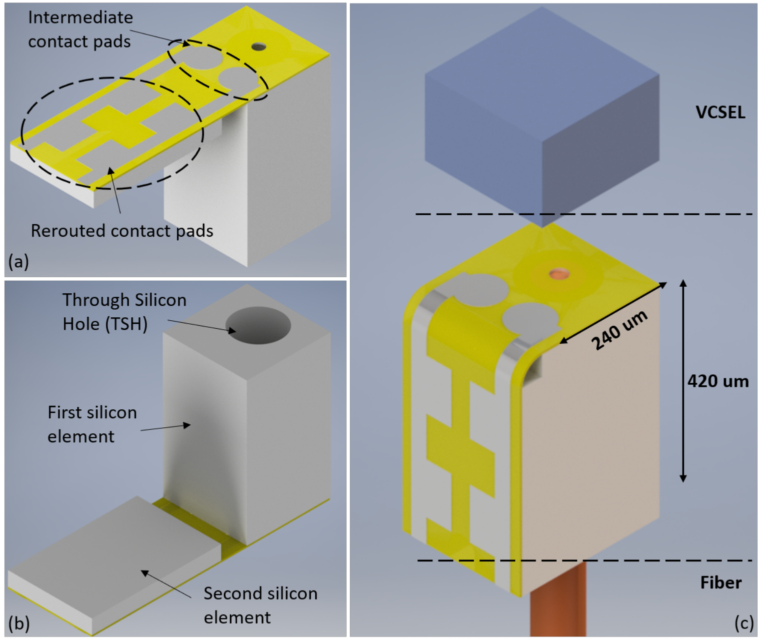

Figure 2.7: ODLM design. (a) Unassembled ODLM; (b) backside view of unassembled ODLM; (c) ODLM with flip-chipped VCSEL and inserted optical fiber.

2.2. DESIGN OF ODLM FOR A DIGITAL IVUS CATHETER

The optical data link module comprises three parts. The first part is a micro-fabricated F2R silicon interposer. The second part is a commercially available Vertical Cavity Surface Emitting Laser (VCSEL), with its electrical contacts and laser emitting spot on the same surface. Due to the tight space in the catheter tip, the selected VCSEL (ULM850-14-CHIPS) only has a dimension of 240 µm × 240 µm × 150 µm[33]. The final part is a 125 µm diameter optical fiber. The F2R silicon interposer incorporates flexible interconnects to

reroute the VCSEL's electrical contacts to a plane perpendicular to the surface of the VCSEL. This design enables the optical link module to be mounted on a flex-PCB within the limited space available in the catheter. At the same time, the VCSEL is optically aligned and connected to a fiber running in parallel to the catheter shaft.

Figure 2.7 presents different views of the ODLM design. The F2R interposer in Figure 2.7(a-b) consists of two silicon elements connected by 6 µm-thick flexible interconnects. The first silicon element is a cuboid-shaped element with a planar dimension of 240 µm × 240 µm and a thickness of 420 µm. The intermediate contact pads for the VCSEL connection are fabricated on the 240 µm × 240 µm top surface. A through-silicon hole (TSH) located at the emitting area of the VCSEL connects the backside to the front side of the structure. The VCSEL is flip-chipped onto the intermediate contact pads with the laser emitting spot aligned to the TSH. Both the TSH and the intermediate contact pads are designed according to the VCSEL layout. Therefore, a multi-mode optical fiber inserted into the TSH from the bottom side will be self-aligned to the laser emitting spot of the VCSEL on the other side (Figure 2.7(c)). The flip-chip assembly techniques guarantee an alignment accuracy within 5 µm [34]. This is sufficiently accurate to align a standard multi-mode fiber. The TSH also serves as a mechanical support for the multi-mode optical fiber. With a small amount of (epoxy) adhesive, the fiber can be fixated in the optical TSH, and a reliable connection can be guaranteed.

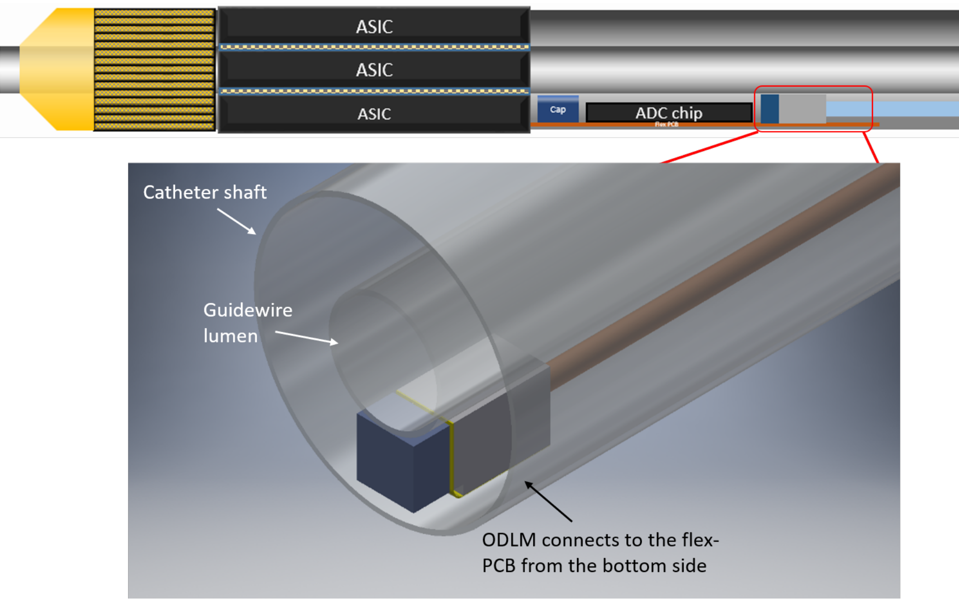

Figure 2.8: Schemetic drawing of an IVUS smart catheter tip with ultrasound transducers, ASICs and other discrete components. The ODLM is at the end of the catheter tip, connected to the flex-PCB and fit in the 200-300 µm gap.

The second silicon element has planar dimensions of 240 µm × 380 µm and a thickness of 40 µm. The rerouted contacts for the PCB connection are fabricated on top of the 240 µm × 380 µm surface. Flexible interconnects connect the rerouted electrical contacts

to the intermediate contact pads on which the VCSEL is mounted. Initially, after the fabrication, the rerouted contact pad surface of the thin silicon element is in the same plane as the intermediate contact pad surface of the cuboid silicon element. The flexible interconnect allows the folding of the thin silicon element by 90 degrees onto the side of the cuboid silicon element, where it is attached with an adhesive, as shown in Figure 2.7(c). Hence, the folding separates the VCSEL laser emitting spot and the rerouted electrical contacts into perpendicular planes. After the assembly, the final size of the entire ODLM is 240 μm × 280 μm with a height of 420 μm. The dimensions are adjustable based on the choice of the VCSEL. By connecting the rerouted electrical contacts to a flex-PCB, the optical link module acts as a stand-alone device that can be positioned inside the 200-300 μm gap inside the IVUS catheter and other components shown in Figure 2.8.

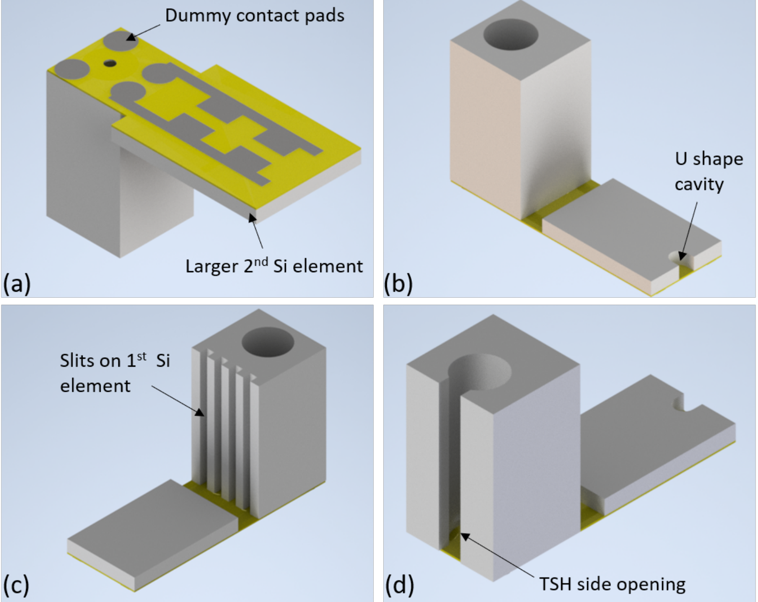

Figure 2.9: ODLM design variation (a) with larger 2nd silicon element; (b)with an U cavity on the 2nd silicon element; (c) slits on the side of the 1st silicon element; (d) opening on the side for TSH etch

Apart from the standard ODLM design, different ODLM design variations were also developed to anticipate possible assembly or fabrication issues. A few variations are shown in Figure 2.9. The variations have two extra dummy contact pads on the 240 μm × 240 μm top surface of the first silicon element. Supportive structures (gold bumps or solder bumps) can be placed on these dummy pads so that the VCSEL will remain horizontal during the VCSEL soldering process. Furthermore, an adhesive will be used in the bending & fixation step of the second silicon element. Controlling the excessive adhesive during the assembly is challenging, especially on such small devices. In Figure 2.9(a), the second silicon element is 50 μm larger than the side of the first silicon element. Figure 2.9(b) shows a small U shape cavity in the second silicon element. These small design changes are incorporated to constrain the extra adhesives during the device assembly. In

the design Figure 2.9(c), slits are created in the sidewall of the first silicon element for the same purpose. Finally, an extra side opening to some TSHs was added, enabling process of for the TSH etching process (Figure 2.9(d)).

2.3. DEVICE FABRICATION

The optical link module fabrication flow is designed based on the interconnect integration platform Flex-to-Rigid (F2R) introduced in the previous chapter. Similarly, it includes three technically critical stages. The buried trench process, in the first place, defines the outline of the design from the front side. Next, flexible interconnects and electrical contacts are fabricated according to the optical link module design. Finally, the silicon substrate is etched to create the cuboid silicon element and release the whole device. Although the TSHs in the designs only have an aspect ratio of around 1:4, they must be etched in the same backside etching step together with the large openings needed to release the whole device. Therefore, a two-step etching process was developed to create straight profile TSHs, and in the meantime, prevent the large openings from over-etching too much. The complete process flow is presented first with cross-section drawings, followed by the processing results at the end of this section.

2.3.1. GENERAL PROCESS FLOW

The schematic representation of the fabrication flow of the ODLM F2R interposer is shown in Figure 2.10. The starting point for the processing are SOI wafers with a device layer thickness of 40 µm and a handle layer thickness of 380 µm. The first step is to deposit and pattern a two-step SiO_2 etching mask onto the backside of the wafer for the deep reactive ion etching (DRIE) process (Figure 2.10(a)). Next, the key feature of F2R, "buried trenches", are fabricated into the SOI device layer. In the buried trench process, a thin plasma-enhanced chemical vapor deposition (PECVD) oxide layer is first deposited and patterned into a mesh mask for the buried trench etching process (Figure 2.10(b-c)). The buried trenches are etched by DRIE using the oxide mesh mask. During DRIE etching through the oxide mesh mask, the under-etch of the DRIE process merges the mesh patterns and eventually forms a larger trench. Finally, the oxide mesh mask is closed by a thick PECVD oxide layer, resulting in closed buried trenches[35]. An SEM image of the open and closed buried trench SEM image is shown in Figure 2.10 (d).

After the closure of the buried trenches, the surface of the wafer is intact again, which allows the first polyimide layer to be coated and cured. Polyimide is not an ideal surface for the bonding process because of its lack of stiffness. Therefore, contact vias are etched into the polyimide, landing on the oxide layer to provide a rigid substrate for the contact pads. AlCu is sputtered on the first polyimide layer and patterned into the routing interconnects. Subsequently, the second polyimide layer is coated and cured. Before backside processing, a metal hard etch mask layer is deposited and patterned on the second polyimide layer for the final polyimide etching step after backside processing has been completed, Figure 2.10(e-f).

Figure 2.10(g-i) present the backside processing. The TSH in the ODLM design has a diameter of around 135 µm and the entire silicon substrate underneath the second silicon element needs to be removed to release the thin silicon island. Both parts are re-

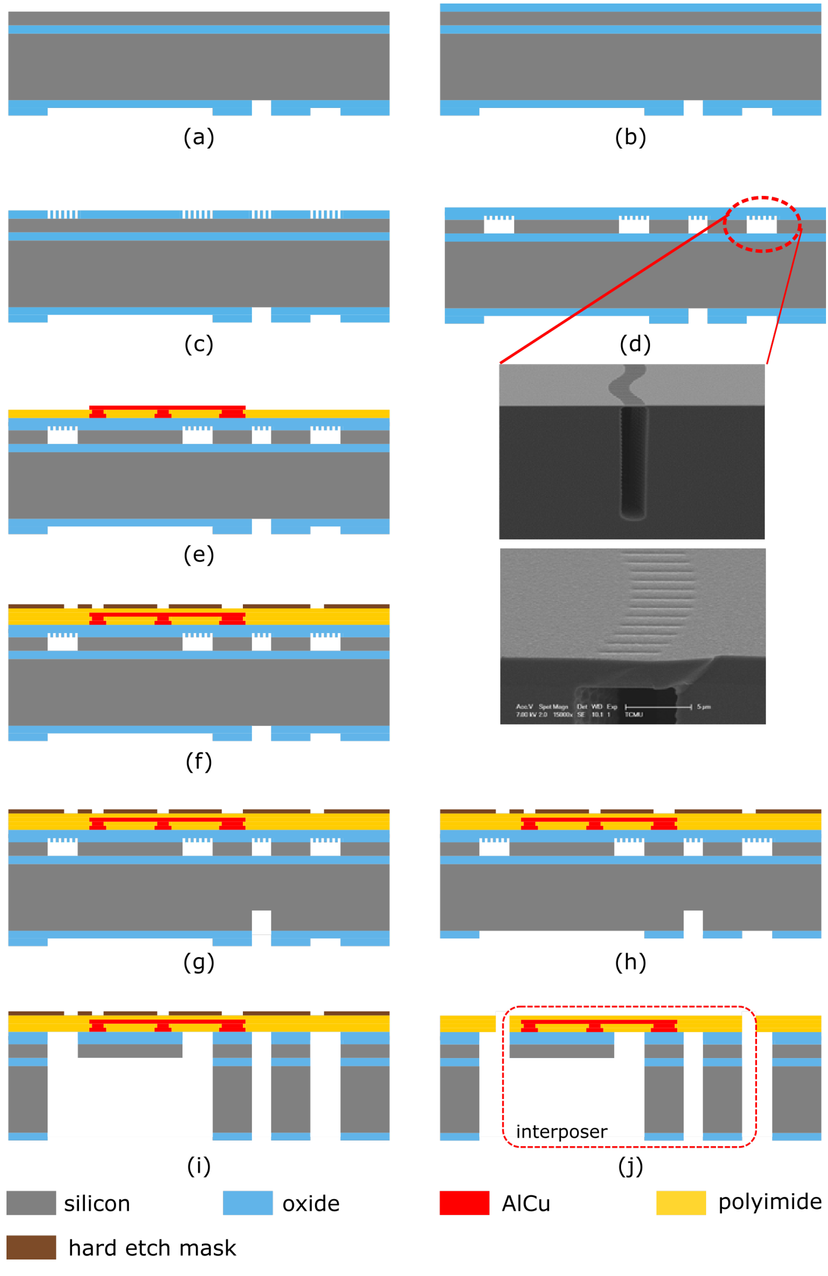

Figure 2.10: Schematic representation of the F2R based ODLM fabrication flow. (a-b) Deposition and patterning of PECVD oxide for buried trench etching. (c) Two-step backside etching mask processing. (d) Etching of the buried trench with DRIE and closing with a thick PECVD oxide layer. SEM cross-section of buried trench shown. (e) Coating of the first polyimide layer, etching of via to the oxide layer and processing of AlCu interconnects. (f) Deposition of the second polyimide layer and hard etch mask for contact pad opening. (g) First backside etch. (h) Thinning down of the two-step backside etching mask. (i) Second backside etch. (j) Etching of the polyimide to open contact pads and release the F2R structures.

moved in the same backside etching step. Because of the higher aspect ratio of the TSH compared to the larger open area, a two-step backside etching method is applied to guarantee a reliable TSH opening process. The oxide mask is patterned into two levels: the first level is the TSH pattern that lands on silicon, and the second level is the larger open area pattern that is half etched into the oxide mask. The first backside silicon DRIE pre-etches the TSH 120 μm into the silicon substrate (Figure 2.10(g)). Next, the oxide mask is thinned down to expose the larger open area mask (Figure 2.10(h)). Now the larger area and the TSH are etched together to land on the SOI buried oxide. The SOI buried oxide and the oxide layer underneath the flexible interconnects are subsequently removed from the backside with a high-pressure oxide dry etch (Figure 2.10(i)). Finally, using the prefabricated aluminum hard etch mask on the front side of the wafer, a front-side polyimide etch opens the contact pads and releases the device. A wet etch process removes the hard etch mask (Figure 2.10(j)). Because of the PI-metal-PI sandwiched structure, the metal layer in the flexible interconnects is in the stress-neutral plane. Therefore, the flexible interconnects can achieve a small bending radius of 10 μm [36].

2.3.2. FABRICATION RESULTS

Figure 2.11 presents some details of the ODLM F2R interposer. Figure 2.11(a) is the front side view of the ODLM interposer attached to the silicon frame by polyimide tabs. The silicon frame allows for handling of the ODLM during the device assembly. The upper squared structure is the first silicon element with the full wafer thickness, which comprises the through silicon hole, intermediate, and dummy contact pads. The bottom rectangular structure is the second silicon element, with a thickness of 40 μm, and the rerouted contact pads. A basic electrical open & short measurement confirms the successful opening of the contact pads and the functionality of the flexible interconnects. By applying backside illumination, light can be observed from the front side through the TSH, which indicates the correct opening of the TSH. Figure 2.11(b) shows the backside view of the ODLM F2R interposer attached to the silicon frame. The two-step backside etch process was successful, as it only resulted in 10 μm under-etch after etching the 380 μm thick silicon handle layer. The backside DRIE process defines the first and second silicon elements and releases them from the Si substrate. To give a more intuitive feeling of the dimension, Figure 2.12 depicts an ODLM F2R interposer released from the silicon frame and placed on a human fingertip.

2.3.3. PROCESS OPTIMIZATION

In the backside etching steps, various designs with different dimensions need to be fabricated. Figure 2.13 shows two backside mask designs of these variations, including structures like:

- Large backside openings to release silicon elements and create rigid silicon frames for device handling;
- Through silicon holes (TSHs) with diameters of 135 μm for optical fiber connection;
- TSHs with a side opening that allows dry etching species to have better access into the holes during the etching process.

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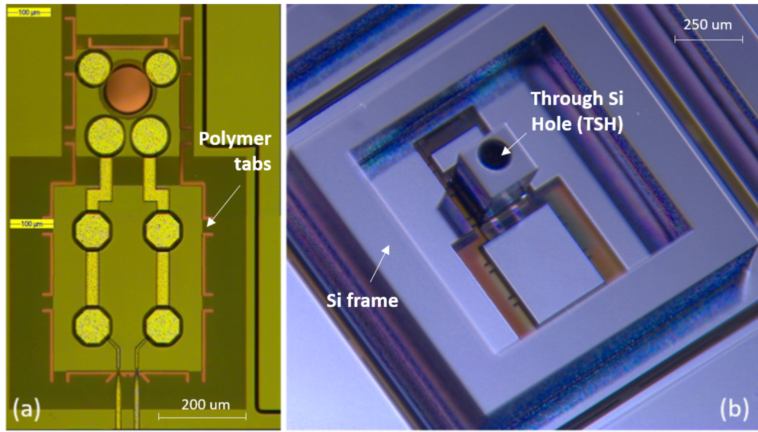

Figure 2.11: ODLM F2R interposer fabrication results. (a) Front side view of the F2R interposer attached to the silicon frame. (b) Backside view of the F2R interposer in the silicon frame.

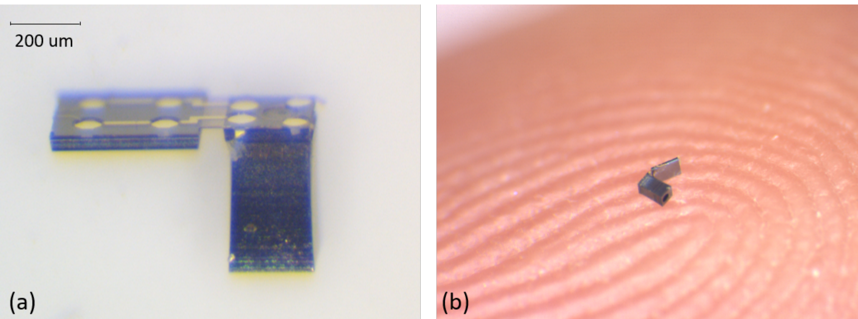

Figure 2.12: ODLM F2R interposer fabrication results. (a) ODLM F2R interposer released from the silicon frame; (b) released ODLM F2R interposer on a human fingertip

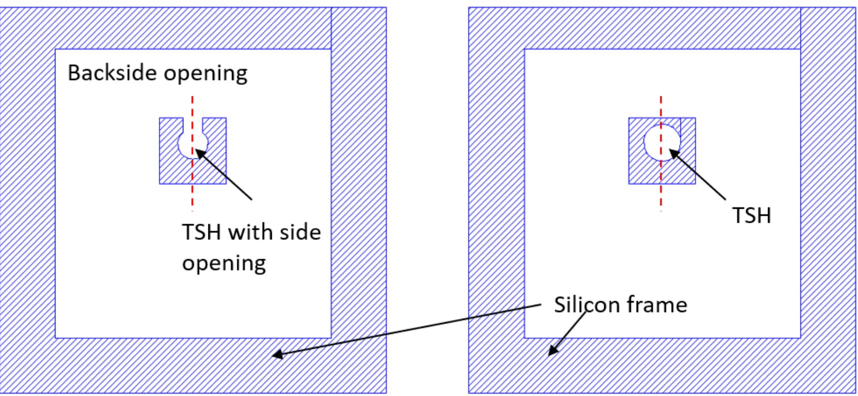

Figure 2.13: Mask designs of two ODLM variations for backside DRIE process, including the large backside opening, silicon frames (colored structures), and different TSHs. Cross-sections were made through the dashed lines for inspections.

These various designs challenge the backside DRIE process. Different sizes and shapes of mask openings (such as TSHs versus large frame openings) result in different etch rates and etch profiles. Although the buried oxide layer of the SOI wafer allows for some over-etch during the etching of the the handle layer, the over-etch might still create unwanted foot-corner notches. More importantly, the TSHs must have a straight etch profile with minimized under-etch so that the inserted fiber can remain stable in the TSH.

The backside etch is performed on the 380 µm thick handle wafer of an SOI substrate. The goal is to ensure the etching of the TSHs and the large openings that land on the BOX layer simultaneously and to achieve a straight TSH profile. The two-step backside etching process described previously uses a customized DRIE recipe, ODLM_03. This recipe was developed based on the Bosch Si etching process. Each etching cycle includes an etching step, a passivation step, and a breakthrough step. The process time ratio between the passivation and etching step was optimized to ensure the etched sidewall profile to be as straight as possible. Other parameters, such as chamber pressure and temperature, were slightly modified to minimize the different etch rates and profiles in narrow/closed structures versus wide-open areas.

During the two-step etch process, 79 etch cycles were first applied for the TSH pre-etch, which resulted in an etch depth of 120 µm. The two-step oxide mask was then recessed to reveal the second mask. Finally, 339 etch cycles of ODLM_03, with a total etch time of 71 minutes, were applied to etch the TSH and the large openings, landing on the BOX (Figure 2.10 g-i). Test samples were diced through the TSH, shown in Figure 2.13, for the cross-section inspection to confirm the etching profile. Figure 2.14(a) depicts the etching result of a 135 µm diameter TSH. The inner side of the TSHs remained straight, as very few width variations were observed in the top and bottom parts of the TSH. The outer side of the silicon pillar, defined by the etching of the large openings, was less straight. Width differences of 5-7 µm were observed between the top and bottom parts. This result clearly shows the different behaviors of the same etching recipe applied to closed structures and wide-open areas. Nevertheless, the few microns of side etching are minor compared to the entire silicon pillar width. Figure 2.14(b) shows the

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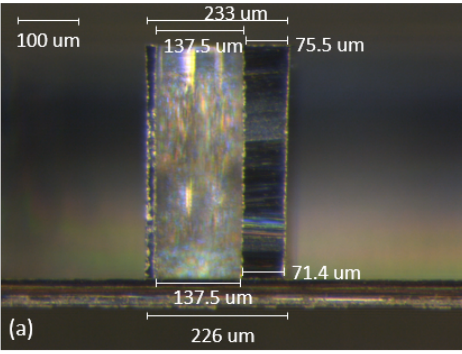

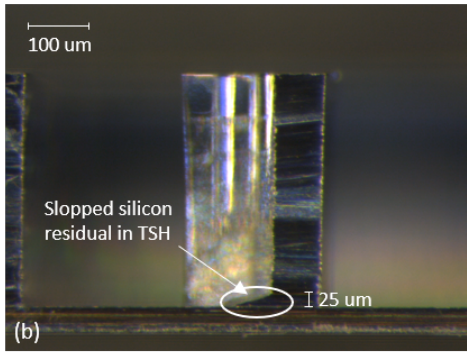

Figure 2.14: Cross-section images of TSHs. (a) Close TSH etched with ODLM_03 reipe 79+339 cycles. (b) TSH with side opening has silicon residual after etched with ODLM_03 recipe 339 cycles.

etching result of the TSH with a side opening. The TSH in this design was not pre-etched, but 339 etch cycles were applied directly. The side opening was expected to give more accessibility to the etching species, which should result in a faster etch rate than the closed TSH. However, although the cross-section image indicates the etch rate was indeed faster, it seems that 339 etch cycles are still not enough to land on the BOX layer. There is a slopped Si residue from the outer to the inner side of the TSH. So, either the dimension of the side opening needs to be enlarged, or more etch cycles should be applied to etch through the side opened TSHs.

The two-step etching process developed above was applied in the final device fabrication. However, although the Si etching successfully landed on the SOI BOX layer, the follow-up oxide etching failed to break through the BOX layer in the TSH. Different oxide etching recipes with various etching conditions (etch time, temperature, pressure, etc.) were tuned and tested, but no recipe could etch through the BOX layer. It seemed that either the etching species had problems reaching the bottom of the TSH due to its high aspect ratio or something on the surface of the BOX layer blocked the etching species. For verification, an etched ODLM interposer was taken out of the wafer and broken through the TSH. Figure 2.15 shows that two oxide membranes can be observed under an angle. The first oxide membrane is around 3.5 µm thick and was created to close the oxide mesh mask openings in the buried trench process. The second membrane is the 500 nm thick BOX layer of the SOI wafer. The two membranes should be transparent, as they are both SiO_2 layers. However, a thin yellow film can be observed on the second membrane. Since the thin yellow film could be removed with 30 minutes of oxygen plasma treatment, it most possibly originated from the passivation step during the backside DRIE process. The extra passivation layer was accumulated on the surface of the second membrane during the over-etching of the TSH, which protected the oxide membrane from being removed by the oxide etching step. Eventually for this batch, we used the current Si etching process in combination with an excimer laser to open the two oxide membranes after the entire microfabrication was completed. For the future production of the ODLM, the TSH etching recipe should be further optimized to reduce

the passivation deposition on the BOX due to the DRIE process.

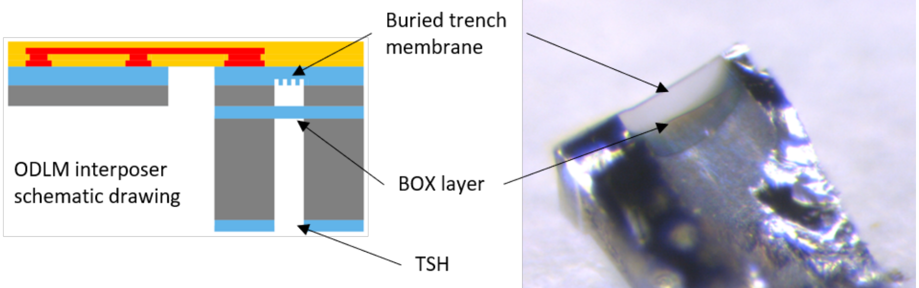

Figure 2.15: Cross-section of a TSH after the two-step silicon etching and oxide etching. The oxide etching failed to remove the BOX layer. A thin yellow film is deposited on the BOX layer after silicon etching, which an be removed by oxygen plasma.

2.4. CONCLUSION

The market demand is driving smart catheters to evolve from analog to digital instruments, and from electrical to optical data communication. As a result, an optical link needs to be integrated into the miniaturized catheter system. In this chapter, the design concept and fabrication of such an F2R-based optical link, the optical data link module (ODLM), is presented. Its dimension of 240 µm × 240 µm × 420 µm is very suitable for miniaturized integrated systems, such as smart medical catheters. The ODLM device in this chapter was designed to provide at least a 1.2 Gb/s data rate and fit in an IVUS smart catheter tip. The ODLM interposer converts the electrical connections of a VCSEL to a plane that is perpendicular to its laser emitting surface. This approach enables the ODLM to be assembled on a horizontal PCB while the VCSEL is optically aligned and connected to a fiber running parallel to PCB. Moreover, the ODLM is a mass-producible stand-alone device that provides a reliable laser to fiber self-alignment and mechanical strength.

The ODLM was designed and fabricated based on the previously introduced F2R interconnect platform. The processes in the F2R platform, such as the buried trench process and flexible interconnect fabrication, have been well developed. Therefore, a large amount of process optimizations for the ODLM fabrication could be avoided. Nevertheless, different ODLM designs still required some detailed process development for the two-step backside DRIE step. Finally, the ODLM device was successfully fabricated in the cleanroom of Philips MMD. Both the dimensions and the thickness of the silicon elements were well defined. The electrical measurement proved the functionality of the flexible interconnects and different contact pads.

The next challenges for the ODLM are assembly and integration. Special processes have been developed to assemble the VCSELs on the fabricated F2R interposer. Finally, the ODLM device will be mounted on a laser driver board to test the data communication.

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3

Optical Data Link Module (Part 2)

Parts of this chapter have been published in [1, 2, 3]

3

3.1. INTRODUCTION

THE previous chapter presented the ODLM design and the fabrication. In this chapter, the ODLM assembly and characterization details are presented. The topics in this chapter are shown in Figure 3.1. After the fabrication, the ODLM interposer is attached to the Si frames by polymer tabs and remains in the Si wafer. The contact pads on the processed wafers are first provided with an electroless nickel electroless palladium immersion gold (ENEPIG) under-bump metallization by an external supplier (PacTech). Next, to assemble the VCSEL to the intermediate contact pads and form a reliable electrical connection for high-speed data transmission the VCSEL was flip-chip soldered to the ODLM interposer with solder spheres. After releasing the ODLM interposer from the silicon frame, the second Si element was bent 90 degrees and fixated to the side of the silicon element holding the VCSEL. The optical fiber was inserted and fixated in the final assembly step. The device assembly was performed in the Greenhouse, Micro Devices Facility, Philips. The main assembly challenge is to handle the extremely small VCSEL and flip-chip it onto the 240 µm × 240 µm assembly surface. A reliable VCSEL assembly process is therefore necessary. Furthermore, the ODLM interposers are all free-hanging in the Si frame after fabrication. The non-sturdy assembly surface challenges the VCSEL flip-chip process.The integration process of the ODLM onto the flex-PCB board still needs to be optimized. Many non-standard assembly processes and materials were developed because of the small form factor and the special semi-flexible F2R structures.

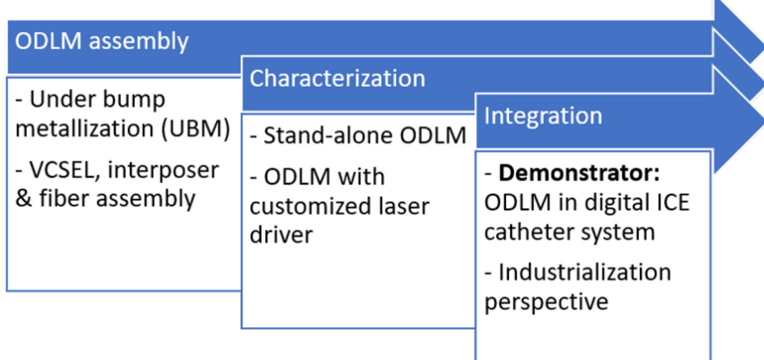


Figure 3.1: ODLM assembly, characterization and integration topics

The assembled ODLM devices were characterized in collaboration with the Electro-Optical Communication Group from the Department of Electrical Engineering at Eindhoven Technical University of Technology (TU/e). Eye diagrams were used to characterize the ODLM performance. The stand-alone ODLM was first driven through a high-speed bias tee, proving that the ODLM can transmit 25.8 Gb/s, $2^{31}-1$ PRBS. The bit error rate (BER) test indicated that error-free operation can be successfully achieved at an optical output of around -4 dBm, which indicates a reliable data transmission. Next, the ODLM was assembled onto a PCB with a customized laser driver ASIC optimized to deliver the best speed-power tradeoff for the IVUS application. The laser driver board was first characterized without the ODLM and then integrated with the ODLM. The driver

board with ODLM can transmit 7 Gb/s, $2^{15}-1$ PRBS. The ODLM was further integrated into a digital ICE catheter lab setup, successfully transmitting at a data rate of 6 Gb/s and resulting in high-resolution ultrasound images. In the end, possible optimizations for high-volume ODLM production and other industrial applications are discussed.

3.2. STAND-ALONE ODLM

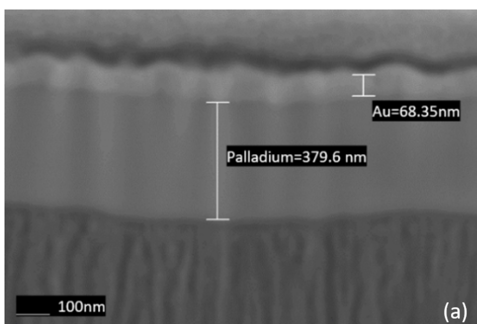
3.2.1. ODLM ASSEMBLY

The first assembly step is to connect the VCSEL to the fabricated ODLM. The two most commonly used micro-assembly techniques were considered: stud bump bonding (SBB) process and solder flip-chip technology. SBB is known for its low cost, high compatibility to contact metal and fine-pitch bumping[4]. In SBB, gold bumps are placed on the contact pads and the devices are connected by thermal compression or ultrasonic bonding. However, the fragile F2R structures of the ODLM interposer cannot handle the high temperature and high bonding force during the SBB process. In contrast, the solder flip-chip process uses soft soldering with reflowed solder bumps, which is compatible with the ODLM interposer[5]. Because the AlCu finishing surface of the ODLM contact pads does not provide sufficient wetting for the solder spheres[6], under-bump metallization is therefore necessary as a diffusion barrier and adhesion layer.

UNDER-BUMP METALLIZATION (UBM)

There are various choices for the deposition of the under-bump metallization, including evaporation, electroplating, sputtering and electroless plating[7]. Because of the semi-flexible F2R features in the fabricated ODLM interposer wafers, an electroless nickel electroless palladium immersion gold (ENEPIG) process provided by an external supplier (PacTech) was chosen[8]. The ODLM interposer wafers were first cleaned, and the native oxide on the contact pads was removed with wet etching chemicals. A zinc oxide solution is then used to activate the pad surface by replacing part of the aluminum on the contact pads with zinc. This zinc layer changes the potential of the AlCu pads in the nickel sulfate solution, where nickel replaces the zinc layer and continues to catalyze the nickel deposition. By adjusting the plating time, temperature, pH, and chemical concentration of the plating baths, around 3.2 µm of electroless nickel and 400 nm electroless palladium were deposited. However, the last immersion gold layer showed a poor deposition uniformity varying from 13 nm to 68 nm across the wafer, as shown in the focused ion beam (FIB) images (Figure 3.2). Moreover, the gold layer was also non-ideally deposited on the wafer backside and the sidewall of the ODLM interposers.

Investigation indicated that the complexity of the 3D F2R structures negatively affects the flow of the wet chemicals during the plating process, which results in a nonuniform thin gold layer. Nevertheless, a solder wetting test proved that the contact pads with nonuniform gold layers still have sufficient wettability to the solder spheres. The unwanted deposition on the wafer backside and the sidewall of the ODLM interposers might be caused by the roughness of the surface, which creates landing spots and catalyze the ENEPIG deposition. This non-ideal deposition became less after an additional chemical stabilizer[9] was applied to optimize the ENEPIG process.



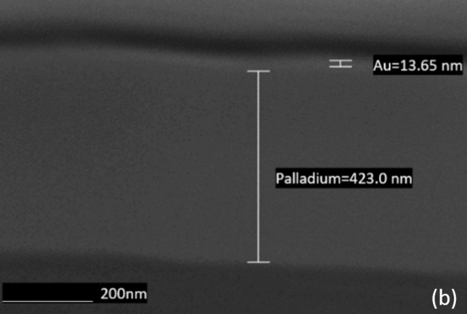


Figure 3.2: FIB image of (a) a normal ENEPIG contact pad with 3.2 µm nickel layer, 379.6 nm palladium layer and 68.35 nm Au layer; (b) a nonuniform ENEPIG contact pad with a thinner gold layer, thickness of 13.65 nm.

VCSEL PLACEMENT

The ENEPIG process resulted in a UBM layer stack of around 3.2 µm of electroless nickel, 400 nm electroless palladium, and 13-68 nm Au, with sufficient solder wettability. With soldering flux (TSF6592 from Flux Kester), solder spheres (SAC305 from Mitsui) with a diameter of 60 µm were placed on all the dummy and intermediate contact pads. The soldering flux helps with the positioning of the tiny solder spheres and cleans the soldering surfaces. After a reflow bake of 30 seconds at 260 degrees in the ATV oven, the soldering flux was decomposed, and the solder spheres were reflowed and connected to the contact pads (Figure 3.3a). The VCSEL was flip-chipped placed on top of the reflowed solder spheres. After a second reflow, the bottom two contact pads formed a good connection to the VCSEL. The solder spheres on the top dummy contact pads acted as mechanical supports to prevent VCSEL tilting during the second reflow. Figure 3.3b shows a side view of the complete ODLM with the VCSEL flip-chip assembled on the ODLM interposer. The VCSEL was well connected and remained in a horizontal position after the assembly process. No underfill was applied at this stage to keep a clear optical transmission path between the VCSEL and the TSH. An X-ray image was taken to check the solder wetting of the assembled VCSEL (Figure 3.3c). The X-ray image indicates that the reflowed solder spheres remained in the contact pad area after the VCSEL assembly. Hence, no solder bridgings were created. The electrical connection was verified by probing the contact pads on the ODLM interposer and sweeping the I-V curve of the VCSEL. The VCSEL forward IV sweep showed a normal diode behavior (Figure 3.3d), confirming the successful VCSEL assembly.

FOLD AND PLUG

The ODLM interposer with the assembled VCSEL was released from the Si frame by cutting the polymer tabs after the VCSEL placement (see Figure 3.4a). The second thin silicon element was free hanging at this step and connected to the first silicon element by the flexible interconnect. The second thin silicon element was folded by 90 degrees and fixated to the side of the first silicon element with a thin transparent biocompatible UV-cure glue (203A-CTH-F from DYMAX), as shown in Figure 3.4b. The previous chapter introduced a few ODLM interposer variants with assemble-friendly features. Among those

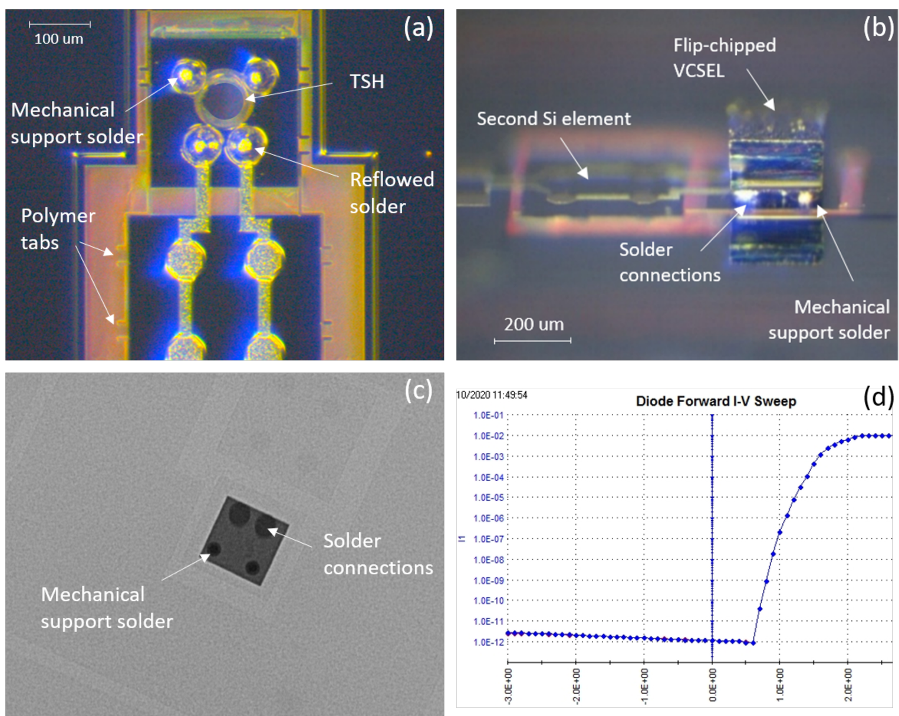


Figure 3.3: VCSEL placement. (a) Solder spheres reflowed on all the dummy and intermediate contact pads of the ODLM interposer in a silicon frame; (b) Tilted view of a VCSEL flip-chip assembled on the ODLM interposer that is in a silicon frame. (c) An X-ray image of a flip-chip assembled VCSEL to confirm solder wetting. (d) Diode forward I-V sweep confirms the functionality of the assembled VCSEL.

variants, the one with a larger second silicon element showed the best performance. The excessive glue was successfully constrained on the second silicon element as expected.

A 125 µm diameter pigtail OM1 multi-mode optical fiber with a fiber core of 62.5 µm diameter was chosen to capture more optical power from the VCSEL. The fiber jacket and coating were stripped at the tip of the pigtail side, leaving only the core and the cladding with a diameter of 125 µm . The end of the fiber tip was carefully cleaved 90 degrees and polished to reduce coupling losses (Figure 3.4c). The stripped fiber tip was dipped in the same transparent bio-compatible glue, inserted into the 135 µm diameter through-silicon hole, until it reached the assembled VCSEL on the other side. The UV-cure glue was temporarily fixated with UV light and finally cured at 100 degrees for 1 hour. Figure 3.4d depicts the final assembled stand-alone ODLM, including the VCSEL, the F2R interposer, and an inserted 125 µm diameter optical fiber placed on a match head. To test the functionality, the assembled stand-alone ODLM was powered by applying electrical bias using a probe station. Optical signals were detected at the other end of the optical fiber, demonstrating the successful assembly of the stand-alone ODLM.

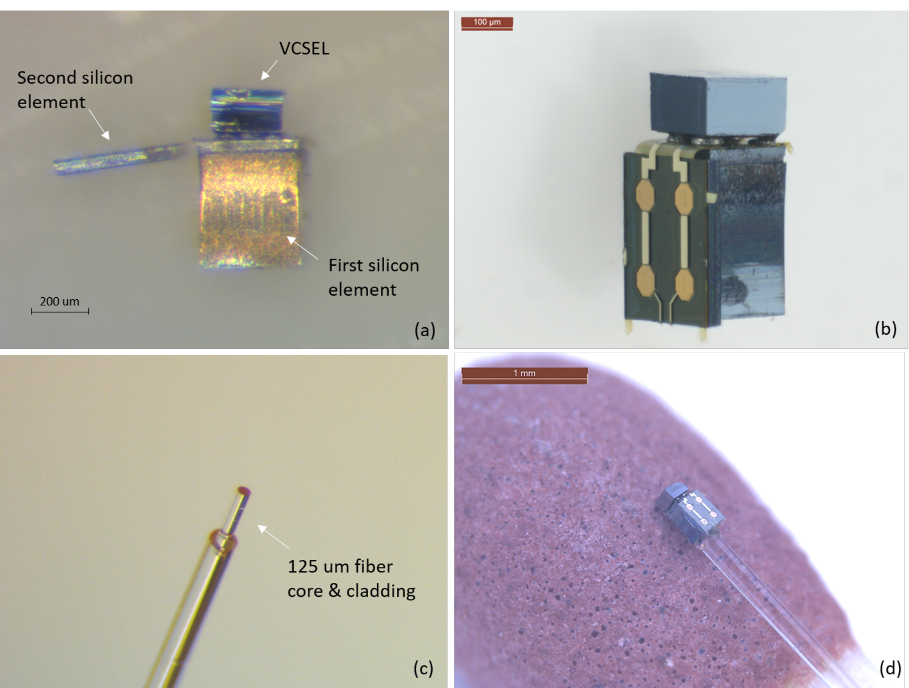


Figure 3.4: ODLM assembly figures. (a) Side view of an ODLM interposer with assembled VCSEL, released from the Si frame. The two silicon elements are connected by flexible interconnects; (b) Second silicon element fixated to the side of the first silicon element; (c) Stripped fiber tip, leaving only the core and the cladding with a diameter of 125 µm; (d) An assembled ODLM, with the VCSEL and an inserted 125 µm diameter optical fiber, placed on a match head. Optical fiber was fixated by biocompatible glue.

3.2.2. CHARACTERIZATION

A schematic diagram of the ODLM optical characterization setup is shown in Figure 3.5. A DC bias voltage is applied to the VCSEL on the ODLM through a bias tee module. The generated high-speed data is transmitted through the bias tee and fed into the ODLM using high-speed differential probes. The data is converted to an optical signal, propagates through the optical fiber into a commercial QSFP (100G-SR4-S from Cisco) transceiver. The QSFP converts the optical signal to an electrical signal connected into an oscilloscope error detector. In this setup, the PRBS data generator and the oscilloscope error detector are integrated into a time-domain analyzer (ML4004-PAM from multiLane).

A bias voltage of 1.91 V was applied to obtain the best bias point for the VCSEL. An optical output power Popt=1.112 mW was detected at the end of the 1-meter long optical fiber. Compared with the specifications of the VCSEL, where a Popt=1.38 mW is achieved at 1.91 V bias voltage, this stand-alone ODLM device delivered 80.5% of the optical intensity generated by the VCSEL. The received optical output power is affected by VCSEL positioning and fiber coupling. A 25.8 Gb/s differential signal, with PRBS $2^{31}-1$ sequence, was fed into the ODLM device through high-speed probes. The converted electrical signal from the QSFP was visualized on the oscilloscope in the analyzer. The

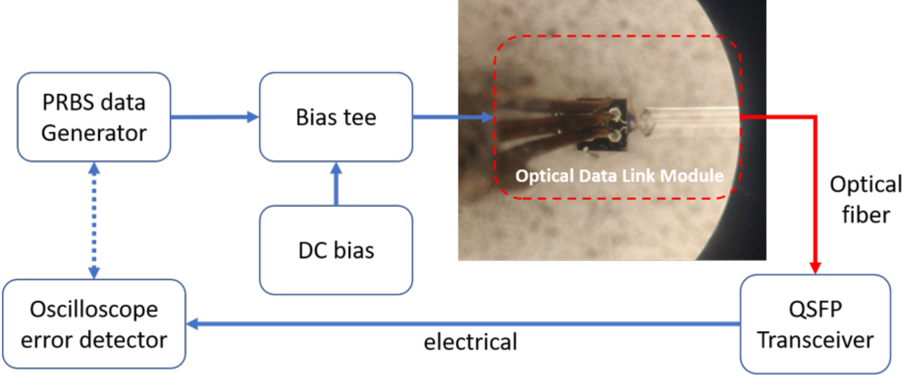


Figure 3.5: Schematic diagram of signal integrity testing setup for the stand-alone ODLM device, with an inserted microphotograph of the ODLM device being probed by high-speed differential probes.

eye diagrams, with and without clock data recovery (CDR), are shown in Figure 3.6a and b, proving the capability of the stand-alone ODLM to support data rates up to 25.8 Gb/s.

The bit error rate (BER) testing was performed with the same test setup. A high-speed probe fed a 25.8 Gb/s differential signal with a PRBS 2^7-1 sequence into the ODLM. The optical output was transmitted to the QSFP and converted to an electrical signal fed into the error detector. The BER testing result is shown in Figure 3.6c. The graph shows how the BER varies as a function of the received optical power. It demonstrated that error-free (BER<10^{-12}) data transmission can be achieved with an optical output of more than -4 dBm from the ODLM device. The BER at such a high data rate highly relies on the entire communication system. The solder connections (such as contact resistance differences) between the VCSEL and ODLM, the interconnect traces on the ODLM, and the high-speed probe connection all can contribute to bit errors.

3.3. ODLM WITH CUSTOMIZED LASER DRIVER

3.3.1. CUSTOMIZED LASER DRIVER BOARD

The ODLM was originally developed as an optical link for a digital IVUS catheter to provide a data communication rate of ≥ 1.2 Gb/s. To further demonstrate the functionality of the ODLM in a digital IVUS system, a customized laser driver ASIC was designed and fabricated by Philips Research for a data rate of 6 Gb/s. The schematic drawing of the customized laser driver ASIC is shown in Figure 3.7.

The differential input signal is applied to the V_{in+} and V_{in-} terminals. After the current mode logic to CMOS (CML2CMOS) format converter block, the input signal can either go through the built-in PRBS block to generate the PRBS signal, or bypass the PRBS block and go directly to the current modulation block. This toggleable PRBS block is controlled by the multiplexer and makes it more flexible to characterize the laser driver functionality. The current modulation circuit consists of two current mirrors and a differential pair. The right current mirror is connected directly to the laser, providing a constant bias current (I_{th}). The left current mirror generates the modulation current

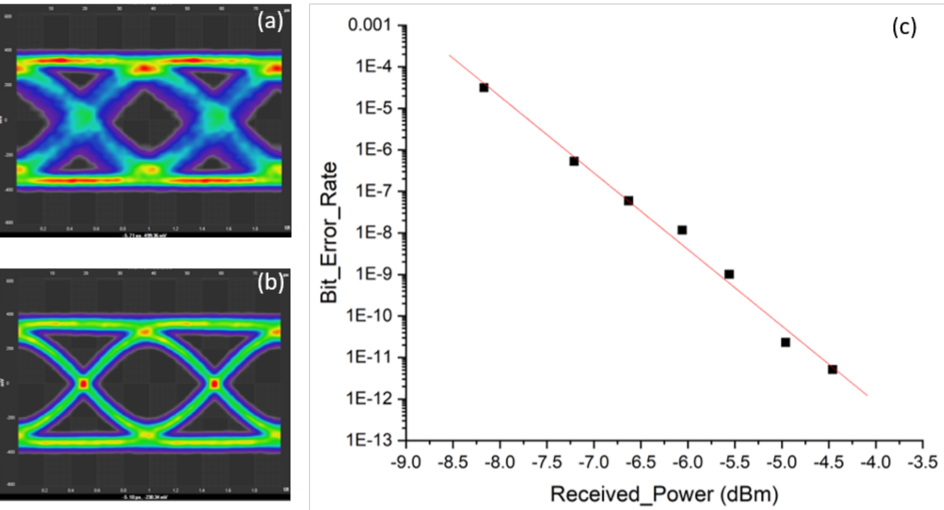


Figure 3.6: Stand-alone ODLM characterization results. Eye diagram of a stand-alone ODLM with 25.8Gb/s, PRBS $2^{31}-1$ sequence. (a) without CDR, (b) with CDR. (200 mv/div, 7.69 ps/div) (c) Fitted BER curve for the stand-alone ODLM 25.8 Gb/s with PRBS $2^{7}-1$ sequence transmitting test.

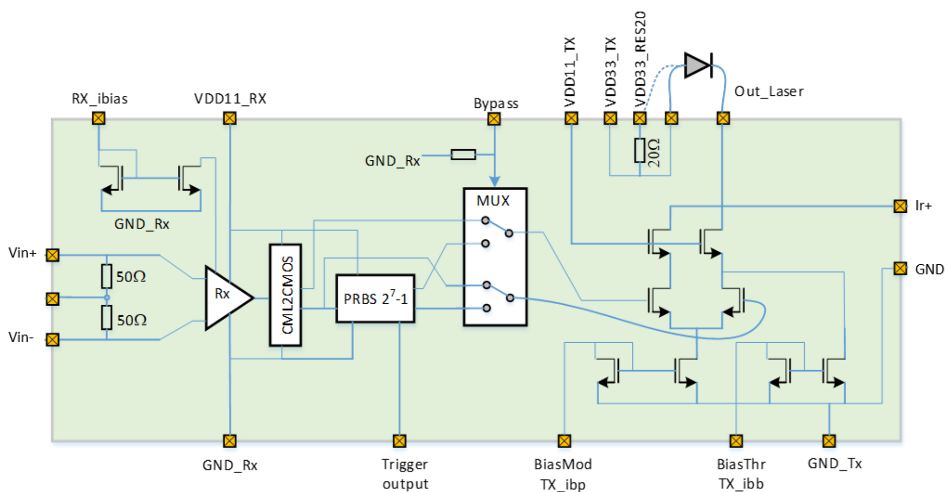


Figure 3.7: Schematic drawing of the customized laser driver ASIC designed by Philips Research, including an amplifier, a toggleable PRBS generator and a current modulation block.

(I_{mod}) that is controlled by the differential pair. Depending on the differential input signal, I_{mod} either adds up to the right branch or goes through the left branch. Therefore, the logic "high" or logic "low" of the laser corresponds to a driving current of (I_{th}+I_{mod}) or I_{th}. The left branch of the modulation circuit is connected to I_{r+} as a reference port. The I_{r+} terminal should have the same potential as the input of the modulation circuit. Hence, I_{r+} monitors the electrical laser input and compares it with the laser optical output. More importantly, because the operating environment of the catheter is in the human body, the speed of the laser driver is sacrificed so that its power dissipation is less than 10 mW, and the temperature of the catheter will remain less than 40 degrees.

The fabricated laser driver ASIC has a dimension of 2.8 mm by 1.3 mm and is flip-chipped onto the PCB board. The driver board can directly control the multiplexer to bypass the built-in PRBS module or not. Moreover, I_{th} can be tuned from 480 to 1800 µA, and I_{mod} can be tuned from 930 to 4850 µA, with a few jumpers on the driver board. This allows for fine-tuning of the laser to achieve the best optical data transmission performance.

3.3.2. Driver board evaluation with single VCSEL

This goal was to test the functionality of the customized laser driver, the VCSEL candidate, and the optical active alignment setup. The same VCSEL was used as the one used in the stand-alone ODLM, and wire-bonded to the laser driver.

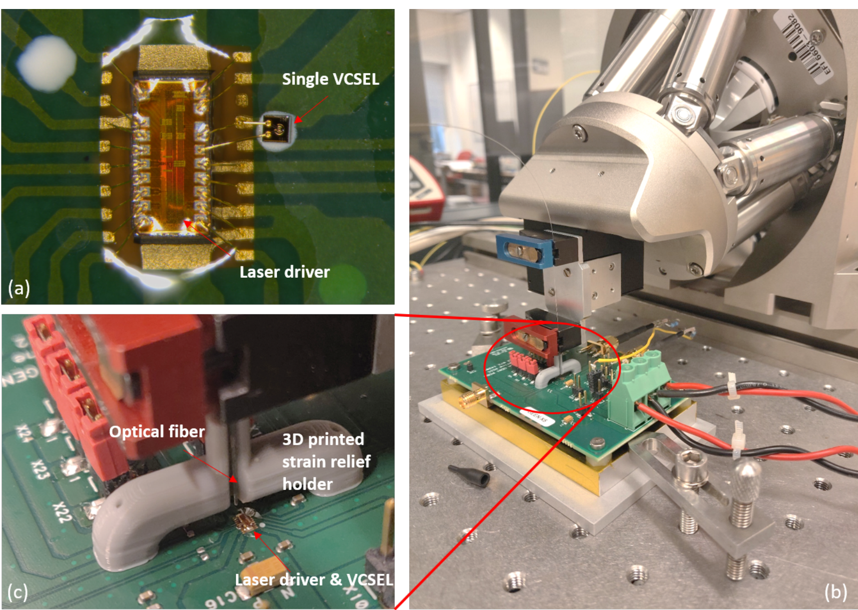


Figure 3.8: Driver board assembly with single VCSEL. (a) Single VCSEL fixated and wire-bonded next to the laser driver. (b) Active alignment setup with six-degrees-of-freedom. (c) Optical fiber coupled to the VCSEL and attached to the 3D printed strain relief holder.

Figure 3.8a shows that the single VCSEL was first fixated facing up on the PCB and

wire-bonded to the laser driver. The VCSEL was placed as close to the laser driver as possible to minimize interconnect parasitic. Protective epoxy was applied over the laser driver and wire-bonded areas. The laser emitting spot of the VCSEL was left clear. The fiber alignment process consisted of two steps: a coarse alignment followed by a fine alignment. In the coarse alignment, the optical fiber was coupled to the VCSEL as close as possible with the active alignment setup (F-712.HA1 from Physik Instrumente) provided by Philips MMD. Figure 3.8c shows that the active alignment setup contains a hexapod and a nanopositioner. The parallel-kinematics design guarantees its motion in six degrees of freedom with submicron precision. In the fine alignment step, the VCSEL was biased with a DC current via the driver board to produce a constant optical signal during the alignment process. The optical fiber used is a pigtail fiber, with one side stripped & cleaved, and the other side with an LC connector. The cleaved side of the optical fiber was controlled by the alignment setup, programmed to find the laser emitting spot of the VCSEL. The other side of the optical fiber was connected to a photodetector, measuring the optical output power captured by the cleaved side. Based on the feedback from the photodetector, the alignment setup was programmed to locate the most optimum fiber position, where it received the most optical output power from the VCSEL. After the optical fiber was correctly positioned, UV curable glue was applied to fix the cleaved fiber end to the VCSEL. In the end, the optimally-coupled optical fiber was attached to a 3D printed strain relief holder that was installed right next to the fiber, as shown in Figure 3.8b. The strain relief holder added extra strength to the fiber and protected the connection joint, ensuring a reliable operation.

To evaluate the assembled laser driven board, it was actively aligned and fixated to the VCSEL, a clock signal with a frequency of 1.5 GHz and an amplitude of 1 volt was applied to drive the built-in PRBS block (Figure 3.9a). The generated PRBS signals were the input to the VCSEL and can be monitored as a reference (Figure 3.9b). The input PRBS signals were converted to optical signals by the VCSEL and transmitted through the optical fiber to the small factor pluggable (SFP). The SFP converted the received optical signals back to electrical signals, which were then visualized on an oscilloscope (Figure 3.9c). The characterization results show that the pattern of the generated PRBS signals was well retained after being converted to optical and back to electrical SFP output. The SFP output had a delay of around 5.5 ns compared to the generated PRBS, probably introduced by the transmission cables in the SFP setup. The built-in circuit in the SFP also smoothened jitters, which added up to the response time. An eye diagram was generated to verify the signal integrity. The eyes in the eye diagram were widely open, indicating that the SFP output had highly recognizable “1” and “0” and a low bit error rate. It seems that the active alignment and the optical connection are reliable enough to provide high-quality optical digital output data. We can also conclude that both the laser driver board as well as the VCSEL are functioning as expected.

3.3.3. ODLM INTEGRATION ON DRIVER BOARD

The laser driver board evaluation demonstrated the functionality of the laser driver and the VCSEL. The next step is to integrate the assembled stand-alone ODLM into the laser driver board. Unfortunately, the contact pads on the laser driver PCB cannot match the fine pitch and dimensions of the contact pads the ODLM has, so the ODLM cannot be

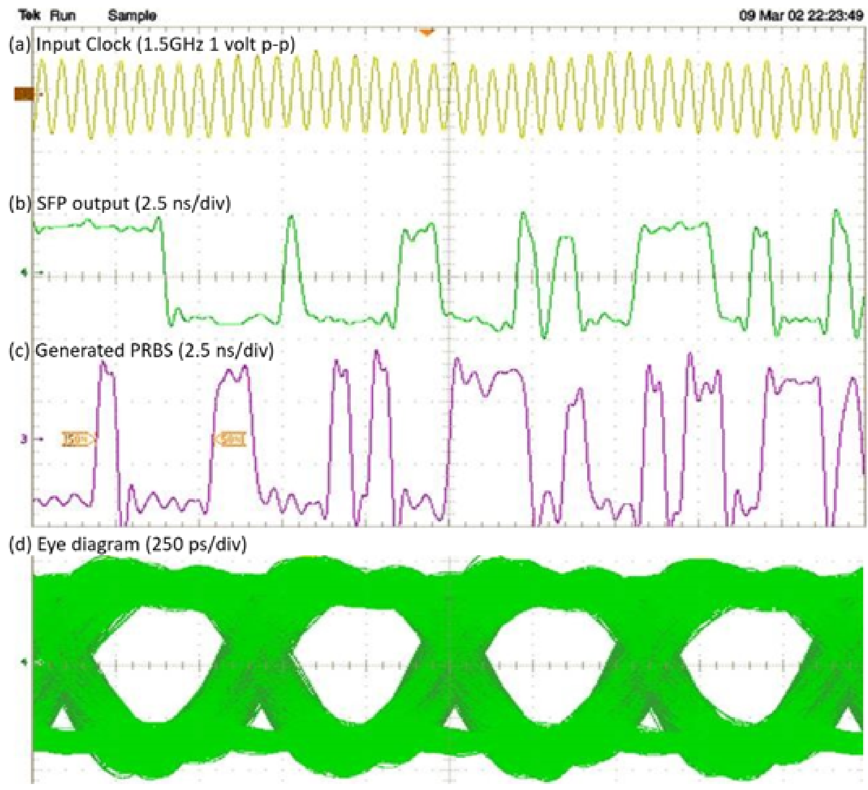


Figure 3.9: Electrical characterization results of the laser driver board with active aligned single VCSEL. (a) 1.5 GHz, 1 volt p-p input clock signal; (b) Generated PRBS signal by the built-in PRBS block; (c) SFP output, converted from the optical output; (d) Eyed-diagram of the SFP output.

directly flip-chip bonded to the driver board. Two alternative plans were made to realize the electrical connection. Plan A was to fixate the ODLM next to the laser driver with its contact pads facing up. The ODLM can be then directly wire-bonded to the laser driver, resulting in an ideal short electrical transmission length. Plan B was to flip-chip the ODLM on a flex PCB first, and then to connect the flex PCB to the laser driver with wire-bonding. Plan B mimics exactly the ODLM integration in the smart catheter tip, where discrete components and the ODLM will be integrated on a flex PCB at the end of the smart catheter tip, as shown in Figure 2.8. Nevertheless, this extra flex PCB makes the wire-bonding and flip-chip process less straightforward and uncertain. In both cases, the ODLM was first placed on the driver board and connected to the laser driver without the optical fiber to develop the integration process. The optical fiber was installed after the electrical connections were successfully made.

Both Plan A and B were carried out in the Greenhouse, Micro Devices Facility, Philips. The ODLM was successfully fixated and wire-bonded to the laser driver in Plan A. However, the fixation glue flowed into the through silicon hole of the ODLM due to capillary force, which blocked the fiber insertion and resulted in poor optical reception. Plan B,

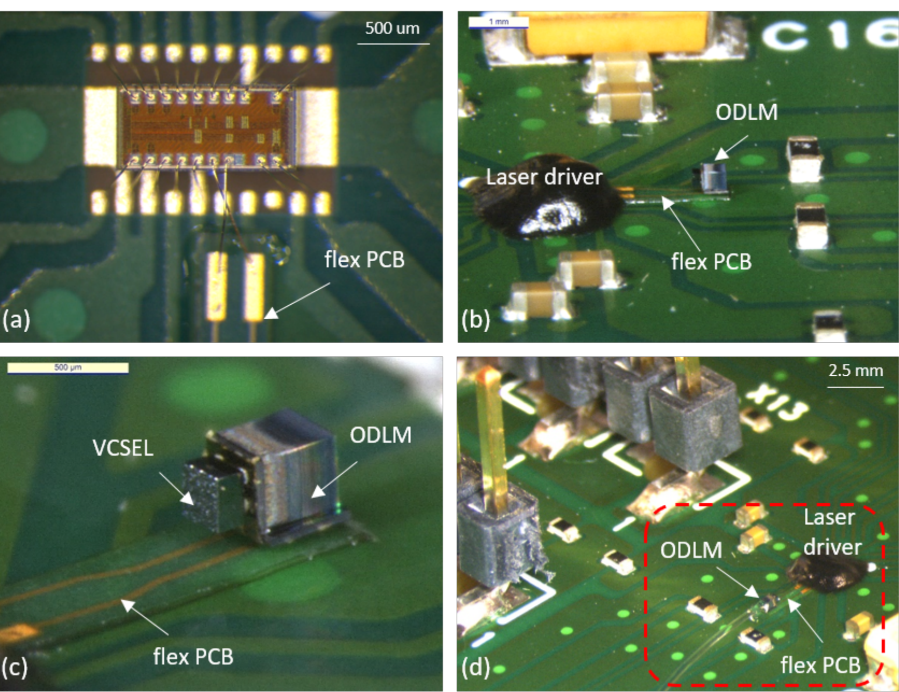


Figure 3.10: ODLM connected to catheter laser driver via flex PCB. (a) Customized laser driver for catheter application, wire-bonded to the test PCB and the 40 μm-thick flex PCB; (b) ODLM is connected to laser driver via a flex PCB. The laser driver is in the black polymer glob top; (c) Side view of ODLM assembled on a flex PCB; (d) overall view of ODLM connected to the laser driver on a testing PCB.

on the other hand, was completed successfully. Figure 3.10 depicts the ODLM connected to the laser driver via a flex PCB. First, the customized 40 μm-thick flex PCB was fixated with a thin adhesive and wire-bonded to the laser driver (Figure 3.10a). A black polymer glob top was applied to the assembled laser driver chip to protect the wire-bond connections. Subsequently, the ODLM without the optical fiber was flip-chip soldered onto the flex PCB (Figure 3.10b-c). Finally, the optical fiber was inserted into the ODLM, and a transparent glob top was applied over the entire ODLM device. Figure 3.10d depicts the integrated ODLM on the driver board, showing its extremely small form factor.

3.3.4. CHARACTERIZATION

Signal integrity tests were performed to evaluate the integrated ODLM on the laser driver board. The testing setup is shown in Figure 3.11. A PRBS data generator (AWG7122B from Tektronix) transmits high-speed data to the laser driver. The laser driver drives the ODLM and converts the electrical signals to optical signals. The optical signals are fed into a QSFP transceiver (100G-SR4-S from Cisco) and converted back to electrical signals. A digital oscilloscope (DPO72004 from Tektronix) is used to visualize the eye diagram.

A bias voltage of 1.94 V was applied to the ODLM device by the laser driver board.

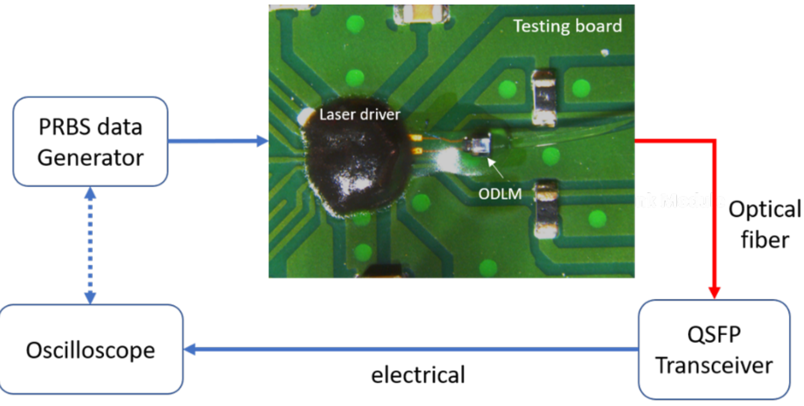


Figure 3.11: Scheme of signal integrity testing setup for laser driver & ODLM testing board, with an attached photo of ODLM device connected to laser driver via a flex PCB.

The QSFP detected an optical output power Popt= 1.065 mW at the end of the 1 m long optical fiber. Compared to the specifications of the VCSEL, where Popt= 1.43 mW is specified at a bias voltage of 1.94 V, this assembled stand-alone ODLM device on the testing board delivered 74.5% of the optical intensity generated by the VCSEL. The difference in the received Popt compared to the stand-alone version is most likely caused by the non-perfect alignment of the fiber with respect to the emitting spot of the VCSEL. 7 Gb/s and 8 GB/s differential signals, with PRBS $2^{15}-1$ sequence, were directly fed into the ODLM device through the laser driver, bypassing the built-in PRBS block on the driver board. The converted electrical signals from the QSFP were visualized on the oscilloscope. The eye diagrams of the assembly are shown in Figure 3.12. It was found that the customized laser driver performed better than expected, and a clear eye diagram was achieved for a data rate of 7 Gb/s, as presented in Figure 3.12a. Due to the limitations of the measurement setup (e.g., signal trigger setting), the signal patterns in Figure 3.12b seemed to be shifted, and the eye-opening was smaller than the ones at 7 Gb/s. Hence, it was uncertain if the driver board and the ODLM can support up to 8 Gb/s. Nevertheless, a data rate of 7 Gb/s is more than sufficient for the digital IVUS catheter application, where a data rate of only 1.2 Gb/s is required.

3.4. DEMONSTRATOR: THE ODLM IN A DIGITAL INTRACARDIAC ECHOCARDIOGRAPHY (ICE) CATHETER SYSTEM

The ODLM development activities fall within the framework of the European project POSITION-II. One of the POSITION-II ambitions was to demonstrate the essential components of digital catheter systems, including a digital IVUS catheter and Intracardiac Echocardiography (ICE) catheter. Although the functionality and the form factor of the high-speed optical data link module (ODLM) were designed to be integrated into an IVUS catheter tip, the IVUS catheter system integration was not completed on time. Therefore, the ODLM was implemented into the digital ICE catheter system, which has

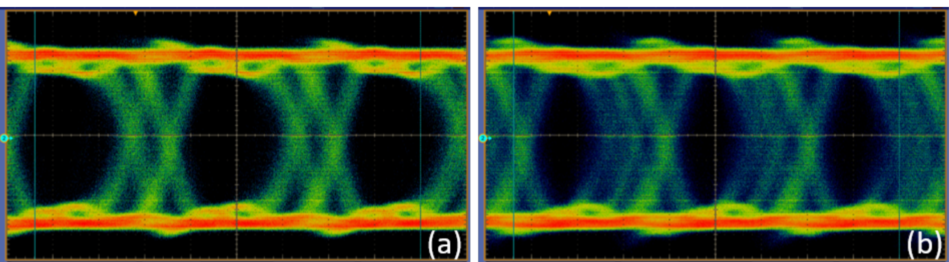


Figure 3.12: Eye diagrams of ODLM & laser driver board with PRBS $2^{15}-1$ sequence (a) 7 Gb/s, (b) 8 Gb/s. (60 mv/div, 40 ps/div)

a larger catheter tip with a diameter of 3 millimeters and requires a data rate of up to 6 Gb/s. Figure 3.13 presents a schematic layout and hardware parts of the digital ICE demonstrator[10]. This digital ICE demonstrator is a lab setup including custom-designed components completed with off-the-shelf components and functions. It consists of the following parts:

- Ultrasound transducer board;
- Analog control board, including T_x transmitting board and R_x receiving board;
- ICE digitization board;
- ODLM laser driver board;
- Finisar FDB-1032-SFP+ evaluation board;
- KC705 – Xilinx Kintex-7 evaluation board;
- Host PC.

The ultrasound transducer array contains 32 channels operating at a fundamental frequency of 5-7 MHz. To control the 32 channels simultaneously, the analog control board has a separate T_x transmit board and a R_x receive board. They manage the selection of the transducer arrays, generate, receive, process, and read out analog ultrasound signals. The ultrasound transducer array and the analog control board constitute the conventional analog ICE catheter system. The digitizing ASIC, integrated on the ICE digitization board converts the generated 32 channels of analog ultrasound signals into digital signals with 32 customized 12-bit ADCs that run at a sampling frequency of 40 MHz. The digital signals generated by the 32 ADCs are temporarily stored in a memory. They are eventually serialized, encoded, and transmitted to the ODLM laser driver board with a data rate of 6 Gb/s. The ODLM laser driver board in this ICE system is the same as previously introduced in Section 3.3. It holds the customized laser driver ASIC connected to an ODLM via a flexible PCB. The previous characterization proved that the combination of the customized laser driver ASIC and the ODLM supports a data rate up to 7 Gb/s. The laser driver board converts the high-speed data into an optical signal and

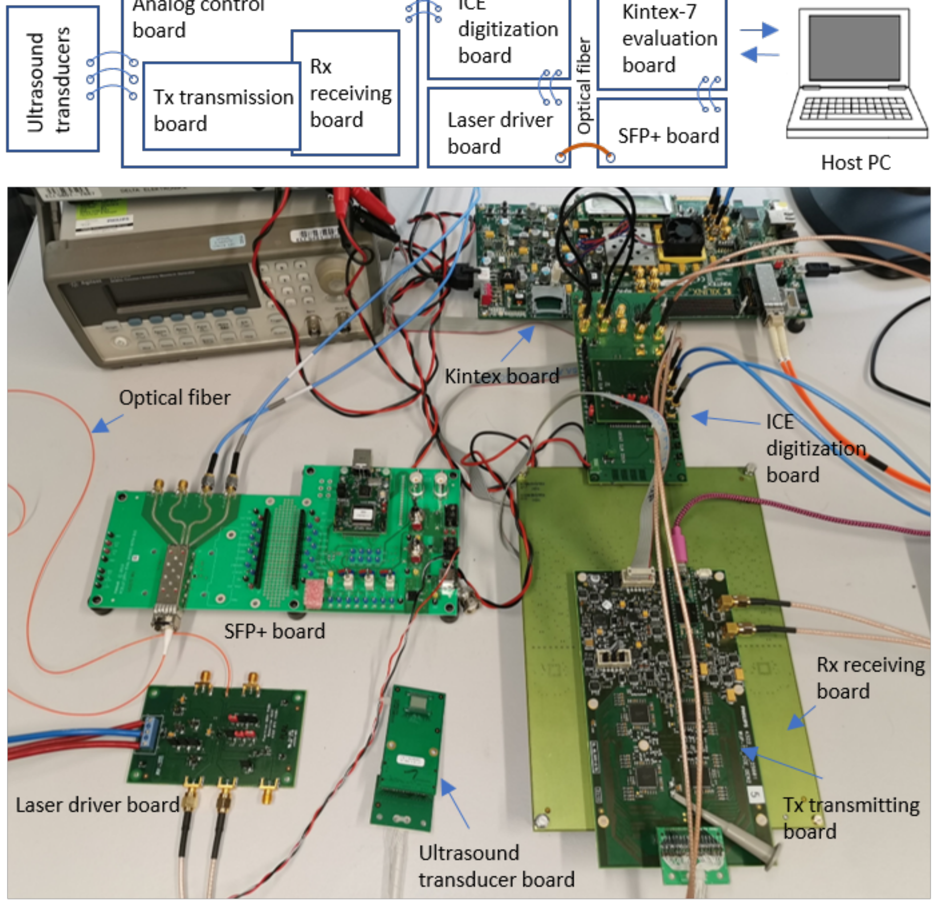


Figure 3.13: Schematic layout and hardware parts of the digital ICE demonstrator

transmits it through a standard multi-mode optical fiber to the SFP+ of the Finisar FDB-1032-SFP+ evaluation board. The Finisar evaluation board drives the SFP+ and converts the optical signal to a digital electrical signal. Eventually, the Kintex evaluation board decodes the digital signal and takes care of the data communication interface with the host PC, which generates and displays the ultrasound images via MATLAB scripts.

The digital ICE demonstrator setup is fully operational, and realistic ICE ultrasound images have been recorded[11]. Figure 3.14 presents the typical generated ultrasound images using the digital ICE demonstrator setup. Both anechoic and echoic features of a multi-purpose ultrasound phantom can be well identified from the generated ultrasound images. The ICE demonstrator result shows the functionality of all system parts, including the ODLM laser driver. Compared to the state-of-art analog forward-looking ICE catheter tip showed in the introduction chapter, Section 1.1.4 Figure 1.5, the digital ICE catheter saved large in-catheter space by reducing the 32 data transmission coaxial

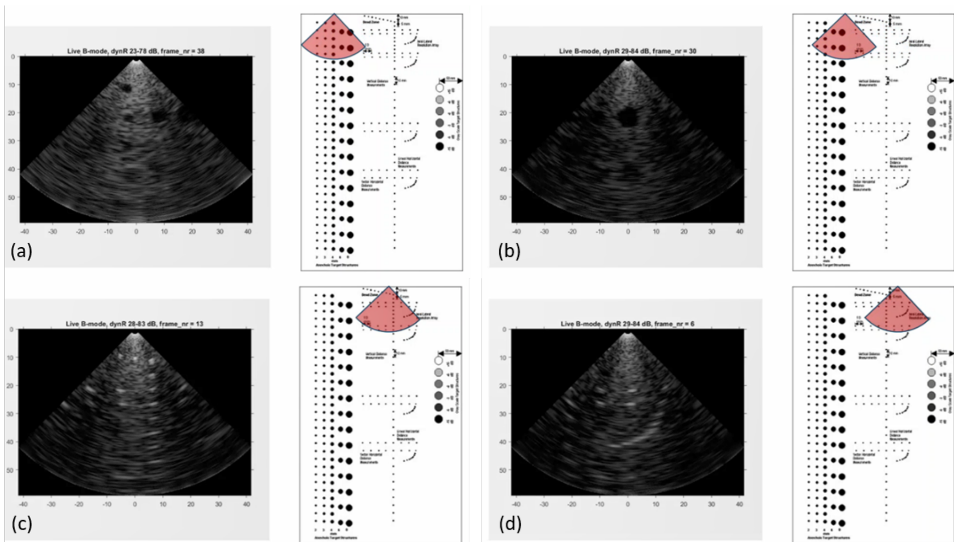


Figure 3.14: Typical generated ultrasound images using digital ICE demonstrator setup, successfully imaging both anechoic (a), (b) and echoic features (c), (d) of a multi-purpose ultrasound phantom.

cables to one optical fiber. It also proves the versatility of the ODLM, which is suitable for IVUS or ICE catheters and other minimally integrated systems that require high speed, galvanically isolated data link.

3.5. INDUSTRIALIZATION PERSPECTIVE

So far, the ODLM fabrication, assembly, characterization, and integration results have successfully demonstrated the proof of concept. From an industrialization perspective, it is attractive to discuss some ideas for the mass production of the ODLM to fit into a future digital catheter production line. Moreover, it is also valuable to discuss more ODLM industrial applications other than in smart catheters. This section addresses these two aspects: device assembly and device applications.

3.5.1. DEVICE ASSEMBLY

The ODLM assembly process presented earlier in this chapter are rather intricate. Because of the nonstandard materials and the semi-flexible F2R components, the assembly process involve many manual manipulatrions, such as high accuracy VCSEL assembly and the ODLM interposer assembly. Manual handling offers great flexibility for process development and optimization for experimental purposes, as in this thesis work. However, these manual assembly processes need to be further adapted for industrial production.

VCSEL ASSEMBLY

The selection of integration components can significantly affect the entire production process, including the design and assembly. However, it is hard to find components

that fit the application 100%. Many extra efforts are necessary to adjust the component compatibility. The candidate VCSLE, ULM850-14-CHIPS, was chosen for several reasons. In the first place, because it is a VCSEL specifically developed for high-speed data communication, its submillimeter dimensions fit in the small space inside a smart catheter tip. Its large laser emitting spot (around 20 μm in diameter) can easily match the multi-mode fiber, which allows for the self-alignment feature in the ODLM. Finally, the two bondpads of the VCSEL are on the same side, together with the laser emitting spot, which is compatible with the ODLM interposer design. In contrast to the experimented assembly sequence presented in this thesis, the optimum assembly sequence is to apply solder bumps on VCSELs first at a wafer level with industrial tools, instead of on the ODLM interposer. Then the VCSELs are diced and directly flip-chipped to the ODLM interposer. However, lacking solder masks on the contact pads makes it impossible to apply solder spheres directly to the VCSEL. Otherwise, the solder spheres will be reflowed uncontrollably and cause solder bridging (short circuits). As a result, the solder spheres were placed on the ODLM interposer manually one by one, as described in the ODLM assembly section, severely complicating the VCSEL placement process.

There are two possible solutions to industrialize the VCSEL assembly process. The first solution is to use solder sphere jetting, which can "shoot" solder bumps automatically on the fragile ODLM interposers at a wafer level. VCSELs can then be flip-chipped onto the ODLM interposer wafer with a pick and place tool. Solder sphere jetting can place a few solder spheres per second, significantly improving the assembly speed. The other solution is to convince the VCSEL manufacturer to develop a customized VCSEL for our application. The customized VCSEL should have the specified dimension (or even smaller), contact pads, and supportive dummy pads suitable for solder bumps, which will significantly simplify the VCSEL assembly process. However, the manufacturer will request a large volume order to customize the VCSEL production. Therefore, this solution can only apply when large market potential exists.

ODLM interposer assembly

The challenge of assembling the ODLM interposer is the handeling of the extremely small semi-flexible structures and the control of the bending & fixation process on a larger scale. In this case, optimized layout design and customized assembly tools & setup should help with simplifying the assembly process.

Instead of placing only one ODLM device in one silicon frame as presented earlier, several ODLM devices can be placed in one silicon frame at a time and lined up in a row, as shown in Figure 3.15a. The VCSELs can be flip-chip assembled onto the ODLM interposer at a wafer level with a pick and place tool. After this, the wafer can be turned upside down, and adhesives can be dispensed onto the thin silicon islands (Figure 3.15b). Finally, all the first silicon elements can be bent 90 degrees and fixated to the thin silicon islands in one step (Figure 3.15c). In this way, multiple ODLMs can be assembled simultaneously, avoiding the one-by-one assembly process. For the fiber insertion process, an alignment tool could be helpful to guide the fiber into the through silicon hole. The alignment tool can be, for example, a 3D printed funnel-shaped module that can be temporarily fixed at the end of ODLM (Figure 3.15d). The funnel shape should guide the fiber into the through silicon hole without requiring any further inspection.

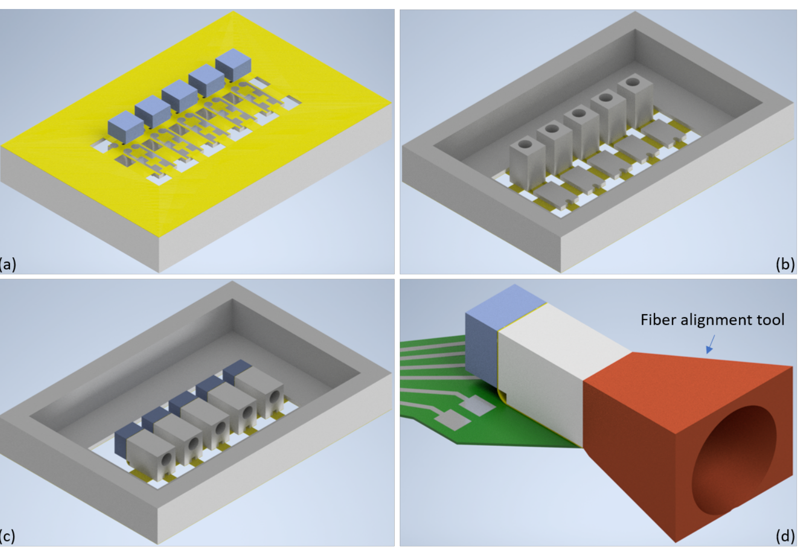


Figure 3.15: Possible ODLM interposer assembly industrialization. (a)Multiple ODLM are designed in a row within a silicon frame. The VCSELs can be flip-chipped on the front side. (b) Dispense adhesives on the thin silicon pieces (c)Release polymer tabs partially and bend all the first silicon elements in one go. (d) Use a funnel-shaped tool to simplify fiber insertion process.

3.5.2. DEVICE APPLICATION

In Section 3.4, we have successfully integrated the OLDM in an ICE demonstrator to demonstrate that the ODLM can be widely applied in smart catheter applications. There are also other potential ODLM applications for optical interconnects in data centers. Optical interconnects are being used in high-speed signal transmission between rack-to-rack, board-to-board, and even chip-to-chip[12, 13]. The trend towards miniaturization challenges the integration of the optical interconnects. Several optical interconnection integration schemes have been proposed in previous studies, such as the silicon optical bench (SiOB) that uses various 45-degree reflectors for non-coplanar coupling of the optical components to the fibers[14], optical PCB technology based on polymer waveguides[15], and silicon interposers with a mechanical optical interface (MOI)[16]. Most of the existing optical interconnection schemes require high-precision optical component alignment, customized PCBs with embedded waveguide routing, millimeter-scale interposers, and long connection distances, most of the time combined with complex assembly steps. The ODLM presented in this thesis work uses highly flexible interconnects to redirect the electrical connections to the side of the module, allowing the optical modules to be directly flip-chipped onto the driving ASICs to reduce the length of the interconnects. Its submillimeter scale dramatically increases the integration density.

We can also extend the stand-alone ODLM to a 1×4 ODLM array to further increase the optical integration density. The 1×4 ODLM is designed and fabricated based on the same F2R concept. It contains four stand-alone ODLMs connected by the silicon substrate, as shown in Figure 3.16a. The fabrication process is the same as the stand-alone

ODLMs. We use a 1×4 VCSEL array with pre-placed Ø60 µm solder spheres on the contact pads for the 1×4 ODLM (Figure 3.16b). These new VCSEL arrays were provided by the VCSEL manufacturer at a later stage of the project. It allows for the VCSEL array to be assembled onto the ODLM array with a standard flip-chip process and results in a final dimension of only 280 µm×960 µm×600 µm (Figure 3.16c). The assembled ODLM array acts as a stand-alone device that can be flip-chipped on chips or PCBs, avoiding the complexity of assembling multiple seperate components. The four VCSELs can be driven simultaneously and achieve an even higher data rate with a customized multi-channel laser driver. Figure 3.16d shows an assembled ODLM array on a 40 µm-thick flex PCB, with four optical fibers inserted into the through-silicon holes.

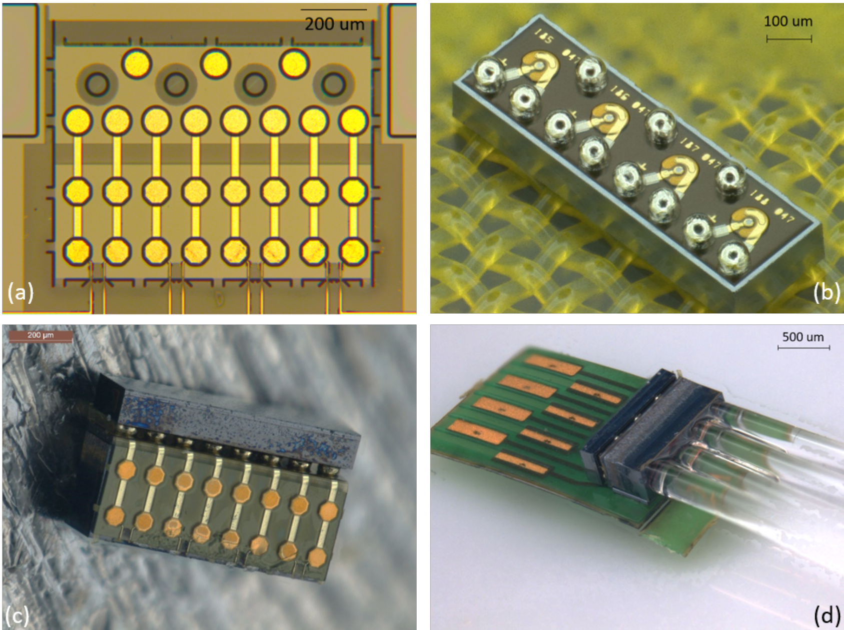


Figure 3.16: 1×4 ODLM array for high density optical integration. (a) Fabricated 1×4 ODLM array in a silicon frame (b) A 1×4 VCSEL array with Ø 60 µm solder spheres on contact pads; (c) 1×4 ODLM array with VCSEL assembled (d) 1×4 ODLM array with optical fibers assembled on the flex PCB.

3.6. CONCLUSION

In this chapter, the ODLM assembly, characterization, and integration work are presented. The fabricated ODLM interposers were provided with UBMs by an external supplier, and VCSELs were assembled with a manual solder flip-chip process. After the device folding, fixation, a 125 µm diameter optical fiber was connected by inserting it into the through silicon hole (TSH) of the ODLM so that it was automatically self-aligned to the emitting spot of the assembled VCSEL. Eye diagrams were used to characterize the optical performance of the ODLM. The stand-alone ODLM can transmit up to 25.8 Gb/s $2^{31}-1$ PRBS when driven through a high-speed bias tee. The BER test indicates that

error-free operation can be achieved at an optical output of -4 dBm. A catheter application customized 6 Gb/s laser driver ASIC was designed for the ODLM and assembled on a laser driver board. The ODLM was connected to the laser driver board via a flexible PCB. The signal integrity test indicates that the ODLM can transmit 7 Gb/s $2^{15}-1$ PRBS when integrated with the customized 6 Gb/s catheter laser driver.

Although the ODLM was designed based on specifications of an IVUS catheter, it can be widely applied in other catheter systems as well. A digital ICE catheter system lab setup was shown to demonstrate the ODLM integration and versatility. The ODLM was integrated into the ICE system, together with other digital modules, successfully transmitting a data rate of 6 Gb/s and resulting in high-resolution ultrasound images.

The results presented in this and the previous chapters demonstrated the feasibility of a coronary-catheter-size compatible ODLM. It is also a good example of the versatility of the F2R platform technology. The ODLM can dramatically reduce the assembly costs and simplify the assembly process to integrate optical data transmission into miniaturized systems, such as smart catheters. A few industrialization ideas are discussed. Some automated assembly steps can be introduced to industrialize the VCSEL flip-chip process.

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4

HIGH-DENSITY EMBEDDED TRENCH CAPACITORS IN THE F2R

Parts of this chapter have been published in [1]

4

4.1. BACKGROUND

4.1.1. DECOUPLING CAPACITORS IN MINIATURIZED SYSTEMS

The tip of smart catheters comprise multiple electronic modules, such as pulser, low-noise filter, time gain compensation amplifier, and control logic. These electronic modules are connected to the power supply through interconnects with non-zero resistance and inductance. Because of this non-zero impedance in the interconnects, the voltage drop at the electronic module changes with the current change. If the electronic modules share the same interconnect to the power supply, current change in one module may produce large voltage drops or ground bounce and affect the operation of other modules, leading to the main cause of signal degradation, known as Delta-I noise [2]. To reduce the power ripples caused by interconnect impedance, decoupling capacitors can provide a bypass path for transient currents [3].

$$i(t) = C\frac{dv(t)}{dt} \tag{4.1}$$

A decoupling capacitor works as a local energy storage between the power supply and the electronic modules. According to Eq.4.1, the decoupling capacitor can provide transient currents when voltage drops occur in the power supply lines. When the capacitance is large enough, the transient current provided by the decoupling capacitor can limit the voltage drop within an acceptable range and, therefore, improves the signal integrity. To reduce the effect of the interconnect impedance, decoupling capacitors are preferably placed as close as possible to the electronic modules.

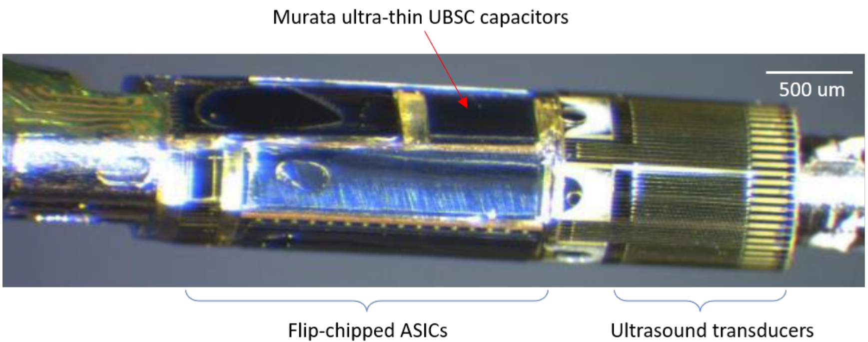

Figure 4.1: Assembled smart tip of IVUS catheter, with flip-chipped discreet Murata ultra-thin UBSC capacitors

Figure 4.1 shows the case study: an assembled IVUS smart catheter tip with a diameter of 1.2 mm and a length of around 5 mm. The ultrasound transducers are microfabricated on the F2R structures, and the ASICs are assembled on top of that. The small form factor of such a smart catheter tip puts severe limitations on the dimension and thickness of all components. The decoupling capacitors used in this case are discrete ultra-thin UBSC capacitors commercially available from Murata [4]. These ultra-thin capacitors have a thickness of only 100 µm, and are assembled next to the ASIC on the F2R thin substrate, consuming lots of catheter tip space and challenge the integration

process. Therefore, a better solution is to embed high-density capacitors into the substrate onto which the ASICs are flip-chipped. Embedded capacitors save the space of the discrete capacitors in the catheter tip and also bring the decoupling capacitors right underneath the ASICs.

4.1.2. EMBEDDED TRENCH CAPACITORS IN F2R

High capacitance may be achieved by decreasing the dielectric thickness, increasing the surface area, or by using high-k dielectrics. Trench capacitors have a high capacitance because of their 3D electrodes increase the surface area. Figure 4.2 presents the 3D drawing of the ultra-high density trench capacitor in silicon developed by F. Roozeboom et al. [5, 6]. High-aspect ratio trenches or pores are etched into the substrate as the lower electrode, creating 3D topography. An Oxide-Nitride-Oxide (ONO) dielectric and top electrodes are deposited on top subsequently. Compared with the single-layer dielectrics, the ONO stack dielectric layer can efficiently lower the leakage current and increase the breakdown voltage [7]. Capacitance density, defined as the total capacitance over the flat surface area, is significantly enhanced by these 3D trench electrodes compared to flat capacitors.

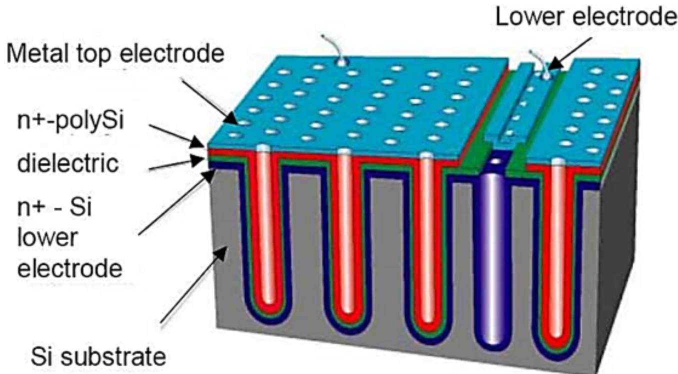

Figure 4.2: Ultra-high density trench capacitors in silicon by F. Roozeboom et al. [5, 6]

The in-substrate feature and high capacitance density make the trench capacitor very suitable for F2R integration. Additionally, its small surface opening makes it possible to close the trenches from the top to enable further F2R processing. Figure 4.3 presents the proposed process flow to integrate trench capacitors in the F2R platform. Trench capacitors can be fabricated using an SOI substrate, as shown in Figure 4.3a. The location of the trench capacitors should be directly underneath the area where ASICs will be assembled. With the proper trench diameter, the trench opening can be closed from the top by depositing a PECVD oxide layer. The same oxide layer can be used for the first step of the F2R flow, the buried trench process, to isolate the different silicon islands (Figure 4.3b). After closing the buried trenches, sensors, transducers, silicon level interconnects, and flexible interconnects can be fabricated on the planer wafer surface (Figure 4.3c). Finally, the silicon islands are released in the same way as in the standard F2R process (Figure 4.3d).

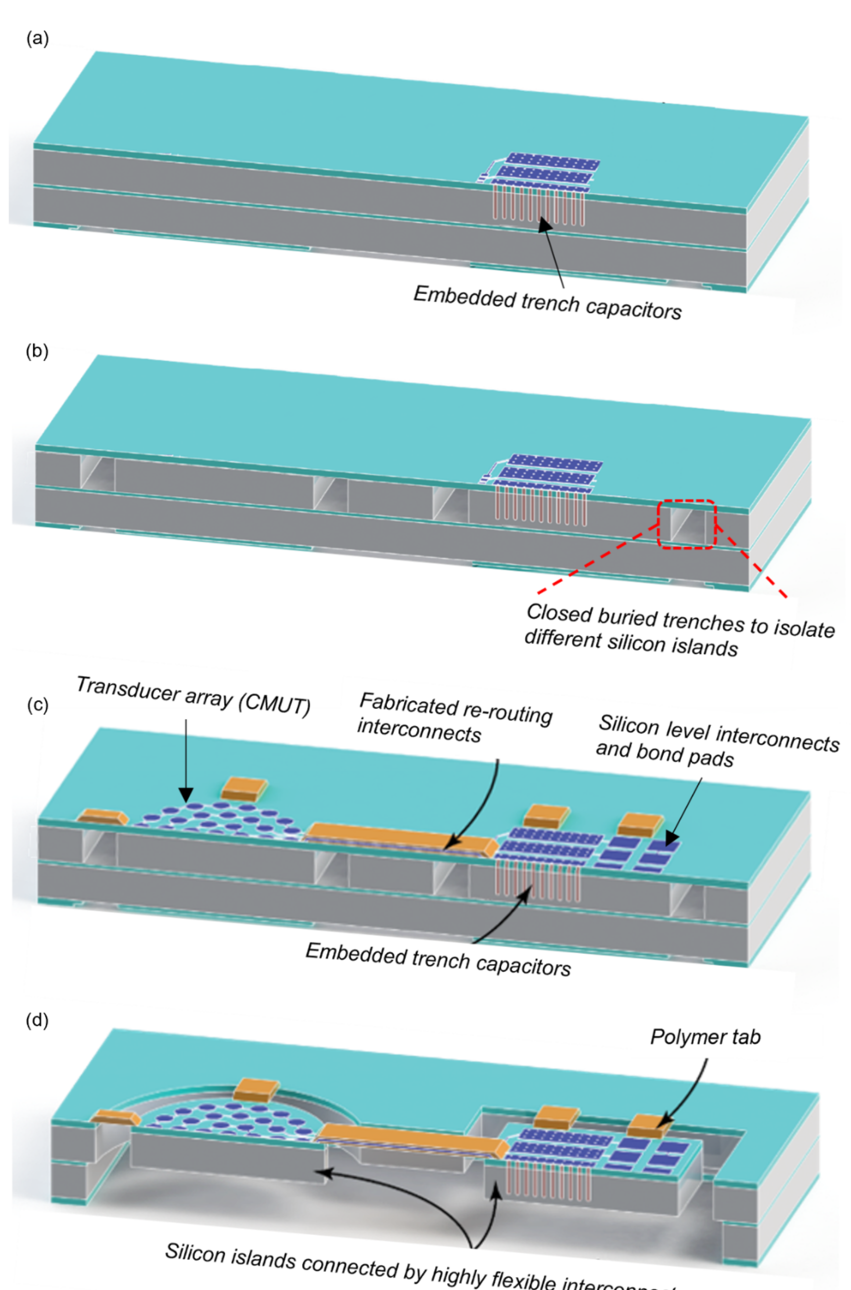

Figure 4.3: Proposed process to integrate trench capacitors in the F2R platform. (a) Fabricate trench capacitors on the specific location where ASICs are to be assembled, (b) Close the trench openings and fabricate buried trenches of the F2R process; (c) Fabricate sensors, silicon level interconnects and flexible interconnects; (d) Release silicon islands with backside etching.

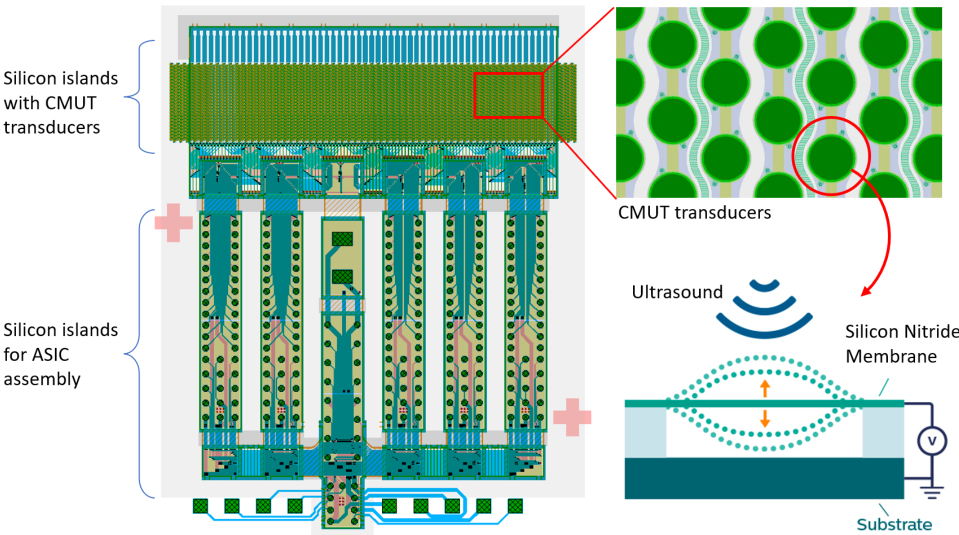

Figure 4.4: Layout design of an IVUS catheter tip and CMUT transducers.

4

This chapter uses an IVUS catheter as a case study. The smart tip of the IVUS catheter is fabriacted using the F2R platform. As shown in Figure 4.4, it contains silicon islands with fabricated CMUT transducers, silicon islands for ASIC flip-chip process, silicon level metal routing, and flexible interconnects. The ideal locations to integrate decoupling capacitors for the ASICs are in the six silicon islands onto which the ASICs will be flip-chipped. Each island has a dimension of 320 µm × 1700 µm × 40 µm. The ASICs require the breakdown voltage of the decoupling capacitors to be at least 30 V with a capacitance as high as possible. There are two compatibility challenges in the integration process. First, the 700 nm-thick PECVD oxide used for the standard F2R buried trench etching should be able to close the trench openings to allow follow-up F2R processing. So, the trench openings on the wafer surface must be sufficiently small after the trench capacitors fabrication. Therefore, a suitable high-aspect-ratio trench capacitor etching process needs to be developed.

Secondly, introducing trench capacitors into the 40 µm-thick silicon islands of the F2R structures removes substrate material, which reduces the substrate rigidity. During subsequential processing, residual stresses from different thin films may result in a deformation of the F2R thin silicon islands, which can be fatal for the device assembly process. In the IVUS catheter case, these thin films that contribute to residual stress include layers from the F2R process (mainly PECVD oxide depositions) and the silicon nitride layer used for the CMUT membrane fabricated on other F2R silicon islands. The possible substrate deformation that may be caused by introducing the embedded trench capacitors needs to be evaluated.

4.1.3. SCOPE OF THIS CHAPTER

This chapter consists of two parts corresponding to the aforementioned compatibility challenges. Part I focuses on the development of trench capacitors suitable as decoupling capacitors and compatible with the F2R process flow. The key process developments include the high-aspect-ratio (HAR) trench etching process and the trench closing process. Different trench diameters and capacitor areas are designed for the process developments. The fabrication and electrical measurement results will be presented.

Part II demonstrates the trench capacitor integration process in the F2R platform developed in Part I and evaluates the F2R thin silicon island bending caused by the introduction of the trench capacitors. Cantilevers with the same dimension as the silicon islands for ASIC assembly in the IVUS catheter are integrated with trench capacitors and fabricated with the F2R process. The trench capacitors have different diameters and pitches. The same silicon nitride layer as in the CMUT process was deposited on the cantilevers to mimic the IVUS catheter tip fabrication. A finite element analysis (FEA) was used to model the cantilever bending. A digital holographic microscope (DHM) was used to determine the bending of the fabricated cantilevers. The fabrication results and electrical measurements of the trench capacitors in the F2R-based cantilevers will be presented. The relationship between the cantilever bending depth and the trench designs will be discussed.

4.2. PART I: PROCESS DEVELOPMENT & INTEGRATION OF TRENCH CAPACITORS

4.2.1. DESIGN OF EXPERIMENTS

The aim of this section is to develop a process for the F2R compatible HAR trench capacitors. The two most critical steps in the process development of Part I include the high-aspect-ratio (HAR) trench etching with micron-scale trench opening and the trench closing. The design layout for a test to develop the trench capacitor process is shown in Figure 4.5. Figure 4.5a depicts the layout of the trench capacitors. Trenches with diameters of 1.1 µm and 1.2 µm are located in a square area of 300 µm × 300 µm and 1000 µm × 1000 µm on a pitch of 4 µm, and the target trench depth is 30 µm. The trenches were designed as octagons instead of circles to reduce the mask file size. These octagons will turn into circles during the lithography process. Each trench capacitor contains two electrodes, one is formed by the silicon substrate, and the other is formed by the top poly-Si electrode. Figure 4.5b shows slanted trench arrays for trench cross-section inspection. For the HAR trench etching development, SEM cross-section inspections were required to determine the profile of the trenches. The slanted arrays can significantly increase the chance of breaking through the micron-scale trenches while preparing cross-section samples. Figure 4.5c presents the process control modules (PCMs) used to verify each process step during the fabrication. These PCMs include Van der Pauw, linewidth control, Kelvin, and daisy chain structures for sheet resistance and contact resistance characterization.

The desired breakdown voltage of the decoupling capacitors should be at least 30 V, and the capacitance as high as possible. As introduced previously, using ONO stack dielectric layers can effectively lower the leakage current and increase the breakdown

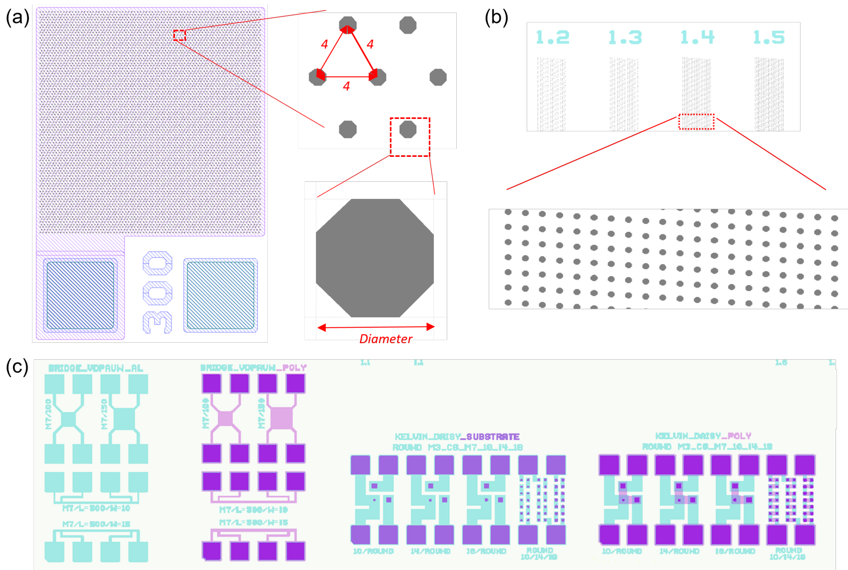

Figure 4.5: Design layout of developing trench capacitor process, including: (a) trench capacitors with area of 300 µm × 300 µm and 1000 µm × 1000 µm; (b) slanted trench arrays for cross section inspection; (c) electrical test structures (from left to right): Van der Pauw structures, linewidth control structures, Kelvin structures and daisy chain structures.

voltage. The ONO stack dielectric layer in the trench capacitors can be simplified as three capacitors in series, as shown in Figure 4.6.

The voltage (V_1) over C_1 can be calculated as:

$$V_1 = V_{tot} \frac{C_2C_3}{C_2C_3 + C_1C_3 + C_1C_2} = V_{tot} \frac{\varepsilon_2 d_1}{\varepsilon_1 d_2 + \varepsilon_2(d_1 + d_3)} \tag{4.2}$$

Where V_{tot} is the voltage applied to the entire ONO capacitor, d_1, d_2, d_3 are thicknesses of the dielectric layers, ε_1 and ε_2 are relative dielectric constants of silicon dioxide and silicon nitride, 3.9 and 7.9, respectively [8]. As $\varepsilon_2 \approx 2\varepsilon_1$, Eq. 4.2 can be simplified to:

$$V_1 = V_{tot} \frac{2d_1}{2d_1 + d_2 + 2d_3} \tag{4.3}$$

The breakdown voltage of such an ONO capacitor is defined as the breakdown of one of the ONO dielectric layers. The breakdown of the dielectric layer is determined by the electrical breakdown field strength, as shown in Eq. 4.4:

$$V_{BV} = E_{BV} \times d \tag{4.4}$$

$$V_{BV1} = E_{BV1} \times d_1 = V_{BV_total} \frac{2d_1}{2d_1 + d_2 + 2d_3} \tag{4.5}$$

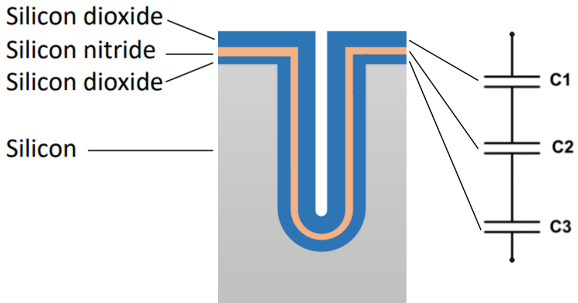

Figure 4.6: ONO dielectric layer in the trench capacitor can be simplified as three capacitor in series.

Literature reports an electric field strength (E_{BV}) of approximately 1 V/nm for both silicon dioxide and silicon nitride [9]. Therefore, combine with Eq. 4.5, the breakdown voltage of the ONO capacitor is given by:

$$V_{BV_total} = d_1 + \frac{d_2}{2} + d_3 \tag{4.6}$$

The thickness of the dielectric layers in the ONO stack can be adjusted based on Eq. 4.6 to obtain the required breakdown voltage of 30 V. Earlier work used a combination of 5 nm SiO_2, 15 nm SiN_x, and 30 nm SiO_2 ONO layer [10], which has a breakdown voltage of 42.5 V. Although it might lower the capacitance density, the higher breakdown voltage guarantees the requested breakdown voltage of 30 V.

4.2.2. FABRICATION

A schematic representation of the trench capacitor process is shown in Figure 4.7. The fabrication starts with a 6-inch n-type silicon substrate that functions as the bottom electrode of the trench capacitor. First, a 700 nm thick PECVD SiO_2 layer is deposited and patterned, creating an SiO_2 hard etch mask with trench diameters of 1 μm and 1.1 μm (Figure 4.7a). The trench openings from the SiO_2 mask are then dry etched 30 μm deep into the silicon substrate to form trenches. The developed HAR DRIE dry etch recipe will be described in the next sub-section. The SiO_2 mask is subsequently removed by wet etching and followed by an oxygen plasma for 45 minutes at 130°C to remove passivation residues inside the deep and narrow trenches (Figure 4.7b). The HAR DRIE trench etching process also introduces undesired silicon scallops on the sidewall of etched trenches that will reduce the breakdown voltage of the trench capacitors. These unwanted silicon scallops can be reduced by a thermal oxidation and wet etching.

The next step is to deposit the ONO dielectric layer in the trenches (Figure 4.7c). The ONO dielectric layer of our fabricated trench capacitors consists of a 5 nm thermal oxide layer, a 15 nm low-pressure chemical vapor deposition (LPCVD) silicon nitride layer, and a 30 nm LPCVD TEOS layer. The thermal oxidation and the LPCVD processes guarantee proper layer coverage inside the HAR trenches. The thickness of each dielectric layer can be adjusted if other capacitance densities and breakdown voltages are desired. A 300 nm thick layer of polycrystalline silicon (poly-Si) is deposited on the dielectric layers

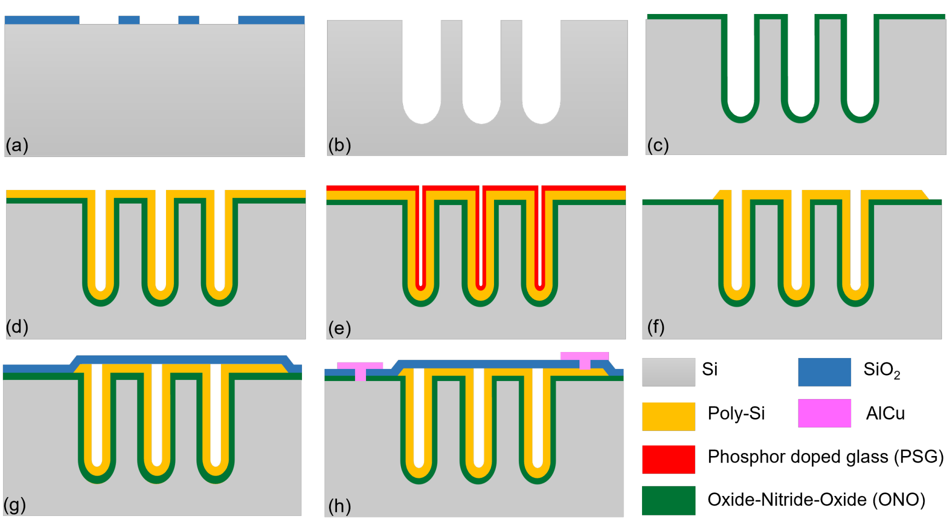

Figure 4.7: Process flow for embedded high-density trench capacitor. (a) Pattern SiO_2 mask for trench DRIE; (b) DRIE etch HAR trenches; (c) Deposit Oxide-Nitride-Oxide (ONO) dielectric layer; (d) Deposit poly-Si as the top electrode; (e) Deposit phosphor doped glass (PSG) and anneal to dope poly-Si; (f) Remove PSG and pattern poly-Si, create slope on the poly-Si edge; (g) Deposit SiO_2 to close trench; (h) Etch SiO_2 landing on substrate and poly-Si, deposit and pattern metal contact.

as the top electrode of the capacitor (Figure 4.7d). To reduce the series resistance of the top electrode, an 85 nm thick phosphor doped glass (PSG) is deposited as a solid dopant source, and a 30 min annealing step at 1000 °C migrates the dopant atoms from the PSG into the poly-Si (Figure 4.7e). The PSG layer is removed in buffered HF (BOE7:1). A poly-Si specific resistance of around 1.1 mΩ·cm is obtained after the doping process.

To pattern the top poly-Si electrode, 1.3 µm positive photoresist is coated onto the wafer. Because of the sub-micron diameter of the trench openings after the dielectric and poly-Si deposition, 1.3 µm positive photoresist is thick enough to cover the trenches during resist spinning. After exposure, the patterned photoresist is hard-baked to create a slope. This slope is transferred into the poly-Si during the dry etching process to provide a better step coverage for the follow-up processes. An oxygen plasma of 45 minutes at 130°C is applied to remove photoresist residues inside the trenches (Figure 4.7f). A 700 nm thick PECVD low-stress SiO_2 layer is subsequently deposited to close the trenches (Figure 4.7g). Next, contact openings are dry-etched through the closing SiO_2 layer, landing on the Si substrate and the poly-Si. Finally, 1 µm AlCu is deposited and wet-etched to make contact with the top and bottom electrodes (Figure 4.7h).

4.2.3. PROCESS OPTIMIZATION

HAR TRENCH ETCHING PROCESS DEVELOPMENT

The HAR trench etching step (Figure 4.7b) is the most critical step in the trench capacitor process. In this Bosch etching process, each etching cycle consists of an etching phase, a deposition phase, and a boost phase. It starts with the etching phase, where the silicon

substrate is isotropically etched. During the deposition phase, a thin Teflon-like passivation film is deposited on the isotropically etched surface. The anisotropic etching in the boost phase removes only the bottom part of the passivation film, leaving the sidewall protected and allowing the new etching phase to continue etching deeper [11].

The SiO_2 mask for trench etching has trench openings with diameters of 1 µm & 1.1 µm. The trench opening size is crucial for the trench closing process and, therefore, only a very small under-etch can be tolerated. The small trench diameters limit the in-and-out flow of the reactive ions or radicals during DRIE etching and also cause the etching species to collide with each other. The collision of the etching species leads to unwanted horizontal etching inside the trenches, and hence results in rough sidewalls and varying widths of the trenches. To reduce the under-etch and optimizie HAR etching, the dry etching is split into two parts. A "start DRIE" transfers the trench diameter from the SiO_2 mask into silicon, followed by a "main DRIE" to complete the remainder of the trench etching.

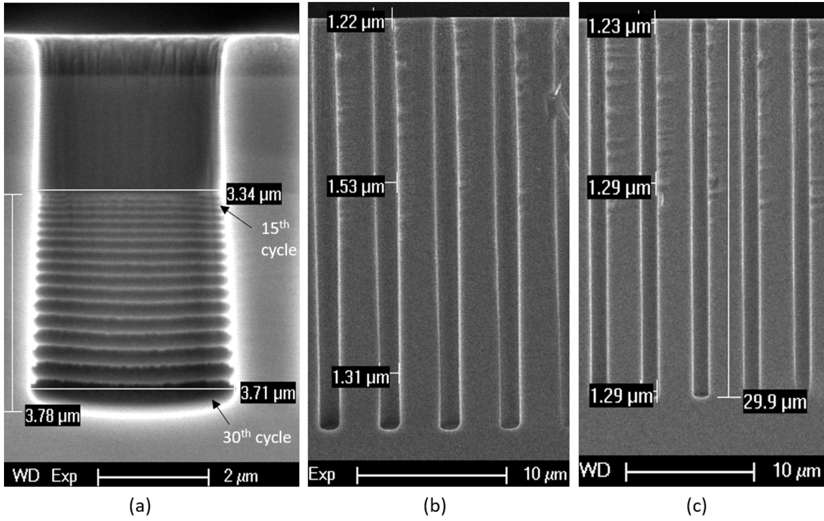

Figure 4.8: SEM images of the trench etching tests (a) Cross-section image of the ramped-up bias power test. 30 etching cycles were applied, only 20 scallops (etched by 10th to 30th etching cycles) can be identified in the silicon. The bias power corresponding to the 15th cycle is chosen to transfer the oxide trench opening mask into the substrate (b) “Belly” trenches etched before the optimization of the etching cycles, the trenches are wider in the middle; (c) trenches etched with the optimized HAR recipe, without unwanted horizontal etching in the middle, and minimized trench wall roughness.

To transfer the oxide hard mask into silicon, the DRIE process usually starts with the anisotropic etching cycle which results in around 300 nm of under-etch. The "start DRIE" part aims to minimize this under-etch caused by the anisotropic etching cycle. The bias power, which accelerates the ions bombarding the etch target, is crucial in the DRIE etching cycles. Sufficient bias power is necessary to break through the passivation layer from the deposition phase and provide a sufficient etching rate, while excessive bias power results in a large nonideal under-etch. The effect of varying of the bias

power on the under-etch was investigated. A test recipe with thirty etching cycles with a ramped-up bias power was applied to the test mask for trench etching. The start of the test recipe had such a low bias power that it could not break through the passivation layer. As a result, the test recipe cannot etch into the silicon in the first few starting cycles. After the bias power was ramped up in the subsequent cycles, a trench could be etched, and the scallops in the sidewall grow larger and larger. Figure 4.8a shows the cross-section SEM image of the ramped-up bias power test. The top part is the SiO_2 mask, and the bottom part has the scallops etched into silicon by the test recipe. Only 20 scallops are identified from the cross-section image, which indicates that the bias power was insufficient to break through the passivation layer in the first ten etching cycles. The 15th cycle shows an under-etch of around 100 nm, and the last etching cycles give an under-etch of 200-300 nm. Therefore, the bias power corresponding to the 15th cycle is chosen.

The challenge for the "main DRIE" part is controlling the etching species. Additional pumping and venting time was added in between each etching cycle so that the etching species could have enough time to flow in and out freely without collision, which reduces the unwanted horizontal etching caused by the species collision. A comparison can be seen in Figure 4.8b and Figure 4.8c. Figure 4.8b shows the "belly" trenches etched before optimization. The top and bottom of the trench are 1.22 µm and 1.31 µm, while the middle of the trench is around 300 nm wider because of the unwanted horizontal etching. In Figure 4.8c, the "belly" is significantly reduced after the optimization. The horizontal etching also affects the roughness of the trench wall. A reduced processing temperature of 10 degrees is chosen to provide a thicker passivation layer during the etching process and to protect the trench wall from the collision effect.

The trenches are etched with the "start DRIE" and the "main DRIE" combined recipe in the final process. For SiO_2 masks with trench diameters of 1 µm and 1.1 µm, the etching recipe results in trenches with a diameter of 1.1 µm and a depth of 25 µm. The trenches with a diameter of 1.2 µm have a depth of 30 µm. The roughness of the trench wall was further reduced by the subsequent thermal oxidation.

TRENCH CLOSING

To be compatible with the F2R process, the fabricated trench capacitors need to be closed with the 700 nm low-stress PECVD SiO_2 layer that is used as the standard F2R buried trench etch mask. The closure test is carried out on the capacitors with trench diameters of 1.1 µm and 1.2 µm. After the dielectric and poly-Si deposition inside the trenches, the trench openings left to be closed are around 350 nm and 480 nm, respectively. Figure 4.9a-b show SEM cross-section images of the closure test. The 700 nm PECVD SiO_2 layer is not sufficient to close the openings. The 1.1 µm diameter trench capacitors still have a gap of around 75 nm, and the 1.2 µm diameter trench capacitors still have a gap of around 188 nm. To demonstrate the trench closure concept, a 1 µm-thick PECVD SiO_2 layer was deposited to close the 1.1 µm diameter trench capacitors (Figure 4.9c), which closed the trenches.

One option to close the trenches with the standard 700 nm-thick SiO_2 layer is to use a thicker poly-Si layer as the top electrode, which will result in smaller openings to be closed. However, the PSG deposition for poly-Si doping also requires a sufficiently wide

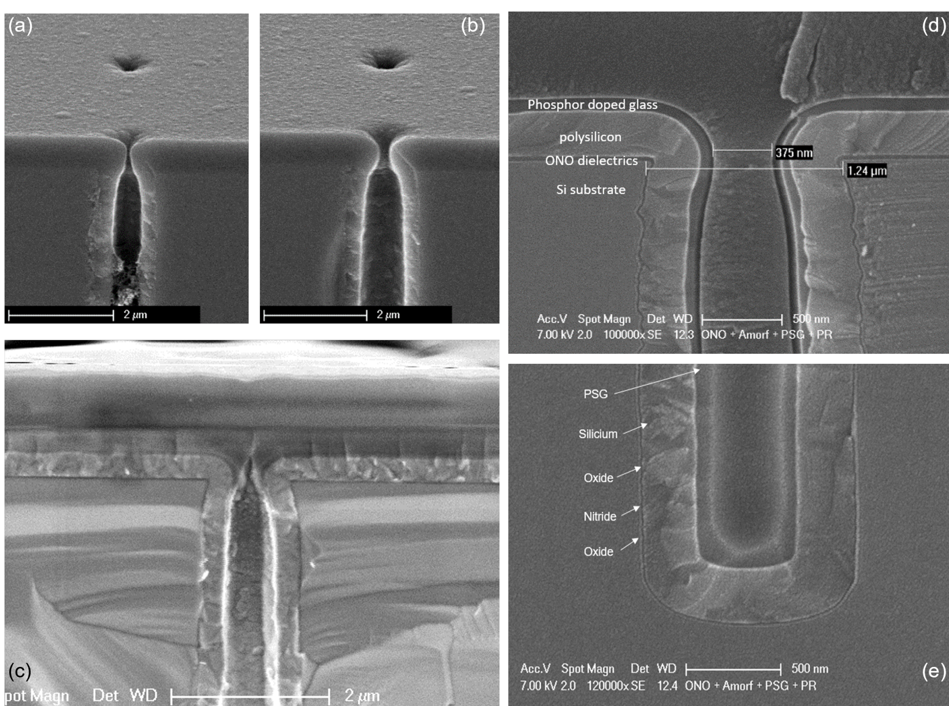

Figure 4.9: SEM cross-section images of (a) 700 nm PECVD SiO_2 deposited on 1.1 µm diameter trench capacitors, (b) 700 nm PECVD SiO_2 deposited on 1.2 µm diameter trench capacitors, and (c) 1 µm PECVD SiO_2 closing the 1.1 µm diameter trench capacitors. (d-e) top part and (e) bottom part of the 1.2 µm diameter/ 30 µm deep trench capacitor with all deposited layers before the PSG removal and trench closing step.

opening for a uniform deposition inside the trenches. Further tests are needed to define the optimal poly-Si thickness. Ideally, in-situ doped poly-Si deposition can also solve the problem, but this requires special deposition equipment. Depositing the 1 µm-thick instead of 700 nm-thick PECVD SiO_2 layer would be the simplest solution to close the trenches, but whether the thicker SiO_2 layer will interfere the remaining F2R process will be verified in the Part II of this chapter.

4.2.4. RESULTS AND CHARACTERIZATION

ONO trench capacitors with a diameter of 1.1 µm and 25 µm in-depth and ONO trench capacitors with a diameter of 1.2 µm and 30 µm in-depth were fabricated on planer wafers. The trenches were designed on a pitch of 4 µm, with total wafer surface areas of 300 µm × 300 µm and 1000 µm × 1000 µm. Flat capacitors with the same total capacitor areas were manufactured for comparison. Figure 4.9d-e shows an SEM cross-section image of a 1.2 µm diameter trench capacitor with all deposited layers before the trench closing step. The SEM image shows that the 100 nm PSG layer, the 300 nm poly-Si, and the ONO dielectric layers all have sufficient and uniform coverage on the trench side walls and in the trench corners.

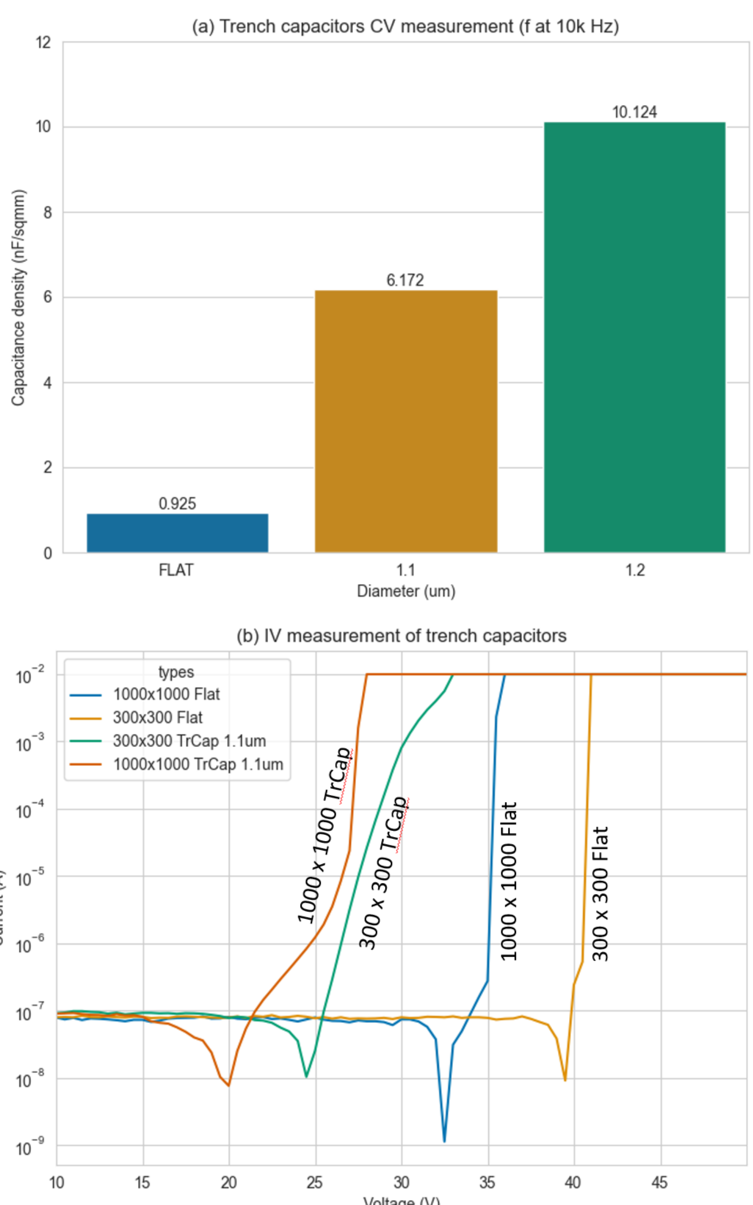

Figure 4.10: Electrical characterization of ONO Trench Capacitors vs ONO Flat Capacitors. (a) Capacitance density (nF/mm^2) of flat capacitors, compared to trench capacitor with 1.1 µm diameter trenches and trench capacitor with 1.2 µm diameter trenches (pitch = 4 µm); (b) Breakdown voltage of 1000 × 1000 µm 1.1 µm diameter trench capacitor, 300 × 300 µm 1.1 µm diameter trench capacitor, 1000 × 1000 µm flat capacitor and 300 × 300 µm flat capacitor; 1.1 µm and 1.2 µm diameter trench capacitors share similar breakdown characteristics.

The electrical characterization is performed using a four-point needle probe system, connected to a KEITHLEY 4200-SCS semiconductor characterization system. The electrical characterization results are presented in Figure 4.10. The CV characteristics of the fabricated capacitors were carried out at 10 kHz. Compared to a capacitance density of 0.93 nF/mm^2 for the flat capacitors, the 1.1 µm & 1.2 µm diameter trench capacitors have a capacitance density of 6.2 nF/mm^2 and 10.1 nF/mm^2, respectively. IV characterization was performed to measure the breakdown voltage of the capacitors. The 1.1 µm diameter trench capacitor with total areas of 300 × 300 μm^2 and 1000 × 1000 μm^2 have breakdown voltages of 32 V and 28.5 V, respectively. In comparison, the 300 × 300 μm^2 and 1000 × 1000 μm^2 flat capacitors have breakdown voltages of 41 and 36 V, respectively.

There are a few possible explanations for the reduction in breakdown voltages. Capacitors with a larger total area have larger functional area so that the chance for a defect in the dielectric layers is increased, hence resulting in lower breakdown voltages. Trench capacitors not only have larger functional areas, but also have complicated topographies. Sharp corners of trench openings, bottom corners inside trenches, and the roughness of trench walls all contribute to lower breakdown voltages. Process optimization to reduce the nonideal topography in the trench capacitors is a possible measure to improve the breakdown voltage and make it less area dependent.

4

4.2.5. DISCUSSION

To integrate decoupling capacitors in F2R, a HAR trench etching recipe was developed to achieve a maximum aspect ratio of 1.2:30 and a straight trench profile. The 1.1 µm and 1.2 µm diameter trench capacitors were not closed by the desired 700 nm thick PECVD SiO_2 layer. However, closing the trench capacitors with 1 µm thick PECVD SiO_2 showed that the trench closing concept needs further development, which will be used in the next section. The fabricated trench capacitors were fully functional. The capacitance density of trench capacitors with a trench diameter of 1.2 µm and pitch of 4 µm has increased by a factor of 11 compared with flat capacitors, and the breakdown voltages of the trench capacitors are around 30 V.

Now that the trench capacitor process has been developed, the next part of the work will explore the possibility of integrating the trench capacitors in the complete F2R process flow. Furthermore, the bending of the F2R silicon islands with integrated trench capacitors will be investigated.

4.3. PART II: F2R SUBSTRATE BENDING INTRODUCED BY TRENCH CAPACITORS

4.3.1. DESIGN OF EXPERIMENTS

Substrate deformation is a major risk of introducing trench capacitors in the F2R process. Stress in thin films on a thin substrate potentially can induce a curvature of the substrate, that can cause fabrication or integration issues. The trench capacitors are meant to be integrated into the thin silicon islands of the F2R structures, normally 40 µm thick. Applying the trench etching process removes a certain amount of Si materials, resulting in a less rigid substrate and more sensitivity to thin-film residual stress. After the trench capacitor integration and the trench closing step, other devices are fabricated

on top of the silicon islands, which introduce more thin films on the same silicon island. In the case of an IVUS catheter, the trench capacitors are integrated into the silicon islands where ASICs will be assembled, as shown in Figure 4.4. The fabrication of the CMUT membrane on other wafer areas will also deposit the same silicon nitride layer on the island with trench capacitors, adding extra residual stress. Therefore, the thin silicon island suffers from residual stress of the poly-Si layer from trench capacitor fabrication, the thick PECVD oxide layers, the polyimide layer from the F2R process, and the PECVD silicon nitride layer from the CMUT process. The residual stress of this multi-layer stack can cause a deformation of the thin silicon substrate and may lead to failure of the device. This part of the work evaluated the effect of this multi-layer stack stress.

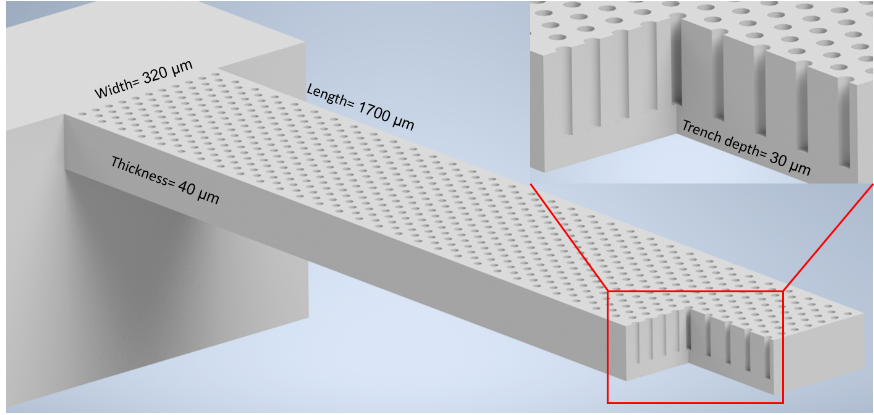

Figure 4.11: 3D design of a cantilever with embedded trench capacitors. The cantilever has a dimension of 320 µm × 1700 µm × 40 µm. The trenches have a depth of 30 µm.

The F2R-based IVUS catheter design was used as a case study. The thin silicon islands onto which the trench capacitors will be integrated have a dimension of 320 µm × 1700 µm × 40 µm. The deformation of the silicon island with embedded trench capacitors was characterized by evaluating a free-standing cantilever, as shown in the 3D design in Figure 4.11. The cantilever has one side attached to the substrate and the rest free-standing. The trench capacitors are integrated into the cantilever, and the dielectric layers of the CMUT and F2R processes are deposited on top. Figure 4.12 shows a schematic cross-section of an F2R silicon island with integrated trench capacitors and the silicon nitride layer of the CMUT process. The cantilever bending was measured with a digital holographic microscopy (DHM). Figure 4.13 depicts the mask layout of the cantilever. The buried trenches from the F2R process define the outline of the cantilever. The diameter of the trenches in the layout varies from 1 µm, 1.1 µm, and 1.2 µm. The pitch of the trenches varies from 2 µm, 3 µm, 4 µm, and 5 µm. The trench counts on each cantilever with different trench pitches are approximately 131000, 58000, 33000, and 21000, respectively. The target depth of the trenches is 30 µm. In these variations, the designs with a trench pitch of 2 µm have the highest trench density, removing the most substrate material. They are expected to result in the most cantilever deflection. Similarly, designs with the largest diameter of 1.2 µm are expected to result in the highest cantilever deflection

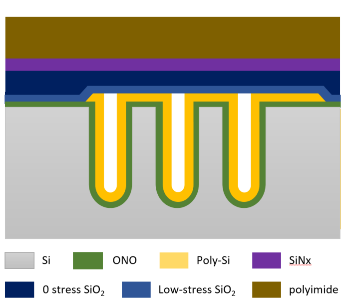

Figure 4.12: A schematic cross-section of an F2R thin silicon island with integrated trench capacitors and dielectric layers from the CMUT.

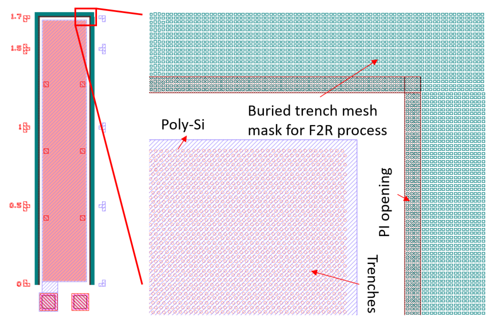

Figure 4.13: The mask layout of the F2R based cantilever with embedded trench capacitors (trench pitch= 2 µm).

for the same pitch.

The second objective of this experiment is to perform a full integration of the trench capacitors in the F2R process. The trench capacitors are fabricated first on the SOI substrate, and then the cantilever is fabricated with the F2R process. This serves to verify that the F2R buried trench process is compatible with pre-fabricated trench capacitors. Especially it will be verified if the 1 µm-thick SiO_2 layer for trench capacitor closing will interfere with the remaining F2R process.

4.3.2. FINITE ELEMENT ANALYSIS (FEA)

Finite element analysis was performed to estimate the bending of the cantilever. To set up a reference case and estimate the simulation accuracy, first, a poly-Si layer on a cantilever without trench capacitors was modeled. The poly-Si layer properties are shown in Table 4.1.

Table 4.1: Layer properties for FEA modeling of cantilever with embedded trench capacitors[12, 13, 14, 15]

Layer name	Thickness	Stress level	Youngs modulus (E)	Poisson's ratio (v)
Si substrate	40 µm	-	169 GPa	0.064
ONO dielectrics*	50 nm	-	-	-
Poly-Si	500 nm	-111 MPa	170 GPa	0.25
Low-stress SiO_2	1 µm	-3.85 MPa	85 GPa	0.2
Low-stress SiO_2	3 µm	-6.4 MPa	85 GPa	0.2
PECVD SiN_x	490 nm	-160 MPa	200 GPa	0.28
Polyimide	3 µm	-1 MPa	8.5 GPa	0.4

Since the film thickness is very small compared to the thickness of the substrate,

and the thin film is in a state of plane stress, with the in-plane stress value direction independent, the Stoney equation to relate the curvature of the cantilever to the stress of the films can be applied. Different versions of the Stoney equation exist for various types of substrates. For elastic isotropic substrates, such as cantilevers in this case, the Stoney equation reads [16]:

$$\sigma_f t_f = \frac{E_s h^2}{6(1 - \upsilon_s R)} \tag{4.7}$$

where σ_f is the in-plane stress component in the film, t_f is the thickness of the film, E_s the Young's modulus of the substrate, υ_s the Poisson's ratio for the substrate, h the thickness of the substrate, and R the radius of curvature of the initial flat substrate after deposition of the film. The curvature of the cantilever, $1/R$, can be expressed as a function of the cantilever deflection, δ, and the cantilever length, L [17, 18]:

$$\frac{1}{R} \approx \frac{2\delta}{L^2} \tag{4.8}$$

Combining Eq. 4.7 and Eq. 4.8, the cantilever deflection δ can be calculated from:

$$\delta = \frac{3(1 - \upsilon_s)L^2}{E_s h^2} \sigma_f t_f \tag{4.9}$$

To determine the modeling accuracy, the simple case of a single thin film on a cantilever without trenches was calculated. The FE model for this case is isotropic linear elastic with a small displacement formulation. In the modeling approach, the substrate is discretized using bilinear hexahedral elements with improved bending and isotropic behavior. The biaxial film stress is applied as an initial stress load case in the model. Comparing the calculation from Eq. 4.9 and simulation results, the deviation of the cantilever deflection FE model result is within 3%.

The final simulation model was constructed based on the cross-section schematic drawing and the 3D design of the F2R cantilever with embedded trench capacitors, as presented in Figure 4.11 and Figure 4.12. The materials and layers involved in the model are silicon substrate, ONO dielectric layer, poly-Si, PECVD oxide layers, PECVD silicon nitride layer, and polyimide layer. The stress of the ONO layer is neglected in the simulation due to its relatively small thickness (around 50 nm). The design and simulation parameters for each layer, including layer thickness, residual stress, Young's Modulus, and Poisson's ratio, are listed in Table 4.1. The cantilever model for trenched capacitor geometry with full layer stack is shown below in Figure 4.14.

Given the dimensions of the Si island and the number of trenches, an FEA model of the full geometry is not feasible. Therefore, the modeling approach was further simplified. The length of the Si cantilever island is half the actual length (850 µm instead of 1700 µm). Since the cantilever length in the model is half the actual length, according to the Stoney equation (Eq. 4.9), the simulated deflection needs to be multiplied by 4 to achieve the actual Si cantilever deflection. As the cantilever width doesn't affect the deflection in the Stoney equation, the width of the trenched Si island is reduced to a narrow representative strip with half the trenches on each side and generalized plane strain

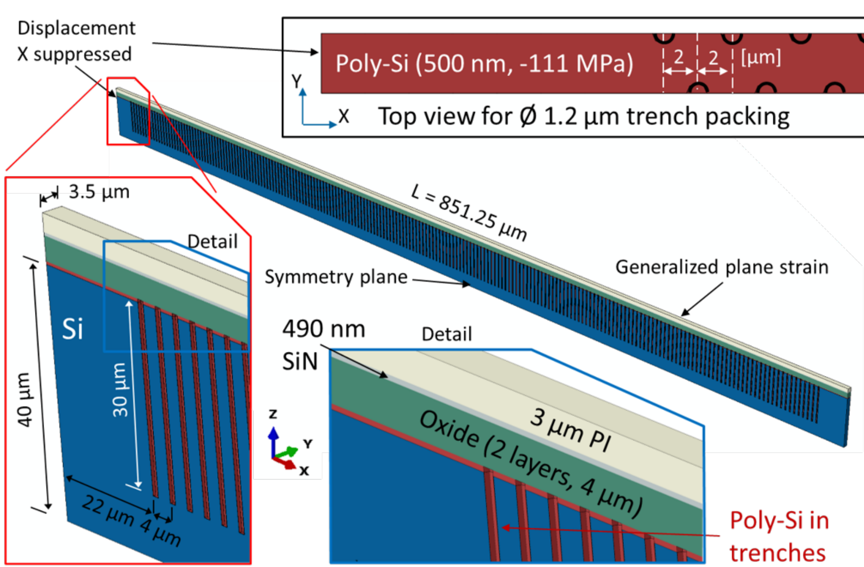

Figure 4.14: FEA modeling of the cantilever with trench capacitors. The model uses half of the actual cantilever length, and a narrow representative strip with half of the trenches on each side for simplification. The poly-Si layer is distributed both inside the trenches and on the cantilever. The two SiO_2 layers, SiN_x layer and polyimide layer are all stacked on the cantilever surface.

boundary conditions. This approach assumes that the model lies between two bounding planes, that may move as rigid bodies with respect to each other, thus causing strain only in the Y-direction. Note that the poly-Si layer in the model is placed both into the trenches and on the cantilever surface. The other layers in the model only cover the cantilever surface. This simplified strip of the cantilever with trench capacitors model can represent the bending of a full cantilever with embedded trench capacitors.

Table 4.2: Cantilever variations for FEA analysis

Variance	Design A	Design B	Design C	Design D	Reference
Trench diameter (in design)	1 μm	1.2 μm	1 μm	1.2 μm	-
Trench diameter (in modeling)*	1.2 μm	1.4 μm	1.2 μm	1.4 μm	-
Trench pitch	2 nm	2 nm	4 nm	4 nm	-

*Note: the modeling takes into account a 0.2 μm trench under etching caused by processing.

The FEA model was used to simulate the four design variations as presented in Table 4.2. A cantilever with no trenches but the same thin-film stack was simulated as a reference to show the effect of introducing the trenches in the cantilever. The modeling results are presented in Figure 4.15. The modeling result shows that the cantilevers, with a length of 1700 μm, only bend less than 10 μm. All bow values are directed downward,

indicating that the multi-layer stack in total has a compressive stress. A smaller trench pitch and larger trench diameter give larger cantilever bow values. This trend is in-line with our hypothesis: more silicon etched makes the cantilever less rigid and more sensitive to thin-film stress.

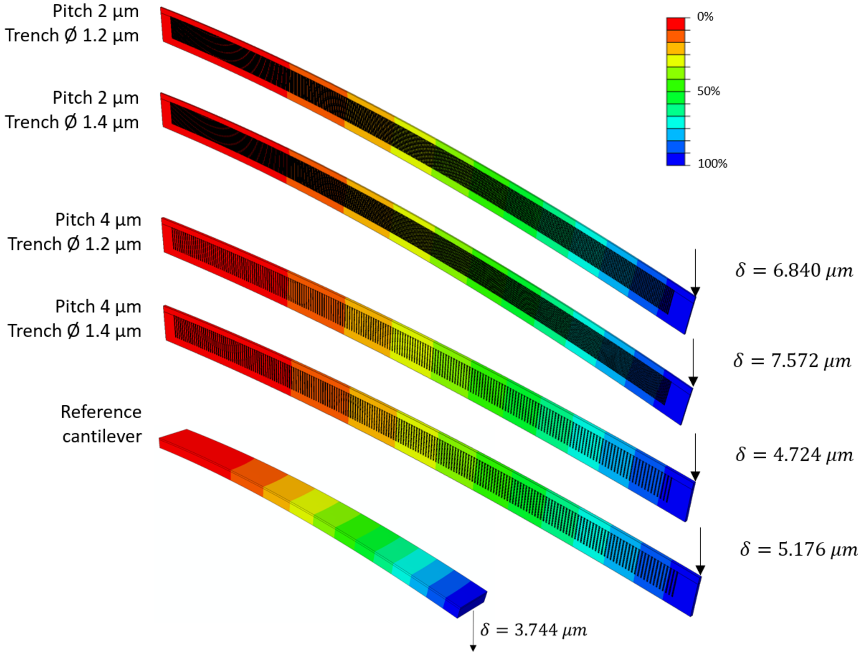

Figure 4.15: FEA modeling result of cantilevers with embedded trench capacitors. The trench diameters are 1.2 µm and 1.4 µm (corresponds to 1 µm and 1.2 µm in the design), and the trench pitches are 2 µm and 4 µm. A flat cantilever (no trenches) with same layer stacks was used as a reference. The simulated deflection δ has been processed to represent cantilevers with full length.

4.3.3. FABRICATION AND RESULTS

In the fabrication of the free-standing cantilever with embedded trench capacitors, the previously developed trench capacitor process was combined with the standard F2R process flow, with a few adjustments for the overall integration. The complete process flow is presented in Figure 4.16. The process started with 6-inch SOI wafers with a device layer of 40 µm, a BOX layer of 1 µm, and a handle layer of 380 µm. Figure 4.16a shows the HAR trench etching and ONO layer deposition process, identical to the trench capacitor process presented previously. An under-etch of 200 nm was introduced to the trench diameters while performing the HAR trench etch process, resulting in trenches with a diameter of 1.2 µm, 1.3 µm, and 1.4 µm, respectively. The trench depths for the different trench diameters are all around 30 µm. The LPCVD ONO deposition resulted in a layer thickness of 4.8 nm silicon dioxide, 14.1 nm silicon nitride, and 28.9 nm silicon dioxide, as measured on monitor wafers after each deposition. The deposition of poly-Si

was different from the previous process. Instead of depositing poly-Si and doping it with PSG, we performed an in-situ doped poly-Si deposition and annealed it at 900 degrees. The poly-Si layer had a thickness of 490 nm and resistivity of 1.73 mohm·cm. The poly-Si layer was patterned in the same way as the previous run, etching through the ONO layer and landing on the device layer of the SOI substrate as shown in Figure 4.16b. Although the landing recipe was carefully optimized, around 100 nm was over etched into the device layer. The trench capacitor process ends with a PECVD low-stress oxide deposition, which closes the trench openings and is also the starting oxide mask layer for the F2R process (Figure 4.16c).

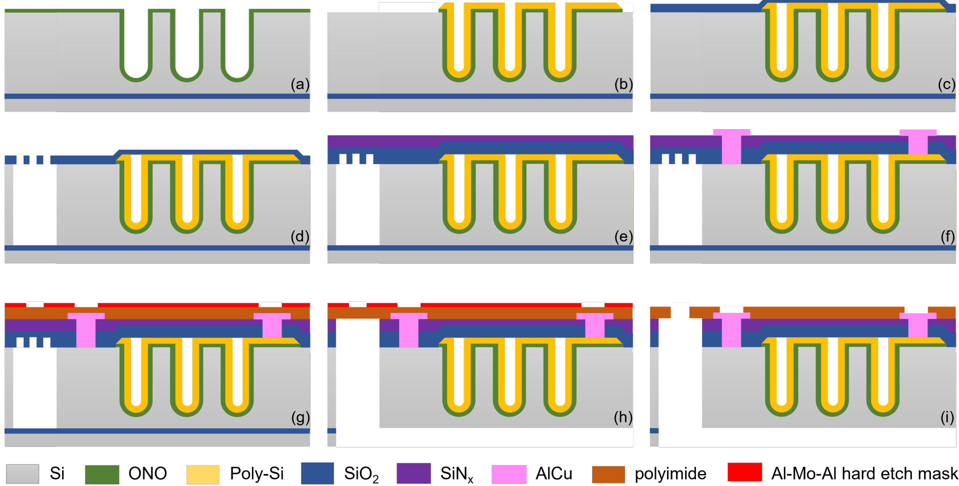

Figure 4.16: Complete process flow for F2R based cantilever with embedded trench capacitors. The layer thicknesses are not drawn to scale. The process is performed on an SOI wafer, mainly on the 40 µm-thick device layer. The "thin" silicon layer underneath the BOX in the drawing is actually the 380 µm-thick handle layer.

Instead of using 700 nm PECVD oxide as in the standard F2R process, a 1-µm thick low-stress PECVD oxide was used to close the trench capacitors completely. Although deviating slightly from the standard F2R process, the low-stress oxide layer was successfully patterned into a mesh mask, followed by the DRIE process developed for the buried trench process (Figure 4.16d). After the resist and passivation material stripping with oxygen plasma, the buried trenches were closed by depositing a 3-µm thick PECVD oxide layer. The wafer surface was flat and intact again after the buried trench closing process. The dummy PECVD silicon nitride layer, used to mimic the CMUT transducer membrane, was deposited with a thickness of 490 nm and stress of -160 MPa (Figure 4.16e). Contact vias were etched through the thick oxide layer, landing on the substrate and poly-Si. After a short etch in 1% HF to remove the native oxide on the silicon and poly-Si surfaces, a 1 µm-thick AlCu layer was deposited and patterned to form ohmic contacts for the two electrodes of the trench capacitors (Figure 4.16f). As the flexible layer in the F2R process, a 3 µm-thick polyimide layer was coated, followed by sputtering of a 200 nm-thick AlCu-Mo-AlCu stack-layer hard etch mask. The hard etch mask was further patterned by wet etching (Figure 4.16g). The release of the cantilevers was realized by

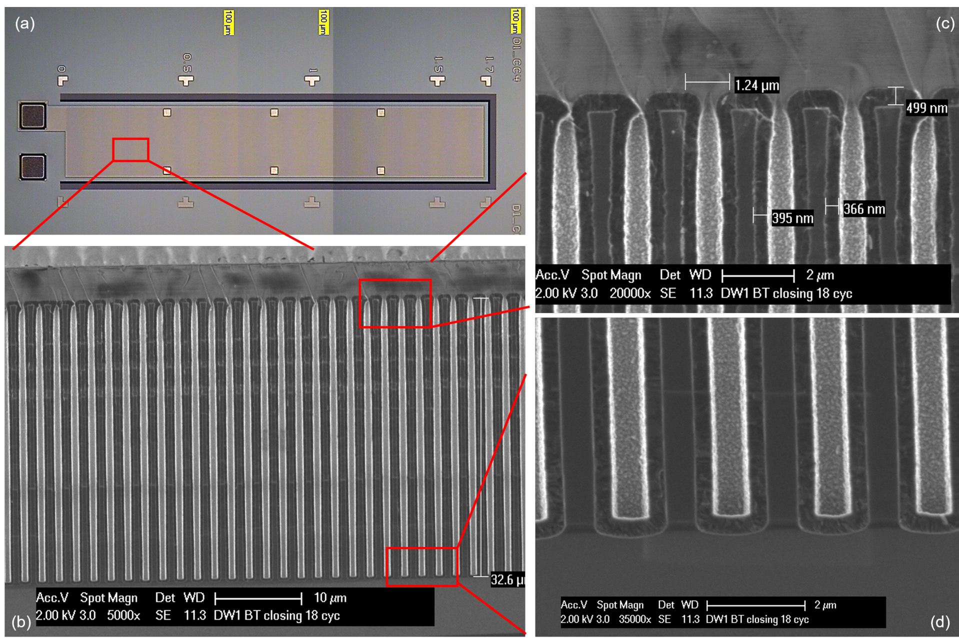

Figure 4.17: Fabrication result of the F2R cantilever with embedded trench capaictors. (a) Optical microscope image of the cantilever; (b) SEM cross section image of the trenches in the cantilevers. The trench pitch is 2 µm, trench diameter is 1.2 µm and the trench depth is 32 µm. (c) Top part of trenches in the SEM cross section image; (d) bottom part of trenches in the SEM cross section.

a backside DRIE process. A 6 µm-thick photoresist was used as the etch mask and the DRIE etched landing the BOX layer. After removing the BOX layer, the thick oxide layer underneath the polyimide was removed with a high-pressure dry etch from the backside (Figure 4.16h). Finally, the polyimide was patterned with a dry etch using the AlCu-Mo-AlCu stack as a hard etch mask (Figure 4.16i). At the same time, the contact pads were opened, and the cantilevers were released from the polyimide sheet. Figure 4.17 depicts the fabrication results of the free-standing cantilevers with embedded trench capacitors.

4.3.4. ELECTRICAL CHARACTERIZATION

The electrical characterization of the cantilevers with trench capacitors was performed with the KEITHLEY 4200-SCS semiconductor characterization system. The CV measurements were carried out at a frequency of 10 kHz with zero bias voltage and represented as capacitance density (nF/mm^2), calculated based on the cantilever dimension of 320 µm × 1700 µm (0.54 mm^2). Seventy cantilevers over the wafer with different trench pitches and diameters were characterized, categorized, and summarized in the bar plot Figure 4.18. The flat capacitor was used as a reference. For comparison, Figure 4.18 also includes the trench capacitors fabricated on the planar wafers, which have a trench pitch of 4 µm. The CV measurement results show two major trends. First, the capacitance density increases significantly as the trench pitch decreases. Secondly, for the same trench

pitch, the capacitance density increases as the trench diameter increases. Both trends are in agreement with the initial hypothesis that larger trench numbers and larger trench diameter result in a larger final capacitance density. However, compared to the trench capacitors made in the first part of this chapter, the capacitance density of the flat capacitors is similar, but the capacitance density of trench capacitors differs considerably. This difference very likely originates from the nonuniform dielectric deposition inside the trenches and will be discussed in the next section.

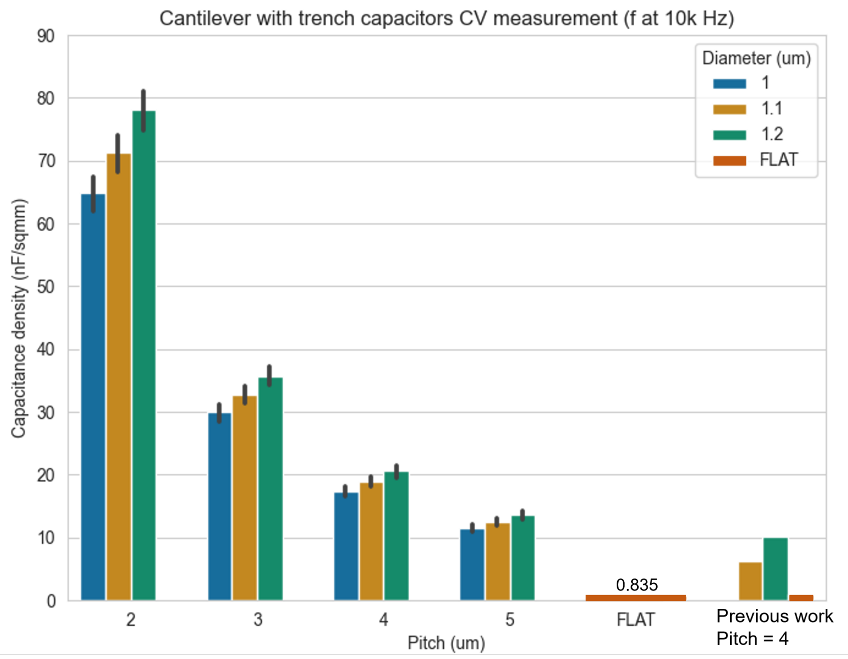

Figure 4.18: Capacitance measurement (frequency 10kHz) of cantilevers with trench capacitors, with varying diameter and pitch. 70 devices across the wafer were measured. Standard deviation (STD) is presented. The previous work, with pitch of 4 μm fabricated on the planar wafer, is listed as a comparison.

IV characteristics were measured to determine the breakdown voltage of the capacitors on the cantilevers. A DC voltage was applied to the two electrodes of the capacitors, sweeping linearly from 0 V to 50 V with a current limit of 0.1 mA. Large non-uniformity was observed across the wafer. Most devices from the wafer center had a breakdown voltage below 5 V. These devices were excluded from this analysis. Forty-nine devices from the wafer edge with different trench pitches and diameters were characterized and plotted in Figure 4.19. The bottom figure shows the breakdown voltage of all measured devices, and the upper figure shows the histogram of all the breakdown voltage distributions. The figure shows that the breakdown voltage of the reference flat capacitors varied between 25.7 V to 31.7 V. For the trench capacitors, the histogram shows two main groups. A group with a lower breakdown voltage ranging from 23.2 V to 25 V, and a group with a higher breakdown voltage ranging from 26.7 V to 29 V. The group with the lower

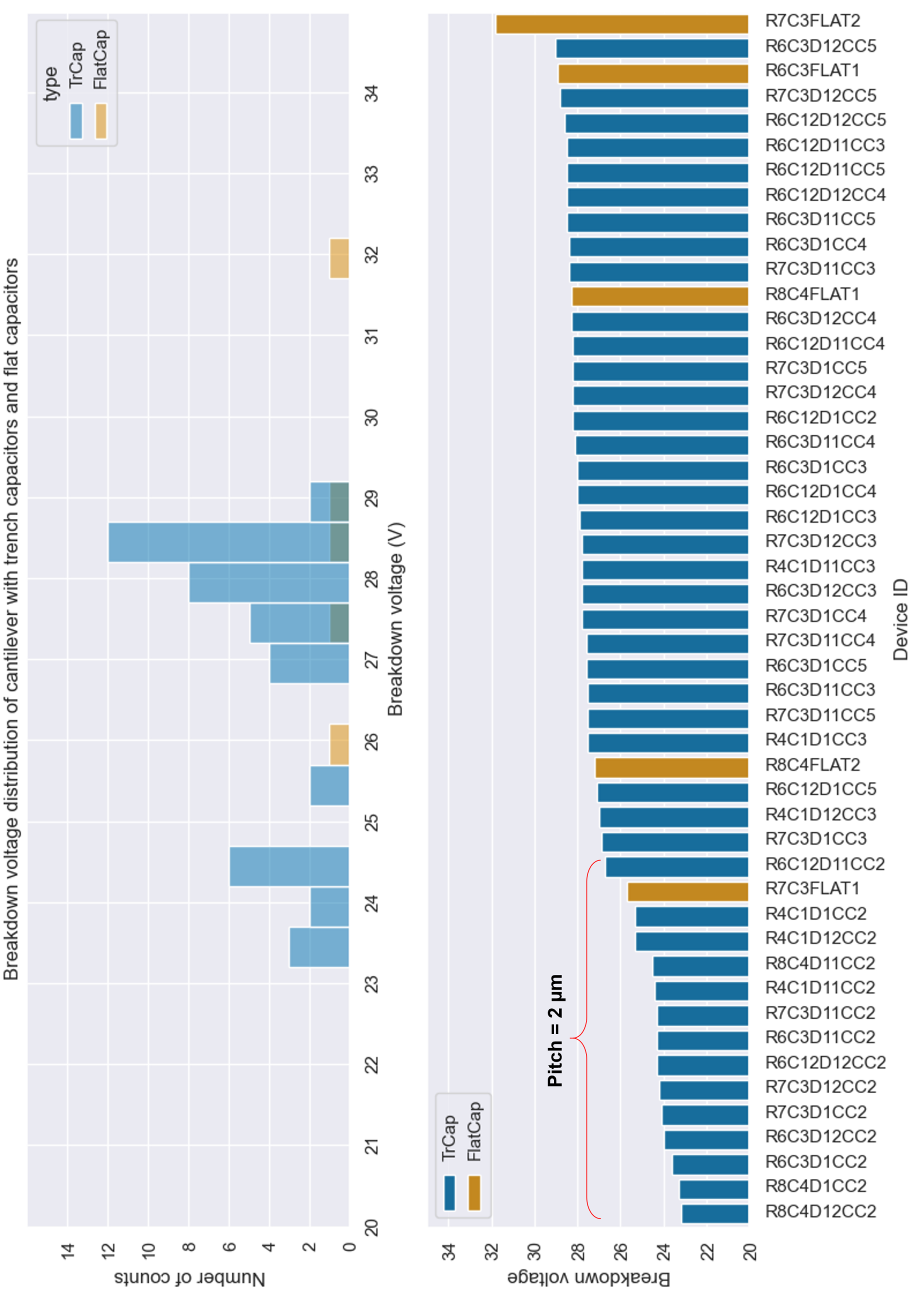

Figure 4.19: Breakdown voltage of trench capacitors embedded in cantilevers. 49 devices including both trench capacitors and flat capacitors were measured.

breakdown voltage mainly consists of capacitors with a trench pitch of 2 µm, while the other group consists of capacitors with the other trench pitches. It seems that the defects introduced during processing have more impact on capacitors with a trench pitch of 2 µm because of the large number of trenches. The breakdown voltages of the other characterized capacitors don't show a clear relationship to their trench pitches. More detailed discussion regarding the breakdown voltage will follow later in Section 4.3.6.

4.3.5. Stress characterization

After fabrication, a Lyncee Tec reflective digital holographic microscope (DHM) R2100 with dual-wavelengths (λ_1= 682.5 nm, λ_2= 758.5 nm) was used to characterize the bending of the cantilevers. DHM is a fast and non-contact profilometric metrology with nanometer-scale resolution. It is widely applied to characterize out-of-plane geometries, especially for MEMS applications with cantilevers and membranes [19]. The employed DHM has a vertical resolution of 0.3/6 nm (with/ without single wavelength mapping) and a maximum field view of 1.2 mm × 1.2 mm [20].

The DHM measurement requires the inspected object to be a continuous structure. A surface step height larger than 0.5λ caused by surface roughness, defects, or design leads to phase discontinuities and results in nonreliable results. As the maximum field view of the DHM cannot cover the entire cantilever, the measurement was performed twice along the cantilever, using the square fiducial markers on the cantilevers as separation. The two measurement data sets were processed with Python and merged to represent the full cantilever bending status. Eighteen silicon cantilevers, with no trenches nor layers on top, were measured to determine the initial bending. The bending depth varied from -403 nm to +217 nm, almost negligible for a cantilever with a length of 1700 µm. Cantilevers with various trench pitches and diameters from different dies over the entire wafer were characterized. Cantilevers with no trenches but the same poly-Si, dielectric, and polyimide layer stack on top, were used as references. Figure 4.20 depicts the DHM cantilever bending results measured in a die on the wafer.

Figure 4.20 shows a distinctive relationship between the bending depth versus the trench pitch and diameter. Consistent with the initial theory that more trenches result in less rigid cantilevers, the smaller trench pitch results in more cantilever bending. In each trench pitch group, for larger trench diameters, less cantilever bending was observed, which contradicts the initial rigidity theory and the simulation results. In the next section, hypotheses that can explain this contradiction between the simulation and fabrication results will be discussed. The largest bending depth, -4 µm, is for the cantilever with a trench pitch of 2 µm and a trench diameter of 1 µm. This bending depth is only 0.23% of the full cantilever length, and therefore has minor effects on its entire physical geometry. This means that introducing the trench capacitors in the thin silicon substrate with the same dimension as in the IVUS catheter will hardly cause any bending, allowing further assembly steps. However, the rigidity of the substrate will be decreased, and the effect on the assembly, application and lifetime of the trench capacitor needs to be further studied. The three measured dies in the left, middle, and lower parts of the wafer have their cantilever bending depth deviating within 10%, showing good repeatability. The relationship between the bending depth versus the trench pitch and diameter is consistent over the three measured dies.

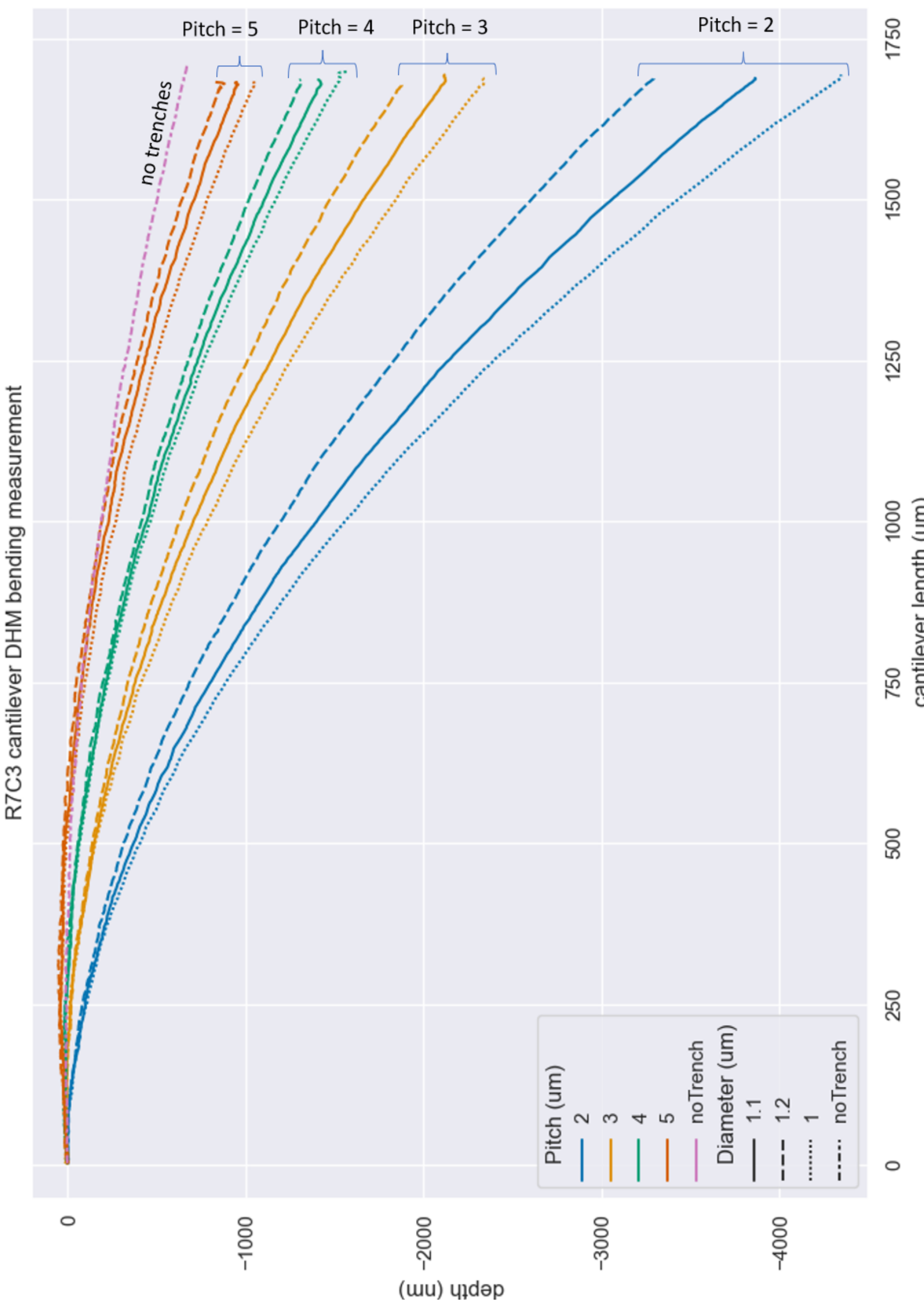

Figure 4.20: DHM cantilever bending measurement on die R7C3. Bending of cantilevers with different trench pitches trench diameters are plotted.

4.3.6. DISCUSSION

HIGHER CAPACITANCE DENSITY

Figure 4.18 shows the capacitance density measurements for cantilevers with different trench pitches and diameters. Compared to the trench capacitors fabricated on the planar wafer, which have similar trench dimensions and trench structures with a pitch of 4 µm, the capacitance density of the trench capacitors in the cantilever batch doubled. However, the capacitance densities of the flat capacitors in both batches remained the same. It suggests the hypothesis that the dielectric layers inside the trenches of the cantilever batch might be thinner than targeted (5,15, 30 nm).

SEM cross-sections of the cantilevers with trench capacitors were prepared to verify the ONO layer thickness. The prepared samples were dipped shortly in 4% HF to delineate the oxide layers in the ONO stack to create better contrast for the SEM inspection. Figure 4.21a shows an SEM cross-section of a flat capacitor, indicating ONO layer thicknesses of 5.8, 17.6, 29.4 nm, which is comparable with the requested thickness. Figure 4.21b is a cross-section at the bottom corner of a trench capacitor. Although the nanometer scale is difficult to observe accurately, the ONO thickness of 5.4, 10.8, 12 nm can be roughly estimated, which is almost half the targeted thickness. This confirms the hypothesis as the half-thick dielectric layer leads to a doubled capacitance density.

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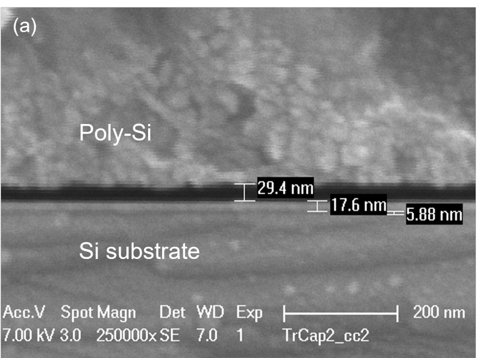

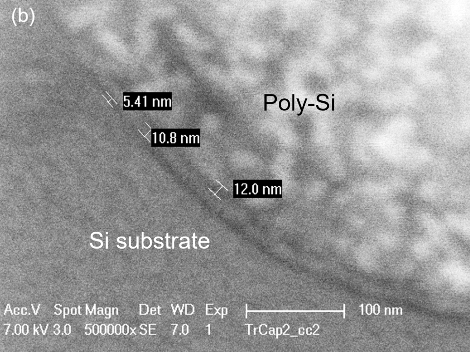

Figure 4.21: SEM cross-section images to observe ONO layer thickness. (a) Cross-section of a flat capacitor, ONO thickness 5.88, 17.6, 29.4 nm. (b) Cross-section at the bottom corner of a trench capacitor, ONO thickness 5.41, 10.8, 12 nm.

Although the same ONO deposition recipe was applied in both batches, only the second batch shows a thinner dielectric layer stack inside the trench. This nonconformity might result from machine deviation, as the two batches have a two-year gap in between. It might also be caused by the different designs of the two batches. The cantilever design has much higher number of trenches than the flat design, meaning more deposition surface for LPCVD deposition. As a result, the same deposition recipe may result in thinner layers on the cantilever design. Therefore, the ONO deposition process needs to be further developed.

FABRICATION NONUNIFORMITY AND INCONSISTENCY

Figure 4.18 shows a uniform capacitance density measured over 70 devices across the wafer. However, the IV measurement showed large non-uniformity between dies in the wafer center and on the wafer edge. Dies in the wafer center (over 60% of the entire wafer) have a low breakdown voltage, most of them less than 5 V. Only the dies on the wafer edge have breakdown voltages in the expected range as shown in Figure 4.19. The uniform capacitance density indicates that the dielectric stack layer is reasonably uniform across the wafer. Therefore, the low breakdown voltage (less than 5 V) most likely originates from fabrication defects. The breakdown voltage distribution matches the nonuniform dry etching profile, which can cause process deviations because of the different etch rates between the center and edge of the wafer. The dry etching process for trench etching was delicately tuned for a high aspect ratio profile and, therefore, very sensitive to machine conditions. Any small changes in the etching gas supply, chamber pressure, or bias voltage can significantly affect the etching result. During the trench etching process, sharp corners or trench profiles result in a lower breakdown voltage. The large number of trenches in a single trench capacitor requires high stability of the dry etching process. When one out of these tens of thousands of trenches fails, a breakdown will occur for the trench capacitor. The delicate, fine-tuned dry etching process has caused the inconsistency of the trench etching results between the work of Part I and Part II. The etch rate, etch depth, etch profile, and the under-etch all have minor differences in the two batches.

4

CANTILEVER BENDING SIMULATION VERSUS MEASUREMENT RESULTS

The first mismatch between the simulation and the measurement results is the overall large difference in the bending depth. The reference cantilevers, for example, are solid silicon cantilevers (without any trenches) that have the same layer stack on top, including poly-Si, dielectric, and polyimide layers. The simulated bending for the reference cantilever is 3.7 µm, whereas the DHM measured reference cantilever bending is only 690 nm. This large difference may be caused by using inaccurate Young's modulus or Poisson's ratio values in the modeling. As the layer stress values used for the stack layer modeling are acquired differently from the real case because the corresponding substrate material is silicon for each measured layer stress value. In the real stack layer case, however, the substrate material changes while the stack layer builds up. So the real layer stress in the stack layer would be very different from those measured in the individual dummy Si wafers. Better metrologies to acquire the real layer stress in the stack layer need to be developed to achieve more accurate modeling.

In the finite element analysis section, the bending depth of the cantilevers with different pitches and diameters was modeled and simulated. The trend that the smaller trench pitch and larger trench diameter result in a larger cantilever bending depth is confirmed. However, a larger trench diameter results in less bending. A few details that were not considered during the simulation can contribute to this mismatch. In the first place, the poly-Si thickness is not uniform. The poly-Si thickness inside the trenches is 400 nm, and on the wafer surface 500 nm. Moreover, the poly-Si grain structure inside the trench wall is unknown, and its effect on the cantilever bending is unpredictable. Secondly, the coverage of the poly-Si on the entrance corner of the trenches, as pointed out in Figure 4.22a, is not included in the simulations. The simulation model did not

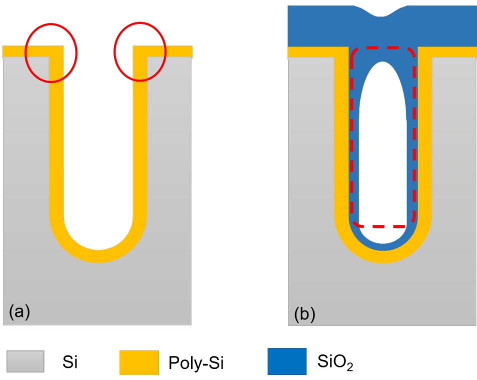

Figure 4.22: Nonideal structures cause mismatch between simulation and fabrication results. (a) poly-Si layer on the entrance corner of the trenches; (b) PECVD oxide deposited inside the trenches while closing the trenches.

consider it as a continuous layer at the entrance corner. It can affect the cantilever bending significantly, as there are tens of thousands of trenches on a cantilever. Finally, a thin PECVD oxide layer is deposited inside the trenches during the trench closing process, as shown in Figure 4.22b. This thin oxide layer in all trenches can make a difference in the cantilever bending. In summary, the FEA model couldn't fully represent all the details in the fabricated device and, therefore, partially matched the final result.

4.4. CONCLUSION

This chapter discussed the development of integrating decoupling trench capacitors into the F2R platform. In Part I, the trench capacitor process was developed and the trench closing possibilities were explored. 1.1 µm and 1.2 µm diameter trench capacitors with a pitch of 4 µm and a high-aspect-ratio (around 1:30) were realised. The capacitance density of trench capacitors increased by a factor of 11 compared to flat capacitors, and breakdown voltages of the trench capacitors are around 30 V.

In Part II, the trench capacitor compatibility with the F2R process was verified. With a minor change of closing oxide thickness from 700 nm to 1 µm, both the trench capacitor closing and the F2R buried trench process are successful and compatible. Furthermore, the substrate deformation caused by the integration of high-density trench capacitors was studied. Trench capacitors with a trench pitch of 2, 3, 4, and 5 µm and a trench diameter of 1.0, 1.1, and 1.2 µm were integrated into F2R-based cantilevers. Apart from the integrated trench capacitors, the same silicon nitride layer that is used for the CMUT transducer membrane was deposited on the cantilevers to verify the process compatibility of integrating both trench capacitors and CMUT transducers. The capacitance densities of these trench capacitors was significantly higher compared to the trench capacitors in Part I, which is most likely caused by thinner dielectric layer deposited inside the trenches. Large non-uniformity was observed across the wafer during IV measurement. Breakdown voltages of functional trench capacitors range from 23.2 to 29 V.

Finite element analysis was performed to estimate the cantilever bending depth and

its relationship to the trench pitches & diameters. The DHM cantilever bending measurements showed that the cantilever with a trench pitch of 2 μm and a trench diameter of 1 μm resulted in the largest bending of -4 μm. The measurement results match the simulation results in as far as that a smaller trench pitch results in a larger cantilever bending. The mismatch between the simulation and the fabrication results regarding the relationship between trench diameter and the bending depth can possibly be explained from fabrication nonidealities. This minor deformation allows for more device integration on the F2R thin silicon substrate and further assembly steps.

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5

Cavity BOX SOI

Parts of this chapter have been published in [1]

5.1. INTRODUCTION

5.1.1. SOI/CAVITY-SOI WAFER AND APPLICATION

SOI substrates were originally developed to enable perfect dielectric isolation in electronic devices. Nowadays, SOI wafers also have become an important substrate for the fabrication of MEMS devices. SOI wafers consist of a handle wafer that provides mechanical strength during the fabrication process, a device layer in/onto which the devices are fabricated, and a buried oxide (BOX) layer that separates the device layer from the handle wafer (see Figure 5.1a). Apart from electrical isolation, the BOX layer also allows for the fabrication of MEMS devices with a well-defined device layer thickness, and it can serve as a release layer in floating structures. SOI wafers are used in a wide range of applications, such as pressure sensors[2], resonators and inertial sensors[3], microchannels[4], and the miniaturization of microfabricated medical devices[5, 6].

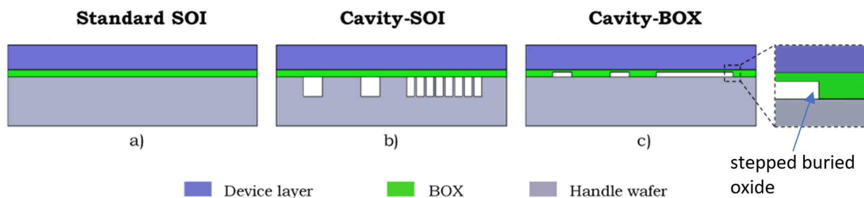

Figure 5.1: A comparison of three substrate architectures: (a) Standard SOI substrate; (b) Cavity-SOI substrate with cavities in the handle wafer; (c) Cavity-BOX substrate with the pre-patterned buried oxide layer.

Cavity-SOI substrates have been derived from the silicon-on-insulator family [7]. They are customized SOI substrates, whereby the manufacturer of the SOI substrates has integrated customer-defined buried cavities in the silicon handle wafer (see Figure 5.1b). It has been demonstrated that customized SOI substrates with pre-fabricated cavities can significantly simplify the fabrication process of complicated MEMS devices, such as pressure or inertial sensors[3, 8, 9, 10, 11]. Cavity-SOI substratse allow for eliminating the cumbersome step of etching cavities in the handle layer later in the process flow, and it permits for pre-patterning of complex cavity systems. However, the range of the cavity dimensions in cavity-SOI wafers is limited. On the one hand, very large cavities that are not supported with pillars make the wafer fragile which can lead to wafer or device layer deformation. On the other hand, very small buried structures are problematic, due to the limited alignment precision of the pre-fabricated cavities with the structures fabricated later on the device layer.

Cavity-BOX are advanced substrates with custom-defined cavities etched in the buried oxide (see Figure 5.1c). They are the newest member of the SOI substrate family. Their exemplar development, preparation process, and application are presented in this chapter. The cavities can be formed by etching through the entire thickness of the BOX or by partially etching the BOX to create a stepped-buried oxide hard-etch mask. In cavity-BOX substrates, only the thin layer of buried silicon oxide is patterned, enabling almost unlimited design freedom for the cavities without weakening the mechanical properties of the wafer. The high-precision alignment (< 500 nm) of the pre-fabricated cavities with the structures fabricated later on the device layer is ensured by applying a newly developed marker transfer strategy. The method uses a set of primary alignment markers

located on the SOI wafer terrace that are transferred onto the device layer using front-to-front alignment[12]. The patterned BOX can serve as an etch-stop layer during the device layer thinning, and it can be used as a hard mask during the device layer patterning from the backside. The high resolution of the deep reactive-ion etching (DRIE) process is maintained by bringing the hard mask, formed by the patterned BOX layer, directly to the device layer. This allows for a precise definition of micron-sized cavities in the device layer from the backside and simultaneously enables the patterning of centimeter-sized structures in the device layer.

5.1.2. Scope of this chapter

This section presents the cavity-BOX substrates and illustrates how such a substrate can facilitate the fabrication of various MEMS devices. For the cavity-BOX SOI, the key is the customized pre-patterned BOX layer in the SOI wafer, which needs to be implemented by the SOI supplier during the SOI manufacturing process. Therefore, the cavity-BOX SOI was developed together with SOI wafer manufacturer Okmetic Oy from Finland in the context of the ECSEL European project POSITION- II [1].

5

The development of the cavity-BOX SOI in this work is split into two phases, corresponding to two demonstrators. To prove the validity of the cavity-BOX SOI concept, the first phase used the design of a deep brain stimulation (DBS) probe developed with another Ph.D. Marta Kluba, since the DBS probe design has larger dimensions and is less critical. The first phase focused on process challenges such as the device layer bonding process with patterned oxide, alignment accuracy between cavity-BOX and patterns on the device layer, and the DRIE process using cavity-BOX as an etching mask. To avoid the lithographic compatibility issue that might be caused by the different exposure tools in the two fabs, the batch in the first phase was shipped back and forward between Philips and Okmetic after each step. The lithography steps were all performed in Philips, and Okmetic did the SOI manufacturing processes. The first phase also used the marker transfer technology developed by Mountain et al.[12], which ensured the alignment accuracy between the patterns on the device layer and the patterned cavity-BOX.

The goal of the second phase was to implement the entire cavity-BOX SOI manufacturing at the site of the SOI supplier. The second phase used an IVUS probe design, which has smaller dimensions and, therefore, is more challenging in process and alignment. By avoiding the back and forth shipping of wafers between the fabs, the cavity-BOX SOI will be suitable for mass production. The biggest challenge in the second phase was to align the different exposure tools, Ultratech AP200 (in Okmetic) and ASML PAS5500 (in Philips), from the two fabs. Such cross-platform machine-to-machine overlay matching is challenging as different lithography systems use different metrology and, therefore can result in overlay issues.

5.2. First Phase: Proof of Concept

5.2.1. State-of-art DBS Probe Process and Design

Cavity-BOX SOI can significantly simplify processes, such as the microfabrication of highly integrated foldable devices[5, 6] or 3-dimensional circuit integration using TSVs,

[1] grant no: Ecsel-783132-Position-II-2017-IA

in the device layer[13]. An example of a cavity-BOX application is a monolithic fabrication process for a foldable deep brain stimulation (DBS) device (see Figure 5.2[6]), which is developed in collaboration with another Ph.D. from TU Delft, Marta Kluba.

Initially, standard SOI substrates and F2R technology were employed to accomplish the monolithic fabrication of a device where small 80 μm-thick silicon islands, separated by 40 μm-wide trenches, coexist with a millimeter-sized flexible area etched from the backside of the wafer [6, 14]. Due to the resolution limitations of the backside through-wafer DRIE process, the precise separation of the small (210 μm × 2070 μm) silicon islands on the front side cannot be achieved. Therefore, HAR trenches were etched in the device layer from the front side of the wafer to separate the silicon islands and, subsequently, sealed with a silicon dioxide membrane (Figure 5.2a) to enable further wafer processing (Figure 5.2b). However, the trench etching and sealing processes require precise optimization and have very tight process windows. Moreover, breaking of the fragile SiO_2 membranes can severely hamper the follow-up processes. Employing cavity-BOX substrates with a patterned buried oxide layer(Figure 5.2e) allows for a more robust process because it leaves the entire device layer intact until the very end of the front side processing (Figure 5.2f,g). All the structures are released by DRIE etching from the backside using the cavity-BOX as a hard mask at the end of the processing.

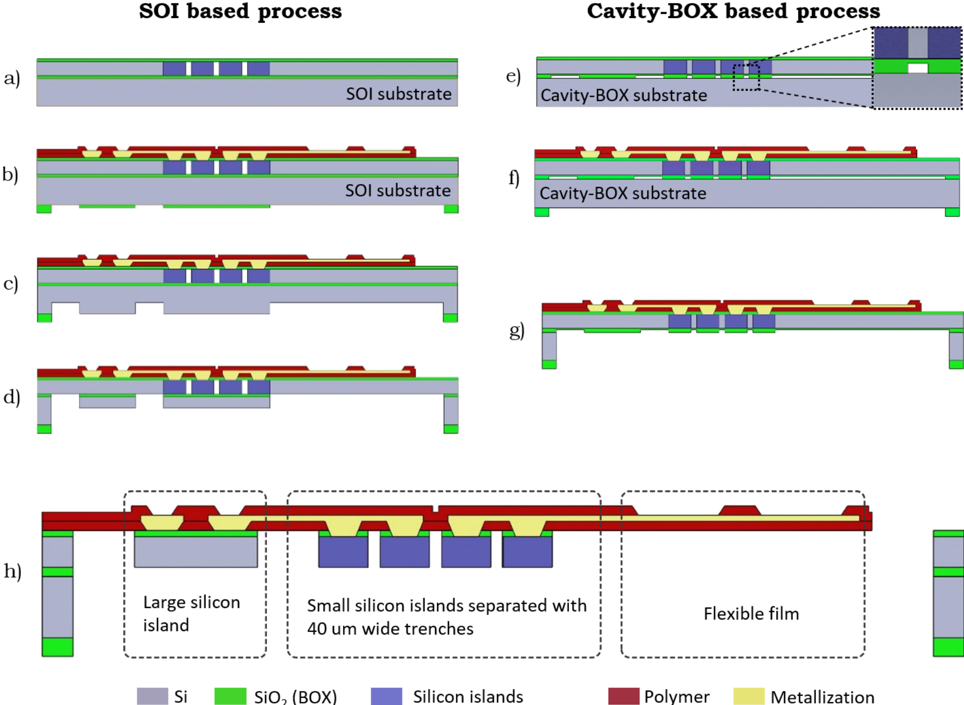

Figure 5.2: Simplified manufacturing process flow of the semi-flexible DBS device using the trench-based F2R technology versus the cavity-BOX substrate. Left (a–d): The SOI-based process with sealed trenches on the front side of the wafer and a two-step backside etch process. Right (e–g): The cavity-BOX-based process using patterned BOX as an etch-stop layer and hard-etch mask. Bottom (h): Finished device.

After the front side processing is finished, DRIE etching is used from the backside of the wafer for thinning down and releasing the flexible structures. In the standard SOI-based F2R process, this is realized by multiple steps of alternating silicon dioxide etch and silicon etch through a two-step hard-etch mask located on the backside of the handle wafer (Figure 5.2c,d,h). The buried oxide layer of the standard SOI wafer serves as an etch stop layer that defines the device thickness. This approach is cumbersome and heavily relies on the uniformity of each dry etching step. In contrast, the cavity-BOX can significantly simplify the process by reducing the processing sequence to just three steps. First, the device is thinned down to 80 µm using a simple hard-etch mask patterned on the backside of the handle wafer and using the BOX as an etch stop layer that balances the DRIE nonuniformity of the handle wafer etching (Figure 5.2g). Secondly, the exposed cavity-BOX with a step mask is thinned down to form the hard-etch mask. Finally, the hard-mask embedded in the BOX is used to separate the 80 µm-thick silicon islands with the 40 µm-wide trenches and simultaneously release the flexible film in the final DRIE step (Figure 5.2h). The high resolution of the DRIE process and coexistence of the structures with a wide range of dimensions is ensured by bringing the hard mask–patterned BOX directly to the device layer rather than optimizing the through-silicon DRIE process to its extreme to etch through the complete handle wafer.

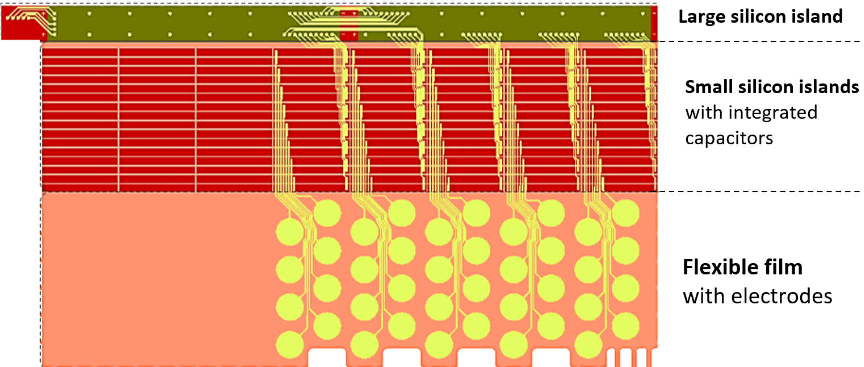

Figure 5.3: Mask design of the 40-electrode DBS prob with integrated electronic components. The large silicon island (18 mm × 1 mm) can contain flip-chipped ASICs. The small silicon islands (210 µm × 2070 µm) are separated with 40 µm wide trenches and can accommodate pre-fabricated decoupling capacitors. The flexible film contains 40 flexible electrodes.

The application of the cavity-BOX substrate is demonstrated using a simplified fabrication process of the 18 mm long Deep Brain Stimulation (DBS) probe. The mask design is presented in Figure 5.3. The highly integrated DBS tip was designed to accommodate 40 circular electrodes on a semi-film substrate. The small silicon islands in the final DBS probe will contain pre-fabricated decoupling capacitors, while the large silicon island permits for wire bonding and back-end integration of application-specific integrated circuits (ASICs) inside the probe. All the structures are connected with flexible interconnects. This enables the activation of each electrode individually, using only a small number of power and signal wires reaching out of the probe. As a result of the semi-flexible structure, the device can be folded and rolled to a 1.4 mm diameter cylin-

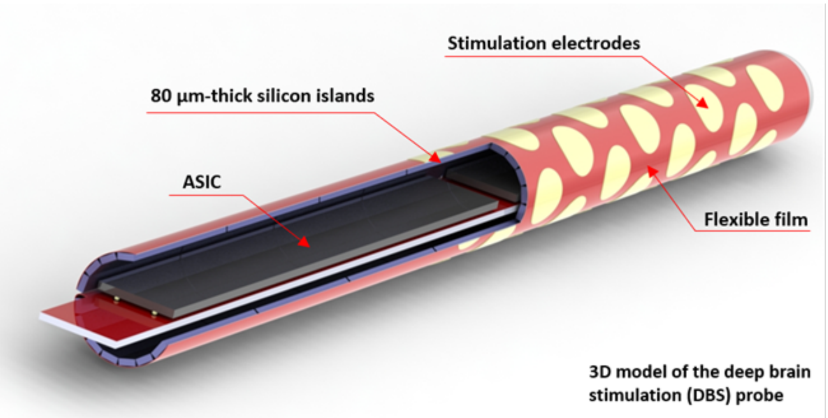

Figure 5.4: 3D model of the 40-electrode DBS probe (ø 1.4 mm diameter) with integrated capacitors and ASICs inside the probe's tip.

der (Figure 5.4).

5.2.2. FABRICATION WITH CAVITY-BOX SOI

The fabrication of the DBS demonstrator can be separated into two parts: the cavity-BOX SOI substrate preparation and the DBS demonstrator fabrication. The main technical challenge arises from the fact that a submicron (less than 1 µm) alignment accuracy between the buried cavity-BOX mask and the structures on top of the device layer must be guaranteed. The second goal of the demonstrator was to demonstrate the functionality of the embedded BOX mask.

CAVITY-BOX PREPARATION

A schematic process flow of the cavity-BOX substrate preparation is presented in Figure 5.5. A 380 µm-thick 6-inch double-side polished (DSP) handle wafer was used as starting material. First, two 140 nm deep ASML markers were etched into the silicon substrate, at 1.2 mm distance from the left and right edge of the wafer. These alignment markers are referred to as "terrace markers". Next, 1 µm of thermal SiO_2 layer for wafer bonding was grown on both sides of the wafer. The customized cavity-BOX pattern was aligned to the terrace markers, and dry etched into the SiO_2 layer, landing on the silicon (Figure 5.5a). The handle wafer was subsequently fusion bonded to the device layer, which also was provided with a 500 nm-thick layer of thermal oxide. The fusion bonding was carried out under a vacuum at room temperature. The two oxide layers were bonded and merged into the cavity-BOX, forming the pre-patterned step oxide mask (Figure 5.5b). This step oxide mask was used as an etch-stop layer during the subsequent process. Finally, the device layer was thinned down to 80 µm, and a terrace with a width of 4 mm was created by a combination of edge trimming and wet etching (Figure 5.5c). The terrace markers on the handle wafer were revealed during this process.

The 4 mm terrace width was chosen to keep the edge of the device layer as far as possible from the alignment markers on the handle wafer in case of any possible optical

interference during the marker transfer processes. The cavity-BOX substrate is ready after the terracing process. At that stage, it consists of a patterned step-buried oxide layer (1.5 μm at its full thickness, 500 nm at its step thickness), an 80 μm-thick device layer, and 1 μm thermal oxide on the backside of the wafer.

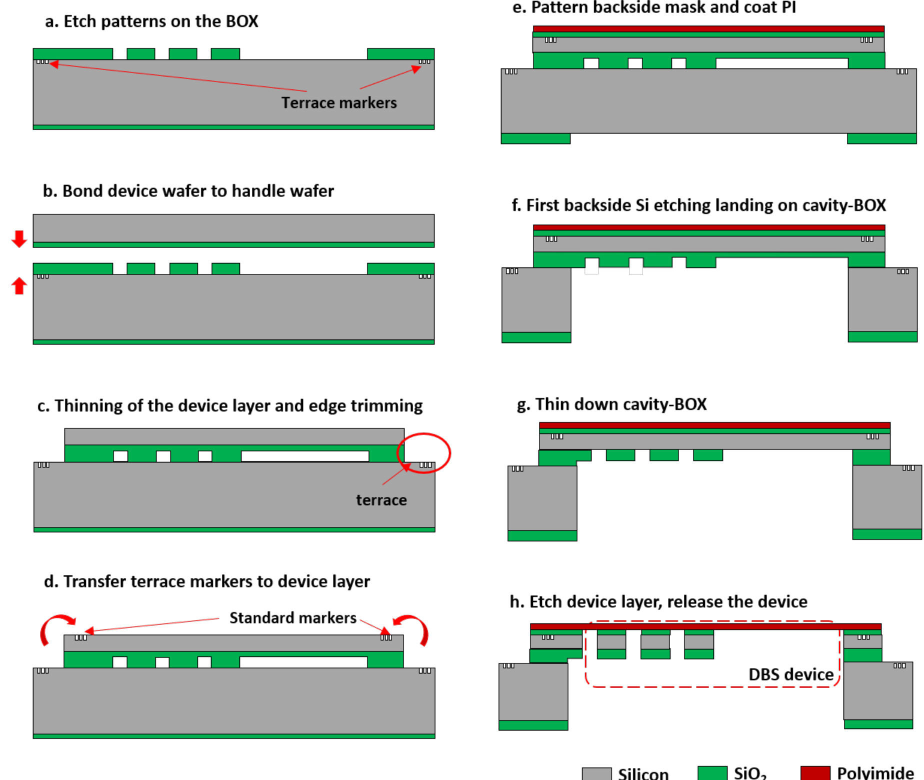

Figure 5.5: Cross-section drawings of the cavity-BOX substrate preparation and DBS demonstrator fabrication. (a) Positioning markers at 1.2 mm distance from the wafer edge and etching patterns in the BOX on top of the 380 μm handle wafer. (b) Fusion bonding of the device wafer to the handle wafer with patterned BOX (in vacuum and room temperature. (c) Thinning of device layer to 80 μm and edge trimming to create a 4 mm width terrace. (d) Transfer markers from the terrace to the device layer. (e) Patterning backside etching mask and coating wafer with polyimide, using silicon oxide as an adhesive layer. (f) Etching of the handle wafer from wafer backside and landing on the cavity-BOX. (g) Thinning down the cavity-BOX and exposing the buried oxide mask for device layer etching. (h) Etching of the device layer and silicon oxide adhesion layer, landing on polyimide.

DBS Demonstrator Fabrication

To continue with the demonstrator fabrication, the terrace markers on the handle wafer were first transferred to the device layer, placed 10 mm from the wafer edge as standard markers, and etched 140 nm deep into the silicon (Figure 5.5d). A 2 μm-thick PECVD SiO_2 layer was then deposited on top of the original 1 μm-thick thermal oxide layer on

the backside of the wafer and patterned with the silicon DRIE etching mask. Next, a 500 nm-thick PECVD SiO_2 layer was deposited on the front side of the wafer to promote adhesion of the subsequent polyimide layer, because SiO_2 is the preferred template for the silica-polyimide adhesion promotor. Subsequently, a 3 µm-thick polyimide layer (PI2610 Microsystems) was coated on top of the SiO_2 layer (Figure 5.5e) and cured. After that, the silicon DRIE etching step was applied from the backside of the wafer to remove the silicon substrate underneath the cavity-BOX, landing on the step oxide mask (Figure 5.5f). The embedded step oxide mask in the BOX layer enabled the silicon over-etch to balance out etching noniformity across the wafer. A blanket SiO_2 dry etch was subsequently applied to thin down the step oxide mask in the cavity-BOX layer until the pre-patterned oxide mask was opened through to the device layer (Figure 5.5g). Finally, the 80 µm device layer and the 500 nm-thick SiO_2 layer were dry-etched, landing on the polyimide layer (Figure 5.5h). After the etching of the device layer, all the silicon islands were separated, leaving them connected with the flexible polyimide film. The finished demonstrator was suspended in the silicon wafer frame through polyimide tabs.

5.2.3. Results and Discussion

Preparation of the Cavity-BOX

The cavity-BOX is formed by the bonding of two oxide layers: 1 µm of pre-patterned SiO_2 layer on the handle wafer and a 500 nm-thick SiO_2 layer on the device layer. (Figure 5.5b). Potential concerns regarding the bonding process include the following: (1) Bonding failures of the small patterned oxide features from the handle wafer; (2) undesired bonding between the handle wafer and the SiO_2 layer from the device layer in large dimension cavities; and (3) recesses in the device layer after bonding due to the large cavities in the BOX.

After cavity-BOX substrate preparation, no visible recesses in the wafer surface were observed in the device layer, especially not on the largest openings in the design with a dimension of 5 mm × 17 mm. Scanning acoustics microscopy (SAM) was used to inspect the bonding quality, as shown in Figure 5.6. The bonded areas have a good transmission of the acoustic waves, which are displayed as dark fields in the picture, while air gaps cause high reflections of the acoustic waves and are, therefore, displayed as bright fields. The images indicate that the area without cavities was successfully bonded, while there was no undesired bonding in the large cavity areas. No bonding defects have been observed among the small oxide features in the SAM images. After the backside etching of the handle wafer landing on the cavity-BOX (Figure 5.5f), the two-step oxide mask was intact, which also confirms the excellent bonding result. This demonstrates the high yield of this cavity-BOX preparation process.

Terrace Width

During the backside processing, it appeared that the 4 mm terrace width on the front side of the SOI wafer caused compatibility issues with the PAS5500 ASML wafer stepper and the SPTS Pegasus DRIE etching tool. During the backside lithography process, the wafer stepper needs to handle the wafer from the front side. The position of a number of the vacuum openings on the wafer stepper robot arm coincided with the 4 mm terrace region, which led to a loss of vacuum. The wide terrace additionally caused helium

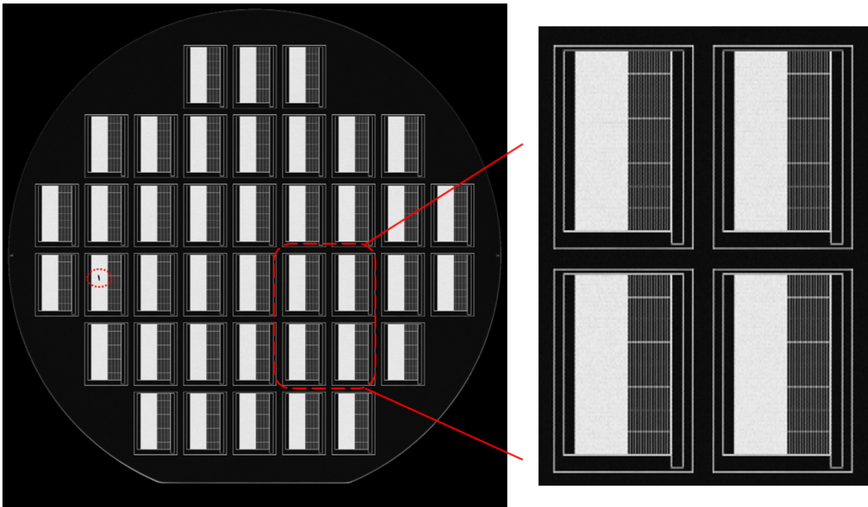

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Figure 5.6: Scanning acoustic microscopy (SAM) to inspect bonding quality. A particle appeared as a black dot on the left side, and a zoomed-in SAM image of four dies.

leakage errors on the chucks of the dry etching tools. To continue processing the 4 mm terrace cavity-BOX SOI wafers, the robot arm of the wafer stepper was explicitly tuned to accept the wafers. Special dry etch recipes with low helium flow were developed for the silicon and SiO_2 etch without a ceramic carrier. As a result of reducing the helium flow in the etching recipes, the wafer temperature could not be maintained during the process, leading to an increased nonuniform etch rate across the wafer. The etching slop was also enlarged due to the loss of temperature control.

Table 5.1: Compatibility of wafers with different terrace width in various processing tools

Terrace width	ASML stepper	SPTS ICP chamber	SPTS APS chamber	SPTS Pegasus chamber
1.8 mm	✓	✓	✓	✓
2 mm	✓	✓	✓	✓
2.5 mm	✓	✓	✓	✓
3 mm	✓	✓	✓	✗
4 mm	✗	✗	✗	✗

To overcome this issue, the terrace width should preferably be as small as possible for cleanroom compatibility. In contrast, the terrace edge should be as far as possible from the markers to avoid its interference with the alignment process. A trade-off test was performed to define the optimal terrace width. Wafers with different terrace widths were

tested in the standard 6-inch cleanroom processing line on the PAS5500 ASML wafer stepper, an SPTS Pegasus, ICP, and APS etching tools. The wafers were loaded into the machines, checking the vacuum on the robot arms and the helium leakage in the processing chamber. The test results indicate that a terrace width of 1.8 to 2.5 mm should provide sufficient compatibility to the processing tools but are still large enough as not to interfere with lithography, as shown in Table 5.1.

Backside Etching

To release the demonstrator from the silicon substrate and form the semi-flexible device structure, several etching steps were performed from the backside of the wafer. These etching steps include the following: (1) The DRIE etching of the handle wafer substrate landing on the cavity-BOX; (2) thinning down the cavity-BOX to expose the pre-patterned oxide mask; (3) etching of the device layer and the front side oxide layer using the embedded oxide mask to separate the silicon islands (Figure 5.5f,h).

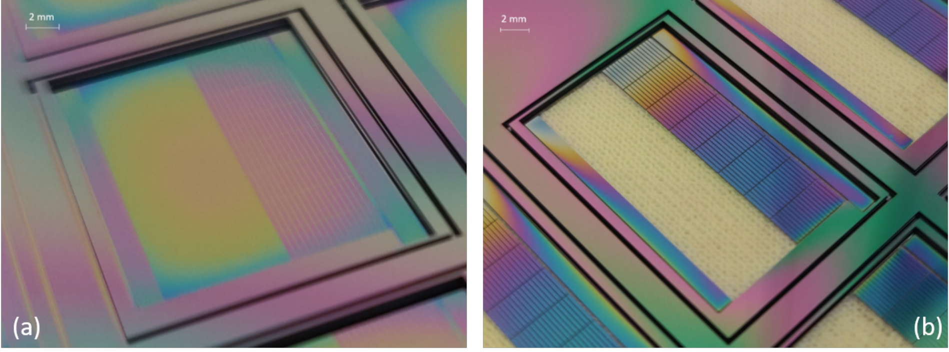
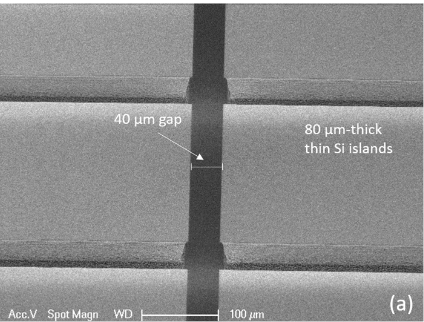


Figure 5.7: (a) Backside etching result of a silicon substrate, landing on cavity-BOX. (b) Etching device layer while using the patterned cavity-BOX as a mask, landing on polyimide.

Figure 5.7a depicts the wafer after the first step of the backside Si etching process landing on cavity-BOX. The device layer was protected by the exposed step cavity-BOX. The thickness of the remaining step cavity-BOX after silicon etching was measured using a reflectometer (Nanospec). The thinner part of the step cavity-BOX ranged from 120 nm to 350 nm (originally 500 nm), and the thicker part ranged from 1150 nm to 1380 nm (originally 1500 nm). Figure 5.7b shows the wafer with the etched device layer after the third backside etching step. The large rectangular opening was transparent, as the etching landed on the polyimide layer coated on the front side of the wafer. All the silicon structures, including the 40 µm-wide trenches between the silicon islands and the gaps that defined the silicon frame, were successfully fabricated.

Figure 5.8 shows SEM microphotographs of the silicon islands separated by the 40 µm trenches. The top part of the trench between the small silicon islands is 41.4 µm wide, while the bottom part is 54 µm wide. The measurement indicates an under etch of 6.3 µm from each side during the device layer etching, which is not ideal considering the fact that the etching depth is only 80 µm. The large under etch was mainly caused by temperature control issues, which resulted from the reduced helium flow that was



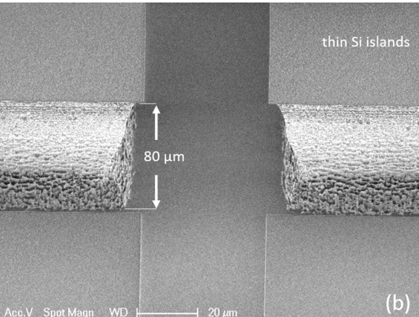


Figure 5.8: (a) SEM image of the 40 µm gaps between the silicon islands. (b) Detail image of the 80 µm-thick device layer etching profile, with 6,3 µm under-etch from each side.

necessary to process the wafer on the chuck of the silicon etcher. A better etching profile can be achieved using terrace widths that can be etched using the standard DRIE process without modifying the helium gas flow.

DEMONSTRATOR ASSEMBLY

After fabrication, the demonstrator was removed from the silicon frame (see Figure 5.9) by cutting the polymer tabs. The demonstrator consists of one large silicon island that can accommodate ASICs, 128 small silicon islands with 40 µm gaps between them, a large flexible film, and a silicon island for handling. In the final DBS device, the decoupling capacitors are located in each of the small silicon islands, and the electrodes are located on the flexible polyimide film. During the assembly of the DBS demonstrator, the large silicon island for the ASICs was first attached to a thin metal string with a double-side adhesive Kapton tape. The metal string was slowly rotated, together with the silicon island, tightening up and wrapping the semi-flexible device into a cylindrical probe. The cylindrical probe was then fixated in a heat-shrink tube. Biocompatible glue was injected into the heat shrink tube to encapsulate the DBS probe demonstrator. Finally, the heat shrink tube was released after the biocompatible glue was cured. In Figure 5.10, the assembled demonstrator has a length of 18 mm and a diameter of 1.2 mm, which is in line with the DBS design.

MARKER TRANSFER OFFSETS

One of the key steps in the DBS demonstrator fabrication is the marker transfer from the terrace on the edge of the wafer to the device layer (Figure 5.5d). Initially, the cavity-BOX layer was processed on the handle wafer, aligning to the markers on the terrace that are 1.2 mm from the wafer edge. These markers are referred to as “terrace markers.” However, after the device layer is bonded, these terrace markers are not preferred for alignment of structures on the device layer because of the height difference between the terrace and the device layer. During the alignment procedure, the wafer stepper levels the wafer by detecting the surface of the wafer and controls the exposure surface to ensure it is positioned within its focal range, specified as ± 25 µm for the ASML PAS 5000 stepper. For cavity-SOI wafers with a device layer thicker than 50 µm, the surface focusing

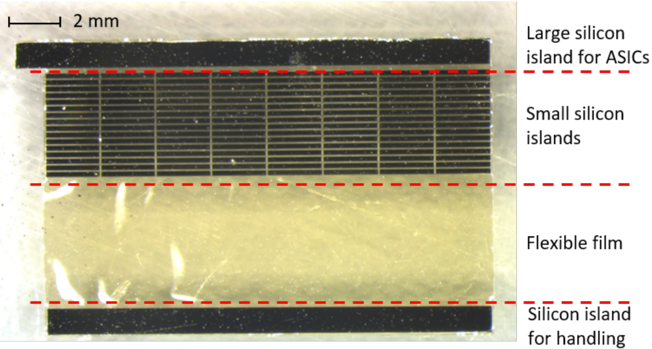


Figure 5.9: DBS demonstrator released after the fabrication. All the 80 µm-thick silicon islands are connected by the flexible film. The small silicon islands are isolated by 40 µm-wide gaps.

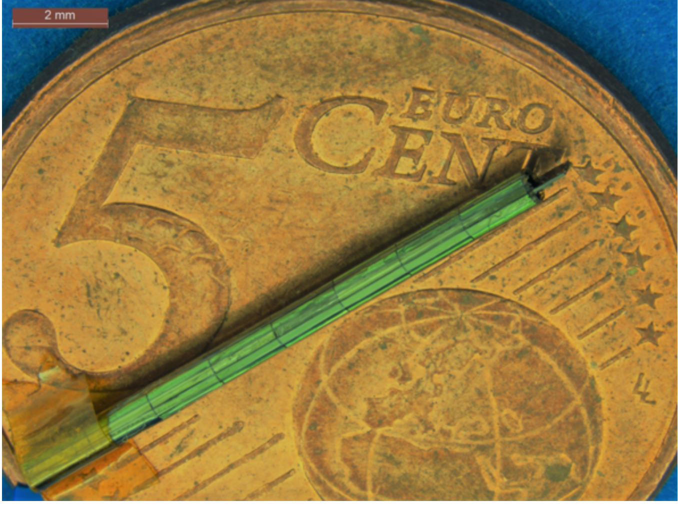


Figure 5.10: DBS demonstrator wrapped into a cylindrical probe with a length of 18 mm and a diameter of 1.2 mm on a 5 cent Euro coin.

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is out of specification, which will introduce alignment offsets for device layer exposures that are aligned to terrace markers. Therefore, two new markers are placed 10 mm from the wafer edge on the device layer, aligned to the terrace markers. These new markers are standard markers. The patterns for the device layer will be aligned to the standard markers, which are at the same height as the device layer surface. This marker transfer strategy was developed by Mountain et al.[12], and they reported a marker transfer offset amplitude increases from 20 nm to 160 nm with increasing radial position for a simulation wafer with a 80-µm-thick polyimide foil. In the first phase of this work, we further verified this marker transfer offset with real cavity-BOX SOI wafers by measuring marker coordinates on wafers throughout the process.

Here is how a coordinate system is built for a wafer in a lithography tool. When a

wafer is in the pre-alignment step in the lithography tool, the tool defines an X-Y coordinate system for the wafer based on its physical shape (wafer edge, flat, etc.), using the wafer center as (0, 0). Different lithography systems can result in different coordinate systems on the same wafer. The coordinates in this section are expressed in (x,y), in millimeters, with reference to the wafer center (0,0). The symbol "±" means on both positive and negative sides of the axis. The blue dots in Figure 5.11a show all the markers involved in the marker transfer offset calibration on the front side of the 6-inch wafer: terrace markers, standard markers, and 3D alignment markers. The terrace markers were first fabricated on the cavity-SOI wafer terrace at (± 73.8 mm, 0 mm). Standard and 3D alignment markers are widely used for the front-to-backside alignment process in an ASML wafer stepper for a 6-inch wafer production line. They should be fabricated on the device layer of the cavity-SOI wafer after marker transfer at (± 44.5 mm, ± 48.3 mm). The two standard markers should be located at (± 65 mm, 0 mm).

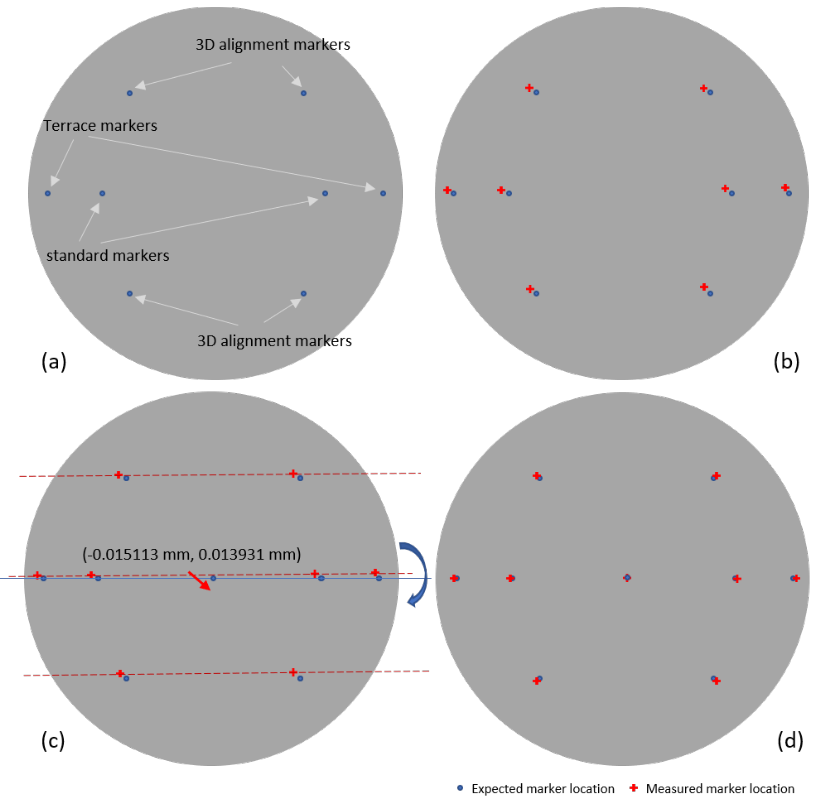

Figure 5.11: Marker transfer characterization on a 6-inch cavity-SOI wafer. (a) Expected marker location; (b) Measured marker location; (c) Compensate marker coordinate for calibration errors; (d) Compensated marker locations.

In Figure 5.11b, the red crosses represent the measured location of all markers after marker transfer. The details of the marker coordinates are shown in Table 5.2 below. All

markers are shifted almost 10 µm to the left-up side, including the terrace markers first placed by the same wafer stepper. Further investigation revealed that the stepper calibrations performed in the previous year caused a large measurement shift. The terrace markers were fabricated three years before the marker transfer process and marker measurements. Because of the machine calibrations during the three years, the definition of the wafer center was shifted. As a result, the wafer stepper defined a new "shifted" wafer center during the marker measurements. So the terrace markers, made by the same stepper, were also "shifted" according to the new wafer center. The same applies to the other exposed markers aligning to the terrace makers. To precisely characterize the marker transfer accuracy, the measured marker coordinates need to be calibrated to eliminate the effect of the shifted wafer center. The new wafer center was derived from the measured terrace marker coordinates and calculated center shifts and rotation. All the markers are moved right-down for (-0.015113 mm, 0.013931 mm) and rotated 0.016 mrad clockwise, as shown in Figure 5.11c. The compensated marker locations are presented in Figure 5.11d.

As shown in Figure 5.11d and Table 5.2, while the wafer center and rotation are corrected to their original location, all the markers show increased displacements between 300 nm to 500 nm in the radial direction from the wafer center towards the edge of the wafer. The distance between the left-right marker was increased by 1.076 µm from 147.6 µm to 148.676 µm. Thermal expansion of the wafer can cause the substrate to expand in the radial direction and result in a radial shift similar to the pattern in Figure 5.11d. As described in Eq. 5.1, the horizontal length change (ΔL), 1.076 µm, of the silicon substrate is proportional to its original length (L) and the temperature variation (ΔT). Okada et al. reported the thermal coefficient (α) of silicon to be $(2.59 \pm 0.05) \times 10^{-6} K^{-1}$ at 298.2K[15]. Supposing that the marker shift is only caused by the thermal expansion of the silicon substrate, and considering the original distance (L) between the terrace markers is 147.6 mm, the temperature change (ΔT) that would result in an expansion (ΔL) of 1.076 µm would be 2.76 °C (Eq. 5.2). In general, the temperature in a cleanroom is 21 °C, with a fluctuation of 2 °C. Therefore, the temperature change may well be the origin of the marker shift.

$$\Delta L = \alpha \times L \times \Delta T \tag{5.1}$$

$$\Delta T = \frac{\Delta L}{\alpha \times L} \tag{5.2}$$

Another assumption that might cause the markers to shift in the radial direction is the bonding process during SOI manufacturing. The terrace markers were first placed on the handle wafer. Next, the device layer was bonded onto the handle wafer and thinned down to the required thickness. The wafer bonding process normally goes through a high bonding pressure and a high temperature (800 °C to 1150 °C) processing environment, affecting the wafer bow, which might result in marker shifts in the radial direction.

In summary, a larger marker transfer offset than Mountain et al. reported was observed. The attached polyimide layer in Mountain's work did not fully simulate the complete status of an SOI wafer, which also involves a high-pressure wafer bonding and a high-temperature annealing process. The observed marker shift in the cavity-SOI wafers

Table 5.2: Marker coordinate prosessing for marker transfer offset measurement

Terrace marker	Left		Right	
	X (mm)	Y (mm)	X (mm)	Y (mm)
Reference	-73.800001	0.000006	73.799999	0.000002
Measured	-73.808184	-0.002918	73.792892	0.000378
Compensated	-73.800538	0.000000	73.800538	0.000000
Deviation	-0.000537	-0.000006	0.000539	-0.000002

3D marker	Left-Up		Right-Up	
	X (mm)	Y (mm)	X (mm)	Y (mm)
Reference	-44.500014	48.299948	44.499946	48.299955
Measured	-44.509066	48.298034	44.491542	48.300031
Compensated	-44.500341	48.300298	44.500267	48.300307
Deviation	-0.000327	0.000350	0.000321	0.000352

Standard marker	Left		Right	
	X (mm)	Y (mm)	X (mm)	Y (mm)
Reference	-65.000010	0.000016	64.999959	0.000001
Measured	-65.008129	-0.002711	64.992787	0.000180
Compensated	-65.000483	0.000010	65.000433	-0.000001
Deviation	-0.000473	-0.000006	0.000474	-0.000002

3D marker	Left-Down		Right-Down	
	X (mm)	Y (mm)	X (mm)	Y (mm)
Reference	-44.500038	-48.299954	44.499959	-48.299976
Measured	-44.506931	-48.302572	44.493715	-48.300604
Compensated	-44.500364	-48.300308	44.500282	-48.300328
Deviation	-0.000326	-0.000354	0.000323	-0.000352

can possibly be explained by the combination of thermal expansion and the wafer bonding process.

5.3. SECOND PHASE: TOWARDS INDUSTRIALIZATION

5.3.1. CHALLENGES FOR INDUSTRIALIZATION

The first phase successfully demonstrated the concept of the cavity-SOI. However, the cavity-SOI substrate preparation is rather cumbersome. As mentioned previously, the wafers in the first phase were shipped five times between the two wafer fabs. Although it avoided the compatibility problem of the alignment tools between the two wafer fabs, it is time-consuming, has potential contamination issues, and is therefore not suitable for high-volume industrial production. The second phase focuses on transferring the cavity-SOI preparation process (Figure 5.5a-d) to Okmetic, the SOI wafer supplier.

The key step of this industrialization is to guarantee lithography compatibility. Lithog-

raphy tools from the customers should be able to successfully detect the terrace markers fabricated by Okmetic and perform good alignment & marker transfer. In our case. the cleanroom of Philips MMD uses an ASML stepper PAS5500/100C, which is widely used in the research and industry, while Okmetic uses a VEECO Ultratech AP200 stepper. The key specifications of the two steppers are listed in Table 5.3[16, 17].

Table 5.3: ASML PAS 5500/100C versus VEECO Ultratech AP200

Type	ASML PAS 5500/100C	VEECO Ultratech AP200
Purpose	Industrial massive production	Advanced Packaging applications
Laser wavelength	365 nm	350 – 450 nm
Resolution	0.4 µm	2 µm
Field size	22.0 mm x 27.4 mm	68 mm x 26 mm
Overlay (front to front)	<60 nm	<350 nm
Overlay (front to back)	<1 µm	Infrared alignment: <1 µm
Substrate size	4-inch, 6-inch, 8-inch	6-inch, 8-inch, 12-inch
Placement reproducibility	<10 µm	± 100 µm
Marker sensor field	Front side: 200 µm x 200 µm Backside: 20 µm x 20 µm	320 µm x 240 µm
Marker location (6-inch)	Standard markers: (± 65, 0) Terrace markers: (± 73.8, 0)	No specific location
Marker layout	413 µm	438.5 µm

The key issue that hampers tool compatibility is how accurately different tool systems define their wafer coordinate systems. As explained previously, after a wafer has been loaded into the lithography tool, it builds a wafer coordinate system by sensing the wafer edge and flat/notch in the pre-align step. However, for the same wafer, the wafer coordinate system can have small shifts if the pre-alignment step is repeated. These small shifts are called placement reproducibility and vary depending on different lithography systems. The placement reproducibility can also indicate how stable the wafer coordinate systems are built between wafers in the same processing lot. The first exposure layer, which usually includes alignment markers, is exposed based on the defined wafer coordinate. The placement reproducibility of the Ultratech AP200 stepper can result in a shift of ±100 µm with respect to the wafer center, which means the markers will also have a deviation of ±100 µm. This deviation is random from wafer to wafer and cannot be controlled. The risk of such a marker deviation is that these markers might not be

able to be detected by alignment sensors of other exposure tools like the ASML stepper.

The ASML stepper has two alignment sensors. The front side sensor detects markers on the wafer front side for exposures on the front side. The front side marker alignment sensing field is 200 µm x 200 µm, and therefore, can cover the ±100 µm marker inaccuracy from the Ultratech AP200 stepper. The backside alignment sensor is used for exposures on the wafer backside with the "backside alignment" option. However, the ASML backside marker alignment sensing field is only 20 µm x 20 µm, which cannot tolerate the large marker deviation from the Ultratech AP200 stepper. To avoid using the "backside alignment" option, Okmetic placed ASML markers on the backside of the wafer using the infrared alignment option so that the front alignment sensor can be used when the wafer is flipped to expose the backside. Alignment markers on the cavity-BOX SOI in the second phase are shown in Figure 5.12. The Ultratech markers are also placed on the wafer, as they are used for patterning the cavity-BOX at Okmetic during the cavity-BOX SOI preparation. With these markers, the full cavity-BOX SOI preparation can be fully accomplished by Okmetic, avoiding the shipment of wafers between the two wafer fabs.

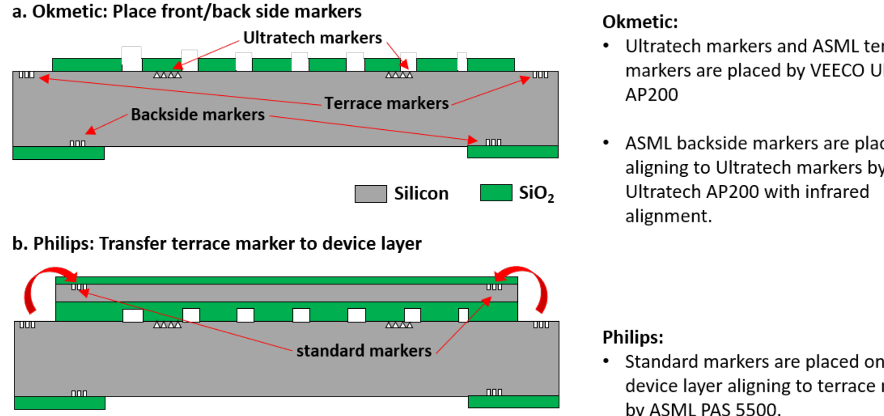

Figure 5.12: Alignment markers in the second phase.

5.3.2. Design, Fabrication, and Results.

The IVUS demonstrator was fabricated to verify the functionality of all markers and cavity-BOX manufactured by Okmetic in an aggressive design with small features. Philips provided the customized cavity-BOX design derived from a mask set for IVUS catheter production. Part of the mask design is shown in Figure 5.13a, with smaller structures than the DBS design used in the first phase. The design consists of 116 silicon islands with a width of 24 µm. The islands are separated by 2-µm wide meander-shaped or straight gaps (blue structures in Figure 5.13a). The pattern of the gaps needs to be etched in the cavity-BOX layer aligned to the Ultratech markers provided by Okmetic. Metal patterns in the center of each island were fabricated on the device layer of the SOI wafer aligned to the transferred standard markers, as shown in the mask design (Figure 5.13a) and the cross-section drawing (Figure 5.13b). The cavity-BOX and metal patterns are

used to verify the alignment accuracy between these two layers, which is actually the marker transfer accuracy. The design also has a backside opening mask to release the F2R device, similar to the DBS design in the first phase.

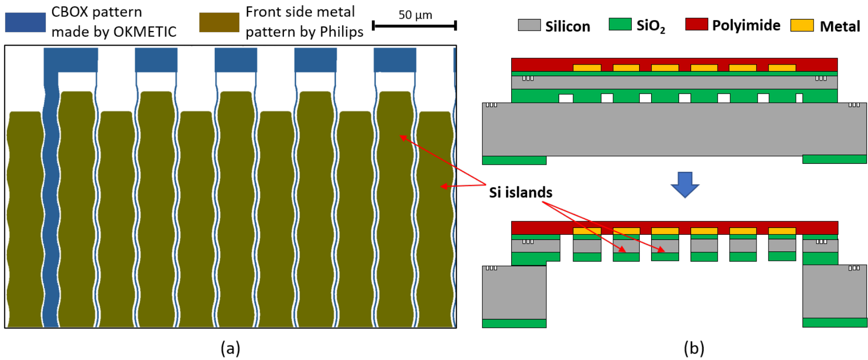

Figure 5.13: (a) Partial IVUS Mask design for second phase. (b) Cross-section drawing for cavity-BOX demo with IVUS design. Extra metal patterns were added on the surface of the device layer to confirm the alignment. Metal patterns should be in the middle of the silicon islands after backside DRIE process.

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The substrate preparation and the follow-up F2R process in the second phase are similar to that in the first phase, as described in Figure 5.5, and therefore not repeated here. The only difference was the additional 1-µm thick AlCu metal structures deposited on the device layer, aligned to the transferred standard markers, followed by the polyimide coating step (Figure 5.13b). Finally, the device was released by performing the backside etching. The entire process was fully developed in the first phase and executed without problems in the second phase. No wafer handling errors from the processing tools were encountered during the processing. Figure 5.14a-b presents the fabrication result of a typical device. Although the backside DRIE process was not precisely tuned for this application, the silicon islands were well-defined by the DRIE etching and the embedded oxide mask, demonstrating the successful combination of the F2R with the cavity-BOX SOI technology. However, some unexpected alignment issues were encountered. According to the mask design, the metal structures should be located in the middle of the silicon islands, which is not the case, as shown in Figure 5.14c-d. The misalignment between the metal structures and the cavity-BOX patterns is up to 3 to 8 µm in the x direction and 3 to 6 µm in the y direction, involving a minor wafer rotation, and much larger than the sub-micron alignment accuracy reported in [12].

A first possible explanation can be the accuracy of the markers placed by Okmetic. Therefore, the terrace markers of the misaligned wafers were measured for their offset, with the wafers from the first phase as a comparison. The measured marker offset represents the deviation to the expected marker locations. As presented in Table 5.4, the offset in the x-direction ranges from 21 to 41 µm, and in the y-direction ranges from 16 to 29 µm, which corresponds to the placement reproducibility of ±100 µm between wafers and batches. The offsets of the markers from the first phase, made by the ASML stepper, were all below 10 µm. Although the offsets of the markers made by Okmetic are higher, they are still within the marker search sensor field range. Therefore, the markers made by

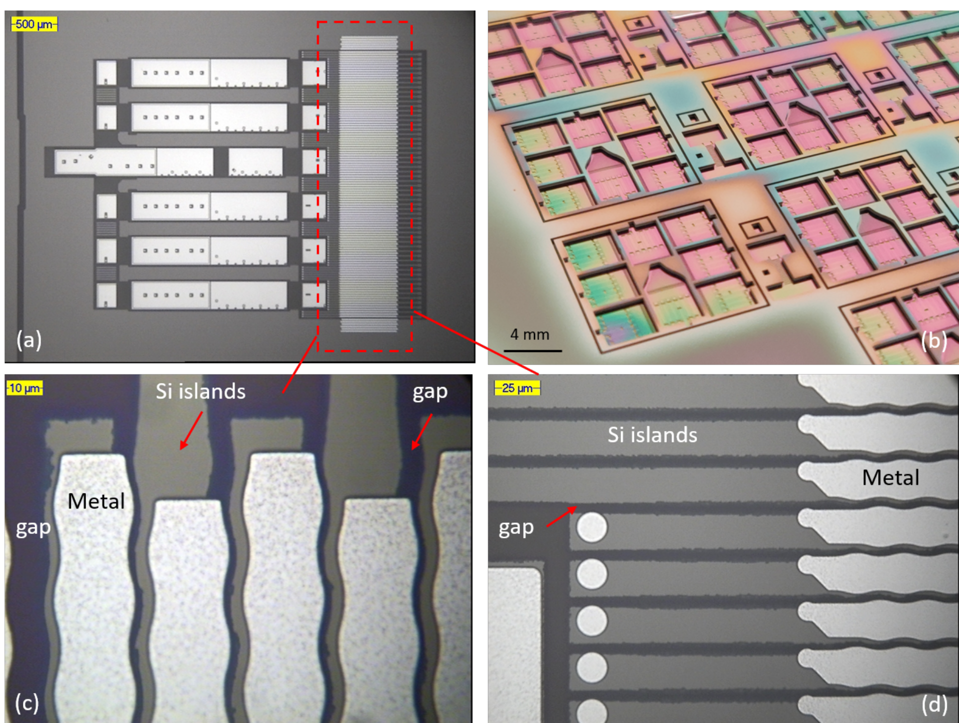

Figure 5.14: Process results of the second phase optimization. (a) front side overall view of the device after fabrication; (b) backside overall view of the fabricated wafer shows good DRIE results (c-d) Front side misalignment between the metal layer and the cavity-BOX mask.

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Okmetic should be able to be located by the ASML stepper to accomplish the alignment.

However, after further consulting with ASML technical support, more ASML alignment mechanisms were discovered. The alignment process is not simply accomplished by locating the markers in the marker sensing field. The alignment phase will move and rotate the wafer to the correct position using its wafer center as a reference. Here, the reference wafer center is defined by the ASML stepper during the wafer exposure. When the difference between the wafer centers defined by the two lithography tools (reflected as marker offset measured in Table 5.4) is larger than 10 µm, the wafer stage of the ASML PAS 5500 is not able to correct this wafer center delta automatically during the wafer alignment procedure, and therefore resulting in misalignment. As a comparison, wafers from the first phase, whose markers were made by the ASML stepper, have their marker offsets below 10 µm. This explains the good alignment and maker transfer process in the first phase.

5.4. DISCUSSION

The microfabrication in the second phase was completed successfully. However, unexpected misalignment problems occurred, although the marker offset detection test was

Table 5.4: Terrace marker offset made by OKMETIC versus Philips

Terrace markers	offset X (mm)	offset Y (mm)	offset theta (mrad)
OKMETIC W1	-0.0211	0.0163	0.3154
OKMETIC W2	0.0412	0.0294	0.4912
1st phase W1	-0.0062	0.0032	-0.0175
1st phase W2	-0.0053	0.0031	-0.0721

performed before the full process. The alignment failure originated from the difference in wafer centers defined by the two machines. The alignment phase of the ASML wafer stepper cannot provide accurate alignment when the wafer center offset is more than 10 µm. Unfortunately, this misalignment problem could not be foreseen while designing the experiments.

There are ways to compensate for the large wafer center offset during design so that the ASML stepper can process the wafers with the markers provided by Okmetic. It is possible to detect the wafer center offset between the lithography tools before the exposure and compensate for it by manually updating the alignment setting. However, the wafer center defined by the Ultratech stepper varies randomly from wafer to wafer because of the large placement reproducibility tolerance. With the current ASML software, the compensation offset needs to be updated manually wafer per wafer, which is not practical in industrial production.

By the time this chapter was written (Feb. 2022), Okmetic has improved the placement reproducibility of their Ultratech stepper and developed a new approach to align with the ASML stepper. It was possible to read out the wafer center of a reference wafer with makers placed by the ASML stepper. Okmetic plans to produce new wafers with markers using the wafer center from the reference wafer. In other words, they want to make "copies" of the initial reference wafer so that the new "copies" have the same wafer center as the reference wafer and can be processed on ASML steppers. To verify the new solution, Okmetic will produce these "copies," and they will be tested on the ASML stepper. If it is successful, it will allow Okmetic to provide customized cavity-BOX wafers that are compatible with variant lithography tools for the industry.

5.5. CONCLUSION

This chapter introduces a new tool in the MEMS development tool box: cavity-BOX SOI. Cavity-BOX SOI offers a pre-fabricated oxide hard-etch mask buried underneath the device layer, allowing for double-sided processing of the device layer. This new processing feature allows for great flexibility in MEMS process and design. This chapter presented the development of cavity-BOX SOI with the SOI manufacturer Okmetic. The development was divided into two phases: proof of concept and industrialization.

In the first phase of the experiment, cavity-BOX SOI substrates with a buried oxide mask were developed, prepared, and applied in the Flex-to-Rigid process. The oxide mask was first fabricated on the handle wafer and then bonded with the oxide to the device layer to form the cavity-BOX. The alignment between the structures on the device

layer and the buried oxide mask was successfully realized by employing the front-to-front marker transfer strategy. The accuracy of the transferred alignment markers was characterized by the ASML wafer stepper, and an expansion of the substrate in radial direction was detected. The cavity-BOX SOI substrate was successfully implemented for a DBS demonstrator fabrication. The cavity-BOX layer was used as an etch-stop layer and a pre patterned two-step DRIE mask to etch through the device layer from the backside of the wafer. The application of the cavity-BOX substrate to the DBS demonstrator fabrication resulted in a more robust and significantly simplified process with an improved design freedom, including the coexistence of high-precision micron-sized features and large millimeter-sized openings.

In order to industrialize the cavity-BOX SOI substrate technology, Okmetic should have the ability to provide cavity-BOX SOI substrates with both customized designs and effective alignment markers for follow-up processes in other foundries. However, the Ultratech stepper in their production line is not suitable for high accuracy and causes compatibility issues with ASML steppers. The second phase therefore focuses on developing a cross-platform machine-to-machine overlay matching strategy. After verification by marker detection tests, Okmetic provided cavity-BOX wafers with an IVUS catheter design and alignment markers. However, an unexpected misalignment still occurred in the final run. The misalignment was caused by the large difference in the wafer centers defined by the two stepper machines. Different solutions for the misalignment are under development.

In summary, cavity-BOX SOI has great potential to simplify the fabrication of various MEMS devices, especially where device thinning and precise silicon structure separation or definition are needed. The terrace of the cavity-BOX SOI wafers also permit for applying the high precision (less than 500 nm) alignment strategy of the BOX pattern and the device layer structures. After improving the marker placement accuracy, the customized cavity-BOX SOI can be provided by the commercial SOI suppliers in large volume, hence, enabling the scaling up of production.

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6

Conclusions and Recommendations

6.1. Conclusions

State-of-art smart catheters are mostly made with point solutions and often using outdated technologies. With the increase of cardiovascular diseases, higher image quality, a smaller form factor, and lower manufacturing costs for smart catheters are needed. The framework of this thesis is the previously developed Flex-to-Rigid (F2R) technology, which is a miniaturization platform for smart minimally invasive instruments such as catheters and implants. To extend the functionality, usability, and the manufacturability of this technology, in this thesis a number of key technology modules, namely an optical data link module, high-density embedded trench capacitors, and cavity-BOX SOI were developed. The main contributions of this thesis work to the field are stated below.

Contribution I

Smart catheters have to migrate from electrical to optical transmission to achieve higher data rates. As a result, an optical link needs to be integrated into the miniaturized catheter system. An optical data link module (ODLM) with a dimension of 240 µm × 240 µm × 420 µm was designed and fabricated in Chapter 2. The details of the ODLM design and F2R-based process modules have been presented. Its submillimeter form factor can easily fit in various smart catheters (e.g. IVUS, ICE), and for these applications should support at least a 1.2 Gb/s data rate. The ODLM is a mass-producible stand-alone device that provides a reliable laser to fiber self-alignment and mechanical strength. It is the world's smallest optical interposer for data transmission (by 2022). The fabricated stand-alone ODLM eventually can transmit up to 25.8 Gb/s, $2^{31}-1$ PRBS when driven through a high-speed bias tee. The BER test indicated that error-free operation can be achieved at an optical output of -4 dBm.

Contribution II

The ODLM was integrated in a digital ICE catheter system lab setup to demonstrate its functionality. The optical transmitted digital ICE catheter system successfully achieved a data rate of 6 Gb/s with a customized laser driver and resulted in high resolution ultrasound images.

Contribution III

Chapter 5 presents an extension of F2R, by integrating high-density embedded trench capacitors into the thin silicon substrate of the F2R platform. The process module for integrating 1.1µm and 1.2µm diameter trench capacitors with a pitch of 4 µm and a high-aspect-ratio (around 1:30) profile were presented. The capacitance density of trench capacitors shows an increase of a factor of 11 compared to flat capacitors. Stress analysis showed that introducing trench capacitors with a pitch of 2 µm and a diameter of 1 µm in the F2R thin silicon substrate with a dimension of 320 µm × 1700 µm × 40 µm did not cause any significantly bending. This allows for further device integration on the F2R thin silicon substrate and further assembly steps.

Contribution IV

A new tool in the MEMS development tool box: cavity-BOX SOI. Cavity-BOX SOI offers a pre-fabricated oxide hard-etch mask buried underneath the device layer, allowing for

double-sided processing of the device layer. This new processing feature allows for great flexibility in MEMS process and design. The concept of cavity-BOX SOI was initially developed to improve the process of the F2R platform and reduce the process costs. The F2R process can be greatly simplified by introducing a pre-patterned oxide mask in the buried oxide layer of the SOI substrate. The alignment between the structures in/on the device layer and the buried oxide mask was successfully realized by employing a front-to-front marker transfer strategy. The functionality of the cavity-BOX SOI was demonstrated by fabricating a semi-flexible deep brain stimulation (DBS) demonstrator with a length of 18 mm and a diameter of 1.39 mm.

CONTRIBUTION V

For industrialization of the cavity-BOX SOI, a process sequence that allows for high accuracy alignment when using the cavity-BOX SOI was developed that involves multiple lithography tools (ASML and Veeco in this case). The process sequence involves transferring of markers from the starting substrate to the SOI device layer and wafer backside for front and back side alignment.

6.2. RECOMMENDATIONS

The technologies and applications shown in the thesis work demonstrate the great potential of integrating miniaturized functional modules using the Flex-to-Rigid platform. However, further research and development are needed to further mature and industrialize the technology. The potential topics for future research are:

- The cavity-BOX SOI technology possesses significant potential and provides various advantages for the manufacturing of MEMS devices. Subsequent research should identify innovative processes that could lead to breakthroughs as a result of cavity-BOX SOI, as well as opportunities to simplify manufacturing processes.

- As the ODLM integration in the smart catheter has been successfully demonstrated in this thesis work, the next step would be to standardize its implementation in the application into instruments with respect to: communication protocol, proximal connection, etc.

- Benefiting from the small form factor, the ODLM can possibly offer rack to rack, board to board, or even chip to chip connections with high data rate. Further research could explore various design optimizations for the ODLM to enhance its data transmission capabilities.

- Similar to the trench capacitors studied in this thesis, more in-substrate devices could be integrated in F2R. Future work can explore additional in-substrate integrations in the F2R, such as manufacturing a laser driver on the F2R in combination with ODLM, more passive devices (e.g. inductors), or microfluidic channels, etc.

- Due to limitations of the foundry fab, flexibility, and time, not all the process steps or recipes could be fully optimized. Therefore, it is also recommended to further

optimize some of the key process steps in this thesis work, such as the trench capacitor etching process and the trench capacitor dielectrics deposition process.

SUMMARY

Around 10% of the population will have to go through a catheterization procedure for the treatment of a cardiovascular disease at a certain stage of their lives. During such a procedure, smart catheters will be the "eyes and ears" of the surgeons, significantly improving the diagnosis and treatment. However, there have been very limited improvements and innovations in smart catheters over the past decade, as most smart catheters are manufactured with technical point solutions, and therefore cannot sustain themselves with enough production volume for continuous innovation. Consequently, Flex-to-Rigid (F2R) was developed as an interconnect platform for heterogeneous integration of electronic components in submillimeter form factors. F2R is an open technology platform that can serve many smart catheter applications from a variety of manufactures. It consists of multiple small and thin silicon islands connected by thin flexible interconnects, which allows devices and components to be mounted with standard assembly techniques or directly fabricated onto the F2R platform. This thesis presents innovations in F2R-based applications, integration, and process optimization for smart catheters.

The first part of the thesis is an example of applying F2R for making a miniaturized device, a submillimeter optical data link module (ODLM). With smart catheters migrating from analog to digital instruments, an optical interposer is needed to realize high-speed optical data transmission. The biggest challenge is the form factor of the optical interposer, as it needs to fit into a catheter tip that is inserted inside human veins. This challenge falls exactly in the scope of F2R. The ODLM was fabricated, assembled, and integrated into an ICE catheter demo system. The second part of the thesis presents high-density embedded trench capacitor integration in the F2R platform. Compared to assembling discrete capacitors on F2R, embedded capacitors in the F2R substrate save space in the catheter tip and bring the decoupling capacitors directly underneath the ASICs, resulting in better performance. The work involved the trench capacitor process development, especially the high-aspect ratio (HAR) DRIE trench etching process. More importantly, the trench capacitor process was optimized to be compatible with the standard F2R process. The last part of the thesis presents the work on improving the fabrication process of the F2R platform. The largest bottleneck and most critical step of F2R is the "buried trench" process, which creates separated thin silicon islands. The buried trenches consist of thin oxide membranes, that are very sensitive to thin-film stress and other mechanical forces, resulting in reduced production yield. Cavity-BOX SOI eleminates the "buried trench" process by introducing a patterned buried oxide layer. The patterned buried oxide mask allows an intact wafer surface during the process until the final DRIE process, which separates the wafer in one go using this oxide mask. The production yield can be significantly improved using the cavity-BOX SOI for the F2R process. A deep brain stimulation (DBS) probe test structure was fabricated with the cavity-BOX SOI based F2R process to demonstrate the technology concept. A method to align the patterns on the wafer to the patterned buried oxide mask was developed.

SAMENVATTING

Ongeveer 10% van de bevolking zal op enig moment in hun leven in het ziekenhuis worden opgenomen voor een hartkatheterisatie. De uitkomst van zo'n procedure wordt aanzienlijk verbeterd door het gebruik van "slimme" katheters die als het ware de ogen en oren van de arts zijn. Desondanks is er de afgelopen tien jaar nauwelijks enige innovatie in deze instrumenten geweest. Een van de redenen hiervoor is dat meestal gebruik wordt gemaakt van hele dure specifieke technologieën (puntoplossingen), waarvan het productievolume en dus ook de omzet te klein is om een continue innovatie mogelijk te maken. Het Flex-to-Rigid (F2R) fabricageplatform is ontwikkeld om hier een oplossing voor te bieden. Het is een universeel platform voor de heterogene integratie van elektronische componenten en systemen met submillimeter afmetingen met als belangrijkste toepassingsgebied slimme katheters. Het bestaat uit hele kleine, dunne siliciumeilandjes die elektrisch verbonden zijn door middel van zeer dunne flexibele folies. Elektronische sensoren en anderen componenten kunnen monolithisch op de siliciumeilandjes worden gefabriceerd, maar ze kunnen er ook als aparte elementen op worden geassembleerd.

Het is de verwachting dat in de toekomst slimme katheters in toenemende mate zullen worden gedigitaliseerd. Hierbij is het de verwachting dat het hoge snelheid datatransport van de tip van de katheter naar het uiteinde buiten de patiënt in het optische domein zal plaatsvinden. De grootste uitdaging hierbij is de realisatie van een submillimeter optische data link module (ODLM) die klein genoeg is om in een katheter in menselijke aderen te kunnen worden ingebracht. In het eerste gedeelte van dit proefschrift wordt de ontwikkeling van deze ODLM beschreven, en gedemonstreerd in een ICE-katheter systeem. Het tweede gedeelte van dit proefschrift laat zien hoe in het F2R platform hoge dichtheid ontkoppel- capaciteiten kunnen worden geïntegreerd. Deze hoge dichtheid ontkoppelcapaciteiten geven een aanzienlijke ruimtebesparing, en kunnen bovendien direct onder de ASICs in de kathetertip worden geïntegreerd, wat resulteert in een betere ontkoppeling. Een belangrijk aspect van het werk was de ontwikkeling van een hoog aspectratio silicium etsproces dat compatibel is met het F2R platform.Een van de meest kritische stappen in het standaard F2R-proces zijn de zogenaamde "buried trenches" die de afmetingen van de silicium eilanden definiëren. Deze buried trenches worden afgesloten met een dun silicium membraan dat zeer gevoelig is voor stress and mechanische krachten, wat de productie opbrengst kan verlagen. Het in dit proefschrift ontwikkelde Cavity-BOX SOI proces maakt de buried trenches overbodig omdat er gebruik wordt gemaakt van SOI wafers met een gepatroneerde begraven oxide laag. Hierdoor kan het siliciumwafer oppervlak intact kan blijven tot de laatste achterkant diepets stap, hetgeen resulteert in een hogere opbrengst. Het Cavity-BOX SOI proces wordt gedemonstreerd aan de hand van een veeleisende "deep brain stimulation probe" teststructuur. Ook wordt een nieuwe methode besproken om structuren op deze speciale SOI wafers aan de patronen in de begraven oxide laag te justeren.

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extensive support from Okmetic. It was a great collaboration between academy and industry with solid application.

Now take a step back and zoom into my life, my PhD work unfortunately went through the Covid pandemic. During this difficult time, I have received a lot of support from my family and friends. Yue, it was always a great pleasure to play LOL with you ;p Hope you all the best! WenCong,thanks for your support in the past 15 years! Yiran and Yifeng, thank you for the lovely small talks. Wenhan and Di, I loved our girls' talks. Xingyu, thanks for sharing your PhD experience and your guidance. I would also like to thank a special group of friends, the Stuyt Family. I met Joop Stuyt 10 years ago when I arrive in the Netherlands for my master study, and introduced to her family in the same year. Through the years, I have received extensive support from Joop and her family, Trudy, Jan, and Tin. They were like my second family here in the Netherlands. During my PhD time, Joop has supported me a lot while she was my roommate. She helped me mitigated lots of stress from research and covid. I've learned a lot from Joop and the Stuyt family. They gave me lots of love and helped me find myself. They have shared my happiness and sorrow with me. I am really luck and happy to have them with me.

Coming to the end, I would like to thank my parents. 10 years ago, they made the decision to support my study in the Netherlands. I understand now it was not an easy decision. In the past years, they have been supporting me in their own ways. And now, I am happy to see they are enjoying their retirement and found their own life. Parent's love is just so great and unlimited. I guess I can never say enough thank you for that.

In the very end of this thesis and my PhD life, I would like to thank myself, especially this young cute naive boy who was brave enough to take this PhD challenge 5 years ago. Now that I think again, I would still take it without hesitation. It was just such an amazing learning experience, and I think I did a good job. Thank you Jian!

Appendix-A: F2R-based ODLM fabrication

Buried trench mask

- Deposition: 700 nm SiO2 deposition.
- Lithography: expose and develop ODLM BT mask on 1.3 um resist.
- Etching: SiO2 dry etching landing on Si.
- Cleaning: Resist strip with plasma, and RCA cleaning.
- Deposition: Deposit 100 nm Ti.

backside oxide mask patterning

- Deposition: 4.5 um low stress SiO2 deposition on the backside.
- Lithography: expose and develop BSM1 mask.
- Etching: Recess etch 1.5 um SiO2.
- Cleaning: Resist strip with plasma.
- Lithography: expose and develop BSM2 mask.
- Etching: dry etch SiO2 landing on Si.

Buried trench process

- Cleaning: Resist strip with plasma, Piranha organic removal cleaning, and RCA cleaning
- Etching: Silicon dry etching with negative slope.
- Etching: wafer by wafer CF_4 plasma etching
- Deposition: 3 um PECVD low stress SiO2 deposition.

First metal

- Deposition: deposit 1 um AlCu.
- Lithography: expose and develop ODLM_M7 mask on 1.3 um resist.
- Bake: reflow bake resist at 125 °C.
- Etching: Etch AlCu in PES at 30 °C.
- Cleaning: Rinse&Dry, resist plasma strip.

First PI & Via etch

- Etching: short oxygen plasma surface treatment.
- PI coating: spincoat polyimide PI2610, with VMX652 primer.
- Bake: bake PI at 150 °C.
- Cure: long-time bake PI at 275 °C.
- Lithography: expose and develop ODLM_C1 mask on 1.3 um resist.
- Etching: dry etch polyimide landing on Si and metal.
- Strip: resist stripping with Microstrip 5010.

AlCu rerouting & second PI

- Etching: short oxygen plasma surface treatment.
- PI coating: spincoat polyimide PI2610, with VMX652 primer.
- Bake: bake PI at 150 °C.
- Cure: long-time bake PI at 275 °C.
- Lithography: expose and develop ODLM_C1 mask on 1.3 um resist.
- Etching: dry etch polyimide landing on Si and metal.
- Strip: resist stripping with Microstrip 5010.
- PI coating: spincoat polyimide PI2610, with VMX652 primer.
- Bake: bake PI at 150 °C.
- Cure: long-time bake PI at 275 °C.

AlCu rerouting & second PI

- Etching: short oxygen plasma surface treatment.
- PI coating: spincoat polyimide PI2610, with VMX652 primer.
- Bake: bake PI at 150 °C.
- Cure: long-time bake PI at 275 °C.
- Lithography: expose and develop ODLM_C1 mask on 1.3 um resist.
- Etching: dry etch polyimide landing on Si and metal.
- Strip: resist stripping with Microstrip 5010.
- PI coating: spincoat polyimide PI2610, with VMX652 primer.
- Bake: bake PI at 150 °C.
- Cure: long-time bake PI at 275 °C.

Second PI hard etch mask

- Bake: pre-bake at 125 °C for longer than 30 mins.
- Deposition: AlCu-Mo-AlCu hard etch mask 200 nm.
- Lithography: expose and develop ODLM_C2 mask on 1.3 um resist.
- Bake: reflow bake resist at 125 °C.
- Etching: etch AlCu in PES at 30 °C.
- Strip: resist stripping with Microstrip 5010.
- Coating & bake: coat 3.9 um resist and hard bake at 125 °C.

Final release

- Backside etching: dry etch 120 um Si.
- Backside etching: dry etch SiO2 900 nm.
- Backside etching: dry etch Si 380 um landing on BOX.
- Backside etching: SiO2 dry etch to remove 500 nm BOX.
- Backside etching: CHF_3 high-pressure SiO2 dry etch 3 um.
- Frontside etching: oxygen plasma dry etch resist and PI, with He-leak detection.
- Etching: etch AlCu-Mo-AlCu mask in PES at 30 °C.
- Clean & Dry: with Soxleth

APPENDIX-B: F2R BASED EMBEDDED TRENCH CAPACITORS FABRICATION

TRENCH CAPACITORS

- Deposition: 1 um SiO2 deposition.
- Lithography: expose and develop TrCAP_02_TRC_TRENCH mask on 1.3 um resist.
- Etching: SiO2 dry etching landing on Si.
- Cleaning: Resist strip with plasma, Piranha organic removal cleaning, and RCA cleaning
- Etching: apply DRIE Si etch for HAR trenches.
- Deposition: LPCVD ONO layer deposition 5/15/30 nm.
- Deposition: in-situ doped poly silicon deposition 500 nm and anneal at 900 °C.
- Backside Etching: remove poly silicon on the wafer backside with dry etch.
- lithography: expose and develop TrCAP_04_TRC_POLY mask on 1.3 um resist and reflow back.
- Etching: poly silicon landing on ONO layer.
- Etching: short etch ONO layer landing on Si.
- Strip: resist stripping with plasma

F2R PROCESS

- Deposition: 1000 nm SiO2 deposition.
- Lithography: expose and develop TrCAP_05_TRC_BT mask on 1.3 um resist.
- Etching: SiO2 dry etching landing on Si.
- Etching: Silicon dry etching with negative slope.
- Etching: wafer by wafer CF_4 plasma etching
- Deposition: 3 um PECVD low stress SiO2 deposition.
- Deposition: deposit PECVD SiN_x and SiO2 layers for stress analysis.
- Lithography: expose and develop TrCAP_06_TRC_VIA mask on 1.3 um resist.
- Etching: dry etch PECVD SiN_x and SiO2 landing on Si substrate.
- Cleaning: Resist strip with plasma, and RCA cleaning.
- Etching: 1% HF etch to remove native SiO2.
- Deposition: AlCu 1 um deposition.
- Lithography: expose and develop TrCAP_07_TRC_RM mask on 3.9 um resist.
- Etching: Etch AlCu in PES at 30 °C.
- Strip: resist stripping with plasma.
- Etching: short oxygen plasma surface treatment.
- PI coating: spincoat polyimide PI2610, with VMX652 primer.

- Bake: bake PI at 150 °C.
- Cure: long-time bake PI at 275 °C.
- Deposition: AlCu-Mo-AlCu hard etch mask 200 nm.
- Lithography: expose and develop TrCAP_08_TRC_RM_VIA mask on 1.3 um resist with reflow bake.
- Etching: Etch AlCu in PES at 30 °C.
- Strip: resist stripping with Microstrip 5010.
- PI coating: spincoat polyimide PI2610, with VMX652 primer.
- Bake: bake PI at 150 °C.
- Cure: long-time bake PI at 275 °C.
- Backside lithography: expose and develop TrCAP_09_TRC_BSM mask on 5.9 um resist with pre and reflow bake.
- Backside etching: dry etch ONO layer deposited on the wafer backside.
- Backside etching: Si DRIE etch 380 um landing on the BOX layer.
- Backside etching: SiO2 dry etch to remove 500 nm BOX.
- Backside etching: CHF_3 high-pressure SiO2 dry etch 3 um.
- Frontside etching: oxygen plasma dry etch resist and PI, with He-leak detection.
- Etching: etch AlCu-Mo-AlCu mask in PES at 30 °C.
- Clean & Dry: with Soxleth

List of Publications

1. Marta Kluba, **Jian Li,** Katja Parkkinen, Marcus Louwerse, Jaap Snijder, Ronald Dekker, *Cavity-BOX SOI: Advanced Silicon Substrate with Pre-Patterned BOX for Monolithic MEMS Fabrication*, Micromachines 2021, 12, 414. doi: 10.3390/mi12040414 | Journal article.

2. **Jian Li,** Chenhui Li, Vincent Henneken, Marcus Louwerse, Jeannet van Rens, Paul Dijkstra, Oded Raz, Ronald Dekker, *25.8 Gb/s Submillimeter Optical Data Link Module for Smart Catheters*, Journal of Lightwave Technology, vol. 40, no. 8, pp. 2456-2464, 15 April, 2022.doi: 10.1109/JLT.2021.3137981| Journal article.

3. **Jian Li,** Andrzej Sielecki, Elena Beletkaia, *A photonic MEMS interposer to solve electronic and optical assembly challenges*, PhotonicsViews 2022-06, vol19, no. 3.doi: 10.1002/phvs.202200027| Journal article.

4. Pan Liu, **Jian Li,** Henk van Zeijl, Guoqi Zhang, *Wafer Scale Flexible Interconnect Transfer for Hetrogeneous Integration*, 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2020, pp. 817-823. doi: 10.1109/ECTC32862.2020.00133| Conference paper.

5. **Jian Li,** Jeroen Naaborg, Marcus Louwerse, Vincent Henneken, Carlo Eugeni, Ronald Dekker, *Embedded High-Density Trench Capacitors for Smart Catheters*, 2020 IEEE 8th Electronics System-Integration Technology Conference (ESTC), Tønsberg, Norway, 2020, pp. 1-5. doi: 10.1109/ESTC48849.2020.9229800.| Conference paper.

6. **Jian Li,** Vincent Henneken, Marcus Louwerse;, Ronald Dekker *Optical Data link Module for Data Transmission in Smart Catheters*, International Symposium on Microelectronics. International Microelectronics Assembly and Packaging Society, 2020.doi: 10.4071/2380-4505-2020.1.000169| Conference paper.

7. Shinnosuke Kawasaki, Jia–Jun Yeh, Marta Saccher, **Jian Li,** Ronald Dekker, *Bulk Acoustic Wave Based Mocrfluidic Particle Sorting with Capacitive Micromachined Ultrasonic Transducers*, 2022 IEEE 35th International Conference on Micro Electro Mechanical Systems Conference (MEMS), Tokyo, Japan, 2022, pp. 908-911, doi: 10.1109/MEMS51670.2022.9699807| Conference paper.

Curriculum Vitæ

Jian LI

1990	Born in Hebei, China.

Experience

2009–2013	Undergraduate in Microelectronics Tianjin University, Tianjin, China
2013–2015	MSc. in Microelectronics Delft University of Technology, Delft, The Netherlands
2015–2018	Process Engineer Else Kooi Lab, Delft University of Technology, Delft, The Netherlands
2018–2022	PhD. Delft University of Technology, Delft, The Netherlands Koninklijke Philips, Eindhoven, The Netherlands
2022– now	Application Engineer ASML, Eindhoven, The Netherlands