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Combined Fabrication and Performance Evaluation of TOPCon Back-Contact Solar Cells with Lateral Power Metal-Oxide-Semiconductor Field-Effect Transistors on a Single Substrate

David A. van Nijen, Tristan Stevens, Yavuzhan Mercimek, Guangtao Yang, René A.C.M.M. van Swaaij, Miro Zeman, Olindo Isabella, and Patrizio Manganiello*

Nowadays, an increasing share of photovoltaic (PV) systems makes use of module- or submodule-level power electronics (PE). Furthermore, PE is used in stand-alone devices powered by PV-storage solutions. One way to facilitate further implementation of PE in PV applications is to integrate PE components into crystalline silicon PV cells. Herein, the COSMOS device is introduced, denoting COmbined Solar cell and metal-oxide-semiconductor field-effect transistor (MOSFET). Specifically, the combined manufacturing of lateral power MOSFETs and interdigitated back contact solar cells with tunnel-oxide passivated contacts (TOPCon) on a single wafer is reported. Many steps of the proposed process flow are used for the fabrication of both devices, enabling cost-effective integration of the MOSFET. Both n-type solar cells with integrated p-channel MOSFETs (PMOS) and p-type solar cells with integrated n-channel MOSFETs (NMOS) are successfully manufactured. NMOS devices perform better in achieving low on-resistance, while PMOS devices exhibit lower leakage currents. Furthermore, the study reveals integration challenges where off-state leakage currents of the MOSFET can increase due to illumination and specific configurations of monolithic interconnections between the MOSFET and the solar cell. Nevertheless, for both n-type and p-type solar cells, efficiencies exceeding 20% are achieved, highlighting the potential of the proposed process for COSMOS devices.

1. Introduction

Power electronics (PE) plays a crucial role in optimizing the performance of photovoltaic (PV) systems. In traditional utility-scale PV systems, the PE is typically located in a central inverter.[1] This central inverter performs maximum power point tracking (MPPT) and connects the PV system to the electricity grid. Nowadays, module-level PE is being adopted in an increasing share of global PV installations, as such solutions offer improved safety capabilities, enhanced energy yield, and improved fault detection.[2] This is done by implementation of DC-DC power optimizers or micro-inverters, which can either replace or work together with traditional central PV inverters.[3] Furthermore, PE is successfully integrated at submodule level, with various topologies and strategies. For instance, one approach involves increasing the number of bypass diodes.[4,5] Nevertheless, this method introduces power losses when diodes are activated. To mitigate this, some publications suggest using transistors to perform bypass functions, resulting in reduced power losses during bypassing.[6–10] Beyond bypass diodes, various other topologies make use of submodule PE to create shade-tolerant PV modules. These include submodule MPPT topologies[11–13] and reconfiguration strategies for PV modules.[14,15] It is important to note that besides their role in full-sized cells and modules, PE components are also crucial in low-power, low-current PV applications. For instance, they enhance system efficiency and extend battery life in low-power autonomous devices using PV-battery combinations.[16] Another example is the Tessera module, where industrial cells are divided into smaller units and in-laminate low-current bypass diodes are employed.[17]

One way to facilitate further implementation of PE in PV applications is to integrate PE components into crystalline silicon (c-Si) PV cells.[18] This integration can take various forms, including the incorporation of PE components during the manufacturing process.[19–21] Another approach aims to exploit the inherent capacitive and inductive properties of solar cells.[22–24] On the one hand, the integration of PE components into PV cells includes challenges such as thermal management and repairability.[18] On the other hand, the integration approach includes several significant advantages. First, it reduces both the cost and the size of

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external power electronic devices. This would pave the way toward small-area system-on-chip solutions that can be laminated in any place of the PV module to enable granular power optimization. Additionally, the reduction in volume and weight can be especially advantageous for specific applications, such as space-based systems, where silicon PV technology already plays an important role.[25] Moreover, the monolithic integration of PE components can enhance system reliability. This is because failure in the solder joints of discrete power transistors has been identified as a major cause of power converter failures in PV applications.[26,27]

This article focuses on the integration of transistors into PV cells. Transistors are crucial for power converters as well as reconfigurable modules and can act as bypass elements with low parasitic power dissipation. Previously, researchers proposed a fabrication process integrating metal-oxide-semiconductor field-effect transistors (MOSFETs) and capacitors with front-back contacted PV cells.[21,28,29] Although they made some innovative steps toward cell-embedded power converters, the PV cell structure has some intrinsic limitations to reaching a high efficiency, which are for instance the nontextured front side and an aluminum plate covering the full back-side of the device. In this current work, we introduce the COSMOS device, denoting COmbined Solar cell and MOSFET. Specifically, we report the simultaneous manufacturing of lateral power MOSFETs and interdigitated back contact (IBC) c-Si solar cells with ion-implanted poly-Si passivating contacts on a single c-Si substrate. The adoption of the tunnel oxide passivated contact (TOPCon) cell architecture ensures that the solar cell can attain state-of-the-art efficiencies. TOPCon technology in front/back-contacted architectures has yielded state-of-the art solar cell efficiencies of 26.4% on n-type wafers and 26.0% on p-type wafers.[30,31] Furthermore, a 26.1% efficiency has been demonstrated in an IBC structure.[32] Although the term TOPCon is commonly used, tunneling through the oxide is not the only current transport mechanism.[33] Thus, the same structure is regularly referred to with the term polycrystalline silicon on oxide (POLO). In the proposed process flow for COSMOS devices, a substantial number of processing steps are common to both devices, promoting cost-effective integration of the MOSFET. It is worth highlighting that the proposed device structure places all contacts of both the solar cell and the MOSFET on the back side of the wafer. This offers design flexibility in terms of the number of transistors and the series or parallel interconnection schemes that may be required for different applications. The devices are characterized in both dark and illuminated conditions, and based on these results, we reflect on the remaining challenges for real-world implementation. Additionally, we investigate how the performance of the MOSFET is influenced when its drain or source has a direct monolithic connection to the solar cell.

2. Experimental Section

This section describes the experimental methodology employed in this study. Section 2.1 outlines the process flow for COSMOS devices, in which solar cells and MOSFETs are fabricated on the same substrate in a single combined process. Subsequently, Section 2.2 describes some practical manufacturing limitations along with some trade-offs inherent to the combined fabrication. In this study, both n-type and p-type double-polished float-zone wafers are used with a thickness of 285 μm, and having <100> orientation and resistivity of 1–5 Ωcm. The photolithographic patterning steps are executed using the soft contact method with a SUSS MicroTec MA/BA8 mask aligner. Although this method allows for UV patterning at once for the full area of the wafer, it offers limited resolution, typically above 1 μm, as compared to image-projection photolithography.[34,35]

2.1. COSMOS Process Flow and Wafer Layout

The process flow used for the fabrication of the COSMOS device is schematically represented in **Figure 1**. This figure shows the fabrication process using a p-type wafer, resulting in p-TOPCon devices and n-channel MOSFETs. The same process can be dually applied to n-type wafers, resulting in the creation of n-TOPCon devices and p-channel MOSFETs (PMOS). Both options were fabricated in this study. In the following part, a description is given outlining the different process steps in Figure 1. These ten different steps are identified by Roman numerals. Some of them incorporate lithographic steps, which are indicated by labels ranging from P1 to P6. The different stages involved in the COSMOS process are as follows: I) The first step is to form a 54 nm-thick SiO_2 layer through thermal oxidation. This layer will eventually become the gate oxide, meaning that it must be sufficiently thick to insulate the substrate from the gate metal. Subsequently, using a patterning step (P1) and buffered HF solution (BHF), this oxide is selectively removed in the area where the solar cell will be located. II) The native oxide is removed by a dip in HF, where it is worth noting that this also slightly etches the gate oxide, which reaches a thickness of ≈40 nm. Directly after, a ≈1.5 nm-thick SiO_2 layer is formed by the method of nitric acid oxidation of silicon (NAOS).[36] III) A 250 nm-thick intrinsic amorphous silicon (i-a-Si) layer is deposited using low-pressure chemical vapor deposition. IV) The poly-Si on the front side is removed by a wet poly-etch solution that has an etch rate of 200–-300 nm min^{-1}. Subsequently, the front side of the wafer is textured using a TMAH solution. V) A patterning step (P2) is used to selectively remove the poly-Si on the back side. This has a double purpose. First, a trench is created in the PV area between the emitter and BSF region. Second, in the MOSFET area the gate structure is created. It is worth noting that this etching step has been done in two different ways, namely i) a wet poly-etch using plasma-enhanced chemical vapour deposition (PECVD) SiO_x as a mask, and ii) reactive ion etching (RIE) using photoresist as a mask. Subsequently, for both these methods, a BHF etching step removes the oxide that remains in the MOSFET region underneath the etched poly-Si. VI) Using photoresist as a mask (P3), an implantation is performed to simultaneously create i) the emitter region of the solar cell and ii) the gate, source, and drain region of the MOSFET. VII) Using photoresist as a mask (P4), an implantation is performed to simultaneously create i) the back-surface field (BSF) region of the solar cell and ii) the doped region underneath the grounding contact of the MOSFET. Subsequently, a 5 min thermal anneal is performed at 950 °C to drive-in and activate the dopants. VIII) An HF dip is performed to remove the native oxide. Subsequently, a 5 nm-thick i-a-Si:H/60 nm-thick SiN_x:H stack is deposited through PECVD on the front side for passivation and antireflection. Furthermore, a 100 nm-thick SiN_x:H PECVD layer is

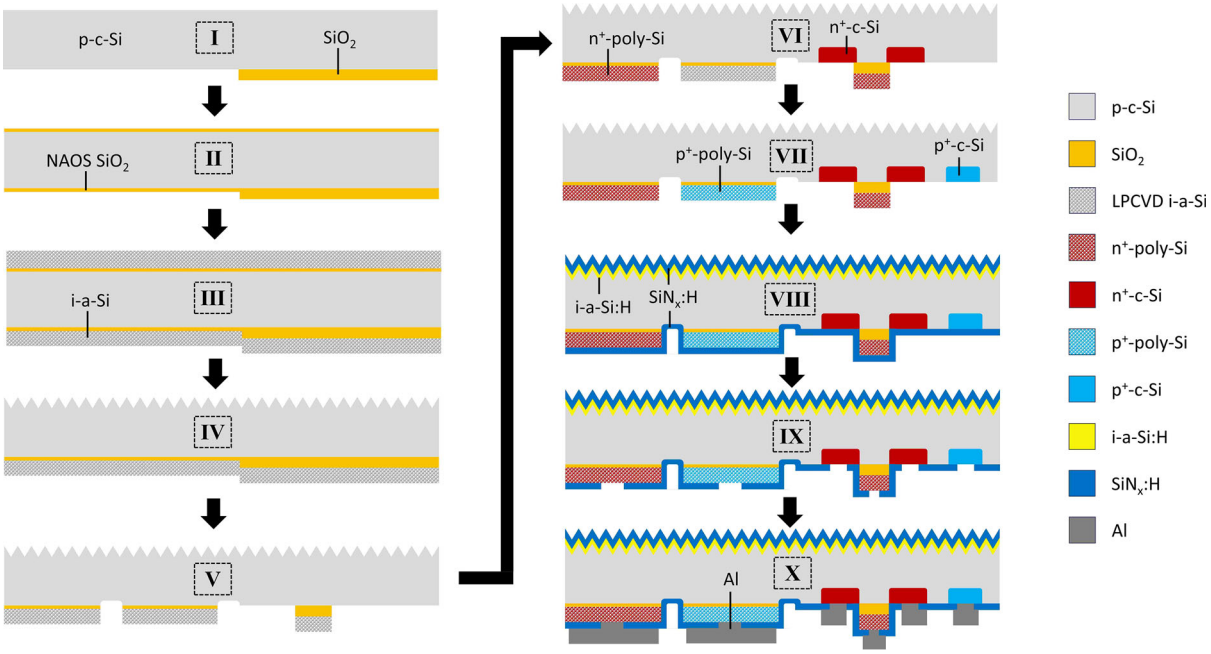

Figure 1. Combined solar cell and MOSFET (COSMOS) process flow.

deposited on the back side. IX) Using photoresist as a mask (P5), openings are created in the SiN_x:H layer on the backside through wet etching in BHF. X) Lift-off is used to form the back side metal pattern with a 2 µm-thick evaporated Al layer (P6). This may be followed by a hotplate annealing step at 350 °C for 5 min.

A more extensive background on the process flow is provided in the Section S1, Supporting Information. Section S1.1, Supporting Information, offers additional context regarding the reference solar cell manufacturing, which is based on previous publications on IBC solar cells with ion-implanted poly-Si passivating contacts.[36–38] Additionally, Section S1.2, Supporting Information, offers close-up views of the photomasks with labels between P1 and P6, allowing correlation with the lithographic steps described previously. Furthermore, more detailed information outlining the precise conditions employed for the processing steps of the COSMOS device is provided in Section S1.3, Supporting Information.

Step I of the COSMOS process requires the formation of a local gate oxide to successfully manufacture the MOSFETs. This is the main step that applies uniquely to the MOSFET and does not benefit the solar cell. However, it is worth noting that the corresponding lithographic step can directly be used to create alignment markers on the wafer. Thus, when comparing the combined process flow in this section to the reference solar cell manufacturing, they exhibit an equal number of photolithographic patterning steps. As such, compared to the solar-cell manufacturing, the COSMOS process requires only a very limited number of additional fabrication steps, allowing for cost-effective integration of the MOSFET.

Furthermore, it is worth discussing some aspects related to the MOSFET manufacturing. The employed COSMOS fabrication method consists of a so-called gate-first process, in which the gate structure is crafted before the source/drain regions. This is in contrast to the gate-last process, which follows the opposite sequence. One notable advantage of the gate-first approach is its self-aligned nature, which means that the entire poly-Si gate region, including the source and drain regions, is implanted simultaneously. As poly-Si is being doped, the SiO_2-poly-Si structure simultaneously serves as a natural mask to protect the channel region during implantation. Consequently, this allows for only a small overlap between the source and drain regions with the gate structure compared to the gate-last method, where mask design misalignment tolerances necessitate greater overlap. Additionally, when the gate-last method would be used for integrating a MOSFET into a solar cell, thermal oxidation might not be the preferred method due to its potential impact on the solar cell passivation. Therefore, a deposited gate dielectric could be considered as a viable solution within the gate-last method. However, this approach might require additional fabrication steps, or would involve a trade-off between meeting the solar cell requirement for excellent passivation and the gate necessity for a dense material with high dielectric breakdown strength.

The final wafer layout is depicted in **Figure 2**. This wafer contains ten solar cells, with four of them being monolithically integrated with a MOSFET. This monolithic integration implies that either the source or drain contact of the MOSFET has a direct connection to one of the solar cell contacts. Additionally, on the bottom two rows of the wafer, there are fourteen MOSFETs present with varying geometries.

2.2. Manufacturing Limitations and Trade-Offs

For achieving optimum MOSFET performance, utilizing a MOSFET with a small gate length is advantageous. For instance, a small gate length leads to a lower channel resistance in the

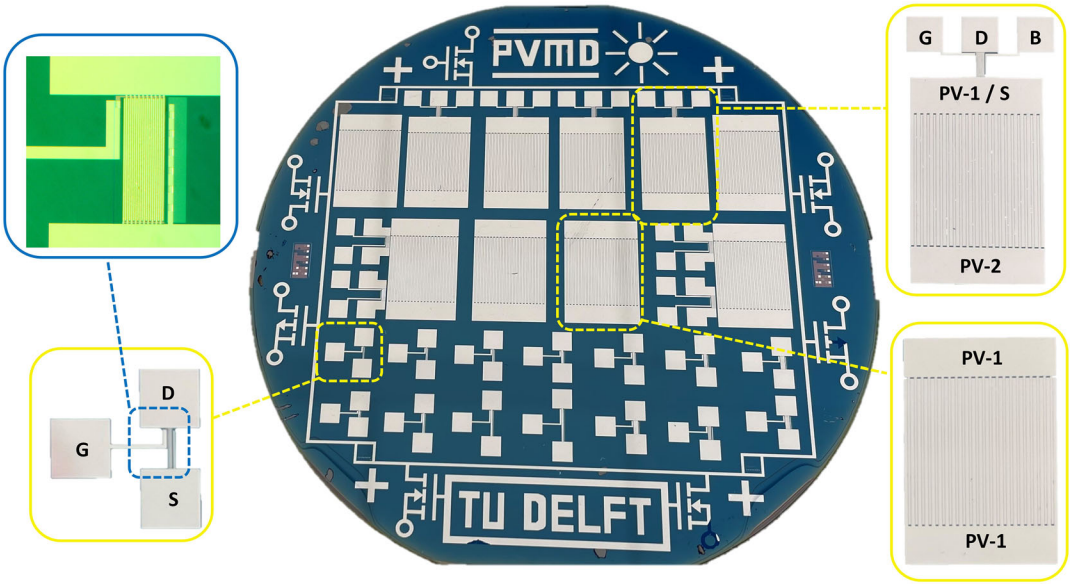

Figure 2. Final wafer layout. The source, drain, body, and gate contact pads of the MOSFETs are labeled as S, D, B, and G, respectively. For the individual MOSFET structures on the bottom two rows, there is no separate body contact, since the body is shorted to the source. Additionally, the contact pads for the IBC solar cells are marked as PV-1 and PV-2. In the top right, a structure is highlighted where the solar cell and MOSFET are monolithically integrated. For the MOSFETs with such monolithic interconnections, the source has a direct connection to the PV contact. Additionally, the body has an independent contact pad (B) and is not shorted to the source. This configuration allows for the interchange of source and drain contacts.

on-state, as will be explained further in Section 3.3. During fabrication performed preliminary to this work, it was observed that with the employed contact photolithography method, gate lengths as small as 4 μm could be reliably transferred onto the photoresist while maintaining the desired pattern. For masks with even smaller gate lengths, instances were noted where portions of the gate structure were not accurately transferred. This occurrence is likely attributed to diffraction effects at the edges of the mask features during the exposure process.[39] As a result, all MOSFETs presented in this study maintain a consistent gate length of 4 μm. Nevertheless, it is important to highlight that a substantial reduction in gate length could be realized through the utilization of the more advanced method of image projection photolithography, using an optical lens between the mask and the wafer.[34] However, such a reduction would bring its own challenges. For instance, an obstacle could arise in patterning the SiO_2-poly-Si gate structure during step P2, where different wafers are subjected to either wet or dry etching of poly-Si. In **Figure 3**, a microscope picture is presented of the gate structure after the etching step. It becomes apparent that in the case of wet etching, there is significant undercutting of the mask, effectively reducing the gate length. Since in this work a rather large gate length of 4 μm is employed, the wet etching's undercutting impact was tolerable. On the one hand, for gate length downscaling, the

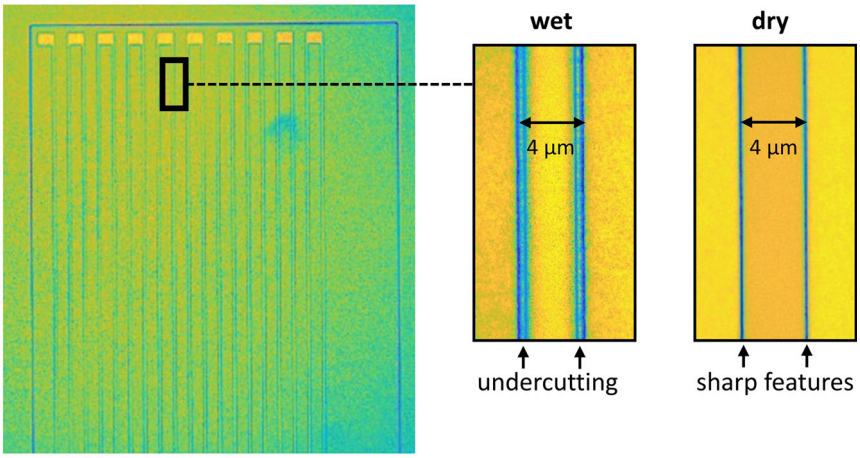

Figure 3. Microscope picture of the SiO_2-poly-Si gate structure after two minutes of wet etching and after dry etching, which is at the end of step V in Figure 1. The poly-Si wet etchant has an etching rate of 200–300 nm min^{-1}, resulting in up to ≈500 nm of undercutting on both sides of the gate structure after two minutes of etching. This figure demonstrates that dry etching produces sharper features with less undercutting.

Table 1. Poly-Si etching details used for the different wafers in this study. N-D and N-W represent n-type wafers subjected to dry and wet poly-Si etching, respectively. P-D and P-W denote p-type wafers undergoing dry and wet poly-Si etching, respectively.

	n-type wafer dry etching (N-D)			n-type wafer wet etching (N-W)					p-type wafer dry etching (P-D)	p-type wafer wet etching (P-W)		
	1	2	3	1	2	3	4	5	1	2	3	5
Etching time	–	–	–	1 m 20 s	1 m 40 s	2 m	2 m 30	3 m	–	1:40	2 m	3 m

enhanced control of dry etching might be essential. Indeed, low-temperature dry etching is the preferred method for transistor fabrication, since it allows for high-resolution pattern transfer to the underlying layer with less undercutting than for wet etching steps.[39] On the other hand, RIE has been reported to lead to reduced passivation quality in solar cells.[40,41] For solar cells, etching methods such as wet etching and atmospheric pressure etching are preferred.[41,42] Thus, the choice between wet and dry etching of the poly-Si is a trade-off that is studied in this work. Specifically, the wafers in this work are split up between different etching method and times. For the COSMOS devices manufactured in this study, the variations in the poly-Si etching process are presented in **Table 1**.

Another challenging factor linked to the pursuit of gate length reduction is the high-temperature thermal annealing during step VII of the COSMOS process, as detailed in Section 2.1. This step serves to drive-in and activate the dopants, meaning that the implanted atoms diffuse through the lattice. However, maintaining adequate spacing between the source and drain regions on either side of the channel becomes crucial. Limited spacing risks source-drain shorting or punch-through effects, discussed further in Section 3.2. While this specific annealing step did not induce these effects in this study, extensive gate length downscaling could necessitate reoptimization of the annealing process to align with the thermal budget of the MOSFET.

Furthermore, a notable trade-off was observed during the fabrication process of COSMOS devices. In the final step, specifically during step X outlined in Section 2.1, a hotplate annealing procedure can be conducted. This step proved vital for stable MOSFET performance, as elaborated in Section 4.1. Interestingly, it slightly improved the STC efficiencies for n-type solar cells, but had a detrimental effect on p-type cells. This example highlights a trade-off where a specific step enhances MOSFET performance but diminishes PV performance. Though optimization was not pursued within the scope of this work, such steps would ideally require a refined fabrication approach that carefully manages this trade-off.

3. Theoretical Background

This section describes some fundamental MOSFET parameters. Furthermore, it is discussed how the desired parameters are achieved, and the inherent limitations that arise from the chosen design are explained. Further theoretical explanations and equations underlying this section are provided in the Section S2, Supporting Information.

3.1. Threshold Voltage

The threshold voltage V_T is an important characteristic of a MOSFET, representing the gate-to-source voltage V_{GS} at which a conductive channel forms beneath the gate. Through deliberate design, a particular V_T can be achieved for a given device. It is important to realize that in the case of an n-channel MOSFET (NMOS) on a p-type substrate, the device is off when $V_{GS} < V_{TN}$, and the device is on when $V_{GS} > V_{TN}$. In the case of a p-channel MOSFET (PMOS) on an n-type substrate, the device is off when $V_{GS} > V_{TP}$, and the device is on when $V_{GS} < V_{TP}$. The threshold voltage of a MOSFET is primarily influenced by parameters such as the substrate dopant density, charge trapped around the oxide–semiconductor interface, oxide thickness, and the specific choice of gate metal, resulting in a particular metal-semiconductor work function difference. While MOSFETs are typically engineered to possess specific threshold voltages, our approach in this study diverges from convention. The central focus here is the integration of the MOSFET with minimal processing steps. The devices fabricated in this study are placed directly onto the wafer bulk, allowing for simple integration with PV cells. This encompasses both NMOS devices on p-type substrates and PMOS devices on n-type substrates. While in solar cells there is a certain flexibility in the choice of substrate dopant density,[24] it is important to acknowledge that for COSMOS devices the choice of substrate has an important effect on certain transistor characteristics, such as the threshold voltage. To achieve better control over the MOSFET characteristics, techniques like epitaxial layer growth or localized doping adjustments through implantation could be considered. However, at this stage of the study, such steps were not included.

3.2. Blocking Capability

Another important characteristic of a power MOSFET is the blocking capability, which is the extent to which the MOSFET is able to block the voltage between drain and source. This characteristic comprises two primary aspects.

First, during the device's off-state, it is crucial for the MOSFET to exhibit low drain leakage current or subthreshold conduction. Lower leakage currents lead to reduced losses, increasing overall efficiency. An important mechanism that can be responsible for drain leakage current in the off-state is band-to-band tunneling in the gate-to-drain overlap region.[43,44] In addition to this, it has been reported that traps around the Si-SiO_2 interface induce further leakage currents.[45]

Second, any MOSFET is susceptible to a drain-to-source breakdown beyond a specific applied drain-to-source voltage V_{DS}. The voltage at which this occurs is called the breakdown voltage V_B, and has a direct impact on its prospective applications within a PV panel. Given that the voltage of a PV cell string scales linearly with the quantity of series-connected cells, the MOSFET breakdown voltage imposes a restriction on the number of series-connected cells that the device can effectively manage. There

are various mechanisms that can cause breakdown in a MOSFET once a certain V_B is exceeded, among which are dielectric breakdown, avalanche breakdown, or punch-through breakdown. Which mechanism is limiting depends on the specific device design. It is important to acknowledge that the chosen MOSFET design in the COSMOS devices has limitations in achieving a high breakdown voltage. First, there is an overlap between the gate plate and drain region, which means that the onset of avalanche breakdown happens at a lower voltage.[46] Moreover, to avoid the occurrence of avalanche breakdown, it becomes imperative to utilize a substrate dopant density that is sufficiently low. Nonetheless, within the context of the utilized MOSFET design, such an approach can give rise to punch-through breakdown, necessitating the imposition of a minimum channel length. In contrast, specific power MOSFET designs do not have overlap between the gate plate and drain region and they manage to circumvent the trade-off between V_B and channel length.[47] However, this comes at the cost of an increase in the number of fabrication steps, which is not aligned with the objectives of this work. Nevertheless, the limited maximum V_B of the MOSFETs does not prohibit usage in applications with constrained voltage requirements. For example, integration into PV modules at the submodule level could remain a viable option, particularly when controlling only a limited number of series-connected cells.

3.3. On-Resistance

An important characteristic of a power transistor is its resistance in the on-state, commonly referred to as the on-resistance R_{on}. Presence of any parasitic resistance in the on-state leads to ohmic losses during operation, meaning that the R_{on} should be as low as possible for maximum efficiency. The primary contributor to R_{on} is often the channel resistance. In the linear operational region, the channel resistance R_{CH} of an NMOS can be expressed as shown in ref. [48]:

$$R_{CH} = \frac{L}{W\mu_n C_{ox}(V_{GS} - V_{TN})} \tag{1}$$

where L denotes the channel length, W is the channel width, and μ_n represents the electron channel mobility. In contrast to the threshold voltage and blocking capability, the control over R_{on} is achieved through mask design within the scope of this work. Furthermore, it is worth mentioning that the mobility in silicon is almost three times higher for electrons than for holes.[48] Consequently, an NMOS with equal geometry when compared to a PMOS will yield a lower R_{CH}, which often makes NMOS devices the preferred choice for power applications.

Although Equation (1) shows an inverse relationship between the device width and R_{CH}, it is important to acknowledge that there can be nonideal effects at play in power MOSFETs. One notable effect is the increasing prominence of power dissipation within metal fingers and interconnections as device width increases, which is an aspect referred to as the scaling issue.[49] To reduce losses due to the scaling issue, lateral power MOSFETs often employ a design that incorporates multiple source-drain couples in parallel, sharing a common gate.[21,47] In the context of the current study, devices are fabricated with varying widths and different numbers of parallel source-drain couples (n_{SD}), allowing for an analysis and quantification of the scaling effect. Specifically, for the devices manufactured in this study, n_{SD} was varied between 1 and 10, the W between 1 and 5 mm, and L was fixed at 4 μm. This approach allows to find the most efficient way to reduce R_{on} in the COSMOS devices.

4. Results and Discussion

This section presents the results that were obtained for the manufactured COSMOS devices. Initially, Section 4.1 exhibits the outcomes of the fabricated MOSFETs. The transistors are characterized using a Cascade Summit 12 000 probe station connected to a Keysight B1500A Semiconductor Parameter Analyzer. Subsequently, in Section 4.2, the solar cell results are detailed. The current-density voltage (J–V) characteristics of the solar cells are measured using a continuous solar simulator (Wacom WXS-156S AAA). The solar cells, which have areas varying between 1.22 and 1.29 cm^2, are exposed through masks that feature 1 cm × 1 cm apertures in the solar cell regions. Finally, in Section 4.3, the challenges related to achieving effective device performance for successful integration are explored.

4.1. MOSFETs

An annealing step after the metallization is known to lead to the alteration of the localized states near the Si-SiO_2 interface.[50,51] In the manufactured NMOS and PMOS devices, such a step resulted in more stable threshold voltages and enhanced charge carrier mobility within the channel. Thus, all MOSFET results presented in this study are for wafers that underwent a hotplate annealing step at 350 °C for 5 min. More information on the performed hotplate annealing experiments and its effect on the charge trapped at the oxide-semiconductor interface are given in the Section S3, Supporting Information.

First, the leakage currents of the manufactured MOSFETs were tested, and the I_D–V_{GS} characteristics of selected NMOS and PMOS devices are presented in **Figure 4**. Since the vertical axis shows I_D on a logarithmic scale, it allows for a detailed analysis of the leakage currents. First, it is important to analyze the shape of the curves in the off-state, which is for V_{GS} below V_{TN} of the NMOS devices in Figure 4a, and for V_{GS} above V_{TP} of the PMOS devices in Figure 4b. For all devices, it is evident that as the device is biased deeper into the off-state, the leakage increases. This phenomenon has been reported in literature and is attributed to tunneling effects at the Si-SiO_2 interface in the gate-to-drain overlap region, which are sensitive to the electric field created by the applied V_{GS}.[43] Furthermore, Figure 4 illustrates that there can be variations in drain leakage current among devices placed on the same wafer. These differences cannot be attributed to the varying n_{SD}. Instead, they might be caused by variations in traps near the Si-SiO_2 interface between different devices. Indeed, publications suggest that that traps near the Si-SiO_2 interface significantly contribute to leakage, caused by effects such as interface trap-assisted tunneling and thermal generation current described by Shockley–Read–Hall theory.[45,52] In general, upon analyzing the drain leakage current of the devices across the different wafers, it can be concluded that the off-state drain leakage currents for the manufactured PMOS

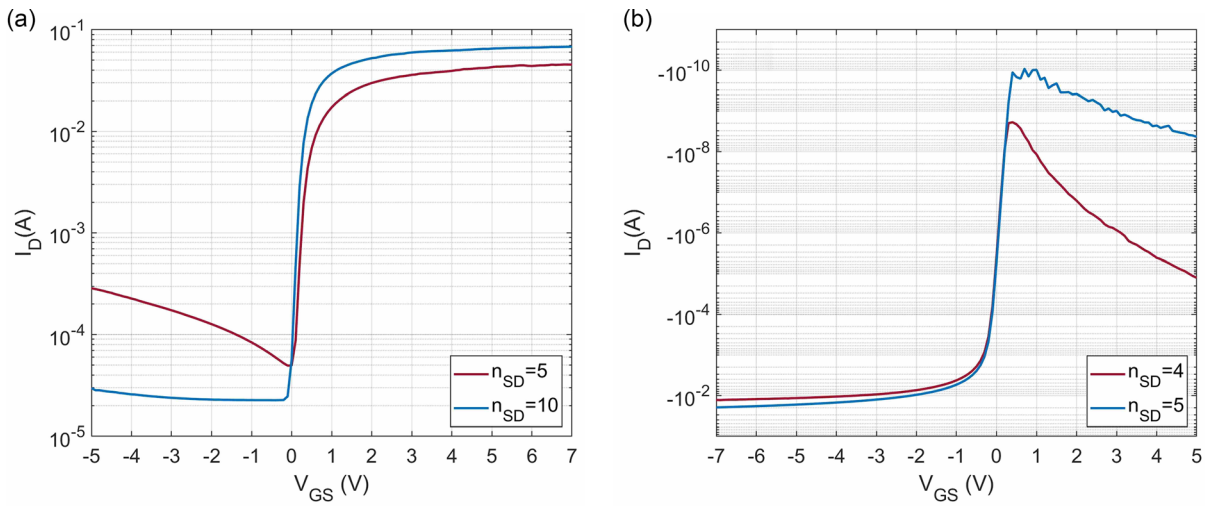

Figure 4. a) I_D–V_{GS} curves of two NMOS devices on wafer P-W-2 with $W = 2$ mm recorded at $V_{DS} = 0.1$ V . b) I_D–V_{GS} curves of two PMOS devices on wafer N-W-1 with $W = 2$ mm recorded at $V_{DS} = -0.1$ V .

devices are notably lower than those for the NMOS devices. In this study, relatively well-performing NMOS devices have a leakage current of approximately $\approx 2 \times 10^{-5}$ A at $V_{DS} = 0.1$ V, whereas the PMOS devices display leakage currents of around $\approx 1 \times 10^{-10}$ A at $V_{DS} = -0.1$ V, which is a remarkable factor of 2×10^5 lower. This disparity between NMOS and PMOS leakage current is not yet fully understood and can have different reasons. For instance, it could be related to the more graded boron doping concentration of PMOS devices near the drain-to-substrate junction compared to phosphorus doping concentration in NMOS devices, which may reduce band-to-band tunneling effects.[53] Additionally, variations in trap concentration at the Si-SiO_2 interface between n-type and p-type wafers might contribute to the observed difference. Although not further explored in this work, it is expected that optimization of the implantation and thermal annealing steps during the fabrication process could lead to more stable leakage currents across different devices on the same wafer and reduce the NMOS leakage currents to levels comparable to those of the manufactured PMOS devices.

Regarding breakdown voltage V_B, an analysis was conducted to determine the maximum V_{DS} voltage that NMOS and PMOS devices could withstand before reaching the point of breakdown. A stepwise increase in V_{DS} was executed to identify the specific V_B value at which I_D began to rise sharply. Frequently, the devices experienced irreversible breakdown when pushed to their limits. **Figure 5** illustrates I_D–V_{DS} curves for different V_{GS} values both before and after breakdown. It is evident that the NMOS device can tolerate V_{DS} up to 9 V, while the PMOS can endure a V_{DS} of 6 V prior to breakdown. Following the catastrophic breakdown, the V_B values of both devices are compromised,

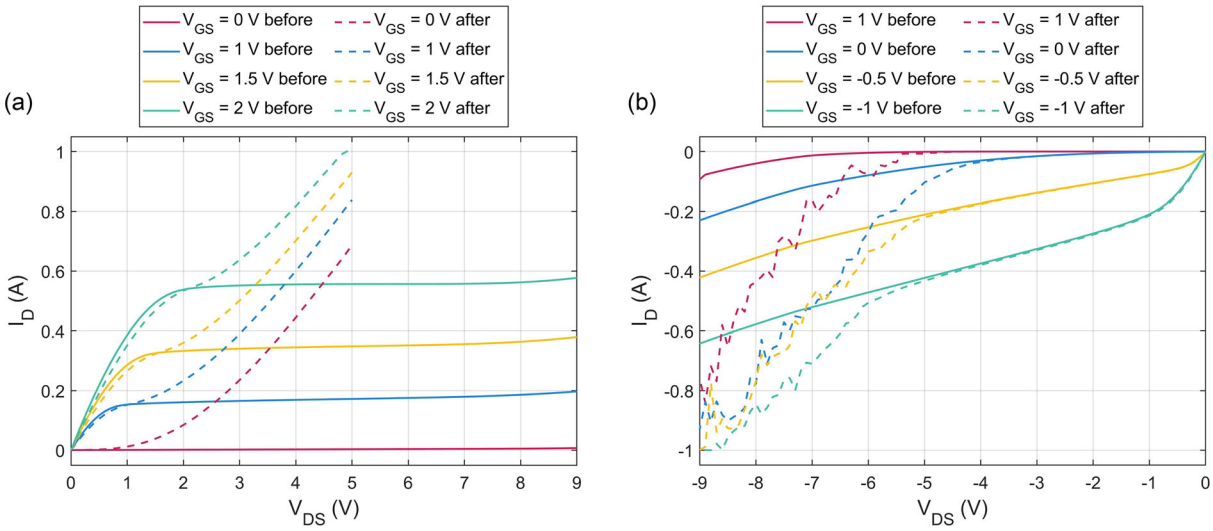

Figure 5. I_D–V_{DS} curves for varying V_{GS} values before and after irreversible breakdown. In a) an NMOS device from wafer P-D-1 is presented, whereas the PMOS device shown in b) is from wafer N-W-5. Both the NMOS and PMOS have an $n_{SD} = 10$ and $W = 2$ mm device structure.

dropping to −1 and −5 V, respectively. The irreversible nature of the observed breakdown makes it plausible that a form of dielectric breakdown occurred. Typically, the V_B value was observed in the range of an applied V_{DS} between 5 and 10 V. It is worth noting that in several of the manufactured MOSFETs, the breakdown behavior was already apparent immediately after the manufacturing process, suggesting the possibility of defects that might have developed within the oxide during fabrication. The breakdown voltage V_B of COSMOS MOSFETs could potentially be elevated by adopting a higher quality or thicker gate oxide, until a point where punch-through or avalanche effects set a constraint on the breakdown effect.

Furthermore, as previously discussed in Section 3.3, the on-resistance R_{on} can be manipulated through various design-oriented MOSFET parameters. This has been examined by comparing the R_{on} of manufactured PMOS devices with different geometries, as depicted in **Figure 6**. To quantify R_{on}, we calculate its values based on the slope of the I_D–V_{DS} curve, specifically within the voltage range of 0–0.1 V at a fixed V_{GS} of −8 V. It is important to note that all the data points in this figure pertain to the same wafer, namely N-W-3 from Table 1. In Figure 6a, the impact of width (W) on R_{on} is presented. According to the theoretical relationship defined by Equation (1), R_{on} is expected to exhibit an inverse relationship with W. However, the experimentally obtained R_{on} values deviate somewhat from this ideal relationship. Thus, the experimental results are compared with an ideal curve that assumes R_{on} follows a W^{-1} relationship starting from $W = 1$ mm. This comparison highlights that as W increases, the experimental R_{on} values decrease at a rate that is less steep than the ideal prediction. This implies that there is an increase in on-resistance per unit of added width. This phenomenon is likely attributed to the presence of nonzero resistance within the metal contacts of the source and drain, a concept described earlier in this study as the scaling issue. Another strategy for reducing the R_{on} involves manufacturing MOSFETs with a common gate, but with multiple source/drain couples in parallel (n_{SD}). Figure 6b illustrates the effect of n_{SD} on R_{on}. In addition, an ideal relationship is provided based on the assumption that R_{on} decreases linearly with the number of parallel channels in the device, using $n_{SD} = 2$ as the starting point. In this case, the experimental results closely align with the expectations derived from this ideal relationship, particularly when compared to Figure 6a. This shows that increasing the number of source-drain couples can be a more effective strategy for reducing R_{on} than increasing W. Furthermore, there appears to be room for further reduction in R_{on} by elevating n_{SD}. By employing devices with $n_{SD} = 10$ and $W = 2000$ µm, this study achieved on-resistances of 1.01 Ω for an NMOS device at $V_{GS} = 10$ V and 1.29 Ω for a PMOS device at $V_{GS} = -10$ V. The lower R_{on} values in NMOS devices compared to PMOS devices can be attributed to the higher electron mobility compared to hole mobility.

4.2. Solar Cells

The outcomes of the COSMOS solar cells are depicted in **Figure 7**. Different colors are allocated for p-type and n-type cells, as well as for wet and dry etching of poly-Si. Each wafer is identified on the horizontal axis using labels that correspond to those in Table 1. The outcomes for n-type cells are presented post hotplate annealing, while the results for p-type cells are shown prior to annealing. This distinction is due to the negative impact of hotplate annealing on the V_{OC} of p-type cells that was observed. Notably, the figure's boxplots only include functional cells on the wafer, excluding nonoperational cells from the analysis. Additionally, it is important to acknowledge that the J–V curves of the fabricated cells often displayed unexpected irregularities or kinks in the low forward bias voltage region. This can be observed in the J–V curves presented in **Figure 8**. The exact cause of these kinks remains unclear. They might be associated with capacitive effects that somehow influence the measurements, shunting between n- and p-type fingers, or it is possible that the current distribution within the solar cell varies with the operating voltage.

In Figure 7, it can be seen that the COSMOS solar cells manufactured in this study yield STC efficiencies ranging between

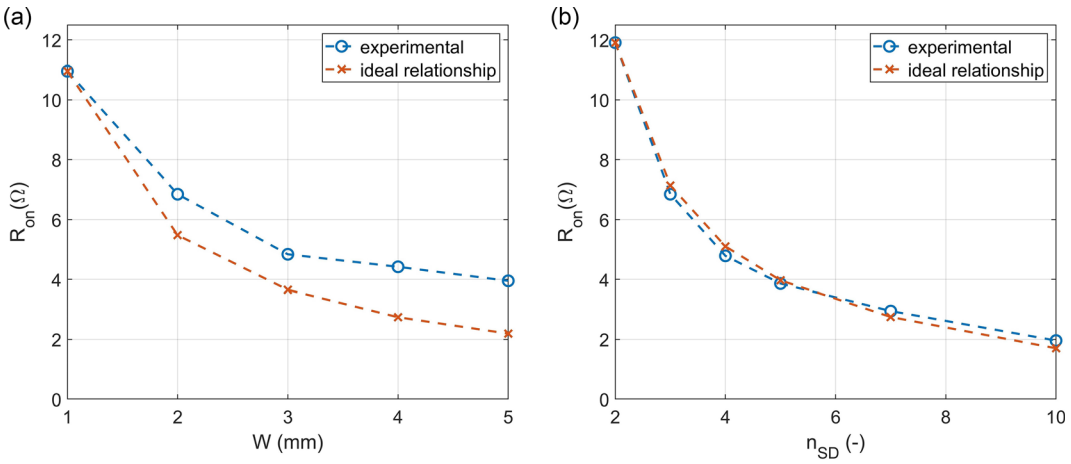

Figure 6. On-resistance for PMOS devices on a wet-etched wafer (N-W-3). The experimental R_{on} values are calculated from the slope of the I_D–V_{DS} measurement between 0 and 0.1 V at $V_{GS} = -8$ V. For a), all devices have an $n_{SD} = 3$, while W is varied. The ideal relationship is based on the assumption that from $W = 1$ mm, R_{on} follows a W^{-1} relationship based on Equation (1). For b), all devices have a $W = 2$ mm, while n_{SD} is varied. The ideal relationship is based on the assumption that R_{on} scales inversely with the number of parallel channels in the device, with $n_{SD} = 2$ as a starting point.

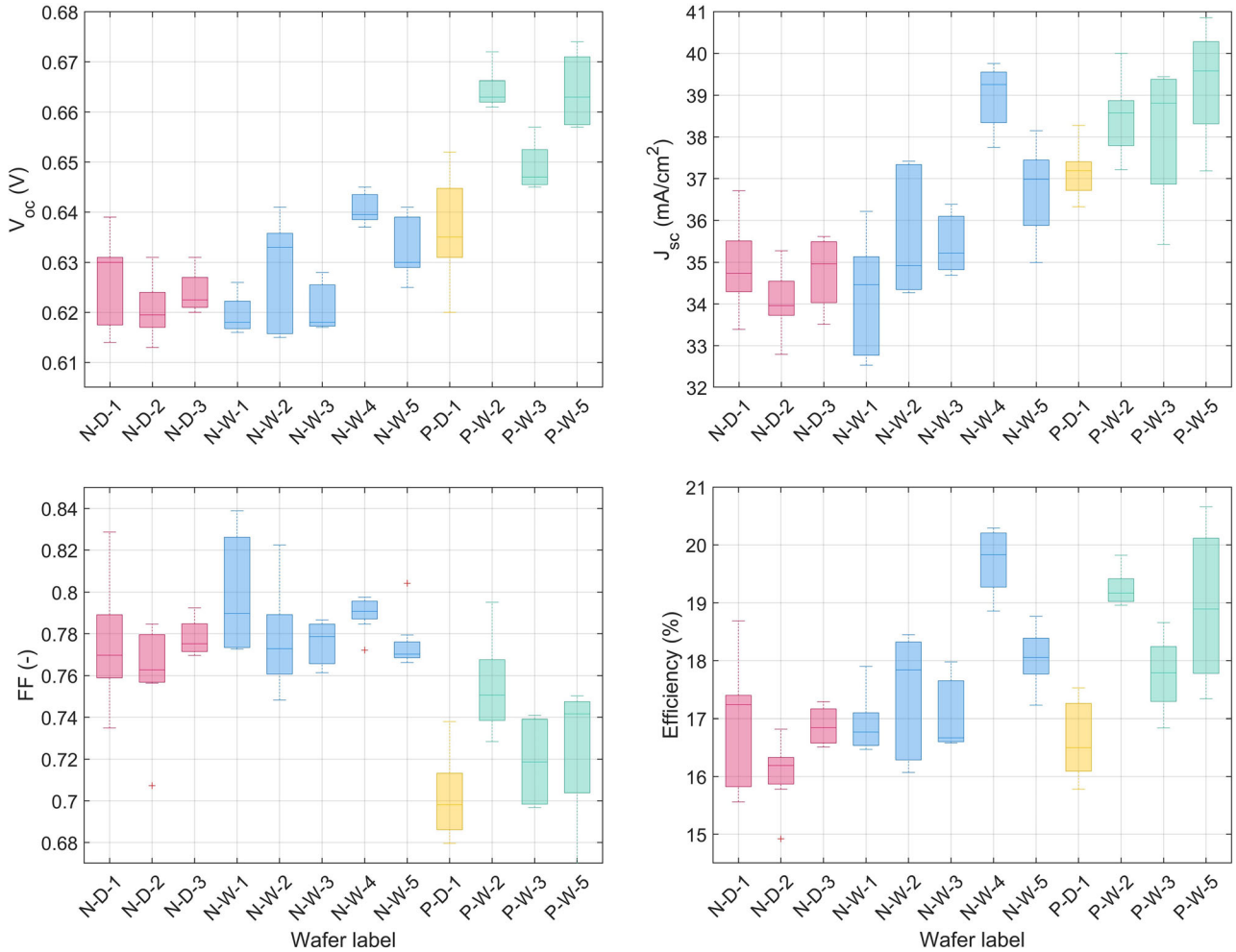

Figure 7. Overview of the solar cell performance in STC conditions across the various wafers. Included in the analysis are the open-circuit voltage (V_{OC}), the short-circuit current (J_{SC}), the fill factor (FF), and the conversion efficiency. The results for the n-type solar cells are recorded after hotplate annealing, whereas the results for the p-type solar cells do not include this step.

approximately 16% and 20%. It is shown that for both p-type and n-type cells, wet etching yields superior efficiencies compared to dry etching. This enhanced efficiency mainly stems from improvements in V_{OC} and J_{SC}. Prior research has also highlighted that RIE can compromise passivation quality,[40,41] aligning with our findings. Although our results underscore the preference for wet etching to achieve optimal solar cell performance, it is important to consider some nuances. First, the utilized dry etching equipment is a shared tool employed for various processes unrelated to solar-cell manufacturing. Hence, the observed drop in passivation quality might not be inherent to the dry etching process itself, but rather a consequence of the specific tool employed. Second, it is important to note that strategies exist for repassivation after RIE.[54] However, within the scope of this study, no such repassivation techniques were explored.

Furthermore, it is worth comparing between the outcomes of n-type and p-type solar cells. The results unveil that n-type wafers exhibit lower V_{OC} values than their p-type counterparts. Conversely, n-type solar cells show higher fill factor values compared to p-type counterparts. Although there is variation in efficiencies across different wafers, the achieved efficiencies for both n-type and p-type solar cells are within a similar range. The best J–V curves for n-type and p-type solar cells within this study are illustrated in Figure 8, having efficiencies of 20.29% and 20.66%, respectively. Increasing the V_{OC} values by further optimization in passivation holds the potential to push the efficiency of the COSMOS solar cells closer to that of state-of-the-art TOPCon solar cells. Nevertheless, the achieved efficiencies exceeding 20% demonstrate the potential of the proposed process for COSMOS devices.

4.3. Integration Challenges

The preceding sections examined the individual performance of MOSFETs and solar cells, each under different conditions—MOSFETs under dark conditions and solar cells under illuminated conditions. Nonetheless, given that the COSMOS approach integrates these devices onto a single substrate, additional

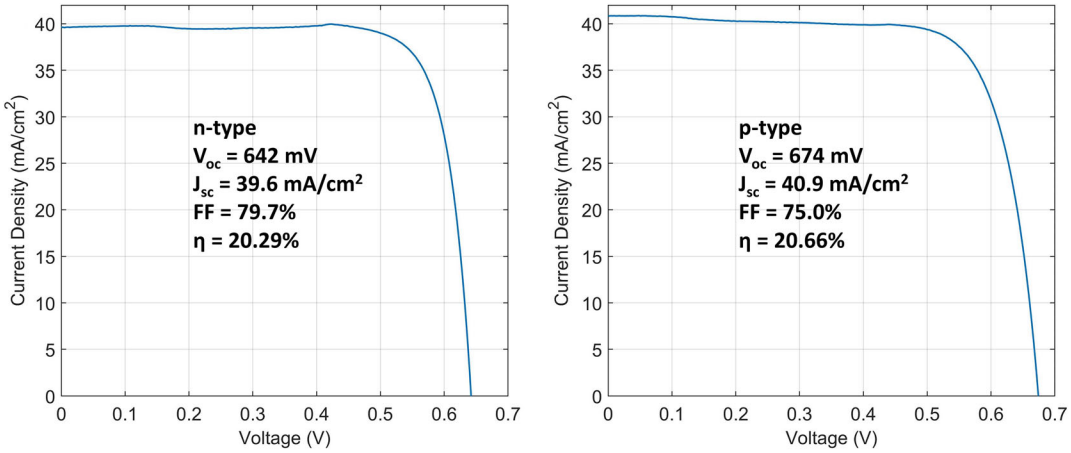

Figure 8. *J–V* curves of the cells with the highest recorded efficiency for both the n-type and p-type devices. The n-type cell is from wafer N-W-4, whereas the p-type cell is located on wafer P-W-5.

complexities emerge. This section identifies and describes the two major integration challenges that arise from this combined approach.

For successful integration of MOSFETs into solar cells, it is important to understand how the devices respond to illumination. To this end, a comparison is made between the dark performance of the MOSFET and its behavior under illumination, with the wafer being exposed to light from the textured front side, featuring a spectrum closely resembling AM1.5 at 1000 W m^{-2}. This analysis is carried out using the Wacom WXS-156S AAA solar simulator. The impact of illumination on the I_D–V_{GS} curves is shown in **Figure 9**. Analysis of both NMOS and PMOS devices reveals that in the on-state of the MOSFET, there is negligible difference between the dark and illuminated curves. However, a significant increase in drain leakage currents during the off-state of the device is observed for both cases when exposed to light. This increase is likely attributed to the photogeneration of free charge carriers near the channel area. Such behavior under illuminated conditions presents a challenge to the MOSFET-PV integration concept. While the most straightforward solution could involve local optical shading of the relatively small MOSFET area, this approach would result in a loss of active area on the wafer. Alternatively, more sophisticated strategies might include the creation of a local electrical barrier to prevent charge carriers from the bulk reaching the channel region of the MOSFET, thereby mitigating these photogenerated leakage currents. For instance, this could be done by introducing an inversely doped well underneath the MOSFET area, creating a different doping profile compared to the bulk of the wafer.

Additionally, it should be noted that while the COSMOS approach offers the potential advantage of monolithic integration between solar cells and MOSFETs, there is an important consideration to take into account. The bulk of the wafer can facilitate leakage currents, meaning that the establishment of monolithic interconnections requires additional considerations compared to configurations where separate discrete devices are interconnected. As depicted in Figure 2, the wafer layout in this study features multiple solar cells monolithically integrated with

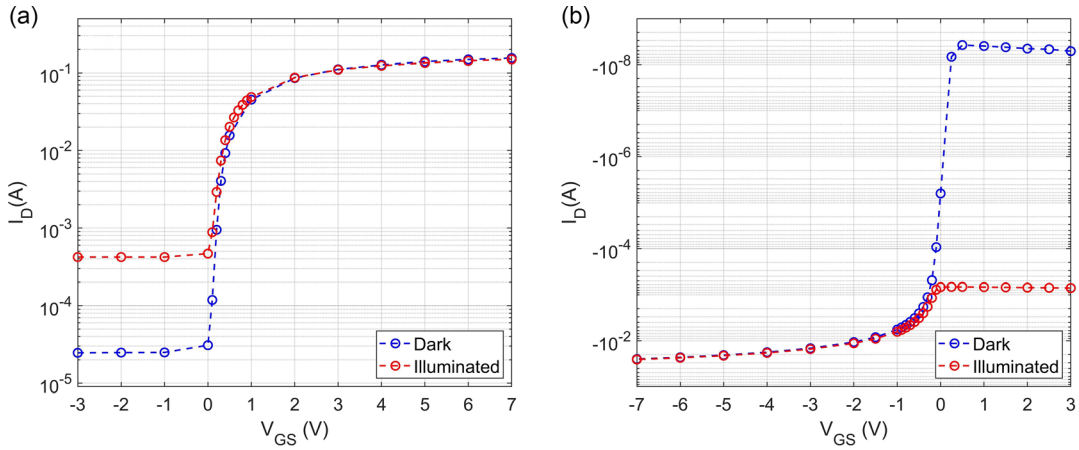

Figure 9. I_D–V_{GS} curves in both dark and illuminated conditions, all obtained using the Wacom WXS-156S AAA solar simulator. a) An NMOS device with $n_{SD} = 10$ and $W = 2$ mm on wafer P-W-2, recorded at $V_{DS} = 0.1$ V. b) A PMOS device with $n_{SD} = 5$ and $W = 2$ mm on wafer N-W-4 recorded at $V_{DS} = -0.1$ V.

MOSFETs. In these particular MOSFETs with monolithic interconnections, the body has an independent contact pad and is not shorted to the source contact. This configuration allows for the interchange of source and drain contacts. Hence, the manufactured structures enable a direct exploration of how a MOSFET's performance is influenced by whether its drain or source has a monolithic connection to the solar cell. The study encompasses all possible connections: NMOS with source/drain connected to p^+ solar cell contact (BSF), NMOS with source/drain connected to n^+ solar cell contact (emitter), PMOS with source/drain connected to p^+ solar cell contact (emitter), and PMOS with source/drain connected to n^+ solar cell contact (BSF). The I_D–V_{GS} curves for these various configurations are illustrated in **Figure 10**. Each subfigure depicts the two curves for the same MOSFET, with only the drain and source contacts swapped during the measurement. These data are obtained in dark conditions using the using the Cascade Summit 12 000 probe station connected to a Keysight B1500A Semiconductor Parameter Analyzer. Furthermore, the monolithic interconnection configuration is presented next to each plot. In the on-state, the performance remains relatively consistent regardless of the interconnection topology. However, distinctions in leakage currents during the off-state are apparent among different interconnection schemes. Notably, for all topologies, the leakage currents are remarkably lower when the source is monolithically connected to the PV cell in comparison to the drain connection. This observation suggests that a monolithic connection between the drain and solar cell can introduce an unintended leakage path. Typically, a MOSFET exhibits low drain leakage in the off-state because the drain-substrate junction is in reverse bias. However, when the drain contact is monolithically interconnected with a solar cell contact, this introduces an additional path for the current into the substrate. Consequently, it is desirable for the device structure employed in this study to solely feature monolithic interconnections between the source and solar cell, while avoiding such connections between the drain and solar cell. To still accommodate integration topologies where the drain is connected to the solar cell, modifications to the device structure should be explored. For example, this could involve creating an inversely doped well underneath the MOSFET. This well could be biased independently of the substrate, potentially offering enhanced control over MOSFET behavior.

5. Conclusions

In this study, the concept of COSMOS devices was introduced, and a process flow was proposed in which IBC TOPCon solar cells and lateral power MOSFETs are simultaneously fabricated on a single substrate. This process was successfully employed to manufacture both n-type solar cells with integrated PMOS and p-type solar cells with integrated NMOS. Important trade-offs related to fabrication, such as the choice between dry or wet etching and the impact of hotplate annealing at the end of the process, were discussed. Notably, efficiencies exceeding 20% were achieved for both n-type and p-type solar cells, highlighting the potential of COSMOS solar cells. In addition, both NMOS and PMOS devices were successfully manufactured. In the off-state, NMOS devices exhibited leakage currents of approximately

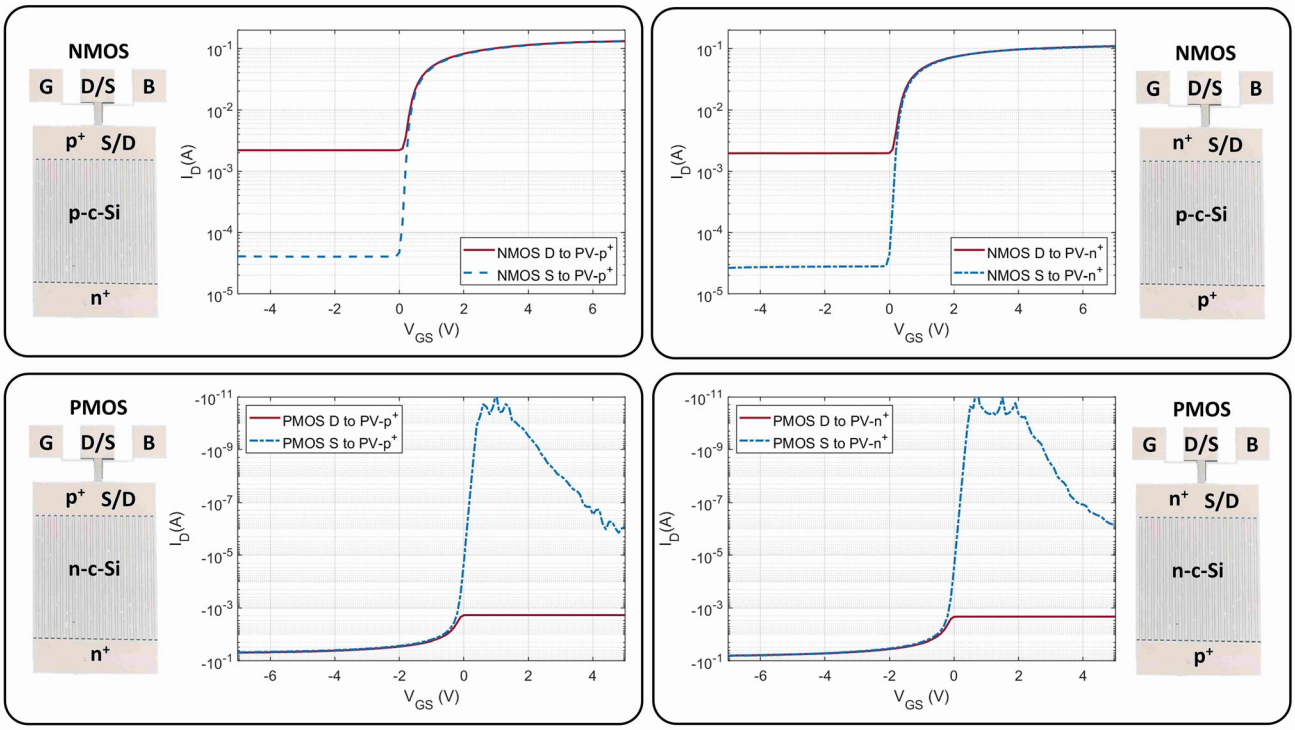

Figure 10. Effect of different monolithic interconnections on I_D–V_{GS} curves. These curves were all measured under dark conditions, at $V_{DS} = 0.1$ V for NMOS devices, and at $V_{DS} = -0.1$ V for PMOS devices. Since the body contact is separated from the source, two I_D–V_{GS} curves were recorded for each configuration: one with the source contact connected to the solar cell and the other with the drain contact connected to the solar cell.

$\approx 2 \times 10^{-5}$ A at $V_{DS} = 0.1$ V, while PMOS devices displayed leakage currents of around $\approx 1 \times 10^{-10}$ A at $V_{DS} = -0.1$ V, a remarkable factor of 2×10^5 lower. Optimizations in the fabrication process are expected to reduce NMOS leakage currents to levels comparable to those of the manufactured PMOS devices. Moreover, the study demonstrated how the on-resistance of the MOSFET in a COSMOS device can be controlled by varying its geometry. Expanding the channel width is effective up to a certain point, beyond which increasing the number of source-drain couples connected in parallel becomes a more efficient strategy. The NMOS devices outperformed PMOS devices in achieving a low on-resistance per unit area due to the higher electron mobility compared to holes.

Furthermore, this study identified several integration challenges. Characterizing the MOSFET under illuminated conditions revealed that off-state leakage currents increase due to illumination. Consequently, for real-world applications of PV-integrated transistors, it is important to develop strategies to mitigate these effects. Additionally, various configurations of monolithic integration between the MOSFETs and solar cells were explored. This analysis revealed that the presence of a monolithic connection between the MOSFET drain and the PV contact leads to a higher drain leakage current as compared to a configuration where the source is connected to the PV contact. This difference can presumably be attributed to the unintended current path introduced through the PV contact and the bulk of the wafer in the former case. Thus, the monolithic integration must be approached with care. In summary, the COSMOS approach presents promising results for advancing the smart integration of transistors in PV applications with high-efficiency cells.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

COSMOS, crystalline silicon, integration, interdigitated back contact, monolithic integration, MOSFET, photovoltatronics, polycrystalline silicon on oxide, power electronics, tunnel-oxide passivated contacts

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