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DOI
10.1063/5.0195013

Publication date
2024

Document Version
Final published version

Published in
Applied Physics Letters

Citation (APA)
Mo, J., Niu, Y., May, A., Rommel, M., Rossi, C., Romijn, J., Zhang, G., & Vollebregt, S. (2024). An analog to digital converter in a SiC CMOS technology for high-temperature applications. *Applied Physics Letters*, *124*(15), Article 152105. https://doi.org/10.1063/5.0195013

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RESEARCH ARTICLE | APRIL 09 2024

An analog to digital converter in a SiC CMOS technology for high-temperature applications

Special Collection: (Ultra)Wide-bandgap Semiconductors for Extreme Environment Electronics

Jiarui Mo ; Yunfan Niu; Alexander May ; Mathias Rommel ; Chiara Rossi ; Joost Romijn ; Guoqi Zhang ; Sten Vollebregt

Appl. Phys. Lett. 124, 152105 (2024)
https://doi.org/10.1063/5.0195013

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Cite as: Appl. Phys. Lett. **124**, 152105 (2024); doi: 10.1063/5.0195013
Submitted: 29 December 2023 · Accepted: 27 March 2024 ·
Published Online: 9 April 2024

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Note: This paper is part of the APL Special Collection on (Ultra)Wide-bandgap Semiconductors for Extreme Environment Electronics.
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ABSTRACT

Integrated circuits based on wide bandgap semiconductors are considered an attractive option for meeting the demand for high-temperature electronics. Here, we report an analog-to-digital converter fabricated in a silicon carbide complementary metal–oxide–semiconductor technology now available through Europractice. The MOSFET component in this technology was measured up to 500 °C, and the key parameters, such as threshold voltage, field-effect mobility, and channel-length modulation parameters, were extracted. A 4-bit flash data converter, consisting of 266 transistors, is implemented with this technology and demonstrates correct operation up to 400 °C. Finally, the gate oxide quality is investigated by time-dependent dielectric breakdown measurements at 500 °C. A field-acceleration factor of 4.4 dec/(MV/cm) is obtained by applying the *E* model.

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Nowadays, silicon (Si) technology is dominating the integrated circuit (IC) market. Nevertheless, an increasing number of applications require integrated circuits to operate in harsh environments, especially in high-temperature environments. For instance, in combustion process control, space exploration, and deep oil drilling, the ambient temperature of these applications is typically beyond the maximum operating temperature of Si devices. Hence, there is an urgent need for a semiconductor technology that can operate at high temperatures to meet the increasing demand.[1–4]

In recent years, silicon carbide (SiC) ICs have attracted much attention from researchers due to their great potential for use in harsh environments. The wide bandgap of SiC allows a theoretical operating temperature of 1000 °C for SiC electronics, as only at this temperature the intrinsic carrier concentration surpasses that of the doped regions.[5] To date, several SiC IC technologies have been developed, for example, SiC complementary metal–oxide–semiconductor (CMOS) technology developed by Raytheon (known as HiTSiC technology) and bipolar junction transistor (BJT) technology (HOTSIC technology) developed by Zetterling's group at KTH.[6,7] These technologies showed much higher operation temperatures than Si-based devices. However, these SiC technologies are either discontinued or difficult to access.

Previously, we have demonstrated an emerging CMOS technology based on 4H–SiC, where SiC transducers and circuits can be implemented.[8–12] The process is currently available through Europractice provided by Fraunhofer IISB and is intended for electronics at high temperatures. With this 4H–SiC CMOS technology, Romijn *et al.* reported the first basic digital and circuit blocks in 2021.[8] A SiC UV detector monolithically integrated with SiC readout electronics was also later demonstrated.[9] In addition to circuit implementations, temperature sensing elements in this technology, such as p–n diode, resistance, and CTAT, were investigated.[10,11] Although the development of this technology showed great potential, the current characterization was limited to only 200 °C, which is around the border of the Si technology's temperature limitation.

This Letter demonstrates the SiC CMOS technology as a promising platform for high-temperature applications. SiC MOSFETs are characterized up to 500 °C, and key technology parameters are extracted over this temperature range. A 4-bit SiC flash analog-to-digital converter (ADC) is designed with this technology and is characterized up to 500 °C. Furthermore, the gate oxide reliability is evaluated by the constant-voltage time-dependent dielectric breakdown (TDDB) experiment at 500 °C.

TABLE I. The sheet resistance of the implanted layer and the specific contact resistivities of the p-type and n-type contacts. (Sheet resistance of n-well is not given as it is not measurable within the n-type epi-layer.)

Layer	R_{sh} ($\Omega/\square$)	ρ_c ($\Omega\,\text{cm}^2$)
p-well	39.7×10^5	NA
Shallow-n+	1043	NA
Shallow-p+	3.9×10^4	NA
n-type contact	NA	2.5×10^{-4}
p-type contact	NA	4.0×10^{-2}

The SiC CMOS technology is implemented on a 6-inch SiC wafer with a n-type epitaxial layer. On the n-type epi-layer, four sets of ion implantations are performed consecutively to create n-well, p-well, shallow-p+, and shallow-n+, respectively. The measured sheet resistances of these layers are reported in Table I. The active region is defined by 55 nm thermal oxide. The oxide is treated by nitric oxide (NO) annealing to minimize the interface defect density. The gate is formed by n-type poly-Si with a sheet resistance of 15–17 $\Omega/\square$, and the minimal gate length was chosen as 2 μm to reduce device variability due to process equipment limitations (e.g., from the lithography tool). On the isolation oxide, windows are opened on shallow-n+ and shallow-p+ contact regions to deposit NiAl and Ti/Al into different types of contact openings, followed by a rapid thermal annealing step to form Ohmic contacts at the interface. A Ni_xSi_y silicide is formed on the n-type region, while a Ti_3SiC_2 layer is formed on the p-type region. With the transmission line method (TLM), the contact resistances (ρ_c) of n-type and p-type contacts are summarized in Table I. Finally, the wafer is metalized by Ti/Al/Ti metal stack. A top view and a cross-sectional schematic of the MOSFET are given in Fig. 1.

The electrical properties of discrete NMOSFETs and PMOSFETs (NMOS and PMOS) were characterized using a semiconductor parameter analyzer. Under a fixed gate-source voltage ($|V_{gs}| = 10$ V), the I_{ds}–V_{ds} relation of the SiC MOSFETs at elevated temperatures up to 500 °C (with steps of 100 °C) is measured and depicted in Figs. 2(a) and 2(b) by the scattered lines. To have a direct comparison between NMOS and PMOS devices, the devices' dimensions are kept the same, i.e., the channel width to channel length (W/L) ratio equals 100/6. From Figs. 2(a) and 2(b), it can be observed that the drain current

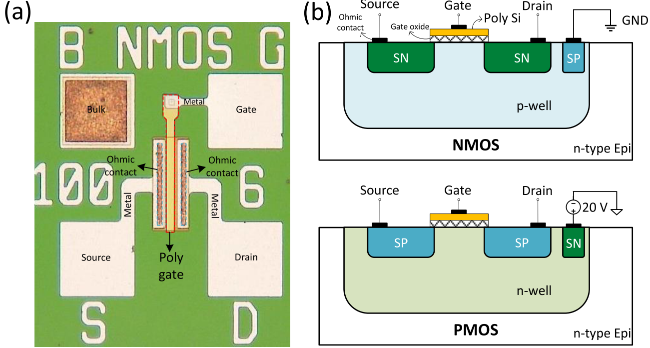

FIG. 1. (a) A top view of a SiC MOSFET and (b) a simplified schematic of the SiC MOSFET's cross section (field oxide and metal layer are omitted).

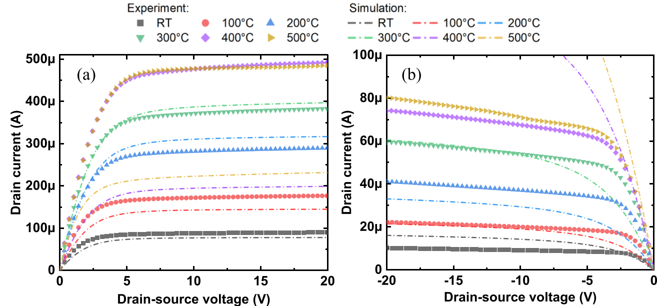

FIG. 2. The simulated and measured I_{ds}–V_{ds} output characteristic of SiC (a) NMOS and (b) PMOS from room temperature to 500 °C, with $|V_{gs}| = 10$ V.

increases with the temperature and then tends to saturate. This behavior might be due to the interplay of different effects, including the incomplete dopant ionization at lower temperatures, limitation of carrier channel mobility by SiC/SiO_2 interface defects at lower temperatures, and finally, increasing limitation of channel mobilities by phonon scattering at higher temperatures.[6,13–15]

Furthermore, the I_{ds}-V_{ds} relations were simulated with device compact models included in the process design kit (PDK) provided by Fraunhofer IISB, as shown by the dashed lines in Figs. 2(a) and 2(b). The model is based on BSIM4, which has been modified to include unique properties of SiC MOSFETs. In the model, both the intrinsic and overlap capacitances are considered. It should be noted that the device parameters were extracted from I–V measurement of MOSFETs with certain dimensions at limited temperature points, i.e., 25 °C, 150, and 300 °C. A very good correlation can be observed when comparing measurements and simulations for this temperature range (i.e., between room temperature and 300 °C). However, when using the compact models for temperatures outside of the valid temperature range, obvious discrepancies between the model and experiment can be observed. Thus, currently, an extension of the compact models' temperature validity range has started. The channel-length modulation parameter λ is extracted from the output characteristic and is listed in Table II. The channel-length modulation parameter λ is almost the same as in the previous study.[8]

The threshold voltages (V_{th}) are extracted from I_{ds}–V_{gs} curves [in Figs. 3(a) and 3(b)] by using the second-derivative method. The drain-source voltages are kept low so that the MOSFET works in the linear region.[16,17] From room temperature to 500 °C, the V_{th} amplitude of PMOS and NMOS drops from 8.5 to 5.8 V and from 4.8 to 0.05 V, respectively. The threshold voltage of NMOS is more sensitive to temperature than that of PMOS because the doping concentration of p-well is around one order of magnitude higher than n-well. To be specific, the temperature-sensitive Fermi potential, which is positively proportional to the nature logarithm of doping concentration, directly relates to the change rate of the threshold voltage with respect to temperature. Due to the high threshold voltage of the SiC MOSFET, the supply voltage of this technology is 20 V to ensure sufficient headroom for circuit design.

Additionally, the field-effect mobility (μ_{FE}) can be extracted from the slope of the I_{ds}–V_{gs} relation,[18–20]

$$\mu_{FE} = \frac{L}{C_{ox} V_{ds} W} \cdot \frac{\partial I_{ds}}{\partial V_{gs}} \quad (V_{ds} \ll V_{gs} - V_{th}). \tag{1}$$

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TABLE II. Extracted values of the threshold voltage and channel-length modulation parameter from room temperature to 500 °C (C_{ox} is 62.8 nF/cm^2 for a 55 nm gate oxide).

$100 \times 6\ \mu m^2$ PMOS		
Temp. (°C)	V_{th} (V)	λ (V^{-1})
RT	−8.20	1.21×10^{-2}
100	−7.60	1.26×10^{-2}
200	−6.90	1.23×10^{-2}
300	−6.40	1.17×10^{-2}
400	−6.05	1.12×10^{-2}
500	−5.80	1.43×10^{-2}
$100 \times 6\ \mu m^2$ NMOS		
Temp. (°C)	V_{th} (V)	λ (V^{-1})
RT	4.80	2.66×10^{-3}
100	3.55	2.81×10^{-3}
200	2.30	2.76×10^{-3}
300	0.70	3.10×10^{-3}
400	0.25	3.24×10^{-3}
500	0.05	1.40×10^{-3}

The extracted μ_{FE} for electrons and holes is plotted in Figs. 3(c) and 3(d). The mobility initially increases with the gate bias and then saturates or decreases. This decrease is caused by the large series resistance from the source and drain, which is mostly contributed by the contact resistance.[19] Based on the extracted ρ_c and designed contact areas, the contact resistance at RT is estimated to be 141 Ω for NMOS and 29 kΩ for PMOS. A low contact resistance to the p-type SiC has been known to be more challenging to form.[21] For both types of charge carriers, the field-effect mobility is much lower than the SiC bulk mobility due to the additional scattering effects and trapped carriers at the interface states.[18] As a result, the channel exhibits a relatively large on-resistance. Despite this, the current driving capability, especially for the PMOS device, has improved significantly compared to previous tape-outs in the same technology.[8]

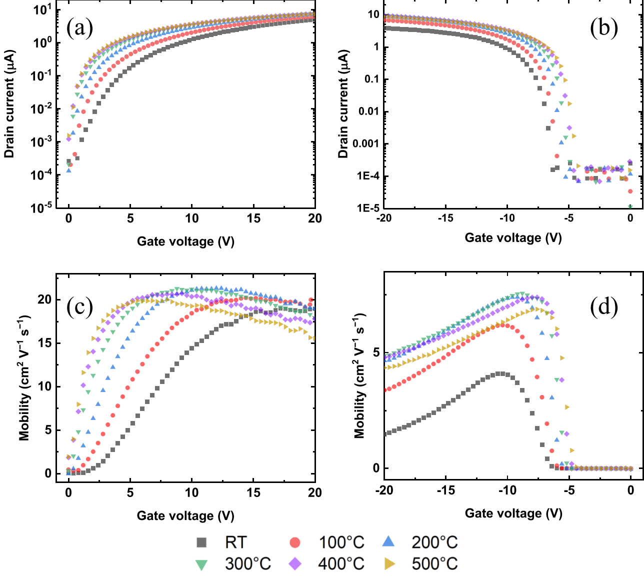

FIG. 3. The I_{ds}–V_{gs} curves of the (a) NMOS ($V_{ds} = 20$ mV) and (b) PMOS ($V_{ds} = -100$ mV) at elevated temperatures. (c) and (d) The extracted field-effect mobilities of electrons and holes, respectively.

The designed data converter is a typical flash ADC, which consists of a resistive ladder, a series of comparators, and a digital encoder circuit, as shown in Fig. 4. The resistive ladder is implemented with 16 shallow-n+ resistors. A single comparator consists of nine transistors and consists of a basic differential two-stage open-loop amplifier with an active load. An inverter is connected to the amplifier as the output stage to improve the slew rate. The comparator compares the input voltage with the reference voltages, which is divided by the resistor ladder. The circuit is biased with an external voltage source. The ADC contains 266 transistors in total, and the dimension of the chip is approximately $8800 \times 1900\ \mu m^2$. Although the chip size is large for a general-purpose data converter, its main application field is less sensitive to dimension compared to the field of consumer electronics. Furthermore, the chip size could be reduced if a better lithography process is employed.

The functionality of the comparator is verified by sweeping the voltage at the input terminal from ground potential to supply voltage with every reference voltage point, i.e., 1.25, 2.5,…,17.5, 18.75, 20 V. The measurement was carried out from room temperature to 500 °C even though the circuit might not function above 300 °C where the valid temperature range of the used compact models ends. The input–output relations at different temperatures are plotted in Fig. 5. From room temperature to 400 °C, the comparator demonstrates correct switching behavior, and the maximum input offset is less than 0.15 V. Generally, a large offset appears at the lower input range, where the input pair does not operate in the saturation region. The offset can also result from the mismatch between transistors and/or the asymmetry of

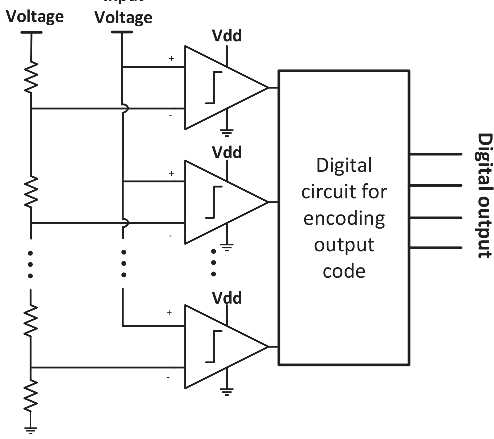

FIG. 4. A circuit schematic of the 4-bit flash data converter. It consists of an on-chip resistive ladder for the voltage references, comparators, and an encoding circuit.

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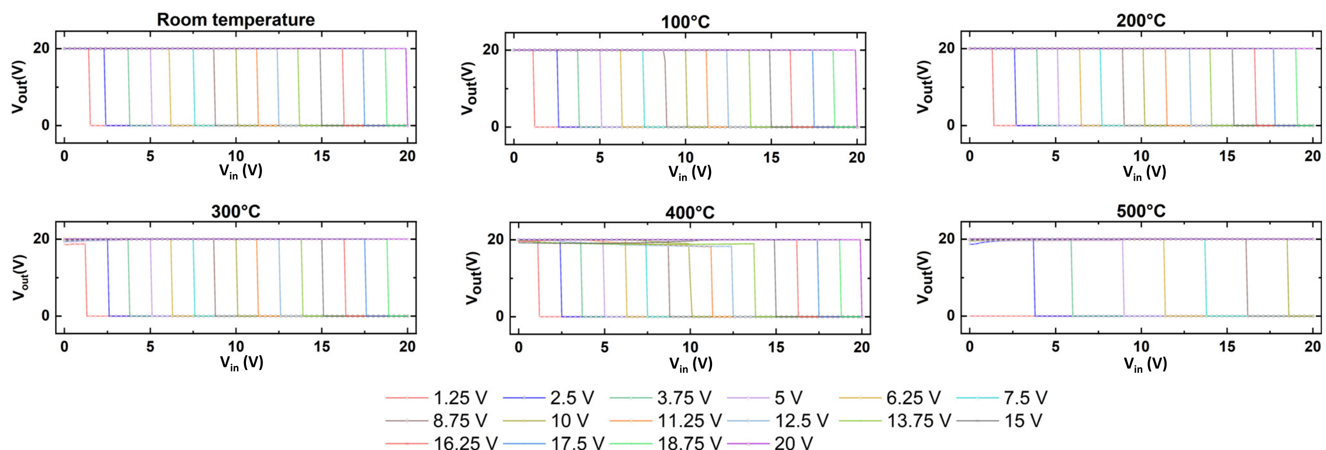

FIG. 5. The switching behavior of the comparator at different reference voltages from room temperature to 500 °C.

the layout, which can be further reduced by an improved layout and partially by process optimization.

At 500 °C, the comparator does not have a proper switching behavior anymore, where the comparator switches at a much higher voltage than the reference. One possible explanation is that the MOSFET device cannot be properly switched off as the threshold voltage reduces to a very small value at high temperatures (as mentioned in Table II). Additionally, the DC gain of the amplifier decreased significantly with increasing temperature. The single-transistor gain of the input transistor (A_0) can be written as

$$A_0 = g_m r_O = \frac{2}{\lambda(V_{gs} - V_{th})}, \quad (2)$$

where g_m and r_O are the transconductance and output resistance of the MOSFET, respectively. According to the expression, there is a drop in A_0 with the increasing temperature resulting from V_{th} variation. From a certain temperature on, i.e., 500 °C, the open-loop gain becomes so small that the comparator cannot switch with a small input voltage difference, leading to a large input offset. This effect was overlooked during the design phase as the temperature range of validity of the compact model is up to 300 °C, and the simulation results were, thus, considered inaccurate.

The same as the comparator, the 4-bit ADC is characterized up to 500 °C. The analog input from 0 to 20 V vs digital output at different temperatures is given in Fig. 6, and the simulation result from room temperature to 300 °C is provided together for comparison. From the simulation result, the data converter has an ideal 4-bit characteristic curve and demonstrates little offset and non-linearity. The measurement result exhibits a staircase response, where the analog input has been digitized into 16 least significant bits (LSB), and no missing code is observed for all temperatures.

From room temperature to 400 °C, the maximum differential non-linearity (DNL) is 0.3 V, which equals 0.24 LSB. The maximum DNL usually occurs at the first code, which might originate from the larger offset of the comparator at low input voltage. The integral non-linearity (INL) is calculated with the code center method. The largest INL is 0.32 LSB at 400 °C. As for 500 °C, it is obvious that the actual transfer function deviates significantly from the ideal curve, where the measured curve shifts toward the left. The maximum INL is almost 1 LSB, and the output stays at 1000 for an input larger than 18.25 V. This is likely to be caused by the comparator's malfunction at 500 °C as mentioned before. The failure of the comparator and data converter at 500 °C implies that an accurate temperature-dependent model for SiC MOSFET above 300 °C needs to be developed to predict the circuit behavior for an extended operation temperature range.

The gate oxide reliability is often recognized as the bottleneck of SiC CMOS technology.[5,18] The most common reliability issue with the SiC gate oxide is known as TDDB, where the gate oxide will gradually degrade and eventually breakdown when it is stressed with a high electric field at a high temperature.[7,22,23] To examine the reliability of the gate oxide in this SiC CMOS technology, we measured the time to failure of MOSFETs with W/L = 200 μm/10 μm at 500 °C. To accelerate the aging of the gate oxide, we applied 48, 50, and 52 V to perform the measurement instead of the standard supply voltage, i.e., 20 V. These voltages were applied between the gate terminal and the bulk, which can be translated to gate electric fields E_{ox} of 8.7 , 9.1, and 9.5 MV/cm for a 55 nm thick gate oxide. For each of the stress conditions, ten samples were measured. The drain and source were kept floating. The leakage current was monitored over time with a Keithley Source Meter 2634B. Here, the Weibull distribution is used to evaluate the obtained TDDB data.

The Weibull distribution is expressed as

$$F(t) = 1 - e^{(-t/t_{63\%})^{\beta}}, \quad (3)$$

where $F(t)$ is the cumulative failure probability as a function of time t, $t_{63\%}$ is the characteristic time, and β is the Weibull slope. As shown in Fig. 7(a), the Weibull slope and $t_{63\%}$ extracted from the failure distribution vary from 1.61 to 2.61 and 11 to 1899 s, respectively. The β values are lower than those reported in the literature with a similar oxide thickness.[22,24,25] The low β value is a sign of extrinsic defects, which could be introduced by the subsequent process steps after the gate oxide formation.[22] The E model, where E_{ox} is considered proportional to $t_{63\%}$ in the log scale, is employed as the field-acceleration model, and

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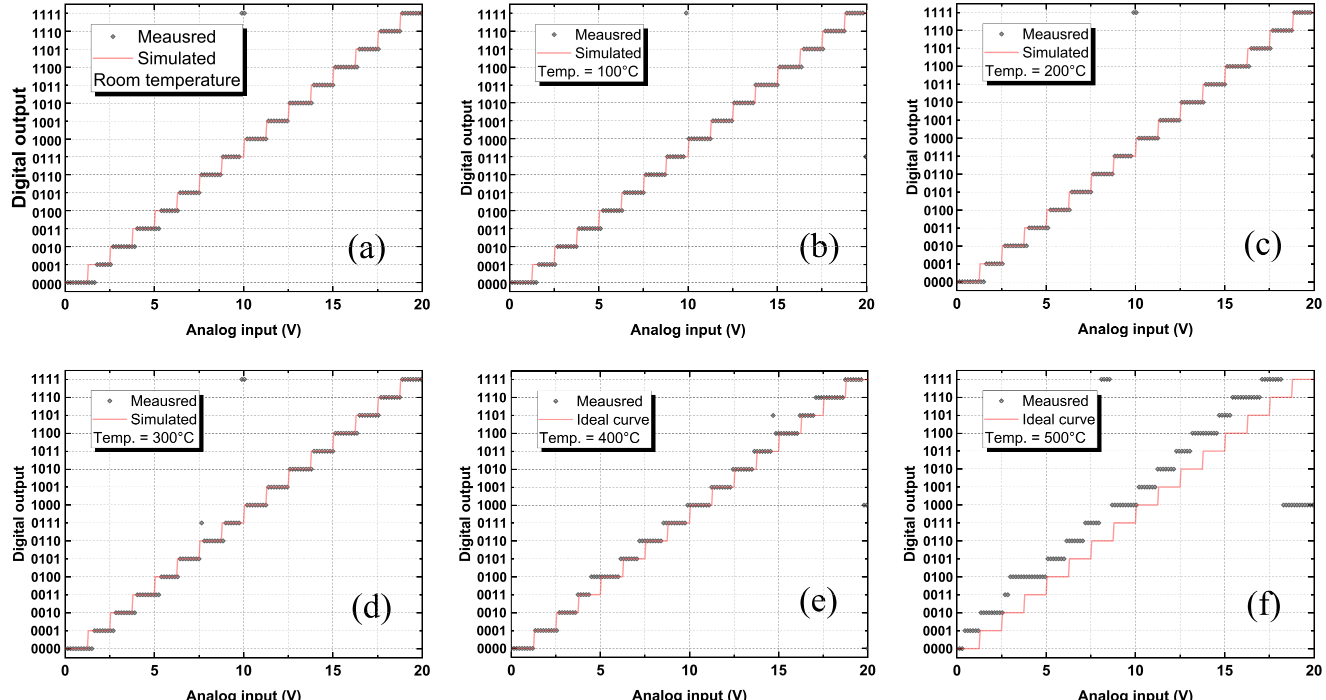

FIG. 6. The characteristic curve of the flash ADC at different temperatures. At 400 °C, the measured curve shifts slightly to the left. At 500 °C, the transfer function deviated significantly from the ideal curve.

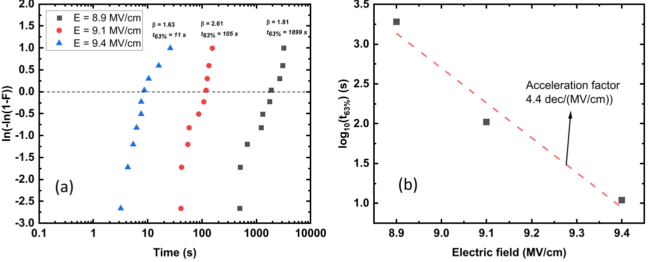

FIG. 7. (a) The Weibull distribution of the gate oxide failure stressed by different electric fields at 500 °C and (b) E_{ox} vs $\log_{10}$ ($t_{63\%}$) and the extracted field-acceleration factor using the E model.

a field-acceleration factor (γ) of 4.4 dec/(MV/cm) is obtained, as shown in Fig. 7(b). It is worth mentioning that a decrease in γ is expected when a lower electric field is applied due to less Fowler–Nordheim tunneling occurring.[25] Therefore, a further TDDB measurement must be conducted at a lower E_{ox} to anticipate an accurate lifetime in the used condition.

In summary, this Letter reports an emerging 2 μm SiC CMOS technology for high-temperature applications. The MOSFETs are measured up to 500 °C, and the measured behavior of the MOSFETs above 400 °C deviated significantly from the model. It implies that the SiC MOSFET model used here needs to be further extended for applications above 400 °C. From the I_{ds}–V_{gs} and I_{ds}–V_{ds} measurement, the important parameters, such as threshold voltage, mobility, and channel-length modulation parameter, are extracted. V_{th} decreases significantly with temperature, and the extracted mobility of the PMOS reduces as the contact resistance becomes dominant. The first 4-bit flash ADC based on SiC CMOS technology was designed, fabricated, and measured. The ADC and its sub-circuit, i.e., a comparator, were measured and demonstrated a proper function up to 400 °C. The incorrect behavior of the ADC at 500 °C could be caused by the V_{th} variation and the gain reduction of the amplifier. Finally, the TDDB measurement was conducted at 500°C. With the E model, a field-acceleration factor of 4.4 dec/(MV/cm) is obtained for E_{ox} ranging from 8.7 to 9.5 MV/cm.

Financial support by the iRel40 Project is acknowledged gratefully. iRel40 is a European co-founded innovation project that has been granted by the ECSEL Joint Undertaking (JU) under Grant Agreement No. 876659. The funding of the project comes from the Horizon 2020 research programme and participating countries. National funding is provided by Germany, including the Free States of Saxony and Thuringia, Austria, Belgium, Finland, France, Italy, the Netherlands, Slovakia, Spain, Sweden, and Turkey.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Jiarui Mo: Data curation (equal); Supervision (equal); Writing – original draft (equal). **Yunfan Niu:** Data curation (equal); Software

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(equal). **Alexander May:** Conceptualization (equal); Investigation (equal); Writing – review & editing (equal). **Mathias Rommel:** Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Chiara Rossi:** Software (equal); Validation (equal). **Joost Romijn:** Conceptualization (equal); Resources (equal). **Guoqi Zhang:** Funding acquisition (equal); Project administration (equal); Resources (equal). **Sten Vollebregt:** Funding acquisition (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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18 April 2024 07:03:05

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