Efficiency and Bandwidth Enhancement of On-Chip Antennas by Using Connected Arrays and Artificial Dielectrics

Cavallo, Daniele; Syed, Waqas H.; Neto, Andrea

DOI
10.1109/IRMMW-THz.2016.7758355

Publication date
2016

Document Version
Accepted author manuscript

Published in
2016 41st International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz)

Efficiency and Bandwidth Enhancement of On-Chip Antennas by Using Connected Arrays and Artificial Dielectrics

Daniele Cavallo[1], Waqas H. Syed[1], and Andrea Neto[1]
[1]Delft University of Technology, Delft, 2628 CD, Netherlands

***Abstract*—On-chip antennas operating in the THz frequency range are characterized by narrow bandwidth and poor radiation efficiency. This is because they are electrically very close to the ground plane that is used to shield the antenna from the lossy substrate. In this work we propose a novel approach to increase the efficiency and the bandwidth of antennas integrated on chip, by exploiting and combining the two concepts of connected arrays and artificial dielectric layers.**

I. INTRODUCTION

INTEGRATED technology, especially CMOS and BiCMOS, has recently received increasing interest for its potential to drastically reduce the costs of terahertz (THz) systems and expand their use for practical applications. The main limitation to the wide spreading of THz low-cost integrated systems has been that the cut-off frequency of the transistors was well below THz frequencies. However, with the continuous advance of integrated circuit technology, the transistor operation is no longer the limiting factor [1]. The poor efficiency of on-chip antennas has now become an important bottleneck in converting the electrical signals (on-chip) into radiated ones (off-chip).

A typical layer stack of a chip (Fig. 1) consists of a thin layer of silicon dioxide (SiO_2), about 10 µm thick, on which the antenna is realized (e.g., a dipole or a slot antenna). A conducting ground plane shields the antenna from a thick silicon (Si) layer, since this latter is characterized by very high losses. The vicinity to the ground plane makes the antenna input impedance strongly inductive yielding extremely narrow bandwidth. Also, in the slot case, most of the power remains confined within the chip, in the form of parallel plate waveguide modes, rather than being radiated. In this work we propose an approach to improve the performance of on-chip antennas and arrays, based on the concepts of connected array of dipoles and artificial dielectric layers (ADLs).

II. PROPOSED ANTENNA CONCEPT

Connected arrays of dipoles [2] consist of arrays with electrical connections between the elements. The electrical connection allows the current distribution to be uniform and frequency independent, unlike the sinusoidal distribution of resonant antennas (see Fig. 2). To achieve unidirectional radiation while maintaining wideband properties, the dipoles should be placed at the distance of about a quarter wavelength from the ground plane. However, since on chip the distance to the ground plane is only in the order of $\lambda/50$, even connected dipoles exhibit narrow bandwidths (Fig. 3(a)). To enlarge the frequency range, we propose to include artificial dielectric layers (ADLs) above the array plane (Fig. 3(b)). The ADLs [3] consist of periodic metallic patches, small with respect to the wavelength, embedded in a host material in order to create an equivalent material with much higher permittivity. The high electrical density enhances the radiation in the direction of the ADL, greatly reducing the negative effects of the ground plane. The ADL is anisotropic, i.e. its equivalent permittivity decreases with the angle of incidence. Thus, unlike homogenous dielectrics, total internal reflection at the interface between ADL and air does not occur, with almost negligible power being lost into surface waves. Figure 3 shows the bandwidth enhancement when a connected array unit cell is loaded with artificial dielectric.

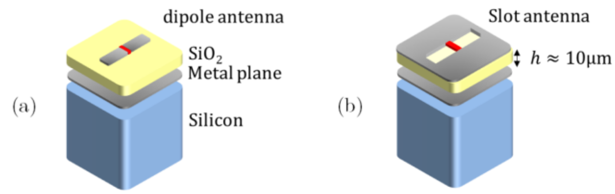

Fig. 1. (a) Dipole and (b) slot antennas on a silicon chip.

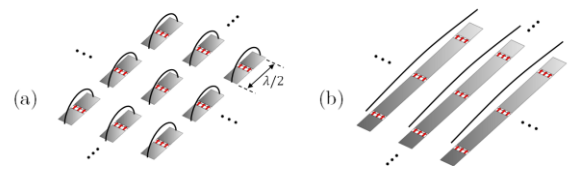

Fig. 2. Current distribution on dipole elements in array configuration: (a) resonant unconnected dipoles; (b) connected dipoles.

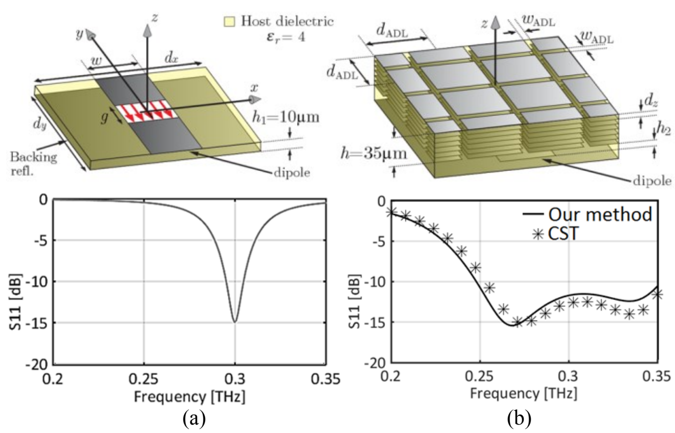

Fig. 2. Active reflection coefficient for (a) a unit cell of a connected array on chip and (b) the same unit cell loaded with artificial dielectrics.

REFERENCES

[1] U. R. Pfeiffer and E. Öjefors, "Terahertz imaging with CMOS/BiCMOS process technologies," *Eur. Solid-State Circ. Conf.*, Seville, 2010, pp. 52-60.
[2] D. Cavallo, A. Neto, and G. Gerini, "Analytical description and design of printed dipole arrays for wideband wide-scan applications," *IEEE Trans. Antennas Propag.*, vol. 60, no. 12, pp. 6027-6031, Dec. 2012.
[3] W. H. Syed, G. Fiorentino, D. Cavallo, M. Spirito, P. M. Sarro, and A. Neto, "Design, fabrication and measurement of 0.3 THz on-chip double-slot antenna enhanced by artificial dielectrics," *IEEE Trans. THz Sci. Tech.*, vol. 5, no. 2, pp. 288-298, Mar. 2015.