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A ±5 A Integrated Current-Sensing System with ±0.3% Gain Error and 16 μA Offset from −55°C to +85°C

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Abstract−This paper presents an integrated current-sensing system (CSS) that is intended for use in battery-powered devices. It consists of a 10-mΩ on-chip metal shunt resistor, a switched-capacitor ΔΣ ADC, and a dynamic bandgap reference (BGR) that provides the ADC's reference voltage and also senses the shunt's temperature. The CSS is realized in a standard 0.13-μm CMOS process, occupies 1.15 mm^2 and draws 55 μA from a 1.5-V supply. Extensive measurements were made on 24 devices, 12 of which were directly bonded to a printed-circuit-board (PCB) and 12 of which were packaged in a standard HVQFN plastic package. For currents ranging from –5 A to +5 A and over a temperature range of –55°C to +85°C, they exhibit a maximum offset of 16 μA and a maximum gain error of ±0.3%. This level of accuracy represents a significant improvement on the state-of-the-art, and was achieved by the use of an accurate shunt temperature compensation scheme, a low-leakage sampling scheme and several dynamic error correction techniques.

Index Terms−Coulomb counter, current-sensing system, metal shunt resistor, dynamic bandgap reference, temperature sensor, temperature compensation.

I. INTRODUCTION

Coulomb counting is a widely used method of estimating battery state-of-charge (SoC). It involves measuring and integrating the battery's current I_{bat} to determine its net charge flow [1], [2]. The overall accuracy of such a battery fuel gauge is primarily determined by the accuracy of the current-sensing system (CSS) [2]. Even a small current measurement error (either gain or offset) can accumulate over an extended period of time and result in a prohibitively large error in SoC estimation. This is more pronounced in scenarios where the battery is partially charged/discharged and hence the estimated SoC cannot be reset, e.g., by means of an "end-of-charge" signal generated by the charging system when the battery is full, or by means of an "empty" signal when the battery voltage drops below a certain level [1], [2].

The current consumption and the current-sensing offset of the CSS should preferably be below the battery self-discharge rate. Assuming a conservative self-discharge rate of 1%/month [3] and a typical battery capacity of 5000 mAh in hand-held devices, this translates into a current of about 50 μA. A gain error of less than ±0.5% for currents up to a few Amperes (±5 A in this work) also facilitates an accurate estimation of battery SoC. Although, Coulomb counting substantially limits the effect of current-sensing noise by integrating I_{bat} over an extended period of time, the presented CSS was also required to provide better than 13-bit resolution (~0.01%) over a 25-ms conversion time. This facilitates rapid calibration, as well as the use of auxiliary digital algorithms to improve the accuracy of the SoC estimation [1], [2].

Of the existing current-sensing techniques, contactless current sensors, such as Rogowski coils and current transformers are not suitable for DC and/or small (sub-mA) current measurement, and tend to be quite bulky [4]. Magnetic sensors such as fluxgates and magneto-resistors, which are able to measure small DC currents, require backend processing due to their

use of ferromagnetic materials [4]–[7]. In addition, fluxgates require large excitation currents to saturate their cores, and hence dissipate several tens of mW [6], [8]. Hall-effect sensors draw similar amounts of current, but are at least CMOS compatible [9]–[11]. Due to their limited sensitivity, however, they are not suitable for sensing small (μA-level) currents. State-of-the-art designs achieve offsets of a few μT, corresponding to current offsets of several tens of mA [11].

As shown in Fig. 1, battery current I_{bat} is usually measured by digitizing the voltage drop V_{shunt} across a small (a few to tens of mΩ) Kelvin-connected shunt resistor R_{shunt} [12]–[20]. This method potentially offers a low-cost and small-size solution, which is in principle compatible with standard CMOS processes. Existing integrated CSSs, however, exhibit more than 500-μA offset and ±3% gain error for *bidirectional* currents up to ±7 A [15]–[18]. This large gain error can be mainly attributed to the temperature dependency and tolerance of R_{shunt}, and to the spread in the ADC's reference voltage. Recently, we have reported a CSS [12] that is significantly more accurate. This design, which is more thoroughly described in this paper, achieves an offset of 16 μA and a gain error of ±0.3% with the help of an accurate temperature compensation scheme, multiple dynamic error correction techniques and a low-leakage shunt-voltage sampling scheme.

The rest of the paper is organized as follows. Section II discusses different methods of realizing shunt resistors and then presents the on-chip shunt used in this work. Sections III and IV describe the design of the dynamic bandgap reference (BGR) and the ADC, respectively. Section V explains the calibration process, and experimental results are presented in section VI. Section VII concludes the paper.

II. SHUNT RESISTOR

A. Shunt Resistance

The shunt's resistance R_{shunt} represents a compromise between the power lost in the shunt and

the magnitude of the voltage drop V_{shunt}. Lowering R_{shunt} reduces power loss at the expense of V_{shunt}, and hence, current-sensing offset and resolution.

At a peak current of 5 A, a 10-mΩ shunt will dissipate 250 mW, which is quite significant. However, portable devices such as cellphones and tablets are usually in low-power/stand-by mode, during which the shunt's power dissipation will be lower than the power dissipated by the continuously-running micro-power ADC used in the CSS. In addition, the battery's internal resistance and that of the associated wiring will typically be in the order of several tens of milliohms, and so there is no point in making R_{shunt} any smaller. In this work, a shunt with a nominal value of 10 mΩ is chosen, for which a current-sensing offset of a few tens of μA corresponds to an ADC offset of several hundred nV, which can be achieved with the help of dynamic offset cancellation techniques [21].

B. Shunt Implementation

The simplest way to realize a shunt resistor is to exploit the resistance of an existing PCB trace [22]–[24]. Although this approach enables a very cost-effective implementation without additional power loss, it suffers from the large temperature coefficient of resistance (TCR) of the copper trace (~0.39%/°C), whose temperature cannot be accurately sensed, and thus compensated for, by an on-chip temperature sensor. In [24], an indirect temperature compensation scheme is proposed. It involves sensing the thermal drift of a replica copper trace by driving a reference current through it. This approach, however, is not able to compensate for the effect of Joule heating in the shunt, and hence is limited to low currents (less than 0.5 A in [24]). In addition, the reference current's spread and drift directly limit the resulting current-sensing accuracy.

Incorporating a shunt resistor into an IC package can potentially improve the thermal coupling between the shunt and an on-chip temperature sensor. The designs reported in [25]–[27] propose the use of a shunt made from the package's leadframe. In [26] and [27], the effect of the

leadframe's large TCR, about +0.335%/°C, is addressed by amplifying V_{shunt} with a gain that is designed to have an equal-but-opposite temperature coefficient. However, the resulting gain error is still significant (> ±5%) over the temperature range from −40°C to +85°C [27]. A bond wire can also be used as a shunt [28], [29]. But the thermal coupling with the die, although better than that of a PCB trace, is still quite poor.

To further improve the thermal coupling, the die can be placed directly on top of a leadframe shunt [30], or under the shunt, as in [31] and [32] where the shunt is realized in the redistribution layer (RDL) of a chip-scale IC package. To avoid the error introduced by the *remaining* temperature gradient between the shunt and the on-die temperature-sensing module, the leadframe can be made from special alloys with low TCR (< 0.002%/°C), such as Constantan or Manganin [33], [34]. The main drawback of this approach, however, is that it requires a custom package, thus increasing production cost.

To be fully compatible with standard packaging technology, we propose the use of a shunt made from the metal layers of a CMOS chip [12]–[14]. As shown in Fig. 2, the shunt consists of four metal layers (M2 to M5) connected in parallel. It occupies a large area of 400×700 μm^2, in order to reliably handle large currents (up to 5 A), and to facilitate low-ohmic contacts to the outside world via eight large (150×150 μm^2) bond pads. The resulting shunt has a nominal value of 10 mΩ, whose spread (up to ±15%) is corrected by *room-temperature* calibration.

For a typical plastic package with a junction-to-ambient thermal resistance of 100°C/W, passing 5 A through a 10-mΩ shunt will result in a 25°C temperature rise. This, results in a significant measurement error, since the shunt has a TCR of about 0.35%/°C. This effect is counteracted by a temperature compensation scheme that involves measuring the shunt's temperature (by *reusing* the PNPs of the bandgap reference) and then performing a polynomial correction on the digitized value of V_{shunt} [12]–[14]. At a temperature T, the resistance of the

shunt $R_{shunt}(T)$ can be approximated as:

$$R_{shunt}(T) = R_{shunt}(T_{0\_shunt}) \cdot [1 + \alpha_1 \cdot (T - T_{0\_shunt}) + \alpha_2 \cdot (T - T_{0\_shunt})^2] \quad (1)$$

where α_1 and α_2 are the resistor's 1st- and 2nd-order temperature coefficients, which are quite constant for the given process (based on process data, and on measurements obtained from two different batches [12]), and T_{0_shunt} is the temperature at which the shunt is calibrated. Since T_{0_shunt} is sensed by on-chip PNPs, this calibration does not need to be performed in a temperature-stabilized environment, thus reducing calibration time and cost.

In contrast to our previous work [13] and [14], the shunt is placed directly above the PNPs, which enhances their thermal coupling. As shown in Fig. 2, this was achieved by realizing the shunt in the top metal layers (M2 to M5), and reserving M1 for connections to the PNPs. The coupling is further improved by the use of thermal vias between the shunt and an M1 plane surrounding the PNPs. Compared to [13] and [14], measurements show that these modifications result in a 3× improvement in the accuracy of the estimated shunt temperature rise caused by its Joule heating.

The parasitic resistance of the connections between the CSS and the outside world increases the battery-to-load resistance, while the associated Joule heating represents wasted power. Furthermore, it causes on-chip temperature gradients, which in turn cause errors in the estimated shunt temperature. As shown in Fig. 3, such parasitic resistances were minimized a) by mounting the chip directly on a PCB (chip-on-board or CoB), to which the shunt was connected by 32 short (< 1 mm long) and thin (25 µm in diameter) bond wires, and b) by packaging the chip in a small ($3\times6\times0.85$ mm^3) thermally enhanced 32-pin QFN package (HVQFN32), to which the shunt was connected by eight short (~1 mm long) and thick (50 µm in diameter) bond wires. The total parasitic series resistance, in both cases, was measured to be less than 10 mΩ.

III. DYNAMIC BANDGAP REFERENCE

A. Operating Principle

As discussed in the previous sections, the function of the bandgap reference (BGR) is both to provide the ADC's reference voltage V_{Ref} and to sense the temperature T required for the shunt's temperature compensation scheme. In addition, it must operate from a minimum supply voltage of 1.35 V (the specified range is 1.5 V ± 10%). As a result of these constraints, we opted for a dynamic BGR design [12]–[14], [35], [36]. As shown in the simplified diagram of Fig. 4, the BGR is designed to *only* generate a complementary-to-absolute-temperature (CTAT) voltage V_{BE} and a proportional-to-absolute-temperature (PTAT) voltage ΔV_{BE} from a pair of substrate PNPs biased at a 1:16 current-density ratio. These voltages are then sampled and linearly combined in a switched-capacitor (SC) ΔΣ ADC to generate a dynamic reference voltage $V_{Ref} = \Delta V_{BE} + V_{BE}/8 \approx$ 150 mV. This is compatible with V_{shunt}, which is typically in the order of tens of mV even as R_{shunt} varies over process and temperature. By configuring it differently, the ADC can also be made to output temperature information by digitizing ΔV_{BE} with respect to V_{Ref}.

Fig. 5 shows the detailed circuitry of the BGR. It can be divided into a bias circuit and a bipolar core. The bias circuit generates a PTAT current I = 1.4 µA (at 25°C) with the help of an opamp and two auxiliary PNPs, which are also biased at a 1:16 current-density ratio. This current is then mirrored to the bipolar core, and used to bias two PNPs at equal emitter currents $4I$ to generate V_{BE} and ΔV_{BE}. In contrast to the common use of scaled emitter *currents* [37], [38], this work uses PNPs with scaled-emitter-*areas*. This approach results in equal PNP transconductances, which, in turn, minimizes the total bias current required to ensure accurate settling when V_{BE} and ΔV_{BE} are sampled.

B. Precision Techniques

To decrease the spread in I, and hence in V_{BE}, the opamp's offset is reduced by chopping, while ΔV_{BE} is made accurate by applying dynamic element matching (DEM) to the PNPs and chopping the current sources of the bipolar core [37], [38]. The voltage drop across the DEM switches (SW_{DEM}), if added to V_{BE} and ΔV_{BE}, will introduce significant errors in both V_{Ref} and T. Calculation shows that switches with an on-resistance R_{on} of only 25 Ω (or R_{on} variation by 25 Ω with process and the supply voltage) will introduce errors of ~0.1% and ~0.3°C in V_{Ref} and T, respectively. One way of mitigating such large errors is to use wide MOS switches with sufficiently low R_{on}; however, these will introduce large leakage currents, especially at high temperatures. To circumvent this problem, the DEM switches are Kelvin-connected so as to prevent unwanted voltage drops from being added to V_{BE} or ΔV_{BE} at all [14]. The base-emitter voltages of the PNPs are directly sampled via the switches SW_{com}, which can be swapped to generate V_{BE} and ΔV_{BE}. Since these voltages are sampled by a SC ΔΣ ADC, the resistance of the switches SW_{com} is not critical as long as the ADC's input circuit settles sufficiently.

Another source of error is the spread in the PNP's saturation current I_{sat}, which leads to PTAT spread in V_{BE} and hence in V_{Ref} [39]. Over process and temperature, this spread can be as large as ±1% [13]. Also since V_{BE} has a nonlinear temperature characteristic or curvature, V_{Ref} exhibits a corresponding curvature error of about ±0.2% [12], [13]. Taking these two non-idealities into account, V_{Ref} can be expressed as

$$V_{Ref}(T) = V_{Ref,nom} + \delta_{PTAT} \cdot T/T_{0\_Ref} + g(T) \tag{2}$$

where $V_{Ref,nom}$ is the nominal value of V_{Ref}, δ_{PTAT} represents its PTAT error term, T_{0_Ref} is the temperature at which δ_{PTAT} is measured, and $g(T)$ represents the curvature. Simulation indicates that $g(T)$ is constant for a given design; measurements on three different batches revealed less than ±0.03% variation. This assertion is also supported by much larger data sets obtained from a

precision bandgap reference implemented in the same process [40].

The PTAT error can be significantly reduced by performing a single PTAT trim at room temperature [39]. The error term δ_{PTAT} is measured by digitizing a *known* external voltage V_{ext} with respect to V_{Ref} at room temperature.

In our previous work [12]–[14], the curvature $g(T)$ was corrected in a digital backend with the help of the known die temperature T. At the start of the process, however, an accurate V_{Ref}, and hence an accurate T is not yet available. So an iterative, and thus cumbersome, process is required because the initial value of V_{Ref} is used to estimate T, the result is used to correct V_{Ref}, from which an improved estimate of T is determined, etc. [14]. In our prototypes, at least two iterations were required to achieve sufficient accuracy. In this work, a simpler approach is proposed. The idea is to *indirectly* correct for the curvature $g(T)$, by accepting errors in the digitized values of T and V_{shunt} and then correcting them by (slightly) modifying the coefficients of α_1 and α_2 in (1). Measurements show that this simplified approach results in a negligible (< 0.01%) increase in the current-sensing error. A more detailed description of the calibration process is presented in section V.

IV. ADC

The CSS employs a 2nd-order switched-capacitor feed-forward ΔΣ ADC. Fig. 6 is a simplified diagram of the ADC, in which the capacitors C_{S1} (5 pF) sample V_{shunt}, while the capacitors C_{S2} (5 pF) and C_{S3} (=C_{S2}/8) sample $\pm\Delta V_{BE}$ and $\pm V_{BE}$, respectively. The sampled voltages are then accurately combined in the charge domain to generate the voltage V_{Ref} [12]–[14]. The modulator's feedback is established by using the output bitstream *bs* to control the polarity of the feedback voltages $\pm\Delta V_{BE}$ and $\pm V_{BE}$. This conversion results in an output bit-stream *bs* with an average value

$$\mu_{Ibat} = V_{shunt}/V_{Ref} = R_{shunt}\cdot I_{bat}/V_{Ref}. \quad (3)$$

To determine the temperature T, the sampling switches connected to C_{S1} are disabled, while the capacitors C_{S2} and C_{S3} perform the charge balancing. When bs is +1, C_{S3} samples $-V_{BE}$ and when bs is 0, C_{S2} is sampling $+\Delta V_{BE}$. This results in an average value of bs equal to

$$\mu_T = C_{S2}\cdot\Delta V_{BE} / (C_{S2}\cdot\Delta V_{BE} + C_{S3}\cdot V_{BE}) = \Delta V_{BE}/(\Delta V_{BE} + V_{BE}/8) = \Delta V_{BE}/V_{Ref}. \quad (4)$$

The temperature T in degrees Celsius is then obtain by linearly scaling μ_T [37]

$$T = A\cdot\mu_T - B \quad (5)$$

in which, $A \approx 623$ and $B \approx 273$.

The ADC is operated at a sampling frequency F_S = 100 kHz. The first integrator uses correlated double-sampling (CDS) to suppress its offset and 1/f noise. Further suppression is achieved by low frequency chopping (CHL), i.e. by averaging the results of two conversions, each with a different polarity of input. The resulting input impedance is $1/(C_{S1}\cdot 2F_S)$ = 1 MΩ, which is eight orders of magnitude larger than R_{shunt}, and hence has a negligible (0.01 ppm) effect on current-sensing gain error. The first and second integrators are based on folded-cascode OTAs, which draw 18 µA and 1.6 µA, respectively.

A. Timing

To digitize both I_{bat} and T, the ADC is operated in incremental mode and time-multiplexed: with conversion times of 22.5 ms for I_{bat} and 2.5 ms for T. As shown in Fig. 7(a), a temperature-averaging scheme (TAS) uses the average of two successive T measurements to compensate for each I_{bat} measurement, resulting in improved accuracy, especially when a current pulse causes dynamic self-heating in the shunt. Even better performance could be achieved by using two separate ADCs for I_{bat} and T, but at the expense of somewhat more complexity. The selected multiplexing scheme ensures sufficient resolution for T measurements (~0.02°C_{rms}) and allows I_{bat} to be monitored at 40 S/s, which is fast enough to compensate for thermal transients

(according to the measurement in section VI). After temperature compensation, the CSS is expected to provide ~14-bit resolution, which is mainly limited by the noise associated with I_{bat} (for currents below 2.5 A) and T (for currents above 2.5 A) measurements.

The frequency of the various dynamic error correction signals in the BGR and in the ADC (DEM, CH, and CHL) was chosen to avoid extra errors due to their interaction. As shown in Fig. 7(b), the frequency of the CHL signal is adjusted such that its period is equal to each I_{bat} and T measurement period. Furthermore, the frequency of CH and DEM is chosen to be 2× (18×) and 4× (36×) higher than CHL during the T and I_{bat} measurements, respectively.

B. Low-leakage Sensor Frontend

To avoid introducing additional current-sensing errors, the switches connected to R_{shunt} should be designed to minimize the leakage current due to their finite off-resistance [12], [14]. As shown in Fig. 8, this leakage current I_{leak} is provided by I_{bat} and flows through the on-resistance R_{on} of the input switches. Assuming that the four input switches are matched, the resulting voltage drop across R_{on} will cause a differential error $V_e = 2R_{on} \cdot I_{leak}$ in the sampled voltage across C_{S1}. This translates into a current-sensing error $I_e = 2R_{on}/R_{shunt} \cdot I_{leak}$. Since R_{on} is on the order of several kΩ and R_{shunt} is only 10 mΩ, I_e is about 6 orders of magnitude larger than I_{leak}. To make matters worse, I_{leak} will be a nonlinear function of V_{shunt} (or I_{bat}). This error is especially significant (up to 0.5%) at high temperatures (> 125°C) and negative I_{bat}, when I_{leak} may be in the nA range.

To tackle this issue, the input switches were realized as low-leakage high-threshold voltage NMOS transistors whose off-resistance is ~15× higher than that of normal NMOS transistors. As shown in Fig. 9, since a super cut-off MOS switch exhibits significantly less leakage [41], [42], the gates of the "off" switches are driven by the lowest available voltage, i.e. by ground when $I_{bat} > 0$, and by V_{shunt}^{+} when $I_{bat} < 0$. The polarity of I_{bat} needed for this minimum selection scheme is obtained from the ADC's output [12], [14]. Simulations show that this scheme reduces the worst-

case gain error due to I_{leak} by more than 60 times: to < 0.01%.

V. CALIBRATION

This section describes the calibration process and the digital backend computation used in the CSS. The PTAT error term δ_{PTAT}, the temperature T_{0_Ref} at which it is measured, and the shunt's resistance $R_{shunt}(T_{0\_shunt})$ at the calibration temperature are unique for each device and are referred to as individual calibration data, meaning that they are obtained by calibrating individual devices. All the other parameters (α_1, α_2, $V_{Ref,nom}$, A, and B) are common for all devices and are referred to as batch-calibration data, meaning that they are obtained by calibrating several devices and then averaging the results. It should be noted that in the following calibration steps, the curvature $g(T)$ is not explicitly taken into consideration (as explained in section III).

The batch-calibration data is obtained by characterizing the chips over temperature T as follows:

1) Determining $V_{Ref,nom}$, A, and B: a known external voltage is applied to the ADC, which then produces $\mu_T(T)$ and $\mu_{Ibat}(T)$. From (3), $V_{Ref}(T)$ can be obtained, the room-temperature value of which is defined as $V_{Ref,nom}$. By substituting $\mu_T(T)$ in (5) and using a linear fit, A and B can be obtained.
2) Determining the shunt's TCRs α_1 and α_2: a known current I_{bat} (3 A in this work) is passed through the shunt, while the ADC measures $\mu_T(T)$ and $\mu_{Ibat}(T)$. From (5), the shunt's temperature can be obtained. By substituting I_{bat}, $V_{Ref,nom}$, and $\mu_{Ibat}(T)$ into (3), $R_{shunt}(T)$ is obtained. The temperature coefficients α_1 and α_2 are then determined by fitting $R_{shunt}(T)$ to a 2nd-order polynomial.

After obtaining the batch-calibrated data (α_1, α_2, $V_{Ref,nom}$, A, and B), all the chips were then

individually calibrated at room temperature as follows:

1) Determining δ_{PTAT} and T_{0_Ref}: a known external voltage is applied to the ADC, and then V_{Ref} and μ_{T0_Ref} are measured. The parameter δ_{PTAT} of each chip is measured as the deviation of its V_{Ref} from $V_{Ref,nom}$. The calibration temperature T_{0_Ref} can be obtained by substituting μ_{T0_Ref} into (5) and also correcting for the spread of V_{Ref}

$$T_{0\_Ref} = A \cdot \mu_{T0\_Ref} \cdot V_{Ref} / V_{Ref,nom} - B \tag{6}$$

It should be noted that T_{0_Ref} doesn't need to be accurately measured, and an error of several degrees Celsius can be tolerated, since the temperature dependency of $V_{Ref}(T)$ is quite small (< 30 ppm/°C).

2) Determining the shunt resistance $R_{shunt}(T_{0\_shunt})$ at the calibration temperature: this is obtained by passing a known current I_{bat} through the shunt at room temperature, while the ADC measures μ_{T0_shunt} and μ_{Ibat}. By substituting μ_{T0_shunt} into (5) and applying PTAT correction to V_{Ref}, the shunt temperature can be calculated as

$$T_{0\_shunt} = A \cdot \mu_{T0\_shunt} \cdot (V_{Ref,nom} + \delta_{PTAT} \cdot \mu_{T0\_shunt} / \mu_{T0\_Ref}) / V_{Ref,nom} - B \tag{7}$$

Subsequently, $V_{Ref}(T_{0\_shunt})$ is calculated form (2). By substituting I_{bat}, $V_{Ref}(T_{0\_shunt})$ and μ_{Ibat} into (3), $R_{shunt}(T_{0\_shunt})$ is obtained.

Since the curvature $g(T)$ is not explicitly considered in the calibration process, its effect propagates through the temperature and reference voltage calculations up to the point when α_1 and α_2 are determined. As a result, α_1 and α_2 will be slightly modified (by ~0.15% and ~2.7%, respectively) so as to account for the effect of $g(T)$.

In normal operation, I_{bat} is measured by inserting the ADC's output μ_T and μ_{Ibat}, and then substituting the calibration data into (7), (1), (2) and (3).

VI. EXPERIMENTAL RESULTS

The CSS was realized in a standard 0.13-µm CMOS process (Fig. 10). It occupies 1.15 mm^2 and draws 55 µA from a 1.5-V supply. Due to the shunt's self-heating, large temperature gradients are created in the die. In order to mitigate their effect on the circuitry, the BGR and the ADC are symmetrically laid out along an axis normal to the middle of the shunt. The ADC and the BGR consume 25 µA and 20 µA, respectively, and 10 µA is dissipated in digital and auxiliary circuitry. For flexibility, the digital backend and $sinc^2$ decimation filter were implemented off-chip. 24 chips, 12 of which were directly bonded to PCB and 12 of which were packaged in HVQFN package, were characterized from –55°C to +85°C in steps of 20°C.

At a clock frequency of 100 kHz and for conversion rates up to 400 S/s, the ADC is *kT/C*-noise limited, achieving 15-bit resolution in a 22.5-ms conversion time. The temperature sensor also achieves 22-mK resolution in a 2.5-ms conversion time. After temperature compensation, the CSS achieves 14-bit resolution.

The ADC's offset was measured by disconnecting the shunt from the current sources; as shown in Fig. 11 it is less than 30 µV (3 mA) from –55°C to +85°C, and drops below 160 nV (16 µA) after low-frequency chopping.

The parameters obtained from the batch calibration (the average of all 24 samples) are shown in Table I. As shown in Fig. 12, the measured curvature of V_{Ref} is less than 0.5%, while the spread among chips in the same package is less than 0.03% after a PTAT trim. The resulting curvature in the temperature sensor's output is about 0.6°C, with less than 0.3°C spread among chips in the same package. Compared to the CoB samples, however, the curvature of the HVQFN samples is slightly (~0.2%) different. This may be due to the thermo-mechanical stress induced by the plastic package, which, due to the piezojunction effect, changes both the minority carrier mobility

and intrinsic carrier concentration in the base of the PNPs and hence modifies V_{BE} (and V_{Ref}) [43], [44]. This may be exacerbated by the fact that the dies were back ground (from ~740µm to ~200µm thick) to fit into the HVQFN package.

Measurements show that R_{shunt} spreads by about ±3% within a batch. After calibration and digital temperature compensation, the CSS achieves a gain error of less than ±0.6% for ±5 A range, from –55°C to +85°C (Fig. 13). However, a systematic gain error remains since the PNPs are somewhat insulated from the shunt by an oxide layer, and so under-estimate its actual temperature. Since this error is proportional to I_{bat}^2, and I_{bat} is (approximately) known, it can be corrected by multiplying the ADC's output by a linear function of I_{bat}^2. The associated coefficients were determined by batch calibration and found to be almost identical for the CoB and HVQFN packaged chips. This residual self-heating compensation (RSHC) reduces the gain error of the CSS to ±0.3% from –55°C to +85°C (Fig. 13).

The batch-calibration data for the results shown in Fig. 12 and Fig. 13 are determined by averaging the data obtained from all 24 devices. To demonstrate the robustness of the proposed calibration method, Fig. 14 shows the current-sensing gain error, for the case when this data is obtained by measurements on *one* sample. The data is then used to calibrate all 24 samples. It can be seen that the gain error is then slightly larger, but is always less than ±0.5%. The slight increase is mainly due to the difference in V_{Ref} curvature of the CoB and HVQFN devices.

The dynamic accuracy of the shunt temperature compensation was evaluated with a 0.1A–to–5A step. As shown in Fig. 15, this causes a temperature rise of about 40°C. Without TAS, the gain error settles within 1 s to –0.04%, and to 0.33% with and without RSHC, respectively. Enabling TAS reduces the settling time significantly at the expense of slightly more gain error in the *first* I_{bat} measurement after the current step. The corresponding improvement in the charge domain (the area under the curve) is ~2.5× after enabling TAS.

Compared to the state-of-the-art (Table II), the proposed CSS significantly improves the current-sensing accuracy, achieving a gain error of ±0.3% over a wide current range (±5 A) as well as an offset of only 16 μA.

VII. CONCLUSION

In this paper, a bidirectional, integrated current-sensing system has been presented. It employs a switched-capacitor ΔΣ ADC to digitize the proportional voltage drop across a 10-mΩ on-chip metal shunt resistor. A dynamic BGR both provides ADC's reference voltage V_{Ref} and senses shunt temperature required for shunt temperature compensation scheme. For currents ranging from –5 A to +5 A and over the temperature range of −55°C to +85°C, it exhibits 16-μA offset and ±0.3% gain error for devices packaged in the HVQFN plastic package and devices directly bonded to the PCB. The error sources in the BGR are effectively suppressed by using chopping, dynamic element matching and a single room-temperature trim, while the ADC is made accurate by using correlated-double sampling, system-level chopping and low-leakage frontend design. The effect of V_{Ref} nonlinearity is highly suppressed by slightly modifying the shunt temperature coefficients. The enhanced thermal coupling between shunt and temperature-sensing PNPs ensures an accurate estimate of the shunt's self-heating, while a temperature-averaging scheme results in accurate temperature compensation even in the presence of large current transients.

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FIGURE CAPTION

Fig. 1. Block diagram of the current-sensing system (CSS).

Fig. 2. A simplified cross-sectional view of the metal shunt and the temperature-sensing PNPs underneath.

Fig. 3. Photo of the chip (a) directly bonded to a PCB, and (b) packaged in a HVQFN plastic package.

Fig. 4. Simplified view of the bandgap circuit with PTAT, CTAT and reference voltages over temperature.

Fig. 5. Simplified schematic of the bandgap reference consisting of a bias circuit and a bipolar core with dynamic error correction techniques.

Fig. 6. Simplified diagram of the 2^{nd}-order switched-capacitor ΔΣ ADC used in the CSS.

Fig. 7. (a) ADC multiplexing and temperature-averaging scheme, and (b) timing diagram of different signals in the ADC and the BGR.

Fig. 8. Leakage sources in the sensor frontend.

Fig. 9. Simplified schematic of the low-leakage sensor frontend.

Fig. 10. (a) Die micrograph, and (b) HVQFN package.

Fig. 11. ADC's offset over temperature, before (top) and after (bottom) using CHL.

TABLE I: BATCH-CALIBRATION DATA.

Fig. 12. Spread and curvature in V_{Ref} and temperature sensor after PTAT trim in HVQFN-packaged chips (solid lines) and CoB (dashed lines).

Fig. 13. Current-sensing gain error at three ambient temperature points, before (top), and after (bottom) residual self-heating compensation.

Fig. 14. Current-sensing gain error at eight ambient temperature points, in which the batch calibration data is obtained by measurements on *one* sample.

Fig. 15. Transient temperature and gain error measurement for a 0.1–to–5A current step driven through the shunt (at room temperature).

TABLE II: COMPARISON WITH THE STATE-OF-THE-ART.