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Syed, Waqas H.; Fiorentino, Giuseppe; Cavallo, Daniele; Spirito, Marco; Sarro, Pasqualina M.; Neto, Andrea

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Design, Fabrication and Measurements of a 0.3 THz On-Chip Double Slot Antenna Enhanced by Artificial Dielectrics

Waqas H. Syed*, *Student Member, IEEE*, Giuseppe Fiorentino*, *Student Member, IEEE*, Daniele Cavallo, *Member, IEEE*, Marco Spirito, *Member, IEEE*, Pasqualina M. Sarro, *Fellow, IEEE*, and Andrea Neto, *Senior Member, IEEE*

* *These two authors contributed equally*

***Abstract*— In this paper we demonstrate, at 300 GHz and with integrated technology, the effectiveness of artificial dielectric layers to enhance the front-to-back ratio of printed antennas. This concept was previously proposed at microwave frequencies and using printed circuit board technology. The artificial material is now realized by introducing non-resonant metallic inclusions in a silicon dioxide host material. This allows to enhance the permittivity of the host medium and renders it anisotropic. By loading an electrically thin dielectric with these metallic inclusions, an engineered slab with effectively quarter wavelength thickness has been realized. Despite the large effective height and density of the artificial dielectric, the surface wave efficiency of the antenna is 99%. This is entirely due to the anisotropic properties of the material. A prototype antenna was built using an in-house complementary metal-oxide semiconductor (CMOS) back-end compatible integrated circuits (IC) process. Measured results from the antenna are presented and show a good agreement with the expected results.**

***Index Terms*— Artificial dielectric, front-to-back ratio, integrated antennas, surface waves.**

I. Introduction

Artificial dielectrics (ADs) were proposed in late 1940s to design low-loss and light-weight lens antennas in [1]. An AD consists of non-resonant periodic metallic structures embedded in a host material in order to increase its equivalent relative permittivity. A completely planar approach embeds periodic patches in a host dielectric as shown in Fig.1 and it is referred to as artificial dielectric layers (ADLs). The resulting medium simulates a homogeneous anisotropic substrate. Under plane-wave incidence, the effective permittivity is dependent on the polarization and the angle of the incidence. A theoretical study of two dimensional artificial dielectrics is reported in [2].

The volumetric and the planar nature of ADLs renders them a promising candidate for the design of integrated and compact passive devices in commercial CMOS technologies [3]. However, we believe that these ADLs can be mostly beneficial when used as superstrates to enhance the radiation performance of on-chip antennas. The design of such antennas presents numerous challenges. First, the vertical thickness of the stack that can be used to design an antenna, depending on the specific technology used, is in the order of 10-12μm. To accommodate high-frequency active front ends, this stack is grown on top of a lossy doped silicon substrate of thickness 250-300μm. The electromagnetic coupling to the lossy substrate is avoided by shielding the antenna with a metal plane. At 0.3 THz, a substrate height of 10μm corresponds to an electrical thickness of $\lambda_d/50$, where λ_d is the wavelength in the silicon dioxide $\varepsilon_r \approx 4$. It is well known that any antenna printed on top of an electrically thin grounded dielectric slab exhibits a very low radiation efficiency. This is because the source and its image radiate out of phase. Recently, the use of a high impedance metasurface as a radiator at 94 GHz was proposed in [4] to mitigate this effect. However, the efficiency of this antenna is still limited due to the close proximity of the radiator to the ground plane.

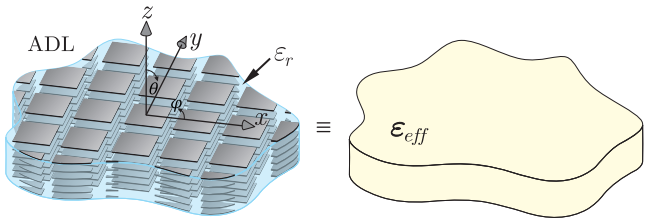

Fig. 1. Artificial dielectric layers embedded in a host medium with relative permittivity ε_r to realize an equivalent effective homogenous medium. Each layer is composed by an array of electrically small patches.

A non-planar solution to the low radiation efficiency issue is to use a dielectric lens with matching layers. The matching layers are used to minimize the losses due to multiple reflections inside the lens [5]–[7]. A planar solution that can bypass a dielectric lens was presented in [8]. In this work, the antenna is printed on an additional low-loss quartz wafer, glued on the chip to increase the distance form the ground plane, and aperture-coupled to the feed structure. The antenna achieved a peak efficiency of 60%. The 40% loss in efficiency is due to the excitation of the substrate modes. Furthermore, a strict alignment accuracy is required between the antenna and the on-chip feed lines. A similar kind of solution has also been proposed for on-chip antenna arrays by the same authors in [9].

In [10], it was shown that ADLs can be exploited to increase

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The authors are with the department of the microelectronics, EEMCS Faculty, Delft University of Technology, Mekelweg 4, 2628 CD Delft, The Netherlands (e-mail: w.h.syed, g.fiorentino, d.cavallo, m.spirito, p.m.sarro, a.neto@tudelft.nl).

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TABLE I
PHYSICAL DIMENSIONS OF THE ANTENNA AND ADL IN μM

l_{slot}	l_{sep}	w_{slot}	w_1	w_2	w_3	d_{adl}	d_z	w_{adl}
195	300	25	46.5	1	8	95	5	10

the front-to-back radiation ratio of planar antennas printed on a electrically thin dielectric slabs, in X-band. Thanks to the enhanced anisotropic properties, virtually no power loss in surface waves was observed. To ensure that no surface waves are excited, the characterization of the dispersion properties of ADL slabs in [11], [12] can be used, which is based on an analytical study of the spectral Green's function of these slabs.

In this work, we present a 0.3 THz version of the double-slot antenna enhanced by an ADL superstrate proposed in [10]. The non-resonant patches composing the ADL, as depicted in Fig. 1, are hosted by an electrically thin silicon dioxide slab with relative permittivity $\varepsilon_{\text{host}} = 4$. Such value is increased by the presence of the ADLs to an equivalent relative dielectric constant $\varepsilon_{\text{eff}} = 32$, for normally incident waves. The ADL superstrate does not suffer from surface-wave losses. This is due to the fact that, in virtue of the anisotropy, the waves incident at angles towards the grazing do not feel the larger effective dielectric constant, which would otherwise induce surface-wave modes. The superstrate and the antenna have been fabricated using an in-house IC process and the silicon on the back side of the antenna has been etched off. Measured results are reported and compared with simulations.

II. ANTENNA DESIGN

The double-slot antenna is shown in Fig. 2(a), with a co-planar waveguide (CPW) feed. The antenna is loaded by artificial dielectrics superstrate placed at a distance of 5 μm above the antenna (see Fig. 2(b)). The dimensions of the antenna and the ADL are summarized in Tab. I. The geometrical parameter have been selected so that the antenna is matched around the frequency of 300 GHz and the ADLs exhibit an effective dielectric constant of 32 for the waves which are incident along the broadside direction. The effective enhancement of the host material by the ADL, in an infinite homogeneous dielectric environment, is reported in Fig. 3.

The two curves represent the equivalent permittivities, as a function of the angle of incidence θ, for a transverse magnetic (TM) plane wave, with the electric field along $\hat{\boldsymbol{\theta}}$, and a transverse electric (TE) plane wave, with the electric field along $\hat{\boldsymbol{\varphi}}$. These values are derived using the procedure described in Appendix A. In [11], [12], we have also shown that, for electrically small dimensions of the metallic inclusions, the TE and TM modes do not couple. Moreover, it was also demonstrated that the equivalent permittivity is independent of the azimuth plane (i.e. φ). This graph also shows that for a TM incident wave, the equivalent permittivity of the enhanced medium tends to the one of the host substrate, i.e. 4, when the angle of incidence tends to 90 degrees. However, in case of TE incidence, the dielectric constant tends to a higher value. The effects of this property were investigated in [12], where the dispersion characteristic of these slabs were described in detail by means of an analytical method.

The total height of the host silicon dioxide substrate is 35μm, which is electrically equivalent to $\lambda_d/14$. Within this slab, an ADL consisting of a stack of 7 layers, each separated by 5μm along the z-axis (see Fig. 2(b)), is realized. This results in a slab with effective height of $0.2\lambda_{eff}$ at 0.3 THz. A starting point for the design has been obtained by following the guidelines outlined in [10] and by using the tools described in [11], [12]. While this allows for a fast selection of quasi-optimal geometrical parameter, the final structure with the details of the feed has been fine tuned using a commercial EM solver [13].

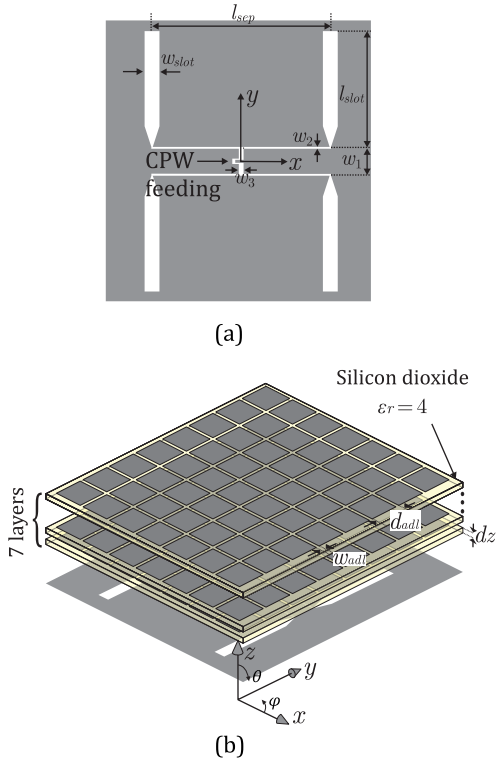

Fig. 2. (a) 2D view of a double slot fed by CPW lines and (b) 3D view of the antenna loaded by the ADL superstrate. For the sake of clarity only 3 layers of the ADL stack are shown.

A. Simulated Results

Figure 4 shows the simulated reflection coefficient with and without metal losses. As expected, the finite conductivity case (aluminum with conductivity $\sigma = 2.6 \times 10^7$ S/m) shows a broader bandwidth of the reflection coefficient, due to ohmic losses. In the fabricated device, the metal thickness of the antenna layer is 2μm, while it is 0.5μm for the ADL patches. In both cases, the thickness is well above the skin depth at 0.3 THz. The -10 dB impedance matching bandwidth of the antenna ranges from 295 till 320 GHz (8% relative bandwidth). This value is typical of a resonant double-slot antenna and not reduced by the presence of the ADL, which has broadband and non-resonant characteristics.

In order to quantify the advantage of using the ADL inclusions, a reference double-slot antenna loaded only with a 35μm slab of silicon dioxide has been designed and manufactured. This antenna without ADL is also matched at around 300 GHz, as shown in Fig. 4.

The simulated normalized radiation patterns of the antenna, with and without ADL, are reported in Fig. 5, at 305 GHz. It can be observed that the antenna with the ADL has a front-to-back ratio greater than 10 dB. On the contrary, the antenna

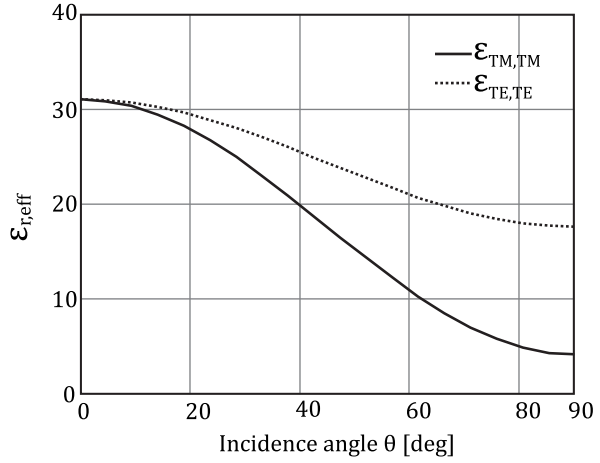

Fig. 3. The value of the the equivalent dielectric constant for scanning angles 0 to 90 degrees.

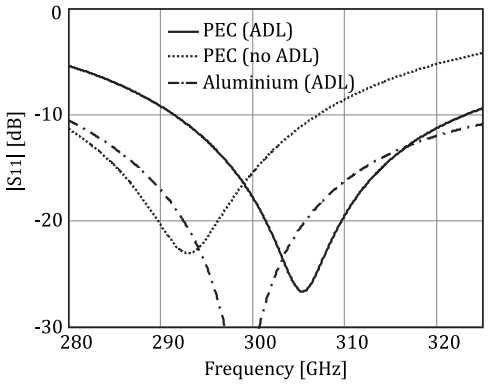

Fig. 4. Simulated reflection coefficient.

in absence of the ADL, loaded only by an electrically thin slab, exhibits a front-to-back ratio lower than 1 dB, since almost equal power is radiated in the two half spaces above and below the slot ground plane. Figure 6 shows the variation of the front-to-back ratio as a function of the frequency for the two antennas. The values for the ADL loaded antenna are higher than 10 dB over the whole matching bandwidth, and linearly increasing with frequency, due to the increasing electrical thickness of the ADL slab. Instead, the reference antenna has an almost frequency independent front-to-back ratio of about 0.7 dB.

In Fig. 7(a), we compare the gain and directivity for the antenna with and without ADL for the perfect electric conductor (PEC) case. This plot shows that the difference between the gain and directivity around the central frequency of the matching bandwidth for both antennas is negligible within the accuracy of the simulations. This means that surface waves, which in principle are allowed to propagate (TM_0 mode), are essentially not excited. The gain presented here also includes the mismatch losses. In the same graph, the comparison between the directivity of the two antenna reveals an enhancement of 2.2-2.6 dB for the ADL loaded antenna. This improvement occurs without compromising on pattern purity or surface wave efficiency. Note that, in simulations, surface wave losses are too low to be estimated accurately despite the use of absorbing boundary conditions along the lateral directions (x and y).

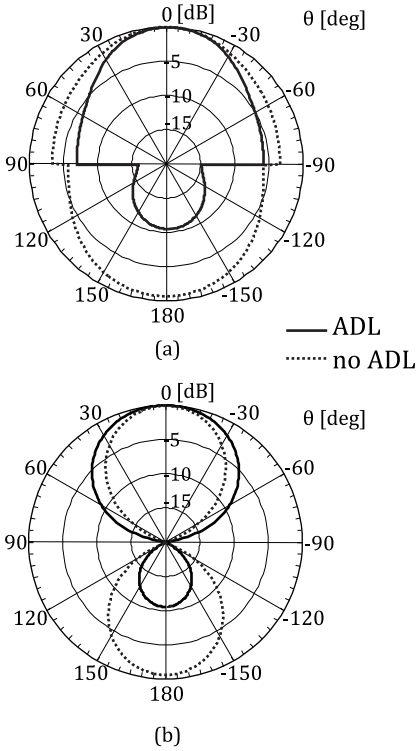

Fig. 5. Normalized simulated (a) E-plane and (b) H-plane radiation pattern in dB at 305 GHz. The solid and the dashed line represent the antenna with and without the ADL, respectively.

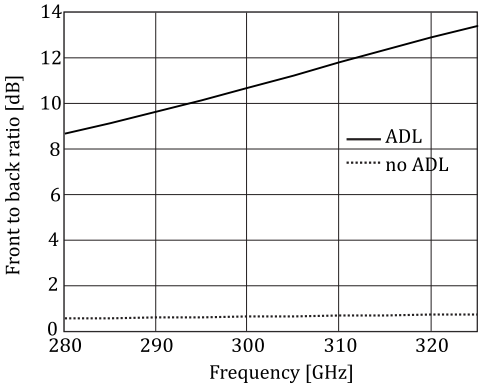

Fig. 6. Simulated front to back radiation ratio.

The simulated gain obtained in the case of lossy metal (aluminum) for the ADL loaded antenna is shown in Fig.7(b). It is 2 dB lower than the PEC case. By means of numerical simulation, we estimated the ohmic losses accounts for 1.3 dB within the slot antenna and 0.7 dB within the ADL.

To feed the double-slot antenna, a 50 Ohm CPW line is used to carry the input power to the center of the H-slot from one side of the antenna, as depicted in Fig. 8(a). Such a feed introduces an asymmetry in the E-plane pattern (see Fig. 8(b)), due to the coupling of the CPW lines with the parallel lines forming the H-slot and with the ADL. However, this asymmetry is kept to a minimum, by designing the CPW as small as possible (strip width of 5 μm and slot width of 2 μm) so that the field is confined in a small region and couples weakly with the antenna structure. On the other hand, such approach comes at the cost of increased ohmic losses due to strong currents in the inner conductor of the CPW. The total

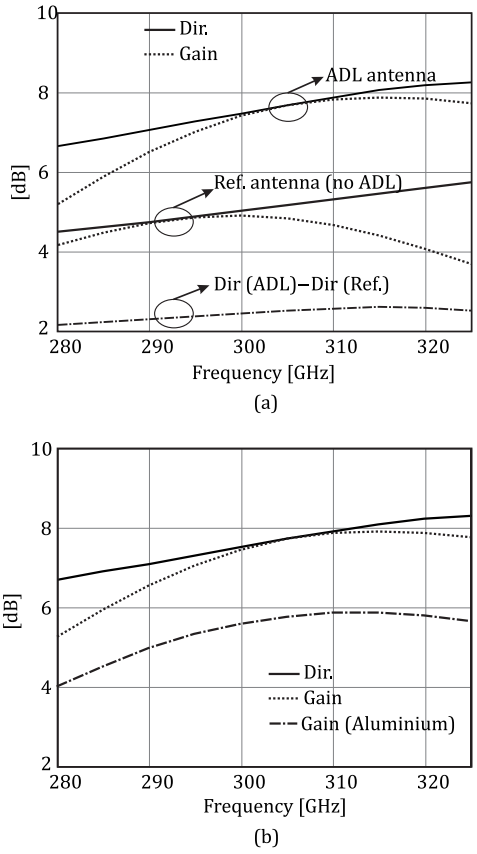

Fig. 7. Simulated antenna efficiency: (a) comparison with a reference antenna (i.e., without ADL) for a PEC case; (b) evaluation of ohmic losses using aluminum.

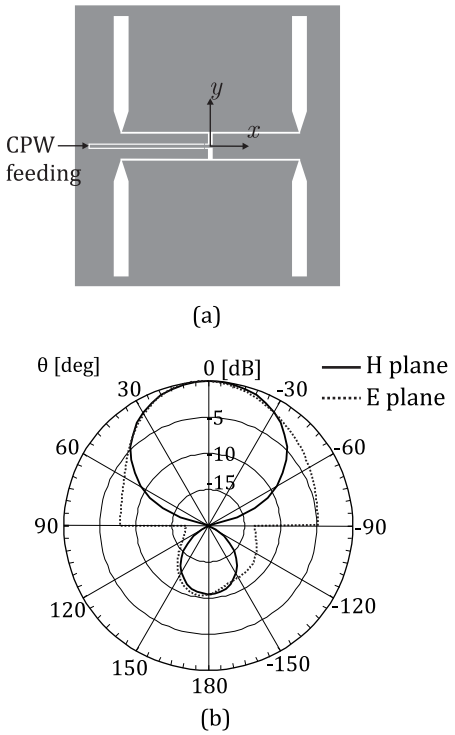

Fig. 8. (a) Schematic showing the extension of CPW line to feed the antenna. (b) The simulated radiation pattern in E and H-plane after inclusion of extended CPW.

losses due to the 860μm long line are estimated to be about 2 dB.

III. Fabrication

The combined antenna/ADL structure has been built using, as substrate, a high resistivity ($3.5\text{k}\Omega\cdot$ cm) n-type silicon (Si) wafer with 100 mm diameter, (100) crystal orientation and thickness of $500\pm25\mu$m. The use of a high-resistivity substrate is mandatory since the charge carriers cause high losses and these losses are even higher in the THz frequency range [14], [15].

The devices are realized using a 20×20 mm die design (see Fig. 9), giving a total of 12 dies on a single wafer. To avoid any cross talk between antennas, the distance of radiating structures has been chosen to be larger than 4 mm. The die is divided in three parts: the antenna/ADL structure on the top left side, the reference antenna on the top right part and the test structures (used for de-embedding the feed lines) on the bottom part (see Fig. 9). Note that further details about the test structures are given in Sec. IV.

In Fig. 10, a schematic cross section of the device is shown. The structure can be divided in three main sections: the feeding/pads section (A), the feed transition (B) and the antenna/ADL one (C). A 2 mm long CPW with uniform width connects the contact-pads, where the wafer probe is landed, to a transition region. In this latter region, the CPW lines undergo a series of tapers and transitions to account for the different z-stratifications along the line. Finally, the feed line is connected to the double-slot antenna that radiates in the presence of the ADL. The antenna/ADL system is suspended by removing the silicon substrate, to avoid that the power is radiated into silicon and then to enhance the effect of the dielectric contrast given by the ADL.

A thin (100 nm) low-pressure chemical-vapor-deposition (LPCVD) low-stress silicon nitride (SiN) layer is firstly deposited on the silicon as hard mask for the back-side of the wafer, followed by 200 nm of plasma enhanced CVD (PECVD) silicon oxide. The antenna layer was realized using a 2 μm thick pure aluminum layer deposited by radio-frequency (RF) sputtering, using an SPTS Sigma 204 DC magnetron system. The deposition temperature of the aluminum was 350°C, resulting in a layer conductivity of about $2.6\cdot10^7\sigma$/m. The residual stress of this layer is 290 ± 23 MPa and has been measured using a TENCOR stress-meter.

The patterning of the metal layer is realized by first coating the wafer with a 2 μm layer of SPR 3017M positive photoresist and then using I-line lithography (ASML PAS 5500/80 wafer-stepper) to define the features.

After the photoresist development, a dry etching process based on chlorine chemistry has been used to remove the aluminum. The etching parameters, such as the gas ratio, etching time and depth uniformity, have been carefully optimized. This is because unwanted effects like over-etching or iso-etching could have resulted in larger features, compromising the impedance matching between the feed and the antenna. Moreover, any aluminum residuals in the thin slots could have shorted the antenna or the feeding lines in some points. For these reasons, accurate scanning electron microscope (SEM) inspections of the thin slots have been performed after the etching and the resist stripping (see Fig. 12). The through, reflect and line (TRL) test structures have been realized on the same metal layer (see Fig. 9, bottom part), with the same

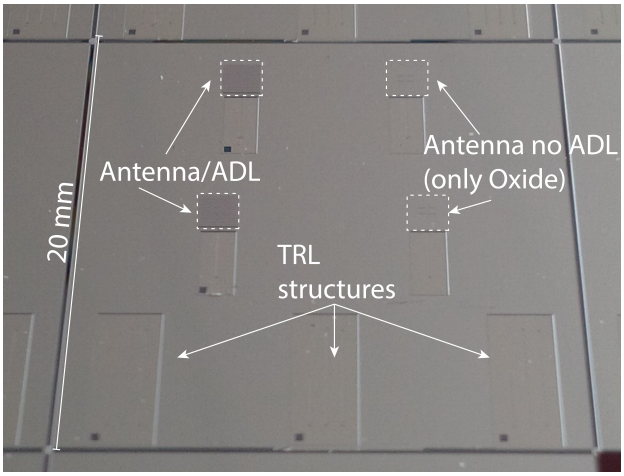

Fig. 9. Top view of the die containing the antenna/ADL, the reference antenna and the calibration structures. The dashed area indicates where the silicon is removed from the back of the wafer.

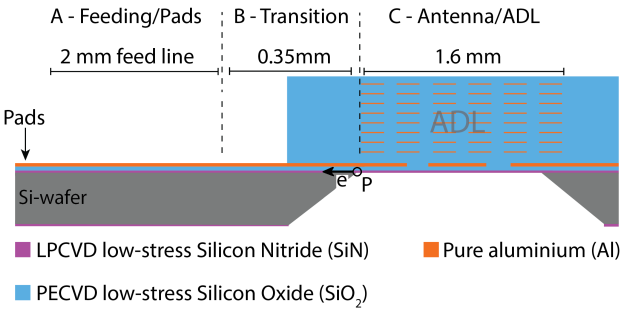

Fig. 10. Schematic cross-section of the antenna/ADL structure. The device can be divided in three main parts: the feeding/pads area, the transition region and the antenna/ADL structure. The overall length of the structure is 4 mm, including the pads and the entire ADL length.

etching process. The PECVD silicon oxide deposited under the antenna layer prevents any damaging of the silicon nitride during the metal etching.

As explained in the previous sections, to ensure a correct matching between the slot antenna and the feeding lines, an accurate transition has been designed and the result is shown in Fig. 13. The structure in region B is designed to implement the transition between the large CPW lines (region A), with a inner conductor width of 22μm, and the CPW lines feeding the antenna slots (region C), with a inner conductor width of 11μm.

After the antenna fabrication, a separation layer of 5μm of silicon oxide is deposited in a PECVD Novellus Concept-One reactor. The ADL consists of a stack of 7 metal layers embedded into a thick layer of PECVD silicon oxide. As first step, a pure aluminum layer (500 nm) is deposited using the same tool and deposition condition of the antenna layer. A layer of 2μm of SPR 3017M positive photoresist is used to define the ADL area. Each ADL layer consists of an array of 16×16 square patches that effectively cover the entire antenna radiation area. The patches are 85μm wide with a separation of 10μm in the xy plane. All the layers are patterned by means of I-line lithography and dry etching process. The details of the fabrication are shown in Fig. 14. After the patches definition, a layer of 5μm of low-stress (-30MPa) PECVD silicon oxide is deposited. Since the ratio between the height of the oxide layer and the metal patches is more than 10, step coverage

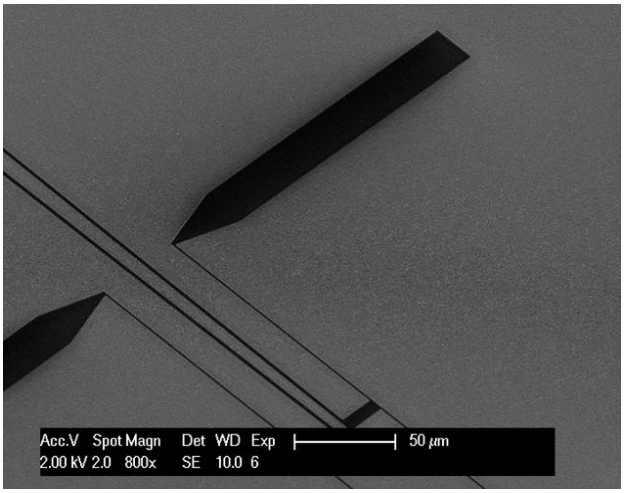

Fig. 11. SEM picture showing the double slots antenna. The grey area is the pure aluminum layer while the dark area is the landing layer of PECVD silicon oxide.

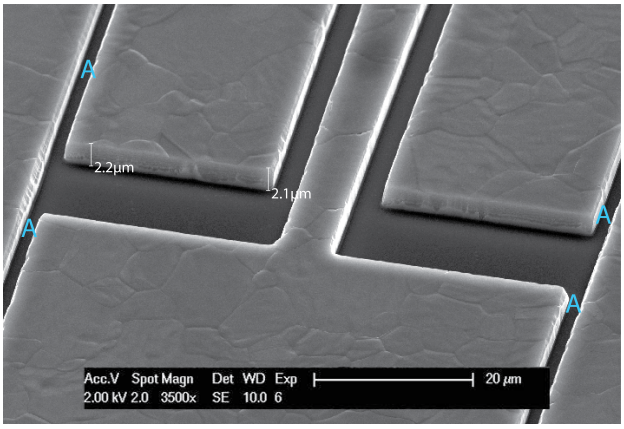

Fig. 12. SEM picture showing a detail of the double slots antenna. The thick aluminum layer is clearly visible and the measurements confirm the thickness of 2μm. No visible aluminum residuals are present in the the structure. The thin opening marked by A are only 1μm wide.

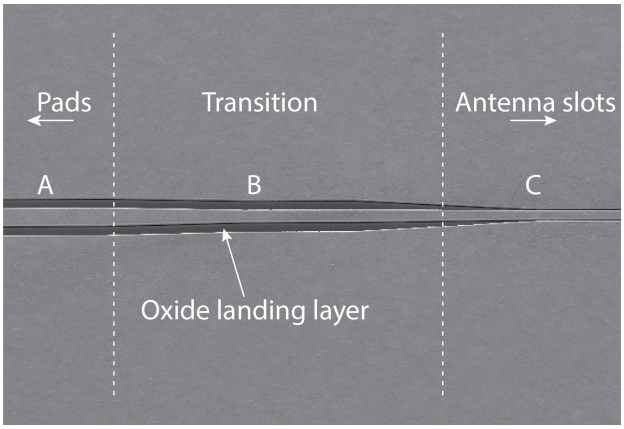

Fig. 13. SEM picture of the transition region on the antenna feeding line.

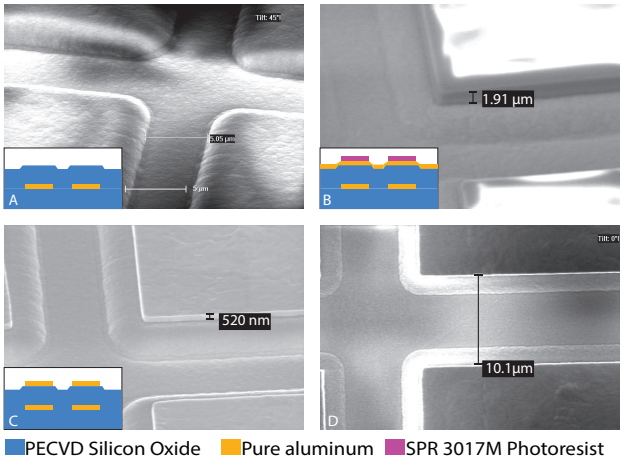

Fig. 14. Series of SEM picture showing the ADL during the fabrication process. A) The 5μm silicon oxide layer is deposited on top of a metal patch layer (see in the inset the layer stack). The brighter area in the figure are given by electron charging phenomena. After the silicon oxide coating, the aluminum layer is deposited and the patches defined by I-line lithography. In B) the photoresist layer is clearly visible and the measured thickness is $\approx 2\mu$m. Due to the non-conductive nature of the layer, electron charging phenomena are clearly visible. Using a dry etching process, the patch layer is defined (C) and the relative distance between the patched measured (D).

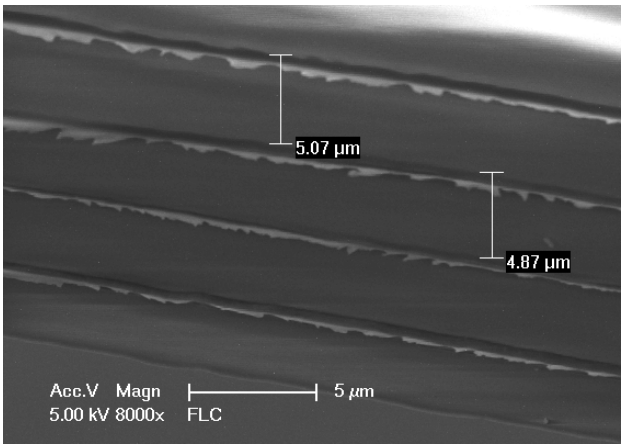

Fig. 15. SEM cross-section showing a detail of the fabricated ADL stack. The overall ADL is $\approx 39\mu$m thick.

is not an issue. After the oxide deposition, a new metal layer is deposited and etched. These process is repeated 7 times. A protective layer of 1μm of PECVD oxide is deposited to prevent possible damages of the ADL during the remaining process steps. The alignment of the different metal layers was done with a standard wafer-stepper, used in IC technology for accurate alignment of the various mask layers. The tool used in this process guarantees a maximum overlay error of 50 nm over the different deposited layers. Simulation have shown that such error has negligible effects on the antenna performance.

To achieve an effective enhancement of the dielectric constant, an accurate control of the oxide thickness and alignment of the metal patches is fundamental. By means of optical reflectometry (Leitz MPV-SP) measurements, the thickness of the layers was determined and carefully monitored during all process steps. A detail of a cross section (Fig. 15) clearly shows the metal patches embedded in the oxide layer. By measuring the oxide thickness, we estimated a maximum thickness deviation of about $\sim$80 nm on the entire wafer area. Numerical simulations have confirmed that such variations

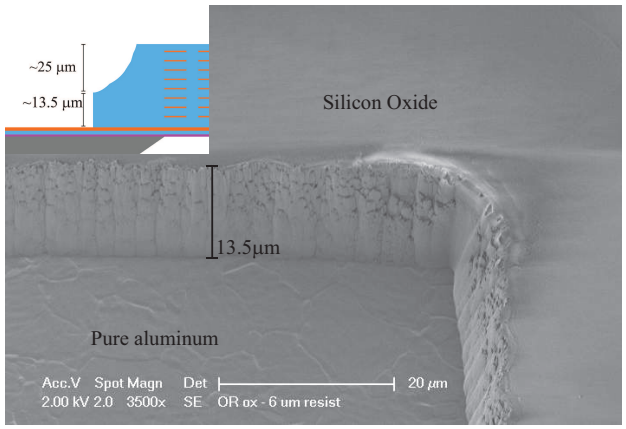

Fig. 16. SEM cross-section showing a detail of the silicon oxide after the etching. The sample is here tilted of 45 to show the inner part of the cavity. The wet etching gives a round corner on the top of the silicon oxide layer (see the schematic in the inset). Approximately 25 μm of silicon oxide are removed with this process. The remaining 13.5μ m are removed by a final dry etching. This last process gives a vertical profile of the etched oxide, clearly visible at the corner.

have negligible effects on the ADL properties.

Using a similar process, a reference test-antenna has been realized on the same substrate, to allow a comparison between the antenna gain with and without the ADL. This structure is similar to the one presented in Fig. 10 and visible on the right side of Fig. 9. These antennas are covered only by the thick oxide layer used to realize the ADL, but no metal patches have been inserted in the fabrication flow.

After the ADL deposition, a final etching is required to remove the thick layer of silicon oxide that covers the antenna contact pads. Due to the large amount of oxide to etch, a single dry etch step would require a very thick photoresist layer to protect the structures and a very long (more than 1 hour) plasma etching. Such long process could cause unwanted phenomena such as photoresist burning or large non-uniformity in the etched layer. For these reasons, a wet/dry combined etching has been performed. To protect the structures, a 12 μ m layer of SPR 3017M photoresist has been used to coat the wafer. After the resist patterning, the oxide is etched in a buffered hydrofluoric acid (BHF) 1:7 solution (etch rate 290 nm/min), for 75 minutes. This step removes approximately $2/3$ of the oxide layer, with a very high uniformity on the wafer area. A final dry etching step is then performed in a Drytek Triode 384T oxide dry etcher. SEM inspection has been performed on the wafer (see Fig. 16) and clearly show the thick oxide being etched and the aluminum layer.

To release the antenna/ADL membrane and the test-antenna membrane, a silicon wet etching in a 33 wt $\%$ KOH at $85\,^{\circ}$C has been lastly performed on the wafer. The wafer backside windows were previously patterned etching the LPCVD silicon nitride layer with a dry etching process. Then, using a special holder, the wafer front-side has been protected from the solution. After the etching (5 hours and 30 minutes), a final rinsing (HNO_3 and water) is performed to clean the wafer. The inspection of the etched cavity has shown that a small mismatch (e=$65 \pm 10\mu$m, see Fig. 11) in the KOH opening position is present. This is probably due to a variation of the wafer thickness and a front-to-back misalignment of the silicon nitride mask used to pattern the wafer backside.

The use of low-stress layer in the ADL fabrication is of

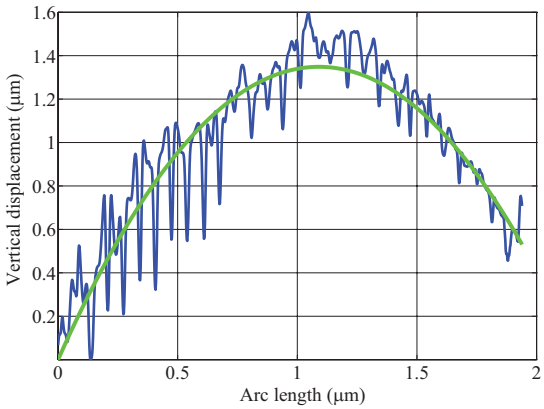

Fig. 17. Membrane vertical displacement obtained by white light interferometry. The maximum deflection is $\approx 1.6\mu$m. The membrane shape can be well fitted by a parabolic trend (green curve).

fundamental importance to achieve a flat structure. To prove that only very small deflections are present, a white light interferometer has been used to map the vertical displacement of the structure. As shown in Fig. 17, the maximum deflection is measured at the center of the membrane, resulting in a maximum displacement of $\approx 1.6\mu$m, almost 10^{-3} times smaller than the membrane side length.

IV. mm-Wave Measurements

The fabricated chip micrograph is shown in Fig. 18(a). The measurement setup consists of an Agilent vector network analyzer (PNA-X N5242A) working from 10 MHz to 26.5 GHz. Frequency extension modules, to operate the VNA in the WR03 band (i.e. 220-325 GHz) band from OML Inc. are used. The feeding to the antenna is realized by using GGB Cascade Infinity ground-signal-ground (GSG) waveguide probes with pitch equal to 100μm. The measured insertion loss of this probe is 1 dB and was calibrated out. The fabricated chip was placed on a metal chuck. A feeding pad to land coaxial probes on the chip of length 105μm and a feeding line was added on the back of the antenna, as labeled in the chip micrograph in Fig. 18(a). The length of this line was selected as 2 mm, to trade off loss levels with scan area: on the one hand, a too short line would cause the bulky wafer probe to be too close to the antenna, limiting the near-field scanning area needed for the radiation pattern measurements; on the other hand a line that is too long would introduce too high losses reducing the accuracy of the measurements.

The long line (i.e., 2mm) is de-embedded from the measured data employing a thru-reflect-line (TRL) technique [16]. Figure 18(b), shows on-chip test structure that are fabricated on the same die as that of the antenna (see Fig. 9) and are measured to apply TRL procedure. The measured de-embedded one port reflection coefficient is presented in Fig. 18(c), compared with the simulations. There is a frequency shift of 6% between the measured and the simulated results. As pointed out earlier in Sec.III, a mismatch during the KOH etching process has resulted in an offset of point P (see Fig. 11) by a distance e=$65 \pm 10\mu$m. The S11, recomputed after including the above-mentioned mismatch in the simulation, is shown in Fig. 18(c). The error difference between simulation and the measurement is now reduced to 3%. Also, the measured and simulated reflection coefficients starts to show a similar trend at the low end of the frequency band (250-280 GHz).

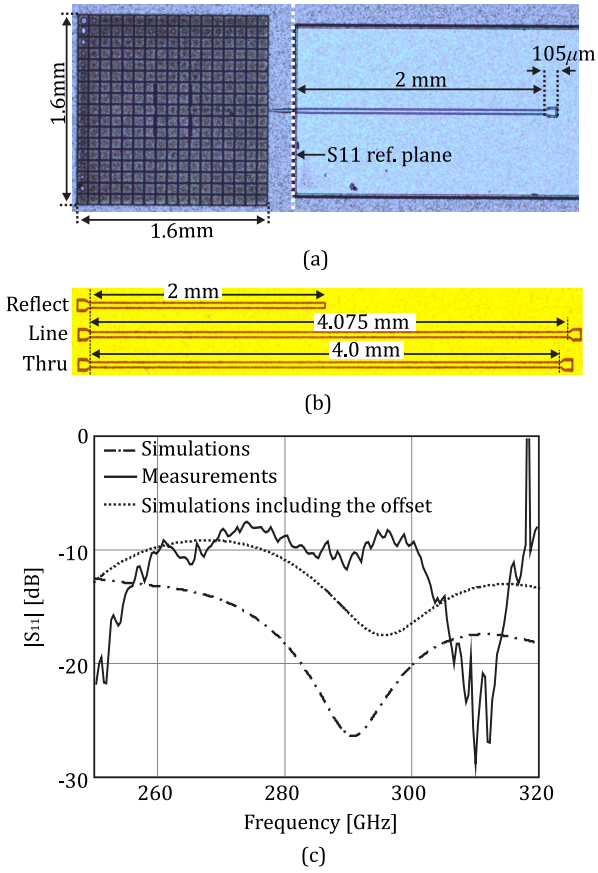

Fig. 18. The fabricated (a) chip micrograph, (b) TRL structure, and (c) simulated and measured reflection coefficient.

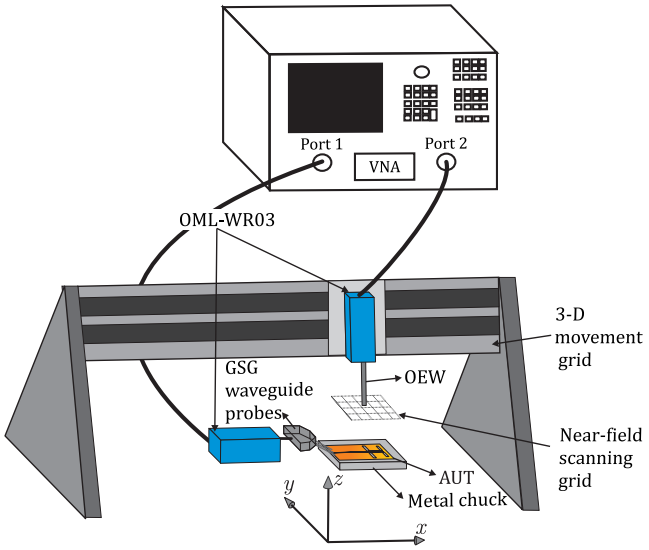

Fig. 19. Schematics of the near-field measurement setup (not to the scale).

The far field radiation patterns are calculated using the near-field measurement setup depicted in Fig. 19 [17]. To avoid the reflections from the metal chuck, commercial absorbers (ECCOSORB MMI-U) are placed below the antenna. A linearly polarized, WR-03 open ended waveguide (OEW) is used to sample the near field of the antenna under test

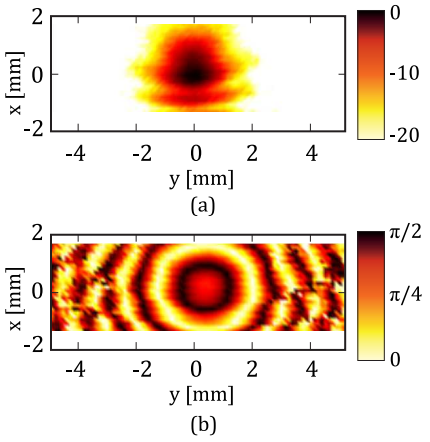

Fig. 20. The measured near field at 300 GHz a). Normalized amplitude in dB b). Phase in radians.

(AUT) on a rectangular grid, while the AUT is kept stationary. The distance between each spatial sample point was set to be $\lambda_0/8$ at 300 GHz, to obtain a high resolution data. The vertical distance (along the z-axis) of the OEW tip from the AUT is about 3.5 mm, i.e. radiative near-field region. The measured normalized amplitude and phase of the electric field radiated by the AUT in the presence of probe is shown in Fig.20 (a) and (b), respectively. Since the AUT and OEW are linearly polarized, only the x-component of the near field was measured. The scan area is rectangular and the maximum of the electric field is around $x = 0$ and $y = 0$, which denotes the center of the AUT. The acquisition of near field data along the $-x$-direction is limited by the presence of the GSG waveguide probe, which is an usual limitation in these type of measurements [4], [8], [18].

The effect of the OEW is de-embedded from the far-field pattern of the AUT by using a standard probe correction technique [19]. The far-field radiation patterns in the upper hemisphere, obtained by Fourier transform of the near-field data, are shown in Fig. 21, in the frequency range from 300-315 GHz. The patterns in the H-plane show an excellent agreement with the simulations. The E-plane patterns are asymmetric and oscillatory. The reason is the scattering from the probe, which interferes with the antenna. Also, the patterns are shown till $\pm 45°$, because the near-field scan area is restricted to ± 1.5 mm (see Fig. 20) by the presence of the wafer probe. Since the near-field area is limited along the x-direction the accuracy of the radiation pattern measurements decreases for angle greater than $\pm 23°$.

At a later moment, a scan over a bigger aperture in the direction where there is no feed probe was carried out. The measured near field data is shown in Fig. 22(a) at 300 GHz. A symmetric near field data is obtained artificially by mirroring the near field data (see Fig. 22(b)) with respect to the x-axis ($x = 0$). Exact symmetry conditions are also imposed on the simulated near field data from CST. The far field patterns after post-processing are shown in Fig.22(c) for both the cases. A better agreement can now be observed between the simulations and the measurements. This approach for artificially symmetrizing the pattern gives an indication of how the antenna would operate in a realistic application scenario, in which there would be no feeding probe.

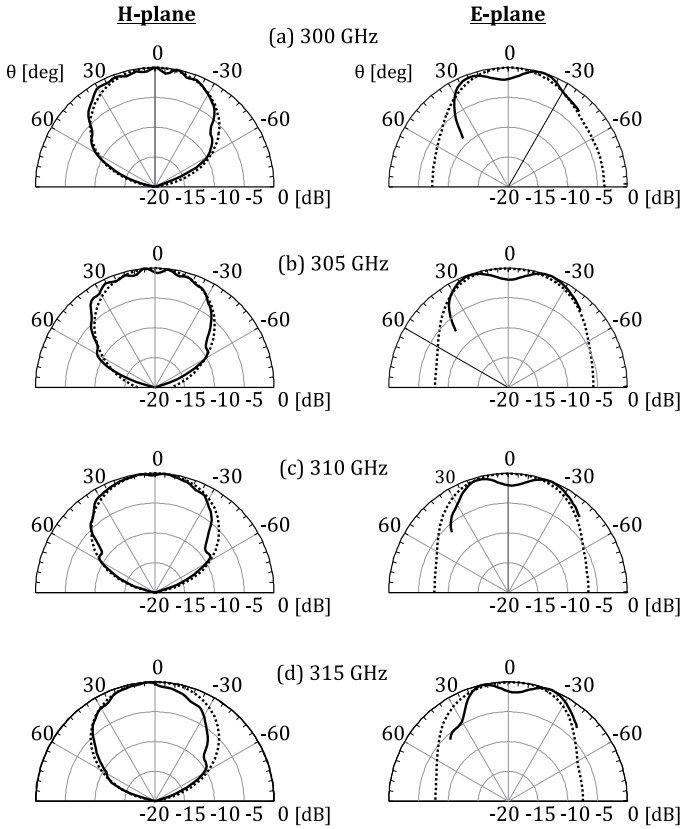

Fig. 21. Measured(-) and the simulated (- -) radiation pattern (dB) with ADL.

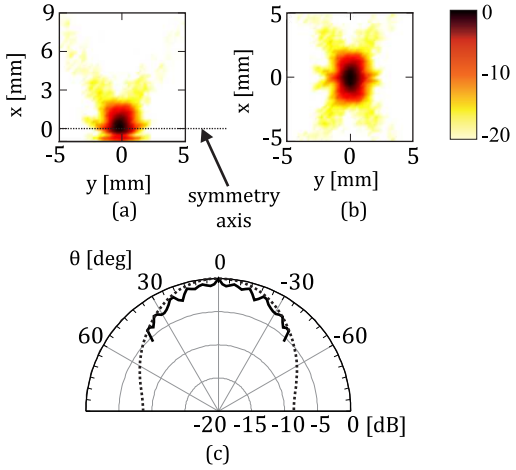

Fig. 22. The near-field expressed in dB (a) measured, and (b) obtained after applying symmetry to the measured data. (c) Measured (-) and the simulated (- -) far-field radiation pattern (dB) in E-plane. The process of symmetry has also been applied for simulated antenna.

Also the reference antenna without the ADL was measured. A comparison between the simulated and the measured far field radiation patterns is shown in Fig. 23, at 300 GHz. Although not shown for the sake of brevity, the radiation patterns at other frequencies show a similar agreement.

The relative difference between the broadside gain of the two antennas (with and without ADL) is presented in Fig. 24. Both simulations and measurements show an improvement of about 2 dB for the ADL loaded antenna with respect to the reference one. The measured results are presented in

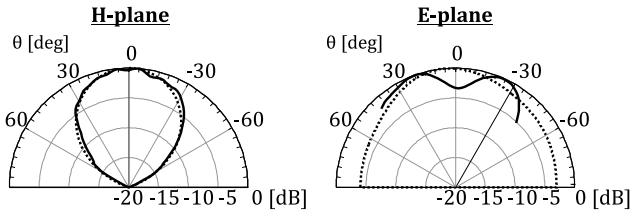

Fig. 23. Measured (-) and the simulated (- -) radiation pattern of the antenna without ADL loading at 300 GHz.

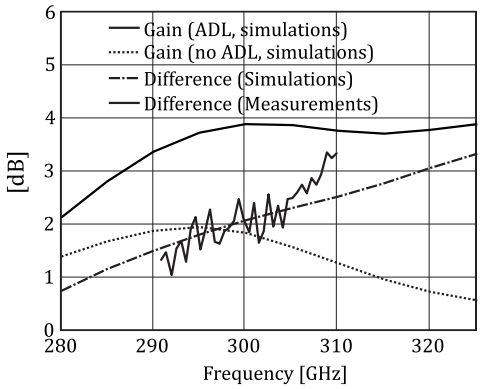

Fig. 24. Simulated gain of the two antennas, with and without the ADL loading; the relative gain difference is also reported and compared with the measured one.

a frequency range of 20 GHz centered at 300 GHz, where the simulated reflection coefficient is well matched for both antenna (see Fig. 4).

V. Conclusions

On-chip integrated antennas typically radiate in the presence of either a lossy silicon substrate or an electrically thin grounded slab. This leads to either high dielectric losses or very narrow bandwidths of operation. To increase the radiation efficiency of such antennas, we demonstrate, at 300 GHz, the effectiveness of artificial dielectrics superstrates, previously proposed at lower frequencies, using printed circuit board technology. In this specific work, the conventional double slot antenna is loaded by an ADL superstrate that substantially increases the front-to-back ratio.

For the fabrication of the antenna and the ADL superstrate, we developed a low-temperature CMOS back-end compatible process. By using pure aluminum as metal and silicon oxide as dielectric host matrix, the ADL was deposited on top of the antenna structure.

The anisotropic properties of the proposed artificial slab allows to achieve high surface-wave efficiency. This is because the ADL is dense and electrically thick for waves radiated by the slot in directions close to the normal, whereas it has lower permittivity and is electrically thin for the waves radiated in directions almost parallel to the slab.

The antenna has a front to back ratio larger than 10 dB, with essentially no power launched in to surface waves. Also an antenna without ADL loading has been fabricated and used as a reference solution to quantify the enhancement due to the ADL. A improvement of about 2 dB in gain has been achieved both in simulations and measurements.

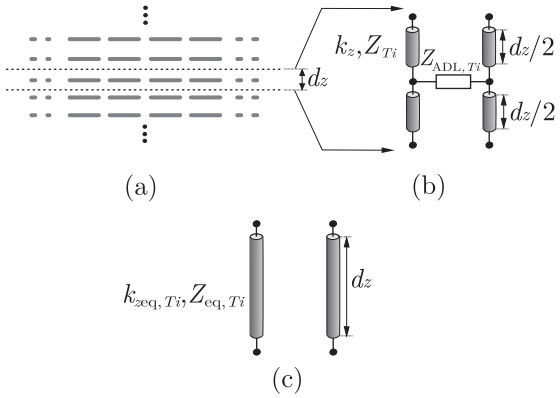

Fig. 25. (a) A 2D view of ADL; (b) a transmission line based representation of a unit cell to retrieve the effective permittivity for TE and TM incidence; and (c) the equivalent transmission line representation of ADL unit cell. Note that Ti can refer to either the TE and TM mode respectively.

The key feature feature of the present ADL superstrate solution is that they can be designed and manufactured independently from the antenna and the IC's. They can be used as add-on components since no alignment is required between the antenna and the superstrate layers. Also, ADL are broadband because of their non-resonant periodic nature. This concept can be beneficial for any on-chip radiating structure, including antenna arrays.

Appendix A: Extraction of Effective Permittivity

In this appendix, we describe the procedure for calculating the effective permittivity values plotted in Fig. 3. To every angle of incidence θ, one can associate a transverse spectral wave number $k_\rho = k\sin\theta$. The parameter k is the propagation constant inside the host medium, $k = k_0\sqrt{\varepsilon_r}$. By solving the equivalent analytical transmission lines for TE and TM modes shown in Fig. 25(b), characterized by $k_z = k\cos\theta$ one can then derive $k_{z\mathrm{eff},TE}$ and $k_{z\mathrm{eff},TM}$ (see Fig.25(c)) respectively using the known expressions for periodically loaded transmission lines [20]:

$$k_{z\mathrm{eff},Ti} = \frac{1}{d_z}\cdot \cos^{-1}\left(\cos(k_z d_z) + j\frac{Z_{Ti}}{2Z_{ADL,Ti}}\sin(k_z d_z)\right) \quad (1)$$

where Ti can refer to either the TE or TM mode respectively. The formula for calculating $Z_{ADL,Ti}$ is analytically derived in closed-form in [12], and it refers to the impedance of a single layer of ADL in an infinite cascade of artificial dielectric layers as depicted in Fig. 25(a). Moreover, the impedance Z_{TE} and Z_{TM} are equal to $\zeta k/k_z$ and $\zeta k_z/k$ respectively, where $\zeta = 120\pi/\sqrt{\varepsilon_r}$ is the impedance of the medium hosting the ADL. The equation to compute the effective permittivity ε_{TiTi} is then:

$$\varepsilon_{Ti,Ti} = \frac{k_{z\mathrm{eff},Ti}^2 + k_\rho^2}{k_0^2}\,. \quad (2)$$

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Waqas H. Syed (S'11) received the B.Sc. degree with distinction in telecommunication engineering from the CIIT, Islamabad, Pakistan in 2007 and M.Sc degree from RWTH Aachen University, Aachen, Germany in 2010.

Currently, he is working towards Ph.D degree at the Terahertz Sensing Group at TU Delft, Delft, NL. His research interests include artificial dielectrics and the design of integrated antennas and arrays.

Giuseppe Fiorentino (S'14) was born in Naples, Italy, in 1983. He received the B.S. and M.S. degrees in solid state physics from the University of Naples Federico II, Naples, in 2007 and 2009, respectively. During his Master's thesis, he joined the ENEA Research Center, Portici, Italy, where he worked on the fabrication by dielectrophoresis of palladium and zinc oxide nanowires for sensing applications. He later joined as a Researcher the Nanotechnology Group, ENEA Research Center, working on porous silicon application for drug delivery applications. In 2011, he began pursuing the Ph.D. in the Laboratory of Electronic Components Technology and Materials, Technical University of Delft, Delft, The Netherlands, on the design and fabrication of an innovative metamaterials for terahertz sensing applications. His research also includes the realization and characterization of MEMS and NEMS devices by atomic layer deposition.

Daniele Cavallo (S'09−M'11) received the M.Sc. degree (*summa cum laude*) in telecommunication engineering from the University of Sannio, Benevento, Italy, in 2007, and his Ph.D. degree (*cum laude*) in electromagnetics from Eindhoven University of Technology (TU/e), Eindhoven, Netherlands, in 2011.

From January 2007 to November 2011, he was with the Antenna Group at the Netherlands Organization for Applied Scientific Research (TNO Defense, Security and Safety), The Hague, Netherlands. From December 2011, he is Postdoctoral researcher in the EEMCS department of Delft University of Technology, Delft, Netherlands. He is the author or coauthor of more than 60 papers published in peer-reviewed international journals and conference proceedings. His research interests include analytical and numerical methods for antenna characterization, the design of antenna arrays and terahertz antennas.

Dr. Cavallo was first author of the paper awarded with the best innovative paper prize at the 30th ESA Antenna Workshop in 2008 and nominee for the best doctoral project in the TU/e Academic Annual Awards 2012. He has been awarded a three-year personal grant from the Netherlands Organization for Scientific Research (NWO VENI, 250 keuro), for developing "Efficient On-Chip Antennas for Terahertz Applications". He is a member of the European Association on Antennas and Propagation (EurAAP).

Marco Spirito (S'01−M'08) received the M.Sc. degree (*summa cum laude*) in electrical engineering from the University of Naples Federico II, Naples, Italy, in 2000, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 2006.

From 2000 to 2001, he was a guest at Infineon Technologies, Munich, Germany. In 2006, he joined the department of Electronics and Telecommunications Engineering, University of Naples Federico II. In April 2008 he joined the Electronics Research Laboratory at the Delft University of Technology as an Assistant Professor, where he is an Associate Professor since April 2013. His research interests include the development of advanced characterization setups and calibration techniques for millimeter and sub-millimeter waves, and the design and integration of mm-wave sensing systems.

Dr. Spirito was the recipient of the Best Student Paper Award for his contribution to the 2002 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) he received the IEEE MTT Society Microwave Prize in 2008, was a co-recipient of the best student paper award at IEEE RFIC 2011, and the GAAS Association Student Fellowship in 2012.

Pasqualina M. Sarro (M'84−SM'97−F'07) received the Laurea degree (*summa cum laude*) in solid-states physics from the University of Naples, Italy, in 1980.

From 1981 to 1983, she was a post-doctoral fellow in the Photovoltaic Research Group of the Division of Engineering, Brown University, Rhode Island, U.S.A. In 1987, she received the Ph.D. degree in Electrical Engineering at the Delft University of Technology, the Netherlands. Since then, she has been with the Delft Institute of Microsystems and Nanoelectronics (DIMES), at the Delft University, where she is responsible for research on integrated silicon sensors and MEMS technology. In December 2001 she became A.van Leeuwenhoek Professor in the Department of Microelectronics.

In 2004 she received the EUROSENSORS Fellow Award for her contribution to the field of sensor technology. In April 2006 she became member of the Royal Netherlands Academy of Arts and Sciences (KNAW) and in November 2006 she was elected IEEE Fellow for her contribution to micromachined sensors, actuators and microsystems. Since 2009 she is the Chair of the Department of Microelectronics. In 2012 she received the IEEE Sensor Council Meritorious Service Award. She has authored and co-authored more than 500 journal and conference papers and supervised a large number of MSc and PhD students. She is a member of the technical program committee and steering committee for several international conferences (IEEE MEMS, IEEE Sensors, Eurosensors, Transducers); Technical Program Co-chair for the First IEEE Sensors 2002 Conference and Technical Program Chair for the Second and Third IEEE Sensors Conference (2003 and 2004); General co-chair of IEEE MEMS 2009, general co-Chair for IEEE Sensors 2014 and TPC co-chair for Transducers 2015. She has been associate editor for IEEE Sensors Journal and is now Associate Editor for the IEEE Journal of Microelectromechanical Systems.

Andrea Neto (M'00−SM'10) received the Laurea degree (*summa cum laude*) in electronic engineering from the University of Florence, Florence, Italy, in 1994 and the Ph.D. degree in electromagnetics from the University of Siena, Siena, Italy, in 2000.

Part of his Ph.D. degree was developed at the European Space Agency Research and Technology Center, Noordwijk, The Netherlands, where he worked for the antenna section for over two years. In the years 2000−2001, he was a Post-Doctoral Researcher at the California Institute of Technology, Pasadena, CA, USA, working for the Sub-Millimeter-Wave Advanced Technology Group. From 2002 to January 2010, he was a Senior Antenna Scientist at TNO Defence, Security, and Safety, The Hague, The Netherlands. In February 2010, he was appointed Full Professor of Applied Electromagnetism in the Electrical Engineering, Mathematics and Computer Science Department, Technical University of Delft, Delft, The Netherlands, where he formed and leads the THz Sensing Group. His research interests are in the analysis and design of antennas, with emphasis on arrays, dielectric lens antennas, wideband antennas, EBG structures, and THz antennas.

Prof. Neto was corecipient of the H. A. Wheeler award for the best applications paper of the year 2008 in the IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION. He was corecipient of the best innovative paper prize at the 30th ESA Antenna Workshop in 2008. He was corecipient of the best antenna theory paper prize at the European Conference on Antennas and Propagation (EuCAP) in 2010. He served as an Associate Editor of the IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION (2008−2013) and IEEE ANTENNAS AND WIRELESS PROPAGATION LETTERS (20052013). He is member of the Technical Board of the European School of Antennas and organizer of the course on Antenna Imaging Techniques. He is a member of the steering committee of the network of excellence NEWFOCUS, dedicated to focusing techniques in mm and sub-millimeter-wave regimes. In 2011 he was awarded the European Research Council Starting Grant to perform research on Advanced Antenna Architectures for THz Sensing Systems. He was the Awards and Grants Chair for EUCAP 2014.