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On Basic Boolean Function Graphene Nanoribbon Conductance Mapping

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***Abstract*— In this paper, we augment a trapezoidal Quantum Point Contact topology with top gates to form a butterfly Graphene Nanoribbon (GNR) structure and demonstrate that by adjusting its topology, its conductance map can mirror basic Boolean functions, thus one can use such structures instead of transistors to build carbon-based gates and circuits. We first identify by means of Design Space Exploration specific GNR topologies for 2- and 3-input {AND, NAND, OR, NOR, XOR, XNOR} and demonstrate by means of the Non-Equilibrium Green Function - Landauer based simulations that butterfly GNR-based structures operating at $V_{DD} = 0.2$ V outperform 7 nm @$V_{DD} = 0.7$ V CMOS counterparts by 2 to 3, 1 to 2, and 3 to 4, orders of magnitude in terms of delay, power consumption, and power-delay product, respectively, while requiring 2 orders of magnitude less active area. Subsequently, we investigate the effect of V_{DD} variations and the V_{DD} value lower bound. We demonstrate that the NOR butterfly GNR structures are quite robust as their conductance and delay are changing by no more than 2% and 6%, respectively, and that AND and NOR GNR geometries can operate even at 10 mV. Finally, we consider the aspects related to the practical realization of the proposed structures and conclude that even if there are still hurdles on the road ahead the latest graphene fabrication technology developments, e.g., surface-assisted synthesis, our proposal opens an alternative towards effective carbon-based nanoelectronic circuits and applications.**

***Index Terms*— Graphene, GNR, graphene-based Boolean Gates, carbon-nanoelectronics.**

I. Introduction

With CMOS scaling approaching atomic feature size, the faster switching speed comes at the expense of increased power density and leakage, decreased reliability and yield, increased production costs, and as a result diminishing returns. Therefore, the development of new materials, structures, and computation paradigms are called upon [1], [2]. One of the post-Si forerunners is graphene, which has enjoyed a research surge in the past decade, paving the way for a wide range of graphene-based applications, e.g., spintronics, photonics and optoelectronics, sensors, energy storage and conversion, and biomedical [3].

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Graphene is a two-dimensional carbon allotrope, in which the carbon atoms are arranged in a honeycomb lattice. Graphene has a wealth of unique, remarkable physical and electronic properties, among which ballistic charge transport, room temperature carrier mobility 10× higher than Si, and ultimate thinness, and offer the possibility of low-cost mass production, providing a strong drive to investigate its usage as a potent contender to Si technology and promising avenue for carbon-based nanoelectronics [4], [5], [6]. Generally speaking, the main impediments to graphene-based Boolean logic can be divided into design and manufacturing related [7], [8], [9], [10], [11]. From the manufacturing point of view, finding a cost-effective, scalable and reliable manufacturing process, which enables mass-production with minimum defects density and highly reproducible features, is the main desideratum. From the design perspective, several aspects have to be considered: (i) ability to control conductivity and yield distinguishable "on" and "off" states, while (a) not compromising any of the graphene intrinsic highly advantageous properties (e.g., high carrier mobility), and (b) providing an I_{ON}/I_{OFF} ratio in the order of 10^6 to 10^7 (i.e., the typical ratio for low power <20nm Si logic process), (ii) encoding the desired Boolean logic transfer function into the graphene electrical characteristics (e.g., conduction maps), (iii) finding proper external electric means (e.g., top gates, back gates) to control the graphene behavior and induce the desired logic functionality, and (iv) ensuring the conditions for cascading digital circuits (i.e., clean and compatible/matching electric levels, e.g., voltage, current, for the gates inputs and outputs).

In this paper, we address (ii) and (iii) related issues and demonstrate that by augmenting the trapezoidal Quantum Point Contact (QPC) topology in [12] with top gates to form a butterfly GNR we can modulate its conductance by means of external voltages, such that it mirrors the behavior of basic Boolean functions. In particular, we consider the basic set of Boolean functions {AND, NAND, OR, NOR, XOR, XNOR} and perform a Design Space Exploration (DSE) with regard to GNR topology and dimensions, such that for each function we identify a GNR structure able to provide the conductance map (conductance G vs. top gate voltages) reflecting its truth table (high G for logic "1", low G for logic "0"). For modelling GNRs' electronic transport properties we employ the NEGF-Landauer formalism [12], [13].

Our simulations indicate that the obtained 2-input butterfly GNR-based structures operating at $V_{DD} = 0.2$V outperform

7nm @V_{DD} = 0.7V CMOS counterparts by 2, 1 to 2, and 3 to 4, orders of magnitude in terms of delay, power consumption, and power-delay product, respectively, while requiring 2 order of magnitude less active area. For 3-input function the butterfly GNR based approach proved to be even more effective, i.e., 2 to 3, 1 to 2, and 3 to 4, orders of magnitude in terms of delay, power consumption, and power-delay product, respectively. Moreover our approach is less sensitive to gate fan-in scaling as when incrementing it from 2 to 3 CMOS area footprint (delay) increases by up to 100% (51%) while for the GNR structures area (delay) changes are up to 26% (42%). We also compared with state of the art graphene based 2-input gates and obtained: (i) 1 order of magnitude smaller delay for all 2-input structures, when compared to [14], and (ii) 3, 1, 1, and 2 orders of magnitude smaller area, delay, power consumption, and power-delay product, respectively, when compared to the NAND in [15].

We subsequently concentrate on the effect of V_{DD} variations and on determining V_{DD} lower bound value. To this end we simulate NOR butterfly GNR structures while changing V_{DD} with $\pm$10% in increments of 2% with respect to the nominal voltage V_{DD} = 0.2V. These experiments reveal that GNR conductance and delay are changing by no more than 2% and 6%, respectively. Concerning V_{DD} lower bound we present AND and NOR GNR geometry able to operate even at 10mV and demonstrate that it is rather GNR geometry and contact topology dependent, 20mV for the considered structures.

Finally, we discuss GNR fabrication status, difficulties and challenges, and explore edge defects influence on butterfly GNR conductance. Our results indicate that GNR's conductance variation is rather substantial, even due to one missing atom in the constriction edge, conductance ratio is decreasing but is also experiencing substantial increase, which is quite interesting as it suggests that defects might be helpful rather than harmful, and despite the performance degradation the GNR can still deliver the expected Boolean functionality. This together with the fact that surface-assisted synthesis approach was utilized to fabricate atomically precise, low-edge-defect GNRs, e.g., 3-Armchair GNRs (1 hexagon width) and 6-Zigzag GNRs (6 hexagon width) [16] indicate that our proposal opens an alternative towards effective carbon-based nanoelectronic circuits and applications.

The remaining of this paper is structured as follows: Section II presents an overview of the utilized simulation framework. Section III entails DSE results in terms of GNR topologies and their afferent conductance maps mirroring the basic set of 2- and 3-input Boolean functions. Section IV presents simulation results (i.e., area, delay, robustness to V_{DD} variation, V_{DD} lower bound), comments on the potential of GNR-based Boolean logic design, discusses GNR fabrication status, difficulties and challenges, and analysis the potential impact of GNR edge defects. Finally, concluding remarks are given in Section V.

II. Simulation Framework

In this paper, we explore the potential of using GNRs as basic building blocks (other than transistors) for future GNR-based logic gates and mainly deal with the following problem:

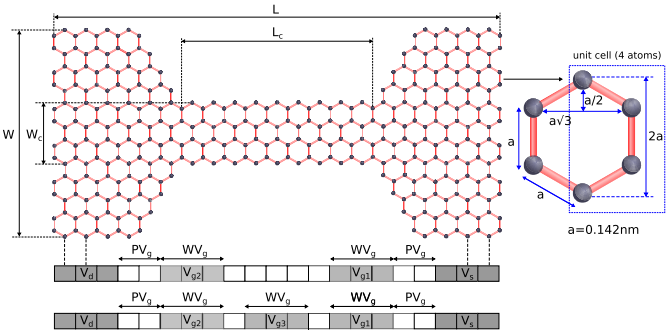

Fig. 1. Butterfly Graphene Nanoribbon (GNR).

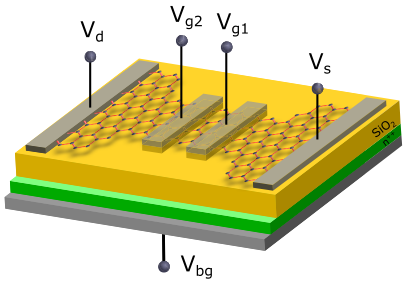

Fig. 2. Butterfly GNR-based basic structure.

Given an initial GNR shape and a basic Boolean function, determine the GNR topology, geometry, and means to modulate its conductance (via, e.g., external gate voltages), such that it mirrors the desired logic functionality while providing good conduction properties, e.g., I_{ON}/I_{OFF} ratio. In relation with this, we subsequently describe: (i) the underlying GNR-based structure, (ii) the utilised simulation model, which is able to capture graphene electronic ballistic transport properties, and (iii) the design space exploration methodology we employ in order to identify a GNR geometry, which conductance best reflects a given Boolean function.

As GNR research vehicle, we build upon the trapezoidal Quantum Point Contact with zig-zag edge alignment, described in [12]. We characterise its geometry and topology as graphically defined in Figure 1 and further denote it as butterfly GNR. As illustrated in Figure 2, we employ the butterfly GNR as a conduction channel, through which the current flow (i) is induced via a bias voltage (i.e., $V_d - V_s$) applied between the drain and source contacts of the graphene sheet, and (ii) is modulated by input voltages (i.e., V_{g1} and V_{g2}), which are applied via the two (in this case) top gates. Graphene's back face is biased by V_{back}, which in manufactured devices is typically a small fraction of the back gate potential, i.e., V_{bg}, (because of the significant potential drop on the dielectric layer - usually SiO_2 - residing underneath the graphene ribbon).

Based on this GNR structure, we vary the nanoribbon geometry and the gate contacts topology, until a conduction map reflecting the desired Boolean functionality, is obtained. We initially consider the set of 2-input Boolean functions {AND, NAND, OR, NOR, XOR, XNOR}, and apply voltage levels via the two top gates, as illustrated in Figure 2. We convene to use 0V and 1V as the voltage levels afferent to

logic "0" and logic "1". We note that this choice is solely for explanatory purpose and is not restrictive in any way; one can also choose other voltage levels (e.g., 10× smaller), and for a certain Pareto butterfly GNR geometry, obtain a conduction map that complies with the desired Boolean logic. We set the left contact (drain) and the right contact (source) voltage to 0.2V and 0V, respectively. For each Boolean logic function, we perform a Design Space Exploration (DSE) by varying the following: (i) the butterfly GNR dimensions defined in terms of the distance between adjacent carbon atoms, a (1.42Å), as depicted in Figure 1 (i.e., the nanoribbon total width, W, and length, L, from 41a to 47a and from $25\sqrt{3}$ a to $27\sqrt{3}$ a, respectively; and the constriction width, W_c and length, L_c, from 2a to 35a and from $3\sqrt{3}$ a to $12\sqrt{3}$ a, respectively), (ii) the top gate contacts topology (i.e., the distance between the two top gate contacts and the source/drain contacts, P_{Vg}, from $2\sqrt{3}$ a to $6\sqrt{3}$ a, and the contact width, W_{Vg} from $3\sqrt{3}$ a to $7\sqrt{3}$ a), and (iii) V_{back} from -1V to 1V (in increments of 0.2V).

For each design point, we derive the conductance map with respect to the 2-input top gate voltages. For modelling the electronic ballistic transport in GNRs, we employ the Non-Equilibrium Green Function (NEGF) quantum transport model, the semi-empirical Tight Binding (TB) computations to obtain the system Hamiltonian, and the Landauer formalism to derive GNR's current and conductance [12], [13], [17]. In particular, the GNR channel is described by a Hamiltonian matrix H, which incorporates all internal and external potentials (e.g., top gates and back gate voltages). H is constructed using semi-empirical TB computations, as:

$$H = \sum_{i,j} t_{i,j} |i\rangle\langle j|, \tag{1}$$

$$\text{where } t_{i,j} = \begin{cases} 0, & \text{if atoms } i \text{ and } j \text{ are not adjacent} \\ \tau, & \text{otherwise,} \end{cases} \tag{2}$$

and $\tau = -2.7$eV. On the channel end sides the drain and source contacts with different electrochemical potentials sustain the channel conduction and the contact channel interactions are modelled via the contact self-energy matrices Σ_1 and Σ_2, respectively. After H and $\Sigma_{1,2}$ are derived, the transmission function $T(E)$, which models the probability of one electron being transmitted between the source and the drain contacts, is computed as a function of energy as:

$$T(E) = \text{Trace}\left[\Gamma_1 \, G_R \, \Gamma_2 \, G_R^{\dagger}\right] \tag{3}$$

where

$$G_R(E) = [EI - H - \Sigma_1 - \Sigma_2]^{-1}$$
$$\Gamma_{1,2} = i[\Sigma_{1,2} - \Sigma_{1,2}^{\dagger}].$$

The channel current is then derived based on Landauer formula, as:

$$I = \frac{q}{h} \int_{-\infty}^{+\infty} T(E) \cdot (f_0(E - \mu_1) - f_0(E - \mu_2)) \, \mathrm{d}E, \tag{4}$$

where $f_0(E)$ denotes the Fermi-Dirac distribution function at temperature T, and $\mu_{1,2}$ represent the source and drain contacts Fermi energy. Finally, the conductance writes as:

$$G = \frac{I}{V_d - V_s}. \tag{5}$$

Generally speaking, the Poisson equation, which accounts for electron-electron interactions should be utilised for deriving the self-consistent solution of the transport equations. However, the Poisson equation can be ignored when calculating GNR's current or conductance for small bias voltages and/or energy scale for which the density of states doesn't changes dramatically, thus the current is independent of the precise spatial potential [13]. In our experiments, we initially simulated GNR conductance values by making use of the transport model with and without Poisson equation. As the obtained conductance values were almost the same with and without the Poisson equation we decided to ignore it in the following GNR simulations.

The convergence criteria that we employed for the Pareto conduction maps are threefold: (i) for each (V_{g1}, V_{g2}) pair of inputs ((0, 0), (0, 1), (1, 0) and (1, 1)), the conductance magnitude should mirror the desired Boolean output logical value, (ii) the standard deviation of all conductance values corresponding to logic "0" (logic "1") should be smaller than a certain imposed percentage, e.g., 10%, and (iii) given that no optimization with respect to the I_{ON}/I_{OFF} ratio is targeted, the worst ratio between the logic "1" and logic "0" conductance should be ≥ 10. Note that for 3-input Boolean functions the same DSE methodology applies.

III. GNR Conduction Carving

This section present DSE results for 2- and 3-input {AND, NAND, OR, NOR, XOR, XNOR} Boolean functions and some comments on the potential applicability of our results for graphene-based Boolean logic gate implementations.

A. 2-Input Boolean Functions

Table I summarizes the optimal butterfly GNR dimensions and back bias voltages, which resulted from the DSE, afferent to each considered 2-input Boolean logic function. All 6 butterfly GNR shapes have the same total width and similar length, but different constriction width and length. The constriction width has a bigger impact on conductance (when compared to the constriction length influence), and thus, its value significantly varies between GNRs corresponding to different Boolean functions. One can also observe in the Table that the distance between the top gate contacts and the source/drain contacts is larger for {NAND, NOR, XOR} and smaller for {AND, OR, XNOR}, while the contact width remains the same for all 6 Boolean functions. As for the V_{back} value, 0V or a low value (≤ 0.4V) is enough to enable the most appropriate top gate control on the conductance. The conduction density maps (conductance G vs. input voltages V_{g1}, and V_{g2} between -1V and 1V) exhibited by the 6 butterfly GNR structures described in Table I are presented in Figure 3. The 4 red outlined squares emphasized in each density plot are denoting the high or low GNR conductance values corresponding to the 4 possible input voltages (V_{g1}, V_{g2}) combinations

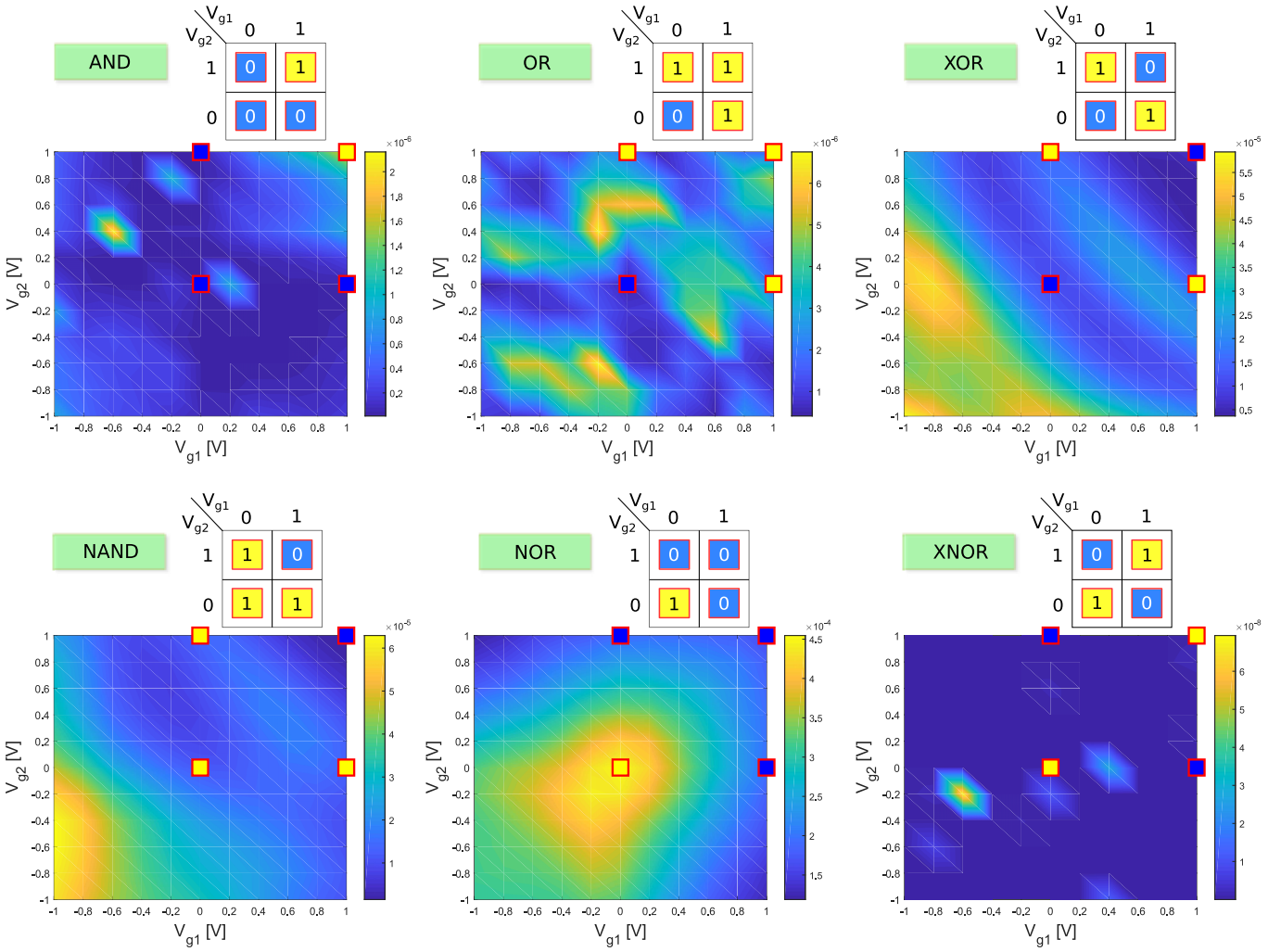

Fig. 3. 2-input boolean functions conduction maps.

TABLE I
2-INPUT BUTTERFLY GNR TOPOLOGIES

	AND	NAND	OR	NOR	XOR	XNOR
W [a]	41	41	41	41	41	41
L [a]	$25\sqrt{3}$	$27\sqrt{3}$	$27\sqrt{3}$	$25\sqrt{3}$	$25\sqrt{3}$	$27\sqrt{3}$
W_c [a]	8	8	14	20	8	14
L_c [a]	$5\sqrt{3}$	$5\sqrt{3}$	$11\sqrt{3}$	$9\sqrt{3}$	$5\sqrt{3}$	$10\sqrt{3}$
P_{V_g} [a]	$2\sqrt{3}$	$6\sqrt{3}$	$4\sqrt{3}$	$6\sqrt{3}$	$6\sqrt{3}$	$3\sqrt{3}$
W_{V_g} [a]	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$
V_{back} [V]	0	0.4	0	0.4	0.4	0.2

(0, 0), (0, 1), (1, 0), and (1, 1). As color convention we utilize yellow for logic "1" conductance (high conductance) and blue for logic "0" conductance (low conductance). For each density plot, the corresponding Karnaugh map mirrored in the conductance magnitude is also displayed. Let us consider for instance the 2-input XNOR GNR structure. The two yellow points correspond to high conductance values (9.23×10^{-10} S and 1.03×10^{-9} S), while the two blue points correspond to low conductance values (1.90×10^{-11} S and 1.78×10^{-11} S). We note that the blue and yellow colors that we utilised for the 4 conductance square points have no significance in relation with the density map color legend, they just denote a low and a high point conductance, respectively. The best and worst high/low conductance ratios for XNOR are 58 and 49, respectively, and logic "1" ("0") conductance values dispersion is 6% (under 10% for all the mapped functions), which enables robust operation.

B. 3-Input Boolean Functions

To explore butterfly GNR structure scalability with respect to the number of inputs, we added a third top gate (equidistant top gates) to enable the possibility to mirror 3-input Boolean gate functionality. The 3-input butterfly GNR structures are similar with the 2-input counterparts geometry-wise, as summarized in Table II, which demonstrates its capability to accommodate multiple top gate inputs.

The obtained conductance maps (conductance G vs. input voltages V_{g1}, V_{g2} and V_{g3} between -1V and 1V) corresponding to the 6 butterfly GNR structures described in Table II,

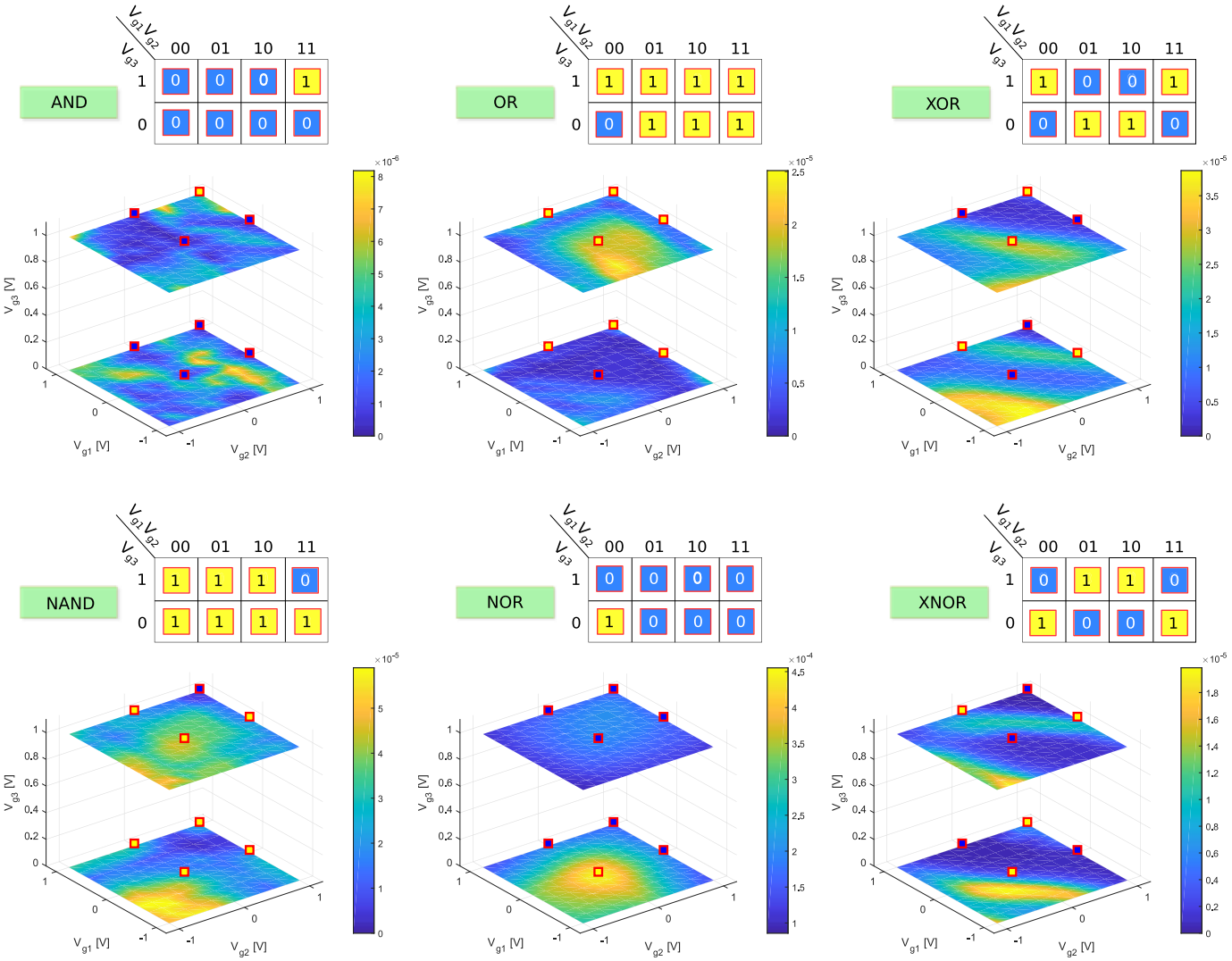

Fig. 4. 3-input boolean functions conduction maps.

TABLE II
3-INPUT BUTTERFLY GNR TOPOLOGIES

	AND	NAND	OR	NOR	XOR	XNOR
W [a]	47	47	41	41	41	41
L [a]	$25\sqrt{3}$	$25\sqrt{3}$	$27\sqrt{3}$	$29\sqrt{3}$	$29\sqrt{3}$	$29\sqrt{3}$
W_c [a]	17	17	8	20	2	2
L_c [a]	$5\sqrt{3}$	$5\sqrt{3}$	$5\sqrt{3}$	$13\sqrt{3}$	$7\sqrt{3}$	$7\sqrt{3}$
P_{V_g} [a]	$5\sqrt{3}$	$6\sqrt{3}$	$5\sqrt{3}$	$4\sqrt{3}$	$5\sqrt{3}$	$5\sqrt{3}$
W_{V_g} [a]	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$
V_{back} [V]	0	0.2	0.2	1	0.8	0.6

are depiced in Figure 4 in a double layered manner. The top layer corresponds to $V_{g3} = 1$ V, and all possible combinations of the other two inputs (V_{g1}, V_{g2}), while the bottom layer corresponds to $V_{g3} = 0$ V. The 8 red outlined squares on the two conductance density plot layers reflect the Boolean output logic value ("0" or "1") corresponding to the 8 possible input combinations: (0, 0, 0), (0, 0, 1), (0, 1, 0), (0, 1, 1), (1, 0, 0), (1, 0, 1), (1, 1, 0), (1, 1, 1). One can observe that the conductance values are in good agreement with {AND, NAND, OR, NOR, XOR, XNOR} true tables, which proves the ability of the butterfly GNR (or GNR in general for that matter) to reflect more complex Boolean functions.

C. Discussion

Some remarks are at hand in relation with the structures introduced above.

While we demonstrated that one single GNR can deliver a Boolean gate behaviour the I_{ON}/I_{OFF} ratio it is rather low (e.g., 38 for the AND function, 49 for the XNOR function for 2-input butterfly GNR structures). However, this can be enhanced by doping [18], or by using per se sawtooth shaped gate contacts instead of rectangular shaped ones [19], or by any other band gap engineering method reported in the literature.

TABLE III
2-INPUT GNRS AND 7nm CMOS GATES PROPAGATION DELAY, AREA, AND POWER

	$\tau_p[ps]$		Active Area $[nm^2]$		Power $[nW]$		Power-delay Product $[ps\text{-}nW]$	
	GNR	CMOS	GNR	CMOS	GNR	CMOS	GNR	CMOS
AND	$2.790 \cdot 10^{-2}$	9.618	$2.428 \cdot 10^{1}$	$1.452 \cdot 10^{3}$	$4.135 \cdot 10^{1}$	$6.242 \cdot 10^{2}$	1.1560	$6.003 \cdot 10^{3}$
NAND	$1.931 \cdot 10^{-2}$	7.556	$2.719 \cdot 10^{1}$	$0.968 \cdot 10^{3}$	$7.218 \cdot 10^{1}$	$5.247 \cdot 10^{2}$	1.3940	$3.965 \cdot 10^{3}$
OR	$1.271 \cdot 10^{-2}$	8.309	$2.453 \cdot 10^{1}$	$1.452 \cdot 10^{3}$	$3.505 \cdot 10^{1}$	$5.535 \cdot 10^{2}$	0.4453	$4.599 \cdot 10^{3}$
NOR	$1.948 \cdot 10^{-2}$	9.175	$2.698 \cdot 10^{1}$	$0.968 \cdot 10^{3}$	$9.884 \cdot 10^{1}$	$4.528 \cdot 10^{2}$	1.9250	$4.155 \cdot 10^{3}$
XOR	$1.086 \cdot 10^{-2}$	9.168	$2.428 \cdot 10^{1}$	$2.420 \cdot 10^{3}$	$8.165 \cdot 10^{1}$	$1.049 \cdot 10^{3}$	0.8864	$9.616 \cdot 10^{3}$
XNOR	$1.602 \cdot 10^{-2}$	10.870	$2.452 \cdot 10^{1}$	$2.904 \cdot 10^{3}$	$6.005 \cdot 10^{1}$	$1.229 \cdot 10^{3}$	0.9617	$1.336 \cdot 10^{4}$

Improving $I_{\text{ON}}/I_{\text{OFF}}$ ratio is future work part of the actual gate design and is beyond the scope of this paper. The GNR shape determines the carrier confinement properties, and as a consequence, in our case, it can open an energy bandgap of, e.g., up to 0.65eV for the butterfly GNR which mirrors the XNOR function. A bandgap of this magnitude was deemed sufficient to effectively switch off a manufactured graphene based device [20].

One can also rely on a butterfly GNR topology, which makes use of one top gate and one back gate in order to apply two Boolean inputs. In this case, V_{back} modulates the energy Fermi level at the Dirac point and thus the back-gated GNR can deliver a much higher $I_{\text{ON}}/I_{\text{OFF}}$ ratio ($10^4\times$ bigger ratio) when compared to the top gate applied inputs case. However, as the graphene sheet and the back gate contact is generally separated by a thick dielectric layer (e.g., ≈300nm SiO_2), back-gated GNR topologies were proven to suffer from very large parasitic capacitances [12], [21], rendering them, at least in the current development state, rather impractical when compared to top-gated GNR structures.

IV. PERFORMANCE EVALUATION

In this section we are concerned with the evaluation of the potential performance of the proposed structures. Given that they are able to deliver basic Boolean gate behaviours the number we report are giving an indication about the expected performance of fully designed butterfly GNR based gates. Apart of the usual area, delay, and power consumption figures of merit we also investigate the sensitivity of the proposed structures to V_{DD} variations and edge defects and attempt to determine the V_{DD}'s lower bound for proper operation.

A. Propagation Delay, Area, and Power

While the butterfly GNR-based structure, graphically depicted in Figure 2, is not a fully design gate it can be regarded as the main building block of a GNR-based Boolean gate. Thus, by analyzing the performance of its 2- and 3-input instances we can gain some insight - even though speculatively - into the potential merit of our approach when compared with CMOS and other Graphene based state of the art designs. To this end, we first evaluate the butterfly GNRs mapping the basic set of 2- and 3-input Boolean functions @$V_{\text{DD}} = 0.2$V and the Boolean logic gate counterparts implemented in a commercial 7nm ($V_{\text{DD}} = 0.7$V) CMOS technology. We are interested in the worst case input to output propagation delay, the active area footprint (the conduction channels area), and power consumptions. The CMOS gates figures were measured in Cadence RTL Compiler [22].

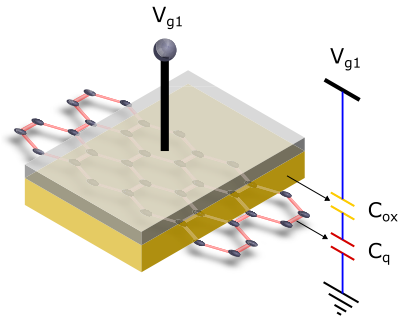

Fig. 5. Top gate capacitance.

For deriving the GNR propagation delay, we assume that a 12nm Al_2O_3 layer is utilized as insulator underneath the top gate contacts [23], and compute the delay τ_p by using Elmore RC delay, as $\tau_p = (R_{\text{gnr}} + 2R_{\text{C}}) \cdot C_{\text{g}}$, where R_{gnr} is the GNR resistance between the drain and source contacts derived by the NEGF model, R_{C} is the ohmic resistance between graphene and metal contacts, and C_{g} is the top gate capacitance (depicted in Figure 5 as a function of the quantum capacitance, C_{q}, and the oxide capacitance, C_{ox} in series) [15], [24]. As metal-graphene contact resistance R'_{C} reported in the literature vary from $100\Omega \cdot \mu$m to $1\text{k}\Omega \cdot \mu$m [25] we set $R'_{\text{C}} = 200\Omega \cdot \mu$m in our evaluations. Furthermore, in order to compute the quantum capacitance C_{q} we followed the approach in [13] and [26], and expressed it as a function of the density of states $DOS(E)$, the thermal broadening function $F_{\text{T}}(E)$, and the energy E, as:

$$C_{\text{q}} = \text{q}^2 \cdot \int_{-\infty}^{+\infty} DOS(E) \cdot F_{\text{T}}(E - (\mu_1 - \mu_2))\, \text{d}E. \quad (6)$$

Table III presents the input to output propagation delay, the active area, and the power consumption corresponding to 2-input butterfly GNR structures dimensionally defined

TABLE IV
3-INPUT GNRS AND 7nm CMOS GATES PROPAGATION DELAY, AREA, AND POWER

	$\tau_p[ps]$		Active Area $[nm^2]$		Power $[nW]$		Power-delay Product $[ps\text{-}nW]$	
	GNR	CMOS	GNR	CMOS	GNR	CMOS	GNR	CMOS
AND	$3.860 \cdot 10^{-2}$	$1.116 \cdot 10^{1}$	$3.056 \cdot 10^{1}$	$1.936 \cdot 10^{3}$	$2.326 \cdot 10^{1}$	$3.998 \cdot 10^{2}$	0.898	$4.461 \cdot 10^{3}$
NAND	$2.339 \cdot 10^{-2}$	7.635	$3.056 \cdot 10^{1}$	$1.452 \cdot 10^{3}$	$8.701 \cdot 10^{1}$	$3.433 \cdot 10^{2}$	2.035	$2.621 \cdot 10^{3}$
OR	$1.804 \cdot 10^{-2}$	8.547	$2.707 \cdot 10^{1}$	$1.936 \cdot 10^{3}$	$6.472 \cdot 10^{1}$	$3.473 \cdot 10^{2}$	1.167	$2.968 \cdot 10^{3}$
NOR	$2.472 \cdot 10^{-2}$	$1.092 \cdot 10^{1}$	$2.973 \cdot 10^{1}$	$1.452 \cdot 10^{3}$	$9.868 \cdot 10^{1}$	$2.983 \cdot 10^{2}$	2.439	$3.257 \cdot 10^{3}$
XOR	$1.479 \cdot 10^{-2}$	$1.373 \cdot 10^{1}$	$2.667 \cdot 10^{1}$	$4.840 \cdot 10^{3}$	$7.167 \cdot 10^{1}$	$1.768 \cdot 10^{3}$	1.060	$2.427 \cdot 10^{4}$
XNOR	$2.262 \cdot 10^{-2}$	$1.637 \cdot 10^{1}$	$2.667 \cdot 10^{1}$	$5.808 \cdot 10^{3}$	$4.090 \cdot 10^{1}$	$2.529 \cdot 10^{3}$	0.925	$4.140 \cdot 10^{4}$

in Table I and 7nm 2-input CMOS gate counterparts. In a nutshell the Table reveals that when compared with CMOS the GNR structures provide input to output propagation delay, power consumption, and power-delay product reductions of 2, 1 to 2, and 3 to 4 orders of magnitude, respectively.

We observe that while for the CMOS case, the propagation delay has similar values for all gates (44% maximum variation with respect to the NAND gate minimum delay of 7.556ps), for the GNR case delay disparities between various gates can go to up to about 2.6×. The high delay variation among GNR structures is related to I_{ON} current dependence on GNR structures geometry and gate contacts topology and it can be dealt with by incorporating delay constraints into the GNR geometries design space exploration. A similar phenomenon can be observed in terms of power consumption, as faster gates consume more power, and to a limited extend in the power-delay product case. When compared in terms of active area the GNR structures require a 2 orders of magnitude smaller footprint. We note that GNR structures have similar areas (which benefit the layout) but somehow different delay and power consumption. This implies that by keeping roughly the same area while changing the GNR geometry we can obtain very different conduction behaviour and performance figures, which is not the case for CMOS based designs.

Table IV summarizes delay, area, and power consumption for 3-input GNR structures and CMOS counterparts. We observe a similar trend as for the 2-input case from Table III, i.e., GNR structures provide input to output propagation delay, power consumption, and power-delay product reductions of 2 to 3, 1 to 2, and 3 to 4 orders of magnitude, respectively, and about 2 orders of magnitude smaller active area. We note that GNR structures advantage over CMOS is even more substantial as their area and delay are only slightly increasing when compared with the 2-input case. By comparing the data in Tables III and IV, we observe that CMOS 3-input gates area footprint (delay) increases by 33% to 100% (up to 51%) relative to the 2-input gates area (delay) while for the GNR structures area (delay) changes are from 9% to 26% (21% to 42%). Thus, we can conclude that while complex CMOS logic gates require larger area and are slower this is not the case for the proposed GNR structures.

To get inside on the way our work positions against state of the art graphene based gates we also compare with 2-input pn-junctions-based gates proposed in [14] and [15]. Table V indicates that our structures outperform the pn-junctions-based Boolean gates introduced in [14] by 1 order of magnitude in terms of delay. Moreover, when comparing with the 2-input NAND in [15] (0.105um^2 area, 0.177ps delay, 3.15μW power consumption and 0.557ps $\cdot\, \mu$W power-delay product), our 2-input NAND mirroring GNR structure requires 3 orders of magnitude smaller area, is 1 order of magnitude faster, consumes 44× less power, and exhibits a 2 orders of magnitude lower power-delay product. The better performance provided by our structures is mainly induced by the fact that we make use of graphene properties to directly evaluate the function instead of relying of the traditional switch (transistor) based approach.

TABLE V
2-INPUT GNR AND pn-JUNCTIONS GATE DELAYS

	$\tau_p[ps]$	
	GNR	[14]
AND	$3.860 \cdot 10^{-2}$	0.486
NAND	$2.339 \cdot 10^{-2}$	0.567
OR	$1.804 \cdot 10^{-2}$	0.486
NOR	$2.472 \cdot 10^{-2}$	0.567
XOR	$1.479 \cdot 10^{-2}$	0.486
XNOR	$2.262 \cdot 10^{-2}$	0.486

All these results suggest that, potentially speaking, GNR-based logic gates built with the proposed structures can substantially outperform advanced CMOS counterparts and can open a novel avenue towards future post-Si nanoelectronics. To get further inside into our approach potential, In the remainder of the section, we investigate operation robustness aspects related to V_{DD} variation and scaling and non-ideal graphene fabrication process and patterning.

B. V_{DD} Variation Robustness

To investigate the effect of V_{DD} variations on GNR's stable operation, we consider the butterfly GNR structures with 2 and 3 inputs that mirror the NOR Boolean functionality, vary V_{DD} with ±10% in increments of 2% with respect to

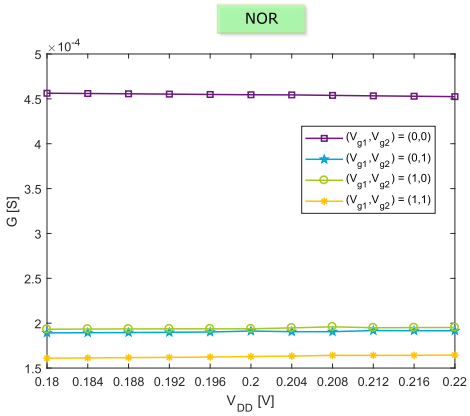

Fig. 6. 2-input NOR GNR G stability to V_{DD} variations.

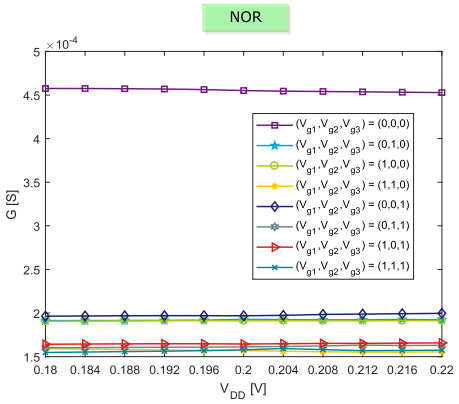

Fig. 7. 3-input NOR GNR G stability to V_{DD} variations.

the nominal voltage $V_{\mathrm{DD}} = 0.2$V, and measure the GNR conductance corresponding to each of the 4 primary 2-input combinations: $(V_{\mathrm{g1}}, V_{\mathrm{g2}}) = (0,0); (0,1); (1,0); (1,1)$ V (or 8 input combinations for the 3-input case). Figure 6 and Figure 7 graphically present G as a function of V_{DD} for the 2-input and 3-input, respectively, NOR butterfly GNR structures.

One can observe that G experiences very little variations (maximum 1.13% for the 2-input case and 1.94% for the 3-input case), with respect to the nominal $V_{DD} = 0.2$V values. Our experiments also reveal that the V_{DD} variation effect on the timing characteristics is relatively small, i.e., the input to output propagation delay varies on average with 6.0% and 5.6% for the 2-input and 3-input case, respectively.

C. V_{DD} Lower Bound

In this section, we attempt to asses the lowest V_{DD} value for which we can still obtain butterfly GNR structures able to mirror basic Boolean functionality while being able to provide an $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ current ratio bigger than a certain threshold (i.e., big enough to allow the differentiation between logic low and logic high voltage levels). To this end, we consider 4 different V_{DD} values (i.e., 0.1V, 0.05V, 0.02V, and 0.01V). For each V_{DD} value, we perform a DSE in order to obtain

TABLE VI
2-INPUT AND GNR TOPOLOGY VS V_{DD}

V_{DD} $[V]$	0.01	0.02	0.05	0.1
W [a]	47	41	47	41
L [a]	$25\sqrt{3}$	$25\sqrt{3}$	$25\sqrt{3}$	$27\sqrt{3}$
W_{c} [a]	11	14	11	8
L_{c} [a]	$3\sqrt{3}$	$7\sqrt{3}$	$3\sqrt{3}$	$9\sqrt{3}$
$P_{V_{\mathrm{g}}}$ [a]	$3\sqrt{3}$	$3\sqrt{3}$	0	$3\sqrt{3}$
$W_{V_{\mathrm{g}}}$ [a]	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$
V_{back} $[V]$	0	0	0	0

TABLE VII
2-INPUT NOR GNR TOPOLOGY VS V_{DD}

V_{DD} $[V]$	0.01	0.02	0.05	0.1
W [a]	47	47	41	41
L [a]	$25\sqrt{3}$	$25\sqrt{3}$	$27\sqrt{3}$	$27\sqrt{3}$
W_{c} [a]	17	17	14	8
L_{c} [a]	$5\sqrt{3}$	$5\sqrt{3}$	$11\sqrt{3}$	$9\sqrt{3}$
$P_{V_{\mathrm{g}}}$ [a]	$4\sqrt{3}$	$2\sqrt{3}$	$4\sqrt{3}$	$3\sqrt{3}$
$W_{V_{\mathrm{g}}}$ [a]	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$
V_{back} $[V]$	0	0	0.2	0.2

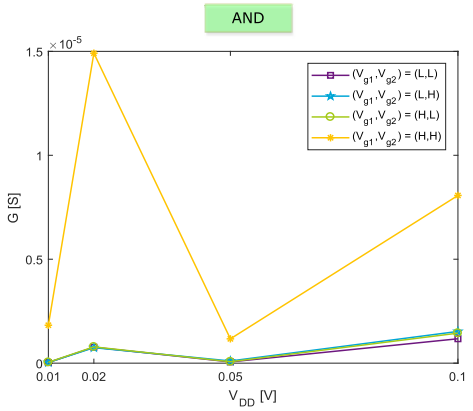

Fig. 8. 2-input AND GNR conductance vs V_{DD}.

butterfly GNR structures which mirror 2-input AND and 2-input NOR functionality.

The obtained GNR geometries and contacts topologies for each V_{DD} value are summarized in Table VI and Table VII, for AND and NOR, respectively. We observe that, while in general both the geometry and contacts topology need to change with either V_{DD} or Boolean functionality change, in some cases, it suffices to modify the contacts topology only. For example, the NOR geometries for $V_{\mathrm{DD}} = 0.01$V and $V_{\mathrm{DD}} = 0.02$V are identical, the only difference being P_{V_g} (the top gate contacts position with respect to the source and drain contacts), $4\sqrt{3}$ versus $2\sqrt{3}$. Another example is for the AND and NOR geometries when $V_{\mathrm{DD}} = 0.01$V, in which case, the only difference is the applied V_{back} voltage value (0.2V versus 0V).

Figure 8 (9) presents the conduction of the four AND (NOR) GNRs corresponding to all possible input combinations

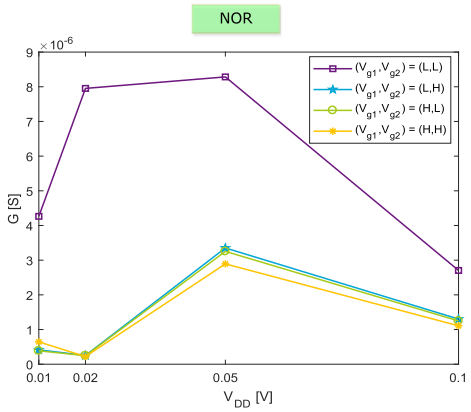

Fig. 9. 2-input NOR GNR conductance vs V_{DD}.

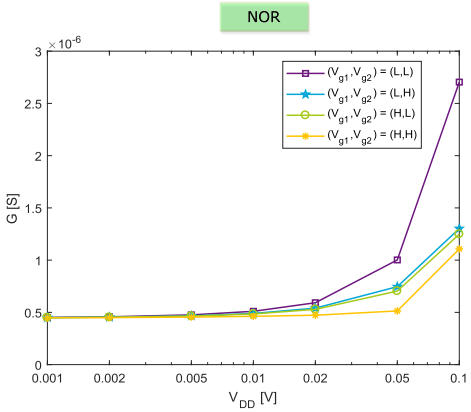

Fig. 11. 0.1V 2-input NOR GNR conductance vs V_{DD}.

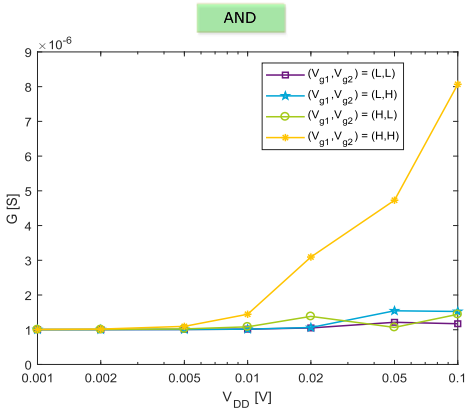

Fig. 10. 0.1V 2-input AND GNR conductance vs V_{DD}.

$(V_{\mathrm{g1}}, V_{\mathrm{g2}}) = (L, L); (L, H); (H, L); (H, H)$, where L and H denote logic low input voltage level and logic high input voltage level, respectively. we note that while L is always 0V, H is equal to the GNR specific V_{DD} value. In Figure 8, the lines colored in (purple, blue, and green) and orange reflect conductance values for logic low and hight output value, respectively. The Figure suggests that the structure tailored to $V_{\mathrm{DD}} = 0.02$V operation provides the best "on" to "off" conductance ratio and by implication the most robust operation. The same observation holds true for the NOR case in Figure 9, which suggest that nonintuitive design optimization avenues are potentially available for the design of butterfly GNR based Boolean gates and circuits.

We further investigate V_{DD} limitations from a different angle by considering the $V_{\mathrm{DD}} = 0.1$V specific GNR AND (NOR) geometry in Tables VI (VII) and varying V_{DD} from 100 to 1mV while adjusting V_{g1} and V_{g2} logic high voltage values accordingly. Figure 10 (11) presents AND (NOR) GNR conductance evolution while V_{DD} decreases from 100mV to 1mV while using the same legend as in Figure 8. One can observe the best performance corresponds to the nominal V_{DD} values for which the structures were designed and that the high to low conductance ratio decreases when V_{DD} is diminished. The desired functionality is maintained until a certain V_{DD} threshold when the G values (which reflect the Boolean function output), become indistinguishable between logic high and logic low, or the Boolean logic is not correctly reflected any longer, which is 20mV for tAND and about 10mV for NOR. This suggests that any GNR structure has its own V_{DD} lower operation value, which is highly dependent on the GNR geometry and contacts topology.

D. Fabrication Challenges and Edge Defects

In this section, we first briefly discuss GNR fabrication status, difficulties, and challenges, and subsequently investigate the GNR edge defects potential impact on the proposed structures.

1) Fabrication Status and Challenges: Up to date, several fabrication methods have been utilized to produce GNRs, such as top-down lithographic patterning [27], [28], chemical procedures [29], and longitudinally unzipping of high quality grown carbon nanotubes [30], [31]. While top-down lithographic patterning is very promising for the fabrication of well-arranged $12 - 20$ nm GNRs for large-scale integration, carbon nanotubes "unzipping" or "unrolling" can successfully produce sub-20 nm GNR [32]. Other GNR fabrication strategies include nanowire mask lithography [33] and block copolymer lithography, which both can produce sub-10 nm GNRs [34].

Despite their fast development, all GNR fabrication approaches are still confronting some major difficulties and challenges, e.g., (i) lack of scalability and designable densely alignment, (ii) GNR damage, edge defects, and electronic properties degradation due to conventional plasma etching, (iii) time-consuming and expensive. Over the last few years, researchers focused on the development of GNR fabrication, and tried to address these issues. Reference [35] provided one approach to scalable graphene, which obtains graphene by means of Chemical Vapour Deposition (CVD) followed by a transfer from the original Ni substrate to a Si/SiO_2 substrate. Reference [36] introduced a facile route for fabricating densely packed aligned sub-20 nm GNRs array by making use of symmetric block copolymer lithography. Huang *et al.* [37] obtained low edge-defects GNRs with 30 nm width by means of electron beam lithography followed by O_2 neutral beam

TABLE VIII
CONDUCTANCE OF IDEAL AND INCOMPLETE 2-INPUT AND GNR

	Conductance $[S]$				Ratio		
	G_{00}	G_{01}	G_{10}	G_{11}	G_{11}/G_{00}	G_{11}/G_{01}	G_{11}/G_{10}
Without defects	$3.829 \cdot 10^{-8}$	$5.668 \cdot 10^{-8}$	$4.138 \cdot 10^{-8}$	$3.012 \cdot 10^{-6}$	79	53	73
Atom 1 defect	$2.010 \cdot 10^{-8}$	$7.068 \cdot 10^{-8}$	$4.761 \cdot 10^{-8}$	$2.462 \cdot 10^{-6}$	122	35	52
Atom 2 defect	$1.115 \cdot 10^{-8}$	$1.982 \cdot 10^{-7}$	$2.763 \cdot 10^{-7}$	$6.936 \cdot 10^{-6}$	622	35	25
Atom 3 defect	$1.654 \cdot 10^{-7}$	$2.198 \cdot 10^{-6}$	$7.446 \cdot 10^{-7}$	$1.073 \cdot 10^{-5}$	65	5	14
Atom 4 defect	$3.541 \cdot 10^{-8}$	$7.741 \cdot 10^{-7}$	$1.082 \cdot 10^{-6}$	$1.338 \cdot 10^{-5}$	378	17	12
Atom 5 defect	$1.479 \cdot 10^{-7}$	$1.373 \cdot 10^{-6}$	$1.304 \cdot 10^{-6}$	$2.036 \cdot 10^{-5}$	138	15	16
Atom 6 defect	$1.611 \cdot 10^{-7}$	$7.553 \cdot 10^{-7}$	$2.210 \cdot 10^{-6}$	$1.679 \cdot 10^{-5}$	104	22	8
Atom 7 defect	$1.132 \cdot 10^{-6}$	$8.786 \cdot 10^{-7}$	$1.676 \cdot 10^{-6}$	$2.148 \cdot 10^{-5}$	19	24	13
Atom 8 defect	$6.791 \cdot 10^{-8}$	$3.360 \cdot 10^{-7}$	$2.133 \cdot 10^{-6}$	$1.251 \cdot 10^{-5}$	184	37	6
Atom 9 defect	$7.262 \cdot 10^{-8}$	$3.872 \cdot 10^{-7}$	$1.559 \cdot 10^{-6}$	$1.345 \cdot 10^{-5}$	185	35	9
Atom 10 defect	$1.679 \cdot 10^{-8}$	$1.470 \cdot 10^{-7}$	$5.185 \cdot 10^{-7}$	$7.223 \cdot 10^{-6}$	430	49	14
Atom 11 defect	$3.078 \cdot 10^{-8}$	$1.050 \cdot 10^{-7}$	$1.116 \cdot 10^{-6}$	$3.615 \cdot 10^{-6}$	117	34	3

etching on large-scale CVD-grown graphene. Reference [38] proposed a fast and inexpensive approach to fabricate GNRs as narrow as 9 nm with an $I_{\text{ON}}/I_{\text{OFF}}$ current ratio of 70 at room temperature and carrier mobility of 300 $\text{cm}^2\text{v}^{-1}\text{s}^{-1}$. Reference [16] made use of the surface-assisted synthesis approach to fabricate atomically precise, low-edge-defect GNRs, e.g., 3-Armchair GNRs (1 hexagon width) and 6-Zigzag GNRs (6 hexagon width), which indicates that the structures we introduced in this paper can be potentially fabricated in the close future. However, there are still hurdles and challenges ahead on the road towards all-graphene electronics, e.g., (i) enable GNR bandgap modulation to the useful value range of $0.5 - 1.5$ eV [16], (ii) increase GNR fabrication process time and cost efficiency, (iii) avoid high Schottky barriers for nerrow metal-GNRs contacts [16], (iv) scale GNR-based prototype devices to high integration densities [39], and (v) fabrication of GNRs interconnects.

Even though new fabrication technologies (e.g., scalable bottom-up approaches and on-surface synthesis methods) are exceeding the precision limit of modern lithographic approach and can produce atomically precise GNRs with well-defined width edge defects cannot be completely eliminated, at least not for the time being and in view of this we evaluate their impact on GNR's electrical properties and by implication on the behavior of the proposed butterfly structures.

2) Edge Defects: As a thorough analysis of random edge defects influence on GNR electrical characteristics is out of the scope of the current paper we restrict our investigation to the case when one or two defects are present in the GNR constriction edge and make use of the NEGF-Landauer formalism while neglecting the phonon and electron scattering.

To this purpose we choose a 2-input AND GNR with $W = 41, L = 25\sqrt{3}, W_{\text{c}} = 8, L_{\text{c}} = 4\sqrt{3}, P_{V_{\text{g}}} = 2\sqrt{3}, W_{V_{\text{g}}} = 6\sqrt{3}, V_{\text{back}} = 0\text{V}, V_{\text{d}} = 0.2\text{V}, V_{\text{s}} = 0\text{V}, V_{\text{g1}} = 0$ or $0.2\text{V}, V_{\text{g2}} = 0$ or 0.2V and derive its conductance

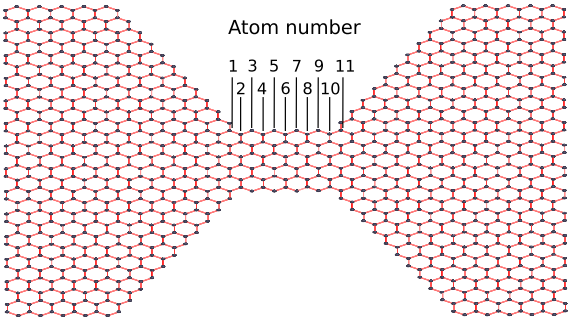

Fig. 12. Missing atoms on the constriction upper edge.

corresponding to the four input combinations for GNR with perfect edges and for 11 defected GNRs, each one missing one of the atoms indicated in Figure 12. Table VIII summarizes the obtained conductance values and high/low ratios for all considered cases. Note that G_{00} corresponds to $V_{\text{g1}} = 0\text{V}, V_{\text{g2}} = 0\text{V}$, G_{01} corresponds to $V_{\text{g1}} = 0\text{V}, V_{\text{g2}} = 0.2\text{V}$, etc. One can observe that the conductance variations are large, i.e., up to $28.6\times$, $37.8\times$, $52.4\times$ and $6.1\times$ for G_{00}, G_{01}, G_{10}, and G_{11}, respectively. Additionally, defect presence induces G_{11}/G_{01} and G_{11}/G_{10} ratios decrease and in most of the cases a G_{11}/G_{00} substantial increase, which is quite interesting as it suggest that defects might be helpful rather than harmful. While from the perspective of high/low conductance ratio edge defects deteriorate GNR's electronic properties one can notice that GNRs with edge defects can still reflect the expected Boolean functionality.

V. CONCLUSIONS

In this paper, we investigated graphene nanoribbons potential as fundamental building blocks for carbon-based implementation of Boolean logic gates and circuits. We augmented a trapezoidal Quantum Point Contact (QPC) topology with top gates to obtain a butterfly Graphene Nanoribbon (GNR)

structure and demonstrated that by adjusting its topology its conductance map can mirror basic Boolean functions, thus one can use such structures instead of transistors to build carbon-based gates and circuits. We identified by means of Design Space Exploration (DSE) specific GNR topologies for 2- and 3-input {AND, NAND, OR, NOR, XOR, XNOR} and demonstrated by means of Non-Equilibrium Green Function - Landauer based simulations that butterfly GNR-based structures operating at $V_{DD} = 0.2$V outperform 7nm @$V_{DD} = 0.7$V CMOS counterparts by 2 to 3, 1 to 2, and 3 to 4, orders of magnitude in terms of delay, power consumption, and power-delay product, respectively, while requiring 2 order of magnitude less active area. We also investigated the effect of V_{DD} variations and V_{DD} proper operation lower bound. To this end we demonstrated that (i) NOR butterfly GNR structures are quite robust as their conductance and delay are changing by no more than 2% and 6%, respectively, (ii) V_{DD} lower bound is GNR geometry and contact topology dependent and AND and NOR GNR geometries can operate even at 10mV. Finally, we considered aspects related to the practical realization of the proposed structures and concluded that even if there are still hurdles on the road ahead the latest graphene fabrication technology developments, e.g., surface-assisted synthesis, our proposal opens an alternative towards effective carbon-based nanoelectronic circuits and applications.

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