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Multi-Path Wide-Bandwidth CMOS Magnetic Sensors

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Abstract: This paper proposes a multi-path multi-sensor architecture for CMOS magnetic sensors, which effectively extends their bandwidth without compromising either their offset or resolution. Two designs utilizing the proposed architecture were fabricated in a 0.18 μm standard CMOS process. In the first, the combination of spinning-current Hall sensors and non-spun Hall sensors achieves an offset of 40 μT, and a resolution of 272 μT_{rms} in a bandwidth of 400 kHz, which is 40x more than previous low-offset CMOS Hall sensors. In the second, the combination of spinning-current Hall sensors and pick-up coils achieves the same offset, with a resolution of 210 μT_{rms} in a further extended bandwidth of 3 MHz, which is the widest bandwidth ever reported for a CMOS magnetic sensor.

Keywords: Multi-path, CMOS, Magnetic Sensor, Hall Sensor, Pick-up Coil, Ripple Reduction Loop

I. INTRODUCTION

Current measurements are widely required in many applications, e.g., motor controls,

overload detections and energy monitoring systems. Traditional shunt-based current sensors [1] suffer from poor galvanic isolation. To improve this, magnetic sensors are often used as contactless current sensors, with the added advantage that the current-carrying path does not need to be broken, allowing them to be easily retrofitted to existing systems [2]. Compared to other types of magnetic sensors, such as Magnetoresistive (MR) [3] sensors and fluxgates [4] [5], Hall sensors have found the widest application, mainly because of their wider dynamic range, compatibility with standard CMOS processes and hence low fabrication cost.

However, due to their limited sensitivity, the accuracy of state-of-the-art CMOS Hall sensors is severely impacted by their offset, which ranges from a few micro-Tesla [6] to a few milli-Tesla [7]. Moreover, the achievable current-to-magnetic field sensitivity is limited by packaging constraints on the distance between the sensor and the current-carrying conductor. In [8], a 30 mA detectable current was achieved by a 10 μT offset Hall sensor, with the help of a lead-frame based current-carrying conductor.

In addition to a requirement on accuracy, a bandwidth of a few MHz [9] [10] is often required in some applications, such as switched-mode power supplies, to capture rapid current transients. This wide bandwidth requirement is even more crucial in overload/short-circuit detection [11] [12], where for safety concerns, detection time in the order of a few micro-seconds is often required [13]. However, state-of-the-art CMOS magnetic sensors are typically optimized for either low-offset [6] [8] [14] or

wide-bandwidth [15], but not for both.

In CMOS processes, Hall sensors can be built as four-contact n-well plates and modelled as a Wheatstone bridge, as shown in Fig. 1. When biased at a current level I_{bias}, the Hall plate produces an output voltage V_{out} at the other 2 terminals in the presence of a magnetic field perpendicular to the plate, which can be expressed as:

$$V_{out} = S_{HS} \cdot I_{bias} \cdot B \tag{1}$$

where S_{HS} is the current related sensitivity of the Hall sensor in V/AT. The sensitivities of CMOS Hall sensors depend on several process and layout parameters, with typically reported values ranging from 100 V/AT to 400 V/AT [16] – [19]. For a magnetic field of 1 mT, a typical Hall sensor with a biasing current of 1 mA can only produce an output signal of 100 – 400 μV. At the expense of extra fabrication cost, the limited sensitivity of Hall sensors can be improved by an order of magnitude with the help of flux concentrators, which can be realized by depositing a ferromagnetic layer above the sensor [20] [21]. However, spread in concentrator geometry results in extra sensitivity spread [22].

Despite their low fabrication cost and good linearity, Hall sensors exhibit raw offsets of about 10 – 50 mT, which is often orders of magnitude larger than the signals of interest. This is caused by n-well inhomogeneity, which can be modelled by resistance mismatch in the arms of the corresponding Wheatstone bridge. Fortunately this offset can be significantly reduced by the well-known spinning current

technique, in which the biasing and readout terminals are periodically rotated [23], as shown in Fig. 2. This operation swaps the relative polarities of the sensor's offset V_{offset} and the magnetic signal V_{Hall}, thus modulating V_{offset} to twice the spinning frequency $2f_{spin}$ and keeping V_{Hall} unaffected. However, due to the necessary amplification of the micro-volt level output signal V_{Hall}, low-offset amplifiers are still required to prevent excessive offset, as shown in Fig. 3. To relax this requirement, the spinning current technique can be modified such that the magnetic signal, instead of the offset, is modulated to $2f_{spin}$ [14], as shown in Fig. 4. A demodulator can be used to reconstruct the magnetic signal, and simultaneously modulate both the Hall sensor and readout offsets to $2f_{spin}$. The up-modulated offsets then appear as AC ripple at the amplifier's output. With this approach, CMOS Hall sensors with 10 μT offset can be achieved [8]. This can be further lowered to 4 μT by the use of 8-phase spinning on octagonal Hall sensors [6].

In practice, the amplitude of the spinning ripple is quite large compared to the magnetic signal, and so ripple reduction techniques are necessary. Conventionally, low-pass filters (LPFs) are used, which unfortunately also suppress high frequency magnetic signals. In addition to this bandwidth reduction, digital LPFs sample the outputs and therefore suffer from aliasing; while analog LPFs require large time constants to achieve sufficient ripple suppression and therefore occupy considerable area. Although these constraints can be eased by increasing f_{spin}, this is at the expense of an increase in residual offset [15] due to the periodic switching transients

and charge injection associated with the spinning current technique. For all the above-mentioned reasons, traditional CMOS Hall sensor designs have to deal with a trade-off between bandwidth and offset. The bandwidth of low-offset CMOS Hall sensors is thus typically less than 100 kHz [15], despite the fact the bandwidth of the Hall Effect extends to a few GHz [24].

A ripple reduction loop (RRL) [25] can effectively suppress 2-phase spinning ripple without the use of LPFs [26]. However due to the anisotropy of the n-well's resistance, a single RRL cannot fully suppress 4-phase spinning ripple [8], as the sensor's offset will change during the various spinning phases. However, any 4-phase signal can be fundamentally decomposed into three ripple components and one signal component (the magnetic signal in this case), as shown in Fig. 6. Based on this insight, it has been shown that the ripple of a 4-phase spinning current Hall sensor can be significantly reduced by the use of three (off-chip) RRLs [27]. The sensor's useful bandwidth could thus be extended above 100 kHz even with much lower spinning frequencies, e.g. 1 kHz, needed to minimize offset. However, as any signal at the ripple frequencies will be mistaken for ripple, this approach creates notches at f_{spin}, $2f_{spin}$ and their even-order harmonics, which may cause slow settling issues.

This paper proposes a multi-path architecture that combines a wide bandwidth sensor in a high frequency (HF) path with a spinning current Hall sensor (with RRLs) in its low frequency (LF) path. The output of the wide bandwidth sensor will then "fill" up the

RRL notches to ensure a flat transfer function. For example, when the wide bandwidth sensor is an AC coupled non-spun Hall sensor [28], the bandwidth of the overall system could be extended to 400 kHz. As the AC coupled non-spun Hall sensor does not introduce extra offset, the system achieves an offset of 40 μT, which is determined by the spinning Hall sensor in the low frequency path. By replacing the non-spun Hall sensor by a pick-up coil in the HF path [29], system bandwidth could be extended, by another order of magnitude, to 3 MHz. Thanks to the differential characteristic of the pick-up coils, the hybrid combination of spinning Hall sensors and pick-up coils achieves better resolution (210 μT_{rms}) than that of the combination of Hall sensors (272 μT_{rms}), but without consuming more power. These two examples show that the use of a multi-path architecture effectively breaks the bandwidth-resolution and -offset trade-offs, and thus enables the realization of wide bandwidth CMOS magnetic sensors.

The rest of the paper is organized as follows: Section II introduces the multi-path CMOS magnetic sensor by combining spinning current Hall sensors and non-spun Hall sensors; the combination of spinning current Hall sensors and pick-up coils is discussed in Section III; after the discussion of the experiment results in Section IV, conclusions are drawn in Section V.

II. Multi-path Hall sensor system

A. System architecture

The proposed system consists of a low frequency (LF) path with a spun Hall sensor and a high frequency (HF) path with a non-spun Hall sensor, as shown in Fig. 7. Both paths use identical Hall sensors and signal paths consisting of two amplifiers: a capacitively-coupled amplifier with a gain of 100, and an inverting amplifier with a gain of 20. Both amplifiers have the same bandwidth of 400 kHz, so that the overall frequency response will be flat. An output stage with a gain of 2 smoothly combines both paths' outputs by high-pass filtering the output of the HF path and low-pass filtering the output of the LF path, as shown in Fig. 8. The spinning ripple in the LF path is suppressed by the integrated triple RRLs, which inject compensation currents at the virtual ground of A_2. This arrangement greatly relaxes the specification of the triple RRLs due to the large gain of the preceding stage. Any residual ripple will be further suppressed by the 1st order low-pass filtering action of the output stage. In this design, the cross over frequency f_{cross} = 2 kHz, and is set by the time constant of R_0C_0 in the feedback of the output stage. This f_{cross} is a compromise between the area and the need to ensure that the notches will be sufficiently filled by the HF path, i.e., $f_{cross} << f_{spin}$. To ensure a smooth cross over between the two paths, R_3C_3 and R_0C_0 are designed to match.

B. Capacitively-coupled first stage

The use of a capacitively-coupled first stage [30] has three advantages: it has a better power efficiency than current feedback instrumentation amplifiers or three-opamp instrumentation amplifiers; its capacitively-coupled input can handle a wide

common-mode input range, so that the biasing current of the Hall sensors can be adjusted freely； and a differential sensing structure can be easily implemented by connecting another set of input capacitors to the virtual ground, as shown in Fig. 9. A set of high-ohmic resistors in the feedback define the DC biasing point of the virtual ground. This effectively creates a high pass filter and configures the opamp in unity gain for offset, which highly relaxes the dynamic range of succeeding stages.

At the final output, the LF path only contributes signals ranging from DC to 2 kHz. With f_{spin} = 10 kHz, the 1st stage requires a flat frequency response from 18 kHz to 22 kHz, as shown in Fig. 10. To assure maximum signal attenuation of <1% due to the high-pass filtering action, the feedback resistors need to be greater than 370 MΩ (C_f = 240 fF). This is achieved by using a pseudo resistor with two back-to-back connected PMOS transistors [31], which results in a resistance of several GΩ.

Since most of the Hall sensor's offset will be blocked by the input capacitors, the first stage only needs to process the magnetic signal and the offset of the first opamp A_1 (~mV). Therefore, A_1 is implemented as a telescopic amplifier with a class-A output to drive the load (R_1 = 50 kΩ) of the next stage, as shown in Fig. 11. To achieve a g_m of 1.2 mS, which is commensurate with the sensor's resistance, the input differential pair is biased at 110 μA (out of a total supply current of 175 μA).

C. Implementation of triple RRLs

Primarily due to the n-well's anisotropic resistance, the Hall sensor's offset changes in different spinning phases. Together with the offset of the 1st and 2nd stages, it appears as a square-wave ripple at the output of the 2nd stage, which cannot be fully filtered by the output stage. Therefore triple RRLs are integrated to continuously measure different ripple components (Fig. 6) and inject a compensation signal at the virtual ground of the 2nd stage. 2 out of 3 RRLs are working in a ping (1st and 2nd phases) – pong (3rd and 4th phases) sequence to fully compensate any ripple at $2f_{spin}$. The residual ripple at f_{spin} will be compensated by the third RRL.

In this work, the RRL implementation is adapted and modified from that in [30], as shown in Fig. 12. Through the sensing resistor R_S, the specific spinning ripple component is converted into current ripple, which is then synchronously demodulated and integrated on a capacitor C_{int}. The compensation is done by injecting a current into the virtual ground of A_2 via R_C. For the sake of parameter analysis, chopper CH_1, CH_2 and CH_3 can be combined to CH_{eff}. This effectively converts the RRL into an active DC servo loop. Assuming A_2 is ideal, then V_{oL} can be expressed as

$$V_{oL} = (I_1 - I_2)\mathrm{R}_2 \tag{2}$$

In the feedback path, the transfer function from V_{oL} to V_C can be expressed as

$$\frac{V_C}{V_{oL}} = \frac{A_0}{1+(1+A_0)sR_SC_{\mathrm{int}}} \tag{3}$$

with which equation (2) can be re-written as

$$\left[\frac{V_{in}}{R_1} - \frac{A_0 V_{oL}}{[1+(1+A_0)sR_SC_{\mathrm{int}}]\cdot R_C}\right]\cdot R_2 = V_{oL} \tag{4}$$

Therefore, the transfer function H(s) from V_{in} to V_{oL} can be expressed as

$$H(s) = \frac{V_{oL}}{V_{in}} = \frac{\frac{R_2}{R_1}}{1 + \frac{A_0 R_2}{R_C\,[1 + (1 + A_0) s R_S C_{\text{int}}]}} \tag{5}$$

Equation (5) can be mapped into the classical feedback theory, whose corresponding Bode plot is shown in Fig. 13. The loop gain Aβ can be expressed as

$$A\beta = \frac{A_0 R_2}{R_C\,[1 + (1 + A_0) s R_S C_{\text{int}}]} \tag{6}$$

with which the high pass corner frequency f_0 can be calculated as

$$f_0\big|_{A\beta=1} = \frac{R_2}{2\pi C_{\text{int}} R_S R_C} \tag{7}$$

And the DC transfer function can be expressed as

$$H(0) = \frac{R_C}{A_0 \cdot R_1} \tag{8}$$

The action of chopper CH_{eff} will translate this high pass filter into a notch filter around the chopping frequency. In this design, R_1 = 50 kΩ, R_2 = 1 MΩ, R_S = 10 MΩ, C_{int} = 20 pF, R_C = 2.5 MΩ, and A_0 = 100 dB, which results in 66 dB of ripple reduction, and a notch width of $2f_0$ = 640 Hz.

The complete implementation of the triple RRLs [28] is shown in Fig. 14. As the residual ripple will be essentially limited by the offset of A_0, all three integrators are auto-zeroed by storing their offsets on capacitor C_{AZ}. The RRL1 and RRL2 are arranged in a ping-pong sequence: in Φ1 RRL1 extracts the ripple associated with 1st and 2nd phases, while RRL2 is in auto-zeroing mode; and in Φ2, RRL1 is auto-zeroed,

while the ripple associated with 3rd and 4th phases are extracted by RRL2. The residual ripple is extracted and compensated by RRL3 which is auto-zeroed once every spinning cycle.

III. Hybrid multi-path system combining Hall sensors and pick-up coils

A. Combination of Hall sensors and pick-up coils

Although wide bandwidth and low offset can be simultaneously achieved by the multi-path Hall sensor system, its thermal noise power increases linearly with bandwidth, as shown in Fig. 15. For a given bandwidth f_{BW}, the SNR of a Hall sensor can be expressed as

$$SNR_{HS} = \frac{(B_{in} \cdot S_{HS})^2}{4kTR_{HS} \cdot f_{BW}} \tag{9}$$

where R_{HS} and S_{HS} represent the resistance and the sensitivity of the Hall sensor, respectively, and B_{in} represents the magnetic field signal.

Conversely, doubling the bandwidth of a pick-up coil will also double its noise power, but quadruple its peak signal power, as shown in Fig. 16. This suggests that the peak SNR of a pick-up coil will increase by 3 dB for every doubling of the bandwidth (10 dB/decade). The SNR of a pick-up coil in a given bandwidth f_{BW} can be expressed as

$$SNR_{coil} = \frac{B_{in}^2 \cdot \ nA^{\ 2} \cdot 4\pi^2 \cdot f_{BW}^2}{4kTR_{coil} \cdot f_{BW}} \tag{10}$$

where n and A represent the number and area of the coil windings, respectively, and R_{coil} represent the resistance of the pick-up coil.

As shown in Fig. 17, the peak SNRs of the Hall sensors and the pick-up coils will intersect at a certain frequency. At this so-called cross-over frequency f_{cross}, the system should maximize SNR by switching from one sensor to another. For a given Hall sensor and a pick-up coil, f_{cross} can be calculated as:

$$f_{cross} = \frac{S_{HS}}{2\pi nA}\sqrt{\frac{R_{coil}}{R_{HS}}} \tag{11}$$

For a Hall sensor with S_{HS}=100 mV/T, R_{HS}=2 kΩ and a pick-up coil with n=32, A≈1 mm^2 and R_{coil}=20 kΩ, f_{cross}=1.5 kHz. In this design, f_{cross} was intentionally set to 2 kHz in order to leave some margin for readout noise and to save chip area.

Fig. 18 depicts the proposed combination network to ensure smooth frequency transition. The Hall sensor in the LF path and the pick-up coil in the HF path are read out by g_{m_HS} and g_{m_coil}, respectively, and then combined by a trans-impedance amplifier with a time constant of R_0C_0. The low-pass filtering action of the trans-impedance amplifier also limits the noise bandwidth of both Hall sensors and coils, so that wide bandwidth and high resolution can be both achieved. Since only one time constant is involved, the proposed combination network ensures that the cross-over frequency is the same for both paths. Spread in the values of R_0 and C_0 will only result in a gain mismatch between the LF and HF paths. This mismatch can be trimmed by adjusting the biasing currents of the Hall sensors.

Due to the presence of the 1st order frequency transition, the bandwidth of the LF path needs to be considerably higher than f_{cross} to prevent any overall gain reduction

around LF path bandwidth. For instance, to ensure a gain flatness of 0.1 dB (1%), the LF path bandwidth needs to be 100x larger than f_{cross}, namely 200 kHz.

B. System implementation

The implementation of the complete system is shown in Fig. 19. The LF path employs spinning current Hall sensors and triple RRLs to ensure low offset, and employs enough bandwidth to ensure a flat frequency response. The implementation is exactly the same as the LF path in the multi-path Hall sensor system.

To suppress the offset of g_{m_coil}, coupling capacitors C_{AC} are used to block the DC current. Together with the output impedance R_{out} of g_{m_coil}, C_{AC} effectively creates a high pass filter whose cut off frequency is given by $1/2\pi R_{out}C_{AC}$. Similar to the LF path bandwidth requirement, this corner frequency needs to be 100x less than f_{cross}, i.e. 20 Hz, to ensure a bandwidth flatness within 0.1 dB. With C_{AC} = 20 pF, R_{out} needs to be larger than 400 MΩ. The circuit diagram of g_{m_coil} is shown in Fig. 20. The input differential pair is degenerated by a 40 kΩ resistor to maximum linear input range. To maximize the output impedance of the current mirrors, transistors M_a and M_c are cascaded. Moreover, a gain boosting transistor M_b is used to regulate the node V_d to further boost the output impedance of the current mirrors. Instead of biased by a constant current, M_b is biased by a copy of the signal current, so that V_d will be made exactly equal to V_g (the gate potential of transistor M_s). As transistors M_s and M_a are identically biased (gate, source and drain), the current signal can be accurately

mirrored independent of the load, which realizes a large output impedance [32]. For better power efficiency, the differential output currents are also mirrored via PMOS current source to a push-pull output stage. A mirror ratio of 5 results in an effective transconductance of 0.25 mS. With a supply current of 1.35 mA, g_{m_coil} can produce a differential output current of ±250 μA at 5 MHz.

To prevent V_{oH} from clipping, a DC servo loop is built. To preserve the output impedance, V_{oH} is first buffered by a pair of source followers, then converted into current via resistor R_{sense} (5 MΩ) and integrated in C_{srv} (10 μF). Since the loop gain has two poles $R_{sense}C_{srv}/A_4$ and $R_{out}C_{AC}$, a compensating zero is created by inserting R_{zero} (2 kΩ) in series with C_{srv} to cancel the effect of the non-dominant pole $R_{out}C_{AC}$.

To accurately handle the large output current from g_{m_coil} at high frequencies. i.e. ±100 μA at 2 MHz, and maximize the output range, a class-AB output stage with a quiescent current of 940 μA was used. Its circuit diagram is shown in Fig. 21.

IV. Experiment Results

The two proposed systems were fabricated in the same batch of a 0.18 μm CMOS process. The chip photos are shown in Fig. 22. Both chip occupies a total area of 8.75 mm^2. In both designs, each Hall sensor consists of four orthogonally coupled Hall plates, and each Hall plate is covered by a p+ layer to reduce 1/*f* noise by isolating the Si/SiO_2 interface. When biased with a total current of 1.4 mA (0.35 mA for each

plate), the Hall sensor has a sensitivity of 50 mV/T, resulting in a combined sensitivity of 100 mV/T. The multi-path Hall sensor system consumes a total of 8 mA, 5.6 mA of which is used to bias the four Hall sensors. In the multi-path hybrid system, the biasing current of the Hall sensors is adjusted to 2 mA (0.5 mA for each plate), so that the Hall sensors have a sensitivity of 71.4 mV/T (142.8 mV/T combined sensitivity) to match that of the pick-up coils. The multi-path hybrid system consumes 7.7 mA, 4 mA of which is used to bias the two Hall sensors in the LF path. Measurement on total 10 samples of both chips shows a maximum offset of less than 40 μT. The multi-path Hall sensor system can measure a differential field up to 12.5 mT, while the multi-path hybrid can measure up to 7.8 mT, with a maximum magnetic field slew rate of 136 mT/μs.

A. Measurement results of multi-path Hall sensor systems

The multi-path Hall sensor chip is packed in a ceramic SOIC package to bring down the distance between the current conducing trace and the Hall sensors. This results in a current-to-magnetic transfer of about 0.2 mT/A. With a 1 A primary current, FFTs of the sensor's output at 2 kHz, 20 kHz and 300 kHz are shown in Fig. 23. It can be noticed that the residual ripple at f_{spin} (10 kHz) is reduced to about -60 dB, equivalent to 7.3 μT, which can be as large as 1.1 mT without triple RRLs. The total integrated noise corresponds to a differential magnetic field resolution of 272 μT_{rms}, or a single-ended resolution of 136 μT_{rms}, which is dominated by the noise of the Hall sensors and the capacitively-coupled first stages. Moreover, hardly any harmonic

distortion can be seen.

The measured bandwidth of the multi-path Hall sensor system is shown in Fig. 24. It extends up to 400 kHz, without any notches, but suffers from a reduction in gain at frequencies above 50 kHz. This is caused by eddy currents induced in the lead-frame pad to which the die is glued. At high frequencies, these currents become large enough to significantly counter-balance the external magnetic field.

B. Measurement result of the hybrid multi-path system

To prevent eddy current from distorting the high frequency response, the hybrid multi-path chip is glued directly on top of a PCB trace using the chip-on-board (COB) technique, with the added advantage of close distance between the primary current and sensors. The resulting current-to-magnetic transfer is then increased to about 0.43 mT/A. The cross-section of a sample is shown in Fig. 25.

Fig. 26 shows the FFT plot of the hybrid system with a primary current at 199 kHz. Clearly, the noise bandwidth is limited by the output stage to 2 kHz. The noise floor is dominated by the noise from the source resistance of the pick-up coil (20 kΩ) as well as g_{m_coil}, which is degenerated by a 40 kΩ resistor. The total integrated noise corresponds to a differential magnetic field resolution of 210 μT_{rms} or a single-ended resolution of 105 μT_{rms}, which can be further improved by reducing the resistance of the pick-up coil as well as the noise of g_{m_coil}. The residual ripple at f_{spin} (10 kHz) is

about 8 μT, which is similar to that of the multi-path Hall sensor system. However, due to the limited linearity of g_{m_coil}, a 2nd harmonic distortion about -40 dB is present.

Fig. 27 shows the amplitude and phase response of the hybrid multi-path system with the biasing current of Hall sensor properly adjusted. A flat frequency response (both amplitude and phase) is achieved with a -3 dB bandwidth of 3 MHz. At higher frequencies (> 1 MHz), the phase response rolls off in a 2nd order fashion. The bandwidth of the system can also be demonstrated by examining its step response, as shown in Fig. 28. The test was done with a 3.3 A_{pp} square-wave primary current at 100 kHz. The settling of both the rising and falling edges is quite symmetrical, with a settling (>90%) time of less than 400 ns.

Fig. 29 shows two benchmark plots of bandwidth vs. offset (a) and bandwidth vs. resolution (b). It can be seen that the combination of the multi-path architecture together with triple RRLs and the spinning current technique breaks the bandwidth-offset trade-off. Furthermore, the bandwidth-resolution trade-off has also been broken by exploiting the differentiating characteristic of the pick-up coils.

Tab. 1 compares the proposed designs against other CMOS magnetic sensors. They are the fastest ever reported with an offset of less than 50 μT. Compared to [8], both achieve comparable offset, but with 40x and 300x bandwidth improvement, respectively. Although [6] achieves a much better offset, its bandwidth is severely

limited by the use of 8-phase spinning and low-pass filtering. The recently introduced fluxgate-based sensor [4] has even better offset. However, despite its higher power consumption, its bandwidth is limited to 75 kHz. The current consumption of the multi-path Hall sensor system is somewhat higher than other CMOS Hall sensors due to the extra biasing currents consumed by the Hall sensors in the HF path. Thanks to the differentiating characteristic of the pick-up coils, the extra bandwidth of the hybrid multi-path system does not involve a similar trade off with power.

V. Conclusions

This paper has proposed a multi-path technique for wide-bandwidth CMOS magnetic sensor. Compared to previous low-offset CMOS magnetic sensors, the combination of spinning Hall sensors and non-spun Hall sensors achieves a bandwidth of 400 kHz, a 40x improvement. The combination of spinning Hall sensors and pick-up coils achieves a bandwidth of 3MHz, which represents a further order of magnitude improvement. These two examples demonstrate that the use of multi-path architectures effectively breaks the usual design trade-off between sensor bandwidth, on the one hand, sensor offset and resolution, on the other.

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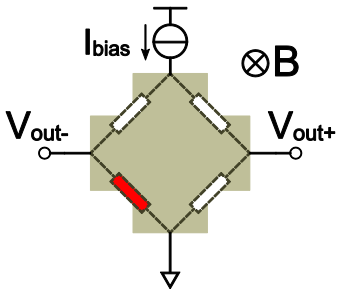

Fig. 1 A model of a CMOS Hall sensor.

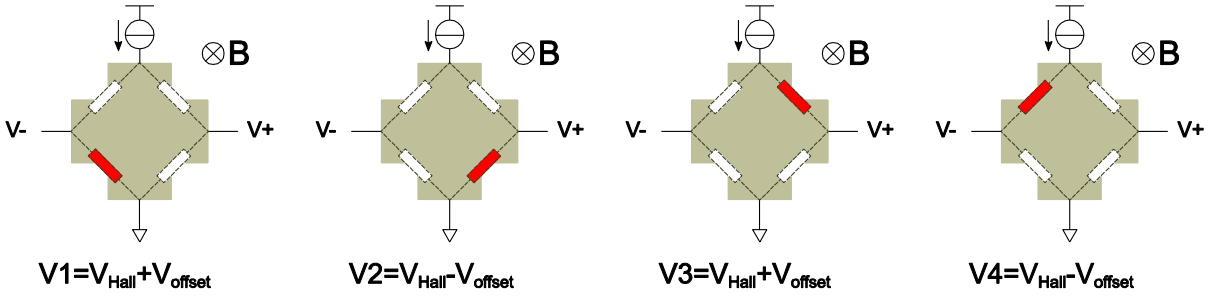

Fig. 2 The operation of the spinning current technique.

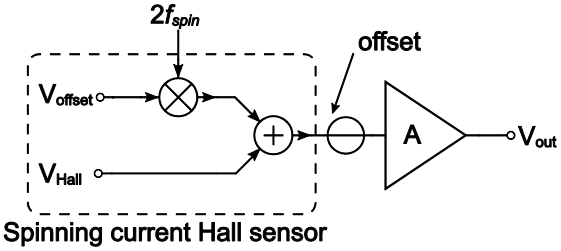

Fig. 3 Extra offset caused by the readout circuitry

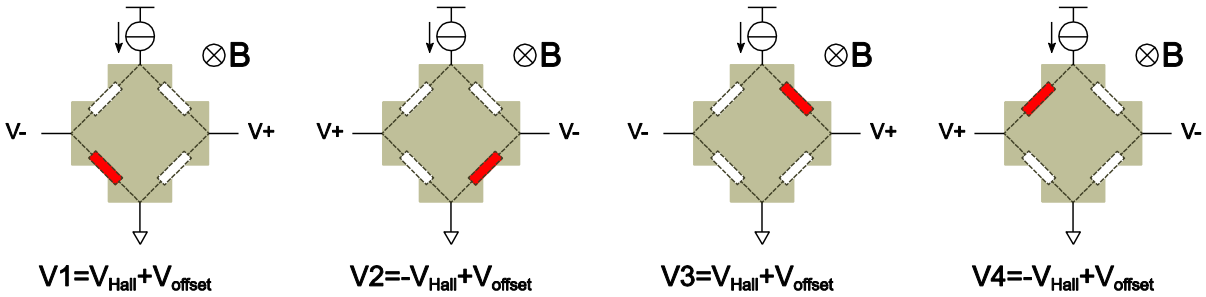

Fig. 4 A slightly modified spinning current algorithm which modulates the magnetic signal to $2f_{spin}$.

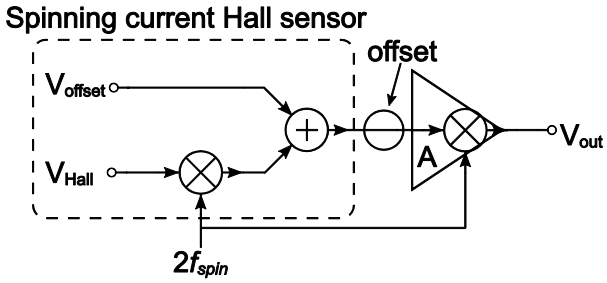

Fig. 5 A demodulator to readout the modified spinning current Hall sensor, where the offsets of the readout and the Hall sensor are merged.

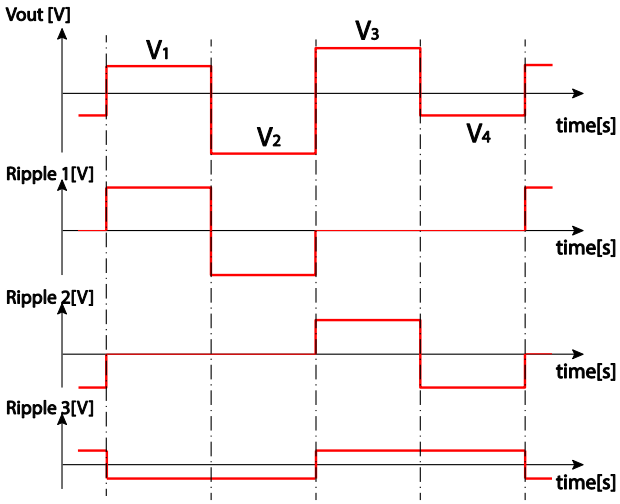

Fig. 6 4-phase spinning ripple can be decomposed into 3 orthogonal ripple components

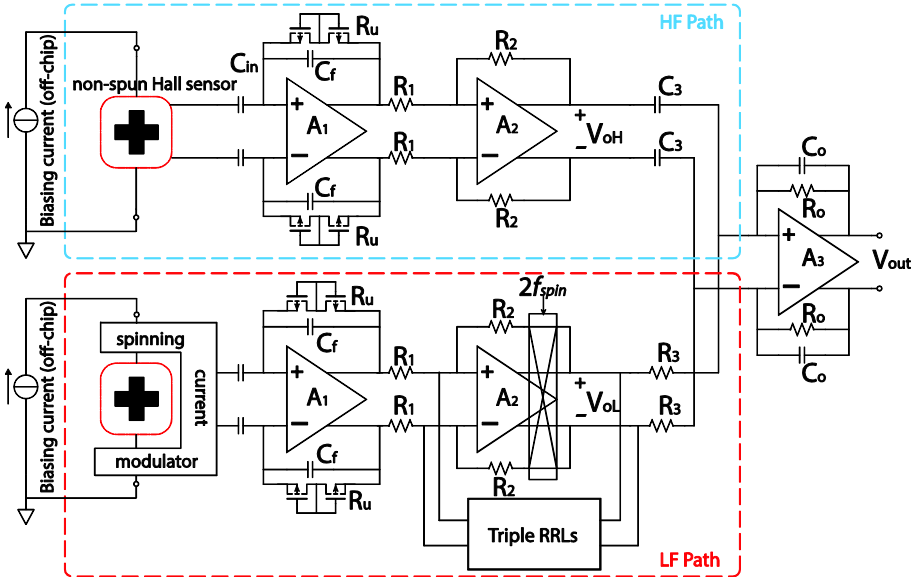

Fig. 7 System diagram of combining a spinning current Hall sensor and a non-spun Hall sensor

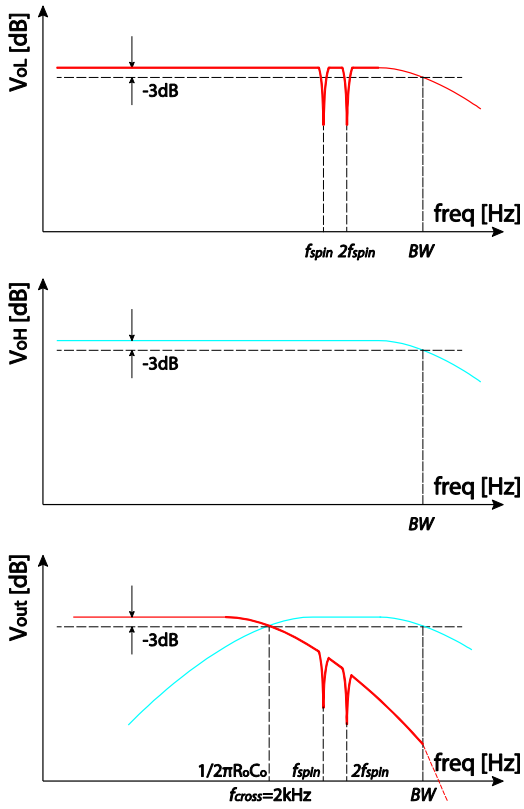

Fig. 8 the Bode plots of the LF path, the HF path, and the multi-path Hall sensor system.

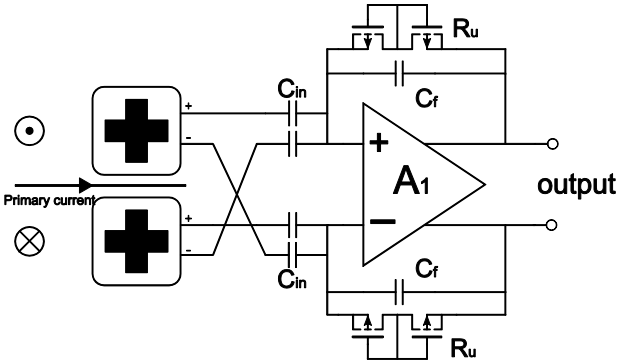

Fig. 9 the capacitively coupled 1st stage combines two Hall sensors at the virtual ground to realize a differential measurement

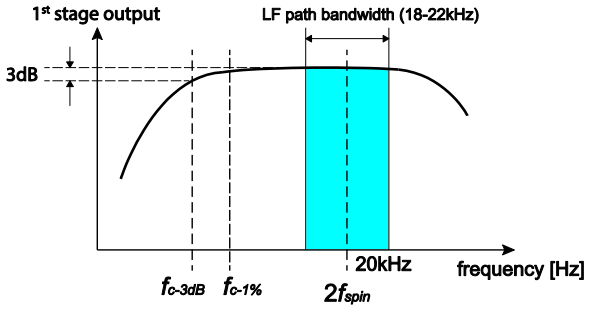

Fig. 10 the 1st stage need to have a flat bandwidth covering 18 – 22 kHz

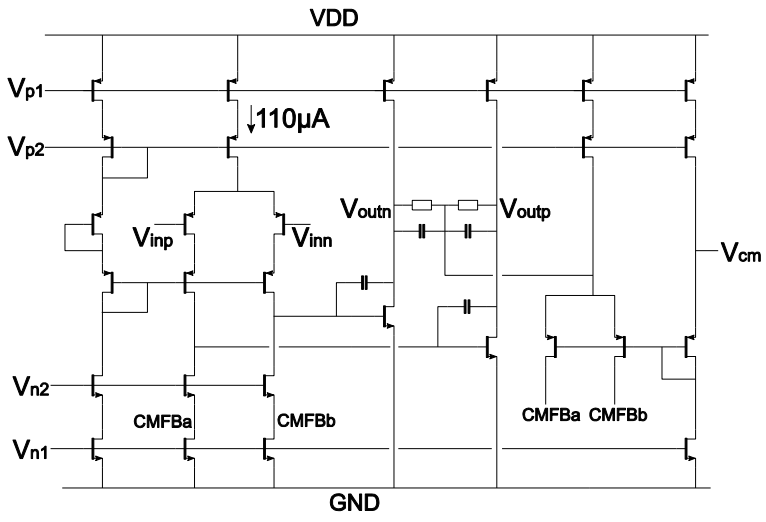

Fig. 11 the implementation of the 1st opamp A1

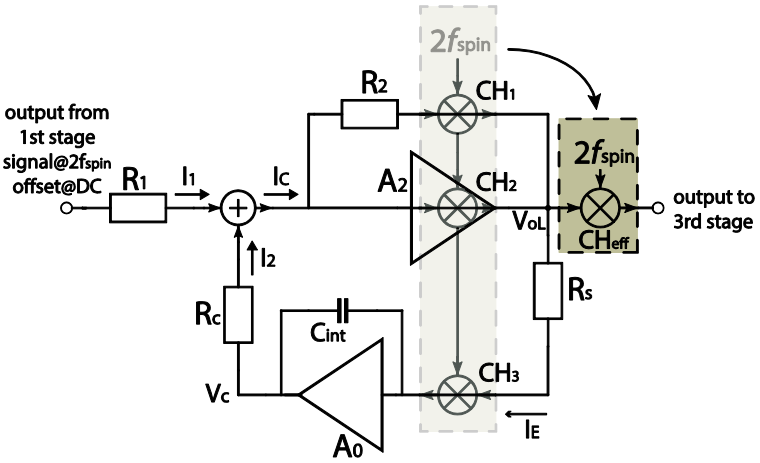

Fig. 12 the implementation model of a single RRL

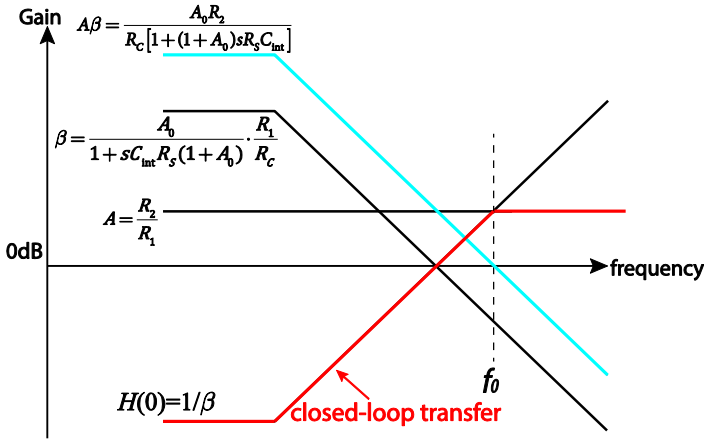

Fig. 13 The Bode plot of simplified RRL model

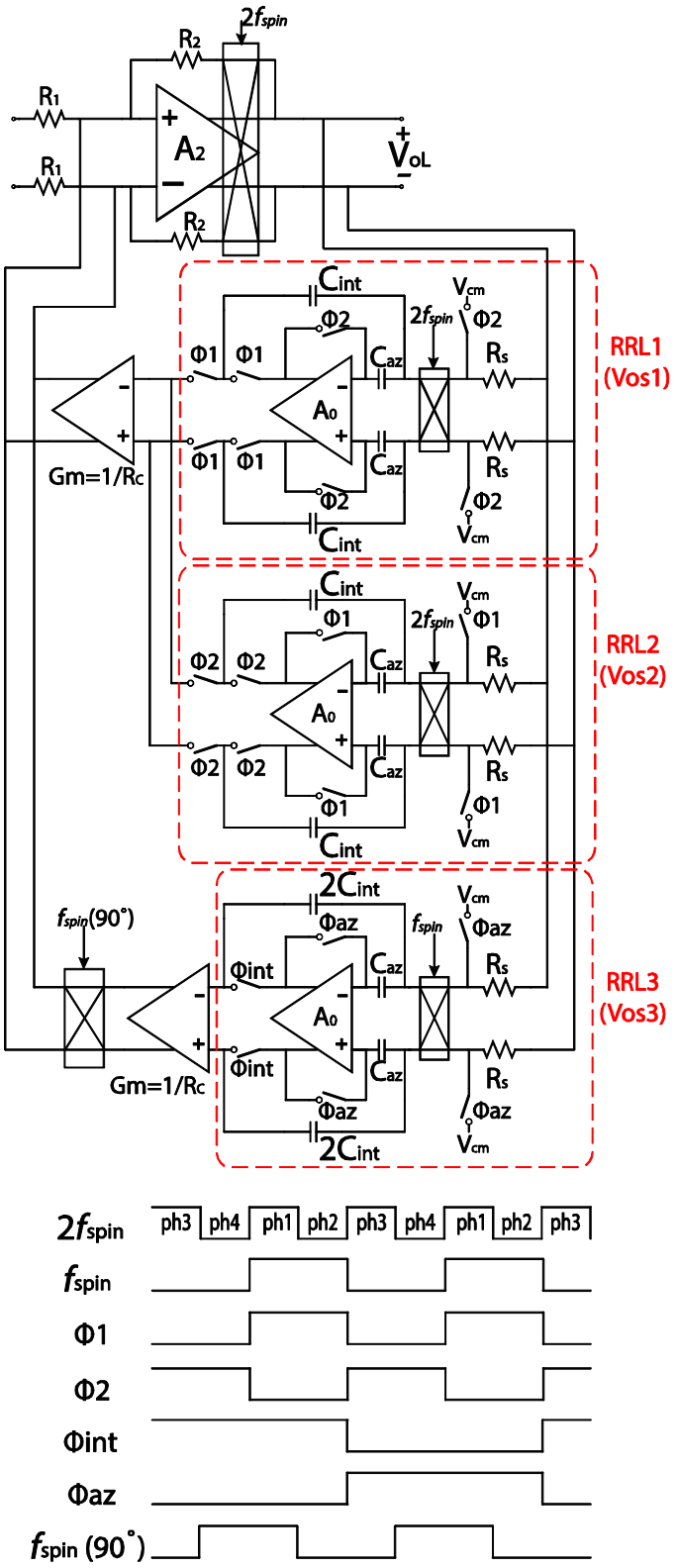

Fig. 14 the complete implementation of the triple RRLs

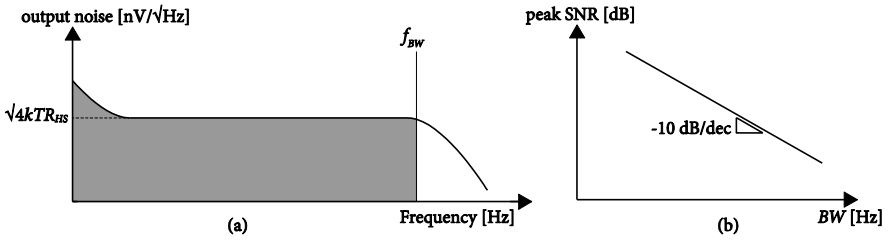

Fig. 15 (a) output noise of a Hall sensor; (b) the decreasing peak SNR with a slope of -10 dB/dec.

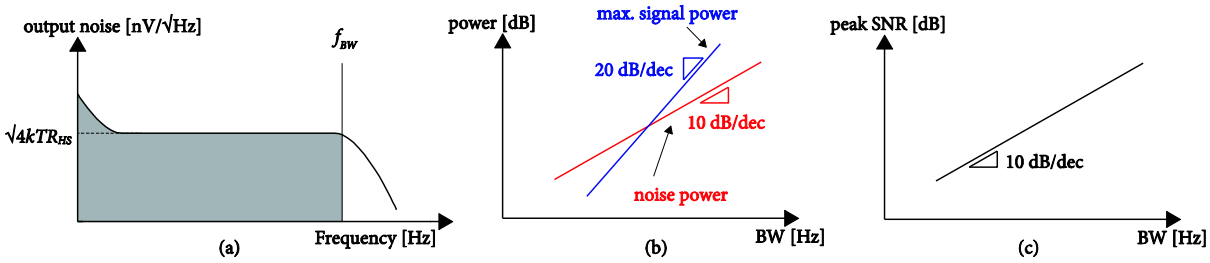

Fig. 16 (a) output noise of a pick-up coil; (b) the increasing noise power with a slope of 10 dB/dec and the increasing signal power with a slope of 20 dB/dec; (c) the decreasing peak SNR with a slope of -10 dB/dec.

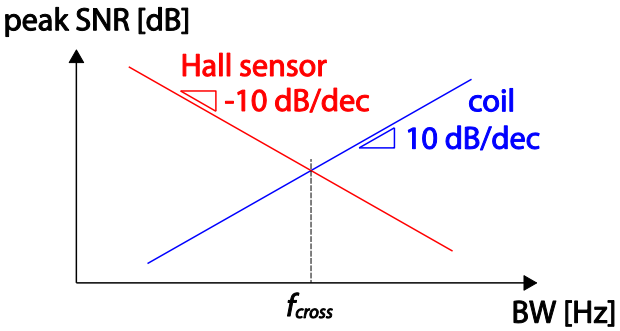

Fig. 17 Peak SNR plots of Hall sensors and coils

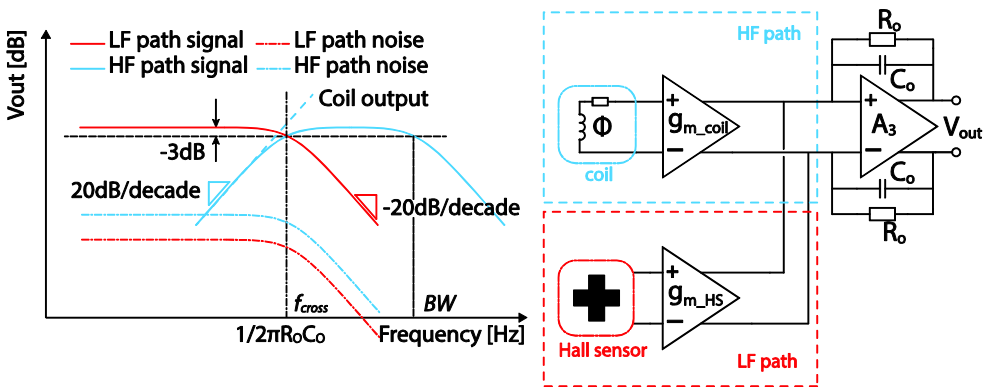

Fig. 18 Proposed network to combine Hall sensors and pick-up coils

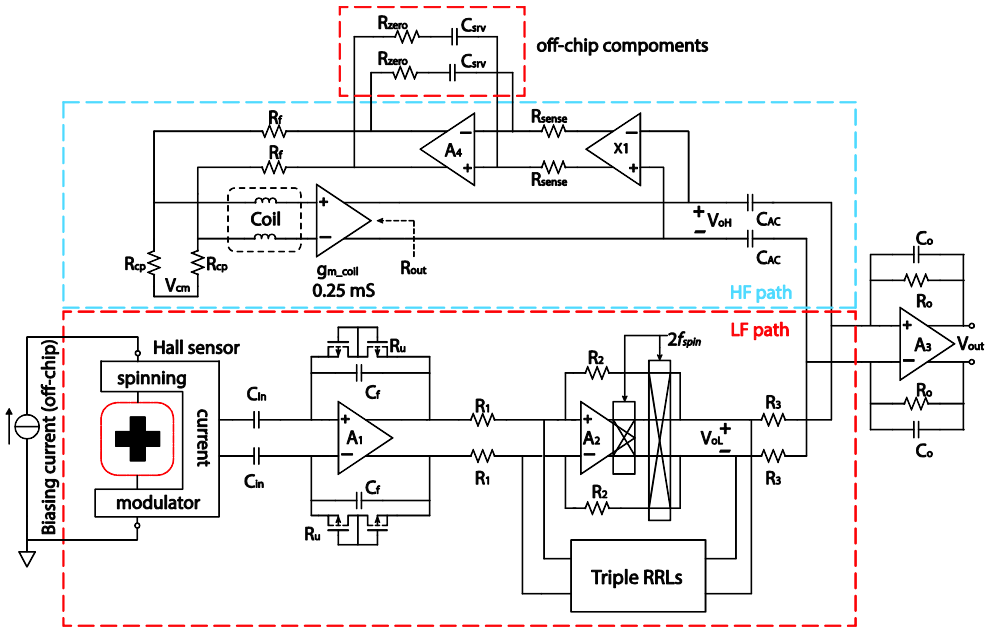

Fig. 19 The detailed implementation of combination of Hall sensors and pick-up coils

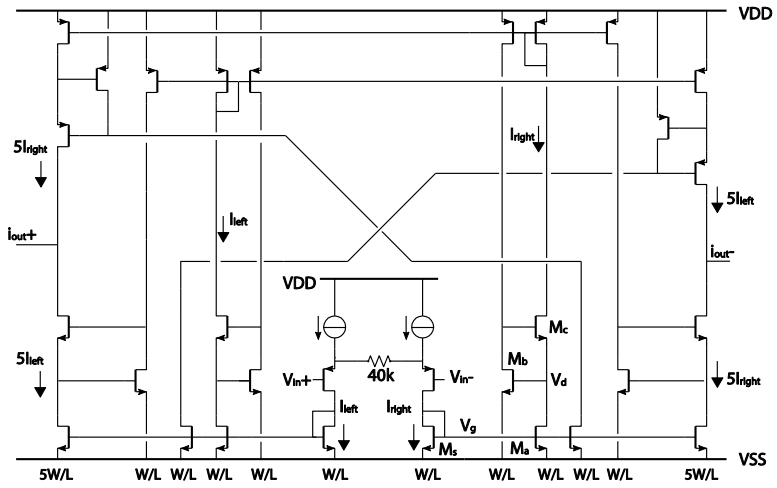

Fig. 20 The implementation of g_{m_coil}

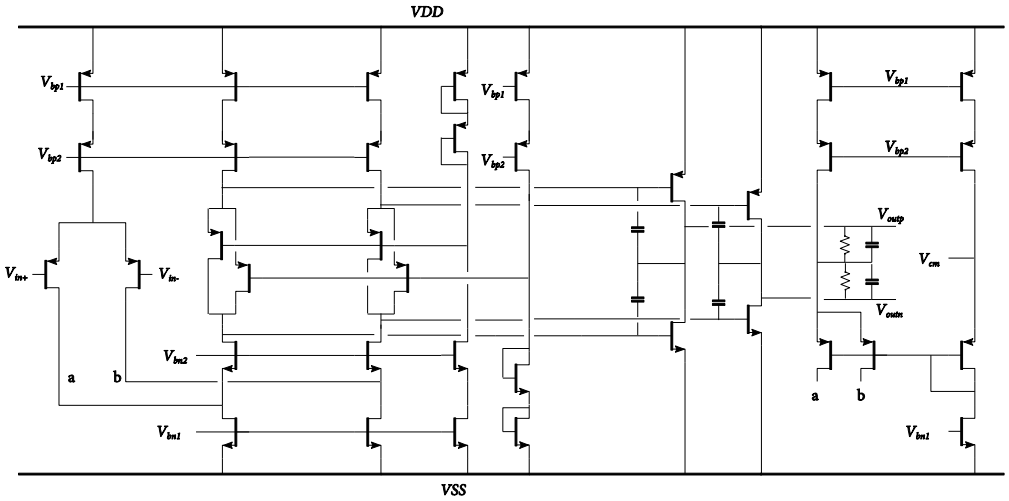

Fig. 21 The implementation of the output stage

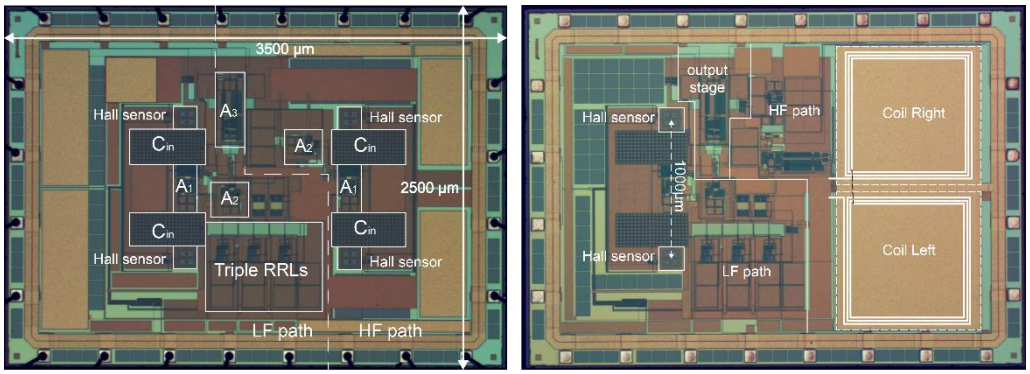

Fig. 22 (a) the chip photo of the multi-path Hall sensor system; and (b) the chip photo of the system combining Hall sensors and pick-up coils

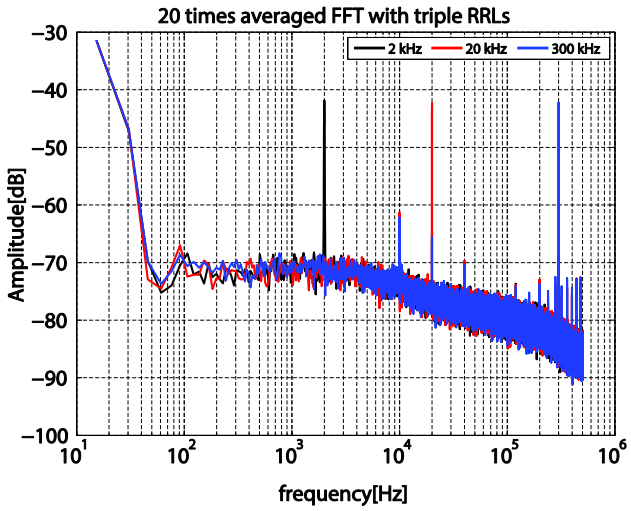

Fig. 23 FFT of the multi-path Hall sensor system with input signals at 2 kHz, 20 kHz, and 300 kHz.

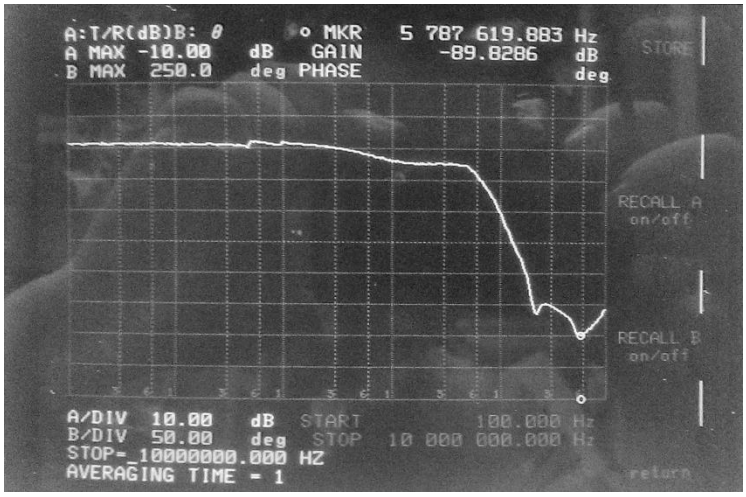

Fig. 24 The bandwidth measurement results of the multi-path Hall sensor system, whose high frequency response is distorted by the eddy current within the frame pad

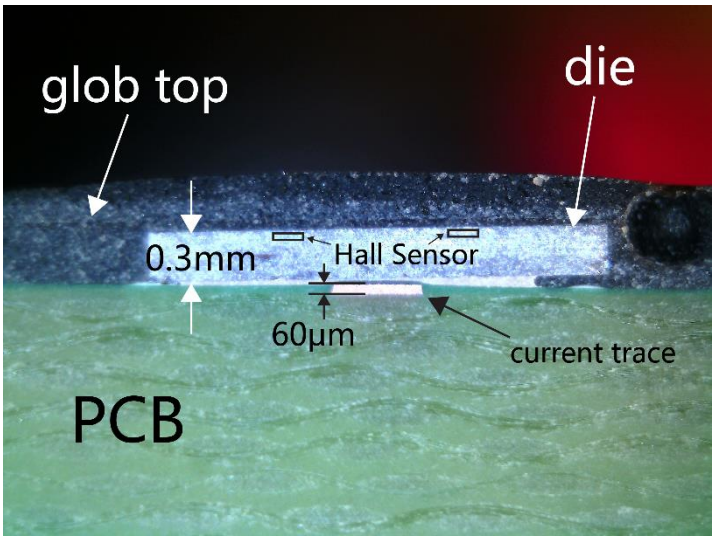

Fig. 25 The cross section of chip-on-board sample

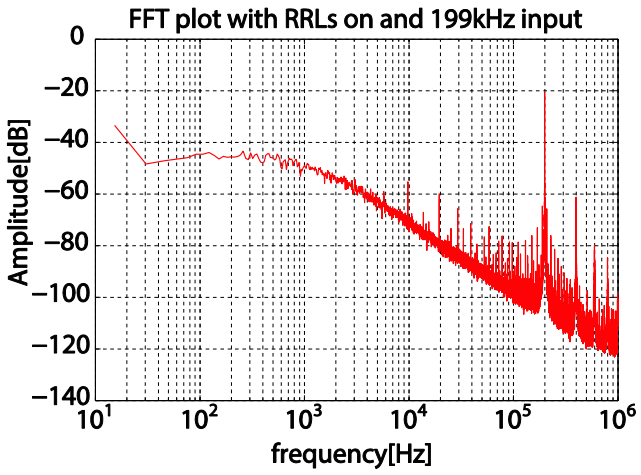

Fig. 26 The FFT plot of the hybrid multi-path system with an input current at 199 kHz

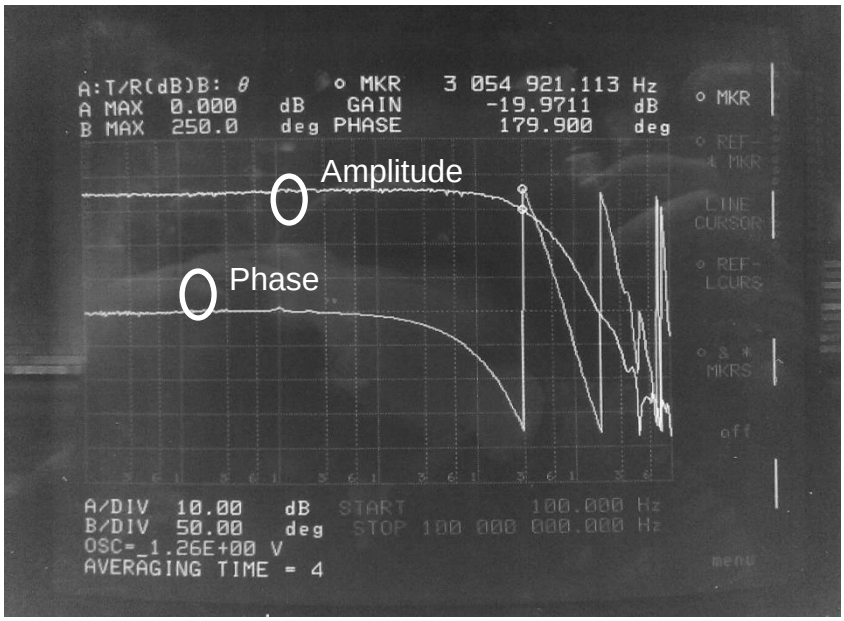

Fig. 27 Measurement result of the amplitude and phase response of the multi-path hybrid system over the frequency range from 100 Hz to 100 MHz

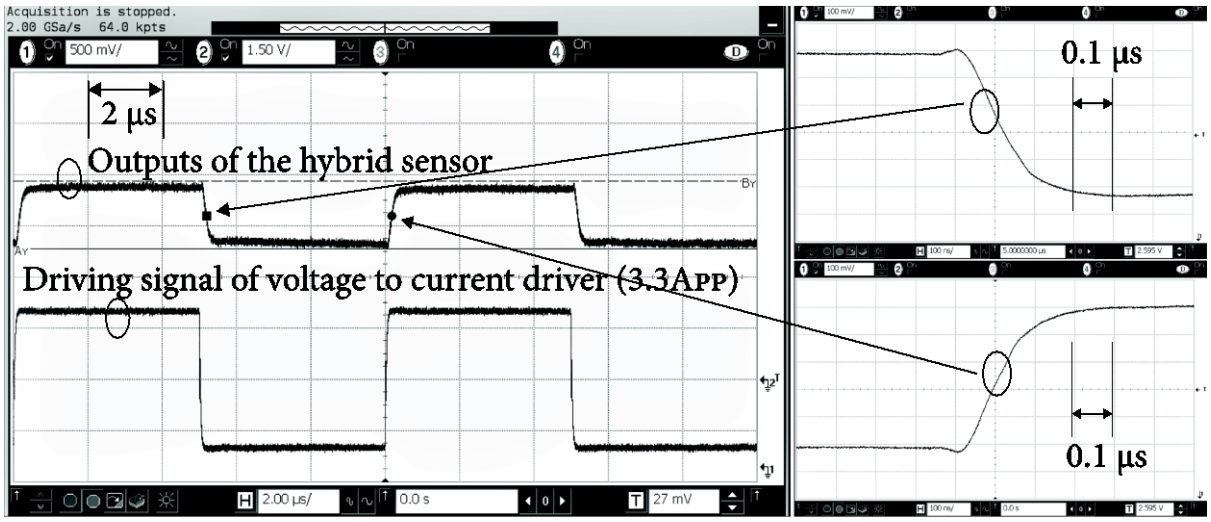

Fig. 28 The step response of the hybrid multi-path system, a settling (90%) time of less than 400 ns has been achieved

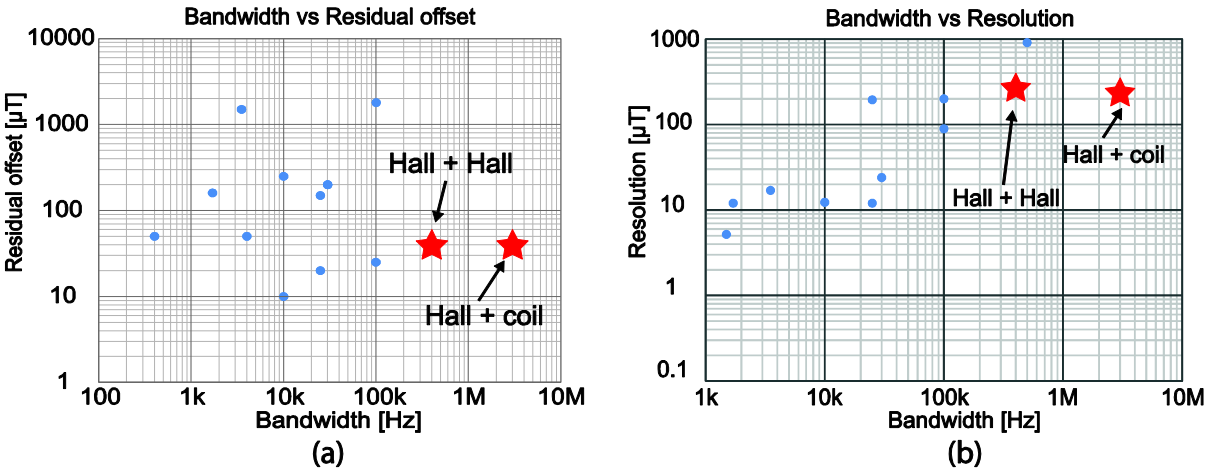

Fig. 29 The benchmark plot of (a) bandwidth vs offset, and (b) bandwidth vs resolution

Source	This work		[3]	[14]	[6]	[8]
Sensor type	Hall + coil	Hall + Hall	Fluxgate	Hall	Hall	Hall
Technology	0.18 µm	0.18 µm	0.6 µm	0.35 µm	0.5 µm	0.35 µm
Maximum offset [µT]	40	40	0.9	10	3.65 (3σ)	10
Area [mm^2]	8.75 (analog front-end)	8.75 (analog front-end)	9.8	5.7	N/A	6.5
Resolution [μT_{rms}]	210 (diff)	272 (diff)	0.1	0.6	0.33	N/A
Input range	±7.8 mT (diff)	±12.5 mT (diff)	±1.32 mT (diff)	±0.5 mT	±10.8 mT	N/A
Bandwidth	3 MHz	400 kHz	75 kHz	100 Hz	5 Hz	10 kHz
Output	Analog	Analog	Digital	Digital	Digital	Digital
Supply current [mA]	7.7	8	56	5	4.2	N/A

Tab. 1 Comparison table