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A Defect-Oriented Test Approach Using On-Chip Current Sensors for Resistive Defects in FinFET SRAMs

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Abstract

Resistive defects in FinFET SRAMs are an important challenge for manufacturing test in submicron technologies, as they may cause dynamic faults, which are hard to detect and therefore may increase the number of test escapes. This paper presents a defect-oriented test that uses On-Chip Current Sensors (OCCS) to detect weak resistive defects by monitoring the current consumption of FinFET SRAM cells. Using OCCS, all our single cell injected resistive defects have been detected within a certain accuracy by applying 5 read or write operations only, independent whether they cause static or dynamic faults. The proposed approach has been validated and the detection accuracy has been evaluated. Simulation results show that the approach is even able to detect weak resistive defects that do not even sensitize faults at the functional level, thus able to increase the reliability of devices.

1. Introduction

Technology miniaturization has presented many challenges on conventional planar Complementary Metal-Oxide Semiconductor (CMOS) transistors [1]. FinFET technology has become the best approach to continue the downscaling of Integrated Circuits (ICs) [2] as it shows improved short-channel behaviour and overcomes the growing subthreshold leakage of CMOS technology [3,4]. Nevertheless, to achieve high storage density and access speed, Static Random Access Memories (SRAMs) are produced at the limits of the process equipment and therefore statistically more prone to be affected by manufacturing defects [5]. As a result, these devices must be efficiently tested i.e., a high defect/fault coverage at low cost.

Weak resistive defects are known for causing dynamic faults, a subset of faults that are only sensitized by a sequence of consecutive operations. Many fault-oriented test approaches, such as standard March algorithms, do not target these types of faults [6–8] or are limited by the number of consecutive operations [9–12]. Using exhaustive March tests to sensitize faults results in expensive manufacturing tests, as the test cost is directly related to the time each product stays on the tester [13]. Disparate approaches, such as monitoring the static or dynamic current consumption of SRAM cells [14–17], have been proposed to improve the detection of weak defects. Nevertheless, their efficacy regarding FinFET devices affected by resistive defects is unknown.

This paper presents a defect-oriented test approach based on On-Chip Current Sensors [18,19] for testing FinFET memories. Rather than focusing on the faults caused by resistive defects, the proposed approach concentrates on their effect on current characteristics. We use OCCSs to monitor and identify discrepancies in the current consumption of each SRAM cell caused by resistive defects. The results show that all our single cell injected resistive defects have been detected within a certain accuracy by applying only 5 read or write operations, independent whether they cause static or dynamic faults. Furthermore, the proposed approach is able to detect weak resistive defects that do not even sensitize faults at the functional level. The main contributions of this paper are as follows:

- A memory test methodology using OCCS

able to detect weak and strong resistive defects. It can significantly reduce test time, and therefore reduce manufacturing test cost.
- Verification of the proposed approach and evaluation of its detection coverage using Spice simulations.
- Evaluation of the overhead of the proposed scheme.

The remainder of this paper is organized as follows. Section II lays out the background related to FinFET technology and testing. Section III details the proposed methodology based on OCCS, whereas Section IV presents its validation. Then, Section V discusses its detection capability based on simulations and the overhead of the approach. Finally, Section 6 concludes this paper.

2. FinFET Technology and Testing

In this section, background information on the FinFET technology and FinFET device testing will be provided.

2.1. FinFET technology

FinFETs transistors are quasi-planar, multi-gate devices consisting of vertical stripes of silicon denominated "fins" that are wrapped by a gate structure [20]. This technology's main advantage are reduced Short-Channel Effects (SCEs) as the gate controls multiple sides of the channel [21]. It consequently reduces the leakage current and boosts the technology miniaturization even further. Other advantages of FinFET technology are its improved electrostatic characteristics [22] and its compatibility with the standard CMOS fabrication process [23]. Furthermore, FinFET technology provides specific advantages to SRAM memories' performance and stability. Conventional CMOS SRAM sizes are limited by the random variations of V_{TH} caused by Random Dopant Fluctuation (RDF) introduced by high doping [23]. As FinFET devices do not require high doping concentration to control the leakage current [4], its RDF is expressively reduced [24], thus minimizes V_{TH} variations and allows the V_{DD} to be scaled down [25].

2.2. FinFET testing

One of the biggest challenges of SRAM testing is using realistic defect and fault models alongside test solutions with minimal application time [26]. As companies adopt FinFET technology in their new products, the use of standard memory test procedures that were developed with defect and faults models of planar technologies may not be sufficient to provide the desired fault coverage for FinFET devices. The reason for this are differences in its physical structure and additional manufacturing steps. Harutyunyan et al. investigated the impact of resistive defects in FinFET-based memories and concluded that such memories are more susceptible to dynamic faults [27] than memories designed with planar technologies. Due to this distinction, they proposed a FinFET-specific March algorithm [12] that relies on the execution of up to 8 consecutive operations applied to the same cell. Faults that require more than 8 consecutive operations are not sensitized, and hence not detected. Dynamic coupling faults in FinFET SRAMs have also been reported by Copetti et al. [28]. Consequently, March algorithms for FinFET memories should also address such faults.

Lin et al. [17] investigated the efficacy of using March Tests as well as I_{DDQ} to detect Gate Oxide Shorts (GOS) in FinFET SRAMs. According to the authors, this type of defects causes more complex fault behaviours in FinFETs than in planar transistors due to their unique structure. They concluded that both methodologies may present limitations for this technology, which can effectively increase the number of test escapes and reduce cell's reliability. Therefore, test solutions that rely on operations executing specific patterns and stressing conditions may not stand to be reliable strategies for investigating the presence of other types of defects in FinFET circuits.

3. Methodology

This paper introduces a defect-oriented test approach based on OCCS to detect resistive defects, including weak defects, on FinFET-based SRAMs. Rather than focusing on faults and observing output of operations, the proposed approach concentrates on the impact of resistive defects on the switching current during read and write operations of the memory cells. Fig. 1 illustrates the schematic of the 6T SRAM cell and the injected resistive defects. They are modelled as resistive-open (RO) defects (Fig. 1(a)), which create resistances in existing connections, and resistive-bridge (RB) defects (Fig. 1(b)), which create connections between two different nodes.

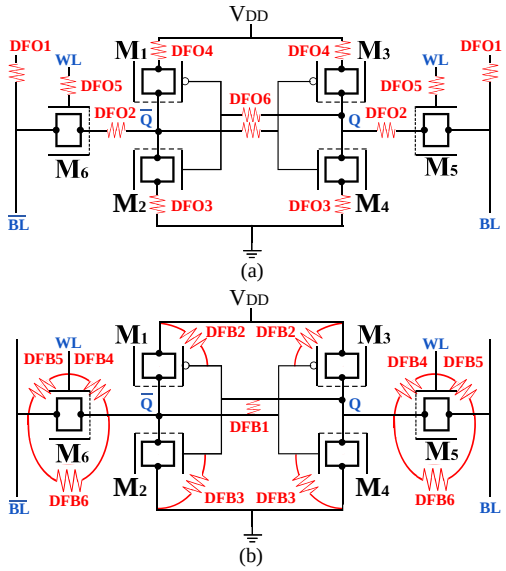

Fig. 1. Set of Resistive defects injected in memory cells: (a) Resistive-Open and (b) Resistive-Bridge defects.

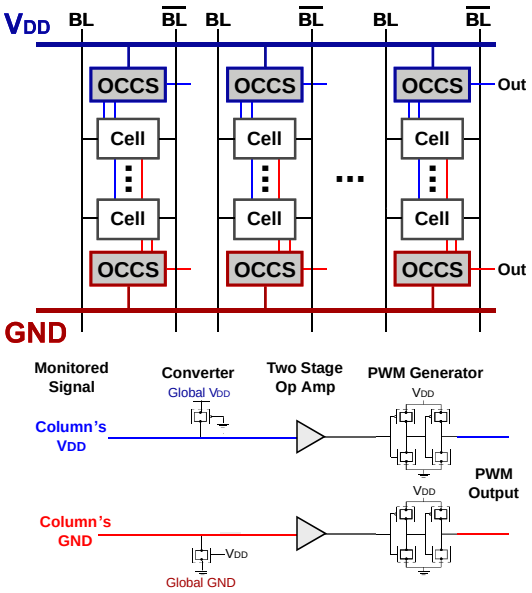

Fig. 2. Architecture of the proposed hardware-based approach.

The proposed methodology monitors the current flowing on V_{DD} and GND by inserting a set of OCCSs [18,19] (one for V_{DD} and one GND) in each column of the memory array. The architecture of the proposed approach is presented in Fig. 2. OCCSs are composed of three functional blocks: (1) a current-to-voltage converter, (2) a two-stage operational amplifier, and (3) a Pulse-Width Modulation (PWM) generator. A current-to-voltage converter is inserted prior to the operational amplifier. This single transistor works as a low impedance resistor that generates small voltage changes in V_{DD} and GND nodes based on the current consumption of each column. Therefore, any current flowing in the column's cells causes voltage changes in the power supply signal. Owing to these variations, this signal is used as the input for the operational amplifier. It generates pulses that are afterwards modulated by the PWM circuitry to represent the unique behaviours of the monitored current consumption signal. Because resistive defects alter current characteristics, defective cells present a different current consumption compared to their defect-free neighbours. This ultimately creates distinct pulses and modulated signals. Finally, a detection logic circuit compares the signals generated by OCCSs and raises a flag whenever a mismatch is observed.

Defects of different magnitudes have been injected to sensitize their detection conditions. Three scenarios were considered: the defect is too weak to sensitize any fault; the defect is strong enough to sensitize dynamic faults; and the defect is strong and sensitizes static faults. The first two scenarios are responsible for the majority of test escapes and reliability problems, and are therefore the focus of the proposed approach. To obtain realistic defect values for the defects in Fig. 1, we use the data presented in [28].

4. Results

4.1. Simulation Setup

The simulation platform consists of an 8 x 8 SRAM array, where the bit lines and word lines have capacitive loads which emulate a 16 KB memory array. The peripheral circuitry around the SRAM array ensure proper execution of read and write operations; each memory column had its own write driver, differential sense amplifier, and pre-charger. The frequency is set to 1 GHz, the operating temperature to 27°C, and the supply voltage to 0.9 V.

A Low Power (LP), Multi-Gate (MG) 20nm FinFET compact model developed by [29] that describes Shorted-Gate, Bulk Mode FinFETs transistors was adopted. All circuits and memory peripherals (buffers, decoders, sense amplifiers, pre-chargers, etc.) were described in Spice using the same compact model.

Table 1
Critical resistances and detection efficacy for the proposed defect-oriented test approach

Defect	Critical Resistances [28]	Resistance Resolution
DFO1	13.6 kΩ	3.85 kΩ
DFO2	145 kΩ	1.30 kΩ*
DFO3	72.5 kΩ	1.40 kΩ*
DFO4	-	1.60 kΩ
DFO5	1.52 MΩ	82 kΩ
DFO6	1.82 MΩ	20 kΩ
DFB1	37.6 kΩ	3.60 MΩ*
DFB2	13.7 kΩ	2 MΩ
DFB3	46 kΩ	4.9 MΩ
DFB4	13.65 kΩ	1.7 MΩ
DFB5	4.8 kΩ	40 kΩ
DFB6	11.4 kΩ	1.28 MΩ

* Weakest defect injected

The current consumption of the cell is analysed using a simple March sequence. This algorithm first initializes all cells, assuring that they are in the same state. Then, it sequentially applies the sequence write '0', read '0', write '1', read '1' (*w0*, *r0*, *w1*, *r1*) to each row of the array. Thus, the algorithm can be written as ⇳(*w1*); ⇓(*w0*, *r0*, *w1*, *r1*).

4.2. Simulation Results

The detection accuracy of the proposed approach is analysed by comparing OCCSs' outputs of defect-free and defective cells for a given defect. The critical resistance values R_C of a defect is the weakest defect value that is able to sensitize any fault using traditional March-based testing. We analyse the detection capability by sweeping the value of the resistive defect between a certain range. For a RO defect, the lower bound of this range equals to 1/100 of R_C, while the upper bound is set equal to R_C. For RB defects, the opposite applies; the lower bound equals 100*R_C, while the upper bound is set equal to R_C.

The results of the experiments are shown in Table 1. The table shows for each defect its R_C and resistance resolution. The latter is defined as the minimum (for opens) or maximum (for bridges) resistance value that is detectable by the output of the OCCS. For some defects, detection was already possible when the weakest defect for this evaluation

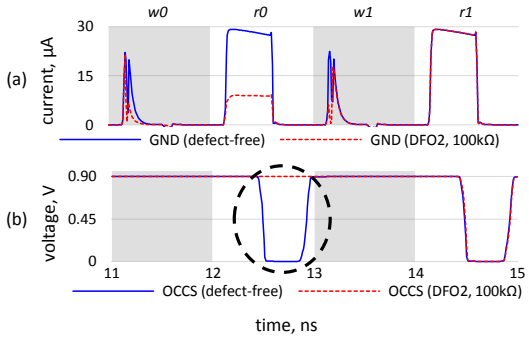

Fig. 3. Simulation of defect DFO2 (a) input of OCCSs (b) output of OCCSs

was injected; such cases are identified with an asterisk. Note that the resistance resolution is always lower with respect to R_C for resistive-open defects, while higher for resistive-bridge defects. Therefore, the detection capability is better than traditional based March tests.

Next, we will analyse two representative cases in more detail. They are the RO defect DFO2 and RB defect DFB5. Fig. 3 depicts the input and output waveform of the OCCS for defect DFO2=100 kΩ when the March element ⇓(*w0*, *r0*, *w1*, *r1*) is executed. Part *a* of the figure shows the input current to the OCCS that is connected to the ground, while part *b* the output voltage. The blue lines represent the signals for a defect-free cell, while red dashed lines represent the signals of the cell with the defect present. During the *r0* operation, there's a sharp discrepancy in current consumption between cells. This disparity results in the PWM circuit producing two distinct signals at the OCCS's output, highlighted on Fig. 3(b). Other small current disparities are observed during write operations but are not visible at the sensor's output. Note that as the defect value of 100 kΩ is lower than R_C=145 kΩ, this defect cannot be detected by conventional March tests.

Similarly, Fig. 4 shows the input and output waveform of the OCCS for defect DFB5=40 kΩ that is connected to V_{DD}. Again, blue lines represents the defect-free cell, while red dashed lines the defective cell. The discrepancy in consumption during the *w0* and *r0* operations caused by the resistive-bridge defect results in distinct OCCS output signals. In fact, during the *r0* operation, the output of the sensor monitoring the column with the defective cells is a strong '1', while the sensor from the defect-free column outputs a strong '0'. Conventional March tests would not detect this defect as the resistance of 40 kΩ is larger than R_C=4.8 kΩ.

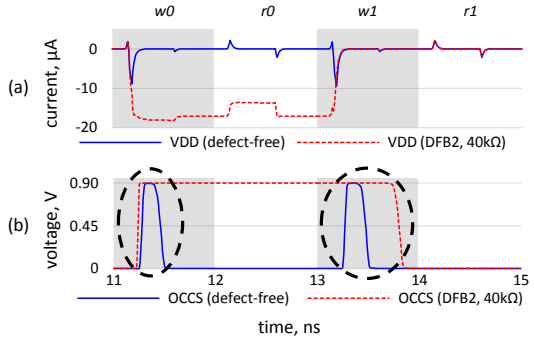

Fig. 4. Simulation of defect DFB2 (a) input of OCCSs (b) output of OCCSs

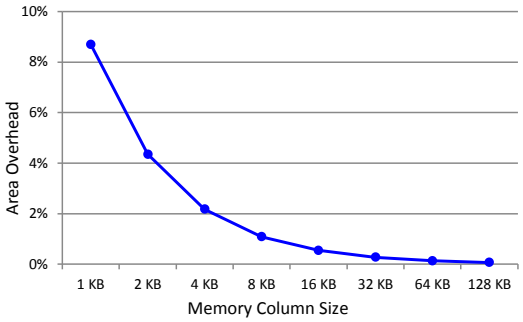

Fig. 5. Area overhead for different column sizes.

4.3. Discussion and limitations

Power consumption, test time, and area overhead of the proposed approach were also evaluated. The power consumption was measured during the execution of the adopted March algorithm before and after the insertion of OCCS monitors. Without the monitors, a power consumption of 806.63 µW has been measured. An increase of 15% has been observed when the monitors were added.

One of the main advantages of the proposed approach is the reduction in test time. Standard test algorithms can be very time expensive, especially if targeting dynamic, coupling, or linked faults. However, the proposed approach does not rely upon what type of faults are sensitized by the defects, or if there are faults at all. Only 5 operations are necessary to ensure that each cell is put under transition scenarios (‘0’ to ‘1’, and ‘1’ to ‘0’). Thus, it can significantly reduce the test time and therefore reduce manufacturing test cost. Moreover, it can also increase the reliability as many weak defects can be detected as well.

An accurate area overhead cannot be estimated as the compact FinFET model does not have a physical layout. However, a general area overhead can be roughly estimated by comparing the number of fins in a column and the number of fins in two OCCSs (one for V_{DD} and one for GND). Note that the word size does not impact the relative area overhead. Fig. 5 shows the area overhead for different column sizes. For a 1 KB memory column, the introduction of sensors has approximately an overhead of 8.69%. For a 4 KB memory column, this overhead decreases to 2.17%. In case the memory contains multiple smaller arrays, the same OCCS can be reused as long as only one memory is active at a time. Therefore, varied memory organizations can be adopted to reduce the area overhead of the approach.

5. Conclusion

This paper presented a defect-oriented test approach that identifies the presence of resistive defects in FinFET-based SRAM memory cells by connecting OCCS monitors to VDD and GND. All injected resistive defects were detected within a certain accuracy applying 5 operations only, independent whether they caused static or dynamic faults. Compared to other March tests, the proposed approach has a very small test time. In the future, we would like to analyse the impact of inter-cell defects as well.

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