High-Pass ΣΔ Converter Design Using a State-Space Approach and Its Application to Cardiac Signal Acquisition

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High-pass $\Sigma\Delta$ converter design using a state-space approach and its application to cardiac signal acquisition

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***Abstract*—Cardiac signal acquisition with high linearity and accuracy of the high-pass cut-off frequency imposes a challenge on the implementation of the analog preprocessing and the analog-to-digital converter. This paper describes a state-space based methodology for designing high-pass sigma-delta (HP$\Sigma\Delta$) topologies, targeting high accuracy and linearity of the high-pass cut-off frequency. Intermediate functions are evaluated mathematically to compare the proposed HP$\Sigma\Delta$ topologies with respect to dynamic range. A sensitivity performance analysis of the noise transfer function with respect to integrator non-idealities and coefficient variations is also described. Finally, to illustrate the design approach, an orthonormal HP$\Sigma\Delta$ modulator is designed to be implemented in 0.18 μm CMOS technology, is tested with real pre-recorded ECG signals.**

***Index Terms*—State-space synthesis, high-pass sigma-delta converter, orthonormal, intermediate functions, sensitivity, ECG, baseline wandering.**

I. Introduction

ELECTROCARDIOGRAPHY (ECG), the recording of electric signals generated by the heart, is used as a diagnostic monitoring method for cardiovascular diseases (CVDs). It contains specific physiological information about the functioning of the heart. To meet the growing demand of the geriatric population and to reduce the burden on the public health-care system, there is a requirement of compact, inexpensive health-care devices that enable continuous ECG recording for the detection of cardiac arrhythmias that manifest themselves as aperiodic events over a period of days or weeks. Acquisition of the ECG is faced with the challenge of removal of the baseline wandering due to respiration or movements while recording. Baseline wandering (BW), which contributes to low frequency interference, is responsible for distortion of the acquired waveform and poses a challenge in accurate interpretation of the CVDs. In order to minimize the effect of baseline wandering, it is necessary to implement a high-pass filter with high linearity and an accurate cut-off frequency. As per the International Electrotechnical Commission (IEC) standards, the recommended ECG bandwidth extends from 50 mHz to 200 Hz. However, the baseline wander, which could be lying inband at the lower end, may require a higher high-pass cut-off frequency for its removal [1], [2]. It can be observed in Fig. 2a, derived from the MIT-BIH normal sinus rhythm database (Record 17453), [3], [4], that there is a large amount of signal energy around the sub-Hz region. Fig. 2b, derived from the MIT-BIH normal sinus rhythm database (Record 16773), shows the effect of baseline wandering resulting from low frequency interference lying in the sub-Hz region.

With the bandwidth of the ECG signal extending from sub-Hz to 200 Hz [5], a major challenge for an ECG readout system lies in implementing the sub-Hz high-pass cut-off

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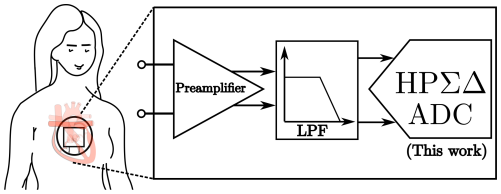
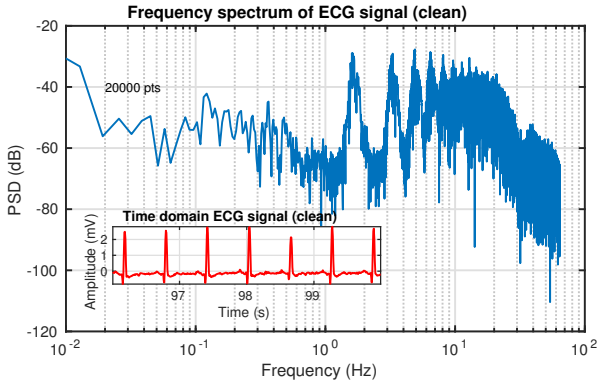
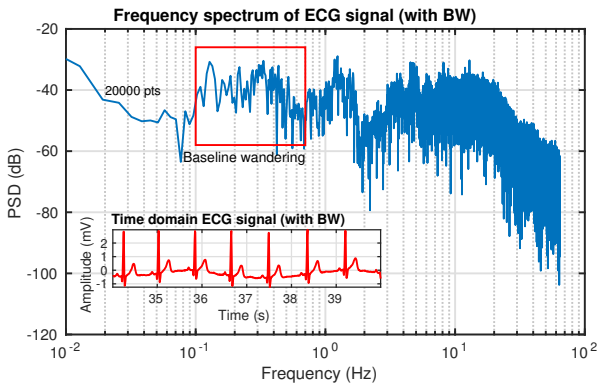


Figure 1: Analog front-end for ECG acquistion



(a)



(b)

Figure 2: Power spectral density of (a) Clean ECG (b) ECG with baseline wandering (Data courtesy: MIT-BIH database [3])

frequency (f_{hpf}) as this translates into the realization of large time constants. To realize large time constants in the order of a few seconds, there exist techniques that employ pseudo-resistors [6]–[8] or g_m blocks [9] or off-chip solutions such as using an IIR-filter [10] or a resistor [11]. Recently, a new technique to implement large time-constants has been introduced, employing duty-cycled resistors [12]. Although this technique is an attractive alternative, the position of the high-pass pole is still determined by the product of R and C, which is less accurate than a switched capacitor implementation. Moreover, the resistance would occupy a larger area as compared to a small sampling capacitor for the same f_{hpf}. Pseudo-resistors, designed using transistors biased in the cut-off region to obtain extremely large resistances are not very robust to PVT variations. As these transistors are intrinsically non-linear, the resistances vary with the signal level, eventually leading to clipping at the extremes [13]. As there is quite some energy in the spectrum around the highpass cutoff frequency, a.o., due to baseline wandering, this leads to a reduced dynamic range. Also, as the momentary value of the resistance depends on the momentary value of the input signal, the RC time-constant is not fixed. Note, in such a case it would be better to talk about the dynamic eigenvalue of the non-linear differential equation implemented by the pseudo-resistor-capacitor combination. Depending on the choice of the implementation of the resistance, there is a trade-off between the area consumption, linearity around the f_{hpf} cut-off and the accuracy of the f_{hpf}. The existing solutions do not focus on achieving the same linearity around the high-pass cut-off frequency as the rest of the signal band, although it is an important performance metric in order to acquire a low-distortion bio-signal waveform, especially in the case of cardiac signals aimed at diagnostic monitoring quality. Hence, when better linearity and accuracy are required, alternative techniques need to be developed.

In this paper, a synthesis procedure for developing HP$\Sigma\Delta$ converters suitable for designing the high-pass filtering analog front-end for ECG signal acquisition is proposed. $\Sigma\Delta$ ADCs take advantage of their noise shaping property to achieve low quantization noise and the use of 1-bit digital-to-analog converter ensures inherent linearity. As opposed to conventional low-pass $\Sigma\Delta$ converters, a signal transfer that accommodates a general filter transfer is considered. Intermediate transfer function analysis evaluates the signal handling capabilities and the noise contributions of each of the integrators and thus helps in the overall ranking of the developed HP$\Sigma\Delta$ topologies. Sensitivity of the developed HP$\Sigma\Delta$ topologies to coefficient variations and non-idealities of the integrator is also investigated.

The rest of the paper is organized as follows. In Section II, the methodology to develop HP$\Sigma\Delta$ topologies is proposed. The entire design procedure is demonstrated through design examples and compared qualitatively. In Section III, intermediate functions are derived for quantitative evaluation of the topologies. Further, the sensitivities to coefficient variations and to integrator non-idealities are described and evaluated in Section IV. Circuit design, simulation results and comparison with related prior art are explained in Section V. Finally, the conclusions are summarized in Section VI.

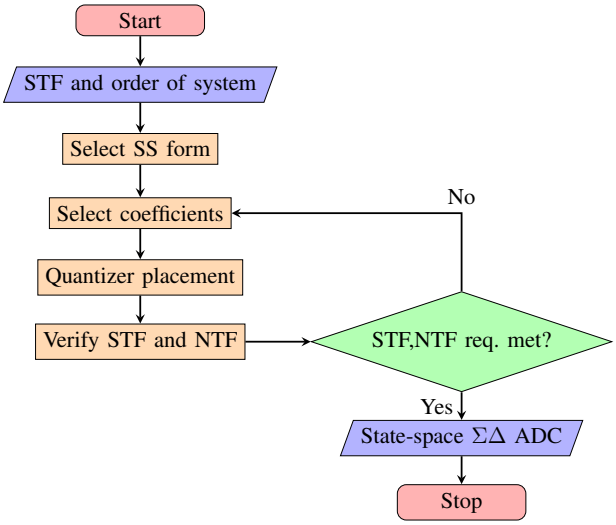


Figure 3: Flowchart of the state-space based approach for $\Sigma\Delta$ topologies [14]

II. Proposed Methodology

System design incorporating digitization and filtering using an orthogonal design methodology allows us to arrive at topologies satisfying the signal and noise transfer function requirements while optimizing the performance metrics relevant to low power and low voltage designs such as dynamic range and sensitivity to coefficient variations. Conventionally, $\Sigma\Delta$ modulator topologies have a low-pass filter signal transfer characteristic. However, in this approach, to accommodate a general signal transfer function including low-pass, high-pass, notch and band-pass filter characteristics, state-space forms can be used to design application-specific $\Sigma\Delta$ modulator topologies. For the target application, viz. acquisition of a cardiac signal whose bandwidth extends from sub-Hz to 200 Hz [5], it is possible to implement the low-pass and the high-pass cut-off frequency separately. The implementation of the low-pass cut-off frequency can be readily merged with the front-end amplifier and will not be discussed in this paper. To implement the high-pass transfer function with good linearity and accuracy, it is embedded in the $\Sigma\Delta$ converter, thus eliminating the need for a dedicated high-pass filter.

For a given state-space form, the coefficients are evaluated for their contributions to the signal and noise transfer function requirements. In this analysis, we have focused only on the inband properties of the modulator. The influence of the sampler on the transfer function in this region is negligible due to the large oversampling ratio (OSR). The placement of the quantizer depends on the requirement of the quantization noise transfer. A single quantizer is considered. Multiple quantizers can also be used and would lead to alternative topologies with different constraints [15], but this is considered beyond the scope of the paper. For the sake of simplicity and clarity, a 3^{rd} order system is considered. A first order high-pass filter is considered sufficient for the application [16]. A higher order high-pass filter would come at an additional power and area

cost. However, the approach can be extended to higher orders as per the application specifications. The requirements of the transfer function for a 3rd order system are:

- Signal transfer function (STF): a high-pass filter characteristic with at least one pole, the location of which can be set independently;
- Noise transfer function (NTF): a high-pass filter characteristic with all real zeros at the origin, leading to a 40 dB/dec slope in the signal band;

Fig. 3 shows the design procedure proposed to develop the desired state-space based high-pass $\Sigma\Delta$ topologies [14]. Based on the resolution and the signal transfer requirements of the target application, the STF type, the order of the system and the state-space form can be chosen. The coefficients of the state-space forms correspond to physical components to be realized in silicon that play an important role in determining the noise, area and power consumption. The quantizer is placed such that the quantization NTF is satisfied. The STF and NTF of the topologies are verified through transfer function calculations. If the requirements of the STF and NTF are not met, the coefficients are re-evaluated until all the requirements are satisfied.

A linear, time-invariant dynamic system can be described using a set of first order differential equations. The general state-space description of an nth order system is given by

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{b}u(t) \\ y(t) &= \mathbf{c^T}\mathbf{x}(t) + du(t) \end{aligned} \tag{1}$$

where $\mathbf{x}(t)$ is an n x 1 vector representing the integrator states or outputs, where n is the number of integrators, ideally equal to the order of the system, $\mathbf{A}$ is an n x n state matrix that describes how the integrators are interconnected through feedback and feedforward paths, $\mathbf{b}$ is an n x 1 vector that describes how the input signal is applied to the integrators, $\mathbf{c}$ is an n x 1 vector that contains the set of coefficients that multiply the output states and are summed together and d is a scalar that represents the feedthrough component from the input directly to the output. $u(t)$ and $y(t)$ are the input and the output signal, respectively. To illustrate the design procedure, biquad, observable canonical and orthonormal based HP$\Sigma\Delta$ ADC topologies are designed that satisfy the NTF and STF requirements, as described in the following paragraphs.

The observable canonical state-space form is investigated first. The observable canonical state-space form is used to develop the observable canonical $\Sigma\Delta$ topology. The output of the system is fed back to the input of each of the integrators through coefficients that determine the poles of the system. The block diagram and the linear model of the observable canonical HP$\Sigma\Delta$ ADC topology are shown in Fig. 4. k_1, k_2 and k_3 are the integrator scaling coefficients of the first, second and the high-pass integrator, repectively. The linear model of the quantizer is modeled as a gain k_q, a quantization error $e(s)$ and a summing node. The value of k_q is given by $2/a_\mathrm{N}$ where a_N is the coefficient of the last integrator, for a single-bit, N^{th}-order modulator as described in [15]. In the proposed design, a_N is given by the scaling coefffient of the second integrator.

The STF and NTF of the observable canonical HP$\Sigma\Delta$ topology can be expressed as

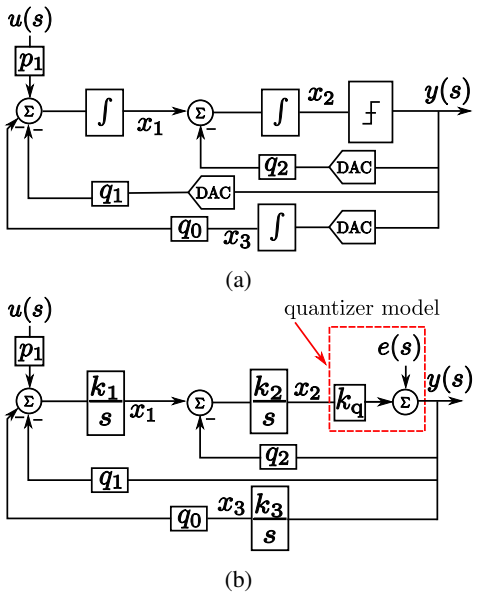


Figure 4: Observable canonical HP$\Sigma\Delta$ topology: (a) Block diagram; (b) Linear model [14]

$$\begin{aligned} STF &= \frac{sp_1k_1k_2k_\mathrm{q}}{s^3 + k_\mathrm{q}k_2q_2s^2 + k_\mathrm{q}k_1k_2q_1s + k_\mathrm{q}k_1k_2k_3q_0} \\ NTF &= \frac{s^3}{s^3 + k_\mathrm{q}k_2q_2s^2 + k_\mathrm{q}k_1k_2q_1s + k_\mathrm{q}k_1k_2k_3q_0} \end{aligned} \tag{2}$$

From (2), it can be seen that the STF and NTF requirements of the observable $\Sigma\Delta$ topology are met. For the STF, there is at least one zero at DC (single-pole roll-off) and the three zeros at DC for the NTF. On solving the characteristic equation (CE) of (2), given by

$$s^3 + k_\mathrm{q}k_2q_2s^2 + k_\mathrm{q}k_1k_2q_1s + k_\mathrm{q}k_1k_2k_3q_0 = 0, \tag{3}$$

the location of the high-pass pole close to DC can be determined. The location of the pole predominantly depends on the value of q_0, q_1 and k_3.

Figures 5a and 5b show the biquad HP$\Sigma\Delta$ ADC and its linear model, respectively. The STF and the quantization NTF of the biquad HP$\Sigma\Delta$ ADC can be written as

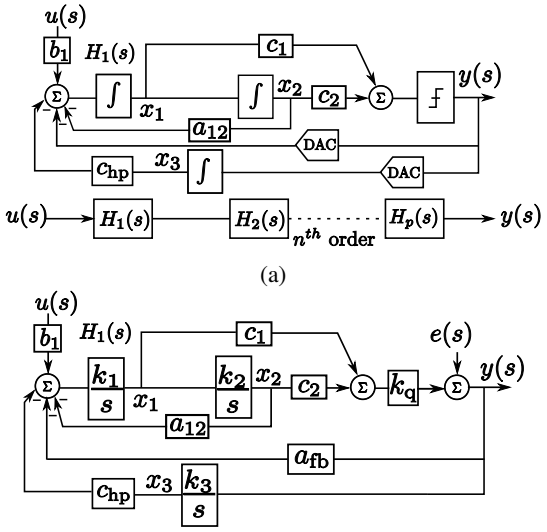
$$\begin{aligned} STF &= \frac{sb_1k_1k_\mathrm{q}(c_1s + k_2c_2)}{s^3 + a_{12}k_1k_2s + k_\mathrm{q}k_1(c_1a_{fb}s^2 + k_2c_2a_\mathrm{fb}s + k_2k_3c_2c_\mathrm{hp})} \\ NTF &= \frac{s(s^2 + a_{12}k_1k_2)}{s^3 + a_{12}k_1k_2s + k_\mathrm{q}k_1(c_1a_\mathrm{fb}s^2 + k_2c_2a_\mathrm{fb}s + k_2k_3c_2c_\mathrm{hp})} \end{aligned} \tag{4}$$

As can be seen from 4, the STF and the NTF satisfy the requirements.

Orthonormal ladder filters [17], a state-space structure that is scaled for optimum dynamic range and less sensitive to component variations, can be used for realizing higher order arbitrary stable transfer functions [18]. Figures 6a, 6b and 6c show the state-space form, the HP$\Sigma\Delta$ topology and the corresponding linear model of the orthonormal HP$\Sigma\Delta$ ADC. The STF and the NTF equations of the orthonormal $\Sigma\Delta$ topology can be written as

Table I: State-space based HPΣΔ topologies: A qualitative comparison

SS topology	Biquad HPΣΔ	Observable canonical HPΣΔ	Orthonormal HPΣΔ
Disadvantage	Biquads in cascade can be used to realize higher order structures but may require modification for stability.	The output is fed back to the input of each of the integrators which imposes tough swing requirements on the integrator.	Existing orthonormal state-space form has to be modified in order to satisfy the STF requirement.
Advantage	Each biquad can be tuned independently while imposing relaxed swing requirements on the integrators.	Only real NTF zeros can be produced while the rest of the topologies offer the freedom to choose between real and complex zeros.	Unique set of coefficients can be derived for any given stable transfer function. The calculation of the coefficients can be automated.



(a)

(b)

Figure 5: Biquad HPΣΔ topology: (a) Block diagram; (b) Linear model

Table II: Coefficients of the HPΣΔ topologies

Coeff.	Orthonormal HPΣΔ	Coeff.	Observable canonical HPΣΔ
b_1	0.5	p_1	0.5
k_1, k_2	0.5	k_1, k_2	0.5
a_{fb}, c_{hp}	1	q_1	0.5
c_1, c_2	0.5	q_2, q_0	1
k_3	0.0005	k_3	0.0005

$$STF = \frac{sb_1k_1k_q(c_1s + k_2c_2)}{s^3 + k_qk_1(c_1a_{fb}s^2 + k_2c_2a_{fb}s + k_2k_3c_2c_{hp})}$$
$$NTF = \frac{s^3}{s^3 + k_qk_1(c_1a_{fb}s^2 + k_2c_2a_{fb}s + k_2k_3c_2c_{hp})} \quad (5)$$

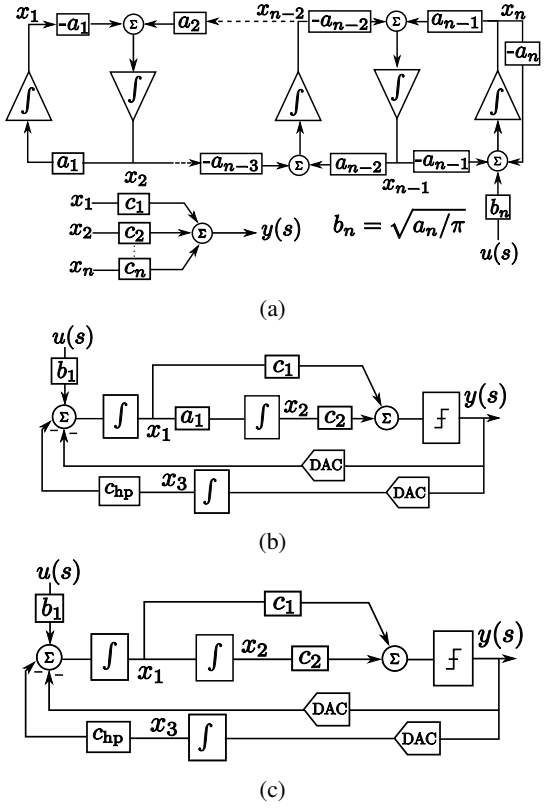
From (5), it can be seen that the STF has one zero at the origin. Also, the NTF has three zeros at the origin. The poles can be determined by solving the characteristic equation given by

$$s^3 + k_qk_1(c_1a_{fb}s^2 + k_2c_2a_{fb}s + k_2k_3c_2c_{hp}) = 0 \quad (6)$$

For frequencies very close to DC, the characteristic equation can be approximated as

$$s \approx -\frac{c_{hp}k_3}{a_{fb}} \Rightarrow f_{hpf} = \frac{1}{2\pi}\frac{c_{hp}k_3}{a_{fb}}f_s \quad (7)$$

and the high-pass pole location can be set. Note that the quantizer gain k_q does not impact the location of the pole. This implies that the signal-dependent gain associated with k_q and thus the momentary value of the input signal of the ADC does not change the exact value of the location of the pole, unlike in the case of pseudo-resistors. The reader is referred to the Appendix for the derivation and the approximations made.



(a)

(b)

(c)

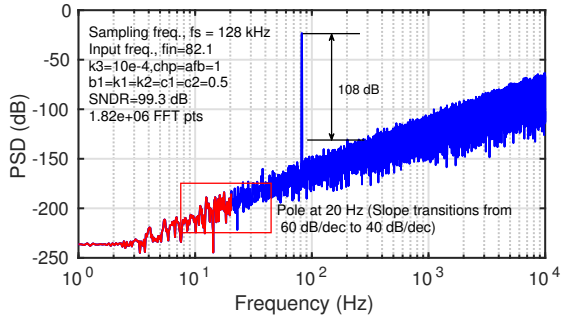
Figure 6: Orthonormal HPΣΔ topology: (a) n^{th}-order state-space form; (b) Block diagram; (c) Linear model [14]

Figures 7a and 7b show the plots of NTF and STF, respectively. Sampling frequency f_s = 128 kHz, scaling coefficient k_3 = 2·0.0005 and a_{fb} = 1 result in an high-pass cut-off frequency f_{hpf} of 20 Hz, selected to observe the slope change clearly. A desired f_{hpf} can be selected by appropriately setting k_3.

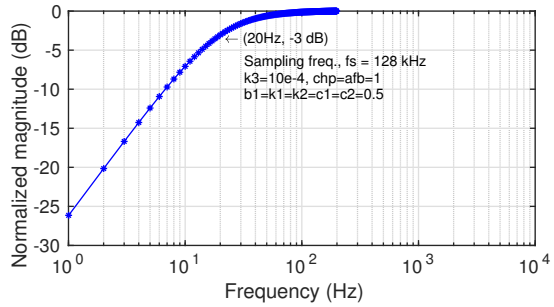
Table I summarizes the advantages and disadvantages posed by the various HPΣΔ topologies. While biquads can be tuned independently, they may be unstable at higher orders and require modifications to stabilize the system. For this reason, we will discuss only the orthonormal and observable canonical HPΣΔ topologies in the sequel.

III. Intermediate functions

In this section, the sets of intermediate transfer functions (IF) [17] are derived to compare the thermal noise contributions of the integrators of the HPΣΔ topologies. Flicker noise



(a)



(b)

Figure 7: System level plots of the orthonormal HPΣΔ topology: (a) NTF, (b) STF [14]

is not considered here since circuit techniques to reduce its effect can be found in the literature and the reader is referred to [19] and [20] for more details. Although both thermal and flicker noise contribute to the total noise of the system, they are minimized through independent circuit techniques. The first set of intermediate functions from the input of the integrators to the output of the system, **g**(s), and the second set, from the input of the system to the output of the integrators, **f**(s), as shown in Fig. 8, can be expressed as

$$f_i(s) \triangleq \frac{x_i(s)}{u(s)}; \qquad g_i(s) \triangleq \frac{y(s)}{n_i(s)}; \tag{8}$$

where $u(s)$ and $y(s)$ denote the input and the output of the system, and $n_i(s)$ and $x_i(s)$ represent the input thermal noise source and output of the i^{th} integrator, respectively.

The IF **f**(s) of the orthonormal HPΣΔ modulator consists of a set of functions $\{f_1(s), f_2(s), f_3(s)\}$ given by:

$$f_1(s) = \frac{b_1 k_1 s^2}{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + + k_2 k_3 c_2 c_{hp})} \tag{9}$$

$$f_2(s) = \frac{b_1 k_1 k_2 s}{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})} \tag{10}$$

$$f_3(s) = \frac{b_1 k_1 k_3 k_q (s c_1 + k_2 c_2)}{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})} \tag{11}$$

The IF **g**(s) of the orthonormal HPΣΔ modulator consists of a set of functions $\{g_1(s), g_2(s), g_3(s)\}$ given by:

$$g_1(s) = \frac{k_1 k_q s (c_1 s + k_2 c_2)}{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})} \tag{12}$$

$$g_2(s) = \frac{k_2 k_q c_2 s^2}{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})} \tag{13}$$

$$g_3(s) = \frac{k_1 k_3 k_q c_{hp} (s c_1 + k_2 c_2)}{s^3 + k_q k_1 (c_1 a_{fb} s^2 + k_2 c_2 a_{fb} s + k_2 k_3 c_2 c_{hp})} \tag{14}$$

The IF **f**(s) of the observable canonical HPΣΔ modulator consists of a set of functions $\{f_1(s), f_2(s), f_3(s)\}$ given by:

$$f_1(s) = \frac{s p_1 k_1 (s + k_2 q_2 k_q)}{s^3 + k_q k_2 q_2 s^2 + k_q k_1 k_2 q_1 s + k_q k_1 k_2 k_3 q_0} \tag{15}$$

$$f_2(s) = \frac{s p_1 k_1 k_2}{s^3 + k_q k_2 q_2 s^2 + k_q k_1 k_2 q_1 s + k_q k_1 k_2 k_3 q_0} \tag{16}$$

$$f_3(s) = \frac{p_1 k_1 k_2 k_3 k_q}{s^3 + k_q k_2 q_2 s^2 + k_q k_1 k_2 q_1 s + k_q k_1 k_2 k_3 q_0} \tag{17}$$

The IFs **g**(s) of the observable canonical HPΣΔ modulator consists of a set of functions $\{g_1(s), g_2(s), g_3(s)\}$ given by:

$$g_1(s) = \frac{k_1 k_2 k_q s}{s^3 + k_q k_2 q_2 s^2 + k_q k_1 k_2 q_1 s + k_q k_1 k_2 k_3 q_0} \tag{18}$$

$$g_2(s) = \frac{k_2 k_q s^2}{s^3 + k_q k_2 q_2 s^2 + k_q k_1 k_2 q_1 s + k_q k_1 k_2 k_3 q_0} \tag{19}$$

$$g_3(s) = \frac{k_1 k_2 k_3 k_q q_0}{s^3 + k_q k_2 q_2 s^2 + k_q k_1 k_2 q_1 s + k_q k_1 k_2 k_3 q_0} \tag{20}$$

From Fig. 9, we can observe that the noise from the first, second and third integrator is first-order high-pass, second-order high-pass and low-pass filtered, respectively. It can be observed that the input signal is high-pass filtered with a slope of 20 dB/dec, while the quantization noise initially begins with a slope of 60 dB/dec but transitions to 40 dB/dec on encountering the pole associated with the high-pass cut-off frequency. The coefficients of both topologies are given in Table II.

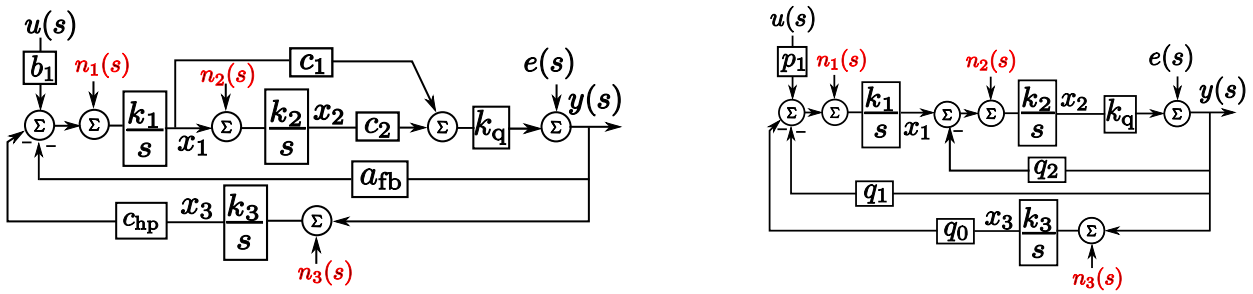
To quantitatively evaluate the performance of the HPΣΔ topologies, a mathematical norm is necessary to measure the magnitudes of the signal level. The two signal types that are often used in such a performance analysis are:

- Sinusoidal input: for a sinusoidal input with a peak amplitude A_p, an appropriate mathematical norm of the signal is the L_∞ norm.
- Power spectrum: if the input signal is assumed to be white, the output power spectrum at the output of the integrators is calculated and the root-mean-square value is given by the L_2 norm of the signal.

In our case, even though this is not exactly the case, as can be seen from Fig. 2, we assume a white input signal L_2-norm value of which is the root mean square of the power spectrum given by

$$\|v\|_2 = \left(\int_0^\infty v(t)^2 dt \right)^{\frac{1}{2}} \tag{21}$$

The dynamic range, given by the ratio of the maximum signal handling capability and the minimum level as determined by the internally generated noise can be optimized through scaling of the integrators. Integrator scaling is the process of readjusting the internal gain coefficients in order to adjust the internal signal swing to a range appropriate for the supply voltage such that the overall transfer function from the input to the output remains unchanged [21]. The L_2-norms of the set



(a) (b)

Figure 8: Integrator input referred thermal noise sources: (a) Orthonormal HPΣΔ; (b) Observable canonical HPΣΔ topology [14]

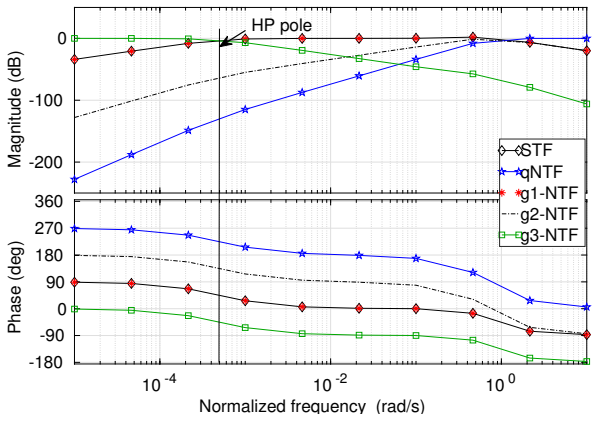


Figure 9: Frequency response of the IF-**g**(s) thermal noise transfer functions of the orthonormal HPΣΔ topology [14]

Table III: L_2-norm calculations of the HPΣΔ topologies

Int.	Before scaling $\|f_i\|_2$	Before scaling $\|g_i\|_2$	Factor α_i	After scaling $\|f_i\|_2$	After scaling $\|g_i\|_2$
Orthonormal HPΣΔ					
First integrator	0.354	0.866	2.8277	1	0.3063
Second integrator	0.25	0.7073	4.001	1	0.1768
High-pass integrator	0.0158	0.0158	63.23	1	0.00025
$\sum_{i=1}^{3} \|g_i(j\omega)\|_2^2$	1.2506			0.12506	
Observable canonical HPΣΔ					
First integrator	0.7501	0.707	1.33	1	0.5304
Second integrator	0.177	1.00	5.66	1	0.1768
High-pass integrator	0.0158	0.0158	63.238	1	0.00025
$\sum_{i=1}^{3} \|g_i(j\omega)\|_2^2$	1.5006			0.31266	

of IF's **f**(s) and **g**(s) are calculated and are tabulated in Table III. A scaling factor, α_i, is calculated for each integrator, given by

$$\alpha_i = \frac{M}{\|f_i\|_2}, \tag{22}$$

where M is the maximum acceptable signal magnitude at the integrator outputs. After **f**(s) has been scaled, **g**(s) is scaled by the inverse factor $(\frac{1}{\alpha_i})$ as given in Table III. The total noise power of the integrators, given by $\sum_i \|g(j\omega)\|_2^2$, can be evaluated and used as a figure of merit [5] for comparing the noise performance of the HPΣΔ topologies. The total noise power for a 3rd order system, given by $\sum_{i=1}^{3} \|g_i(j\omega)\|_2^2$ for the orthonormal HPΣΔ is 0.12, which is smaller than that of the observable HPΣΔ, which is 0.31, which is a significant 3.9 dB difference. Therefore, the orthonormal HPΣΔ is a preferred choice for circuit implementation. The noise performance of the HPΣΔ topologies can be further improved by balancing the integrator noise contributions, i.e., making g_i of the integrators equal. This can be carried out by appropriate capacitance sizing of the integrators, while keeping in mind the practical tradeoffs between noise and current consumption. The noise contributions of individual integrators can be seen in Table III. It can be observed that the total noise contribution of the observable canonical HPΣΔ ADC is about 1.25 times that of the orthonormal HPΣΔ ADC before scaling, while it is three times that after scaling. Therefore, the orthonormal HPΣΔ ADC is a better topology with respect to noise performance.

Following the intermediate function analysis from a linearized model, the topologies are now compared using a nonlinear model of the HPΣΔ topologies, which models the quantizer as a *sign* function on MATLAB. Fig. 10 shows the dynamic range comparison between the observable canonical and orthonormal HPΣΔ topologies. It can be observed that the orthonormal HPΣΔ topology has a larger dynamic range and can handle larger input signal amplitudes.

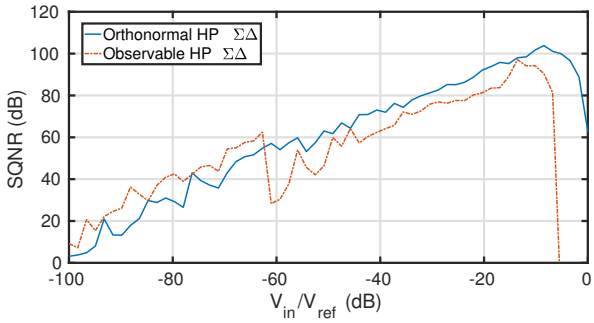


Figure 10: Simulated dynamic range performance of the HPΣΔ topologies

From system simulations, it follows that the difference between the noise performance of these types of modulators becomes more pronounced for higher orders, in favor of the orthonormal HPΣΔ modulator topology.

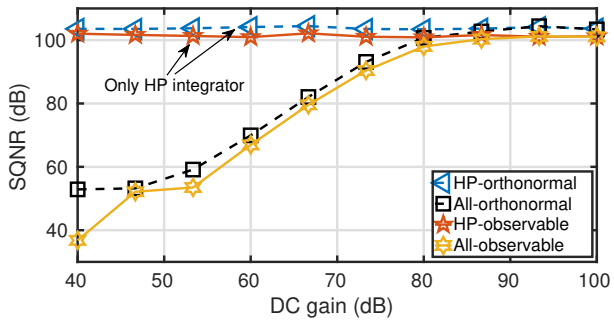


Figure 11: Effect of finite DC gain on the performance of the HPΣΔ topologies

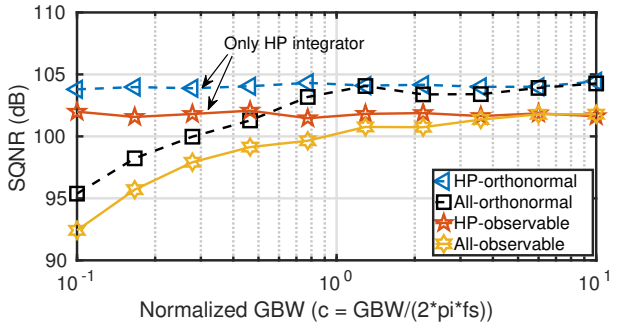


Figure 12: Effect of finite GBW on the performance of the HPΣΔ topologies

IV. Sensitivity

In this section, the sensitivity of the noise transfer function to integrator non-idealities and coefficient variations is discussed. In order to determine the impact of integrator errors on the noise transfer function of the HPΣΔ topologies, the integrator errors are modeled and simulated at the system level. The effects of finite DC gain, finite GBW and time constant variation of the integrators on the performance of the system are investigated. Assuming an RC implementation, the ideal integrator transfer function (ITF) can be expressed as

$$ITF_{RC,i} = \frac{k_i f_s}{s} = \frac{1}{sRC} = \frac{\omega_u}{s} \tag{23}$$

Taking the finite DC gain effect of the integrator into account, the non-ideal integrator transfer function can be expressed as

$$ITF_{A_0} \approx \frac{k_i f_s}{s + \frac{k_i f_s}{A_0}}, \tag{24}$$

where A_0 is the finite DC gain of the integrator. Comparing (24) to the ideal ITF expressed in (23), it is observed that the pole is displaced to $\frac{k_i f_s}{A_0}$.

Fig. 11 shows the impact of finite DC gain of the high-pass integrators and compares the performance between orthonormal and observable canonical HPΣΔ ADC topologies. It can be observed that, on lowering the DC gain of the high-pass integrator alone, the performance of the topologies does not degrade. The overall performance of the topologies mainly depend on the first or the second integrator.

The non-ideal ITF due to finite GBW can be expressed as [15]

$$ITF_{\text{GBW}}(s) = \frac{\frac{k_i f_s}{s}\frac{GBW}{GBW+k_i f_s}}{1 + \frac{s}{GBW+k_i f_s}}, \tag{25}$$

where GBW is the gain-bandwidth product of the integrator.

From Fig. 12, one can observe how the performance of the HPΣΔ topologies depend on the GBW of the integrators. As the GBW product of the high-pass integrator decreases, the performance of the modulator degrades only marginally. At the lower end, the GBW values of the 1st and 2nd integrator are important to maintain the performance of the HPΣΔ topologies. To minimize the effect of finite GBW, a GBW value of $0.7 \cdot f_s$ or higher would suffice.

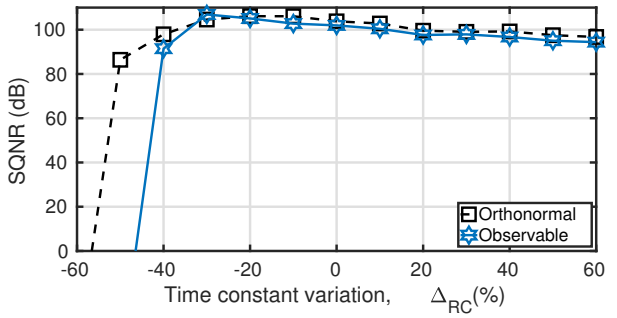


Figure 13: Effect of time constant variation on the performance of the HPΣΔ topologies

RC mismatch can be expressed as

$$ITF_{RC,\Delta_{RC}} = \frac{1}{sRC} \cdot \frac{1}{(1+\Delta_{RC})} = \frac{k_i f_s}{s} \cdot \frac{1}{(1+\Delta_{RC})} \tag{26}$$

When the time constant increases, i.e. the gain of the integrator decreases, the performance of the HPΣΔ topologies degrades. The trend is similar to the effect of finite GBW on the performance. When the time constant decreases, i.e. the gain of the integrator increases, the modulator can become unstable beyond a threshold, as can be seen in Fig. 13. The overall performance of the high-pass modulator mainly depends on the first or the second integrator and not on the feedback integrator.

In case of filters, the sensitivity of the transfer function to the integrator non-idealities is dependent on the integrator time constant [17]. A higher integrator gain would result in larger sensitivity to the integrator non-idealities. Given that the gain of the integrator is proportional to the row sum given by [17]

$$|A_{ij}| + |b_i|, \tag{27}$$

where A_{ij} and b_i are elements of the **A** and **b** matrices respectively, the first and second integrator are expected to be more sensitive to the integrator non-idealities than the high-pass integrator, which confirms the observations made in Figures 11, 12 and 13. The row sum of the high-pass integrator is very low, and therefore, the sensitivity to finite DC gain, finite GBW and time-constant variation is marginal. But the row sums of the first and second integrator are quite large as compared to that of the high-pass integrator and hence they

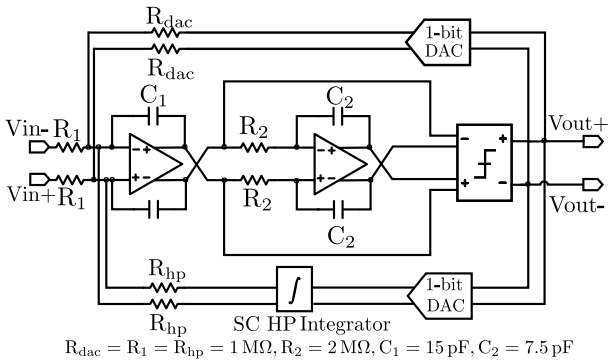


Figure 14: Top level circuit block diagram of the CT orthonormal HPΣΔ modulator [14]

suffer from larger sensitivities to integrator non-idealities. In general, the larger the row sum of the integrator, the larger the sensitivity to its non-idealities.

V. Circuit implementation and simulation results

Illustrated in Fig. 14 is the top level schematic of the proposed orthonormal HPΣΔ topology targeting the implementation of the high-pass cut-off frequency with good accuracy and linearity. Opamp-RC integrators are used to realize the first and second integrators to achieve good linearity. The amplifiers are designed using a two-stage opamp topology for the high current driving capability that is required to drive the large capacitances, minimizing the performance degradation due to slewing. A multiple-input dynamic comparator is used to realize the summer and the quantizer. A very large time-constant, parasitic-insensitive and area-efficient switched-capacitor Nagaraj integrator [22] as shown in Fig. 15 is used to implement the high-pass integrator in the feedback loop. The location of the high-pass pole is determined by ratios of capacitors and by the clock frequency and, as such, offers a high accuracy and is robust to PVT variations. c_{hp} and a_{fb} are implemented as a ratio of resistors while k_3 is implemented as a ratio of capacitors, both of which can be very accurate. The circuit consists of three different capacitors and operates in two non-overlapping phases. The input voltage is attenuated and integrated by capacitor C_{I}. A charge equivalent to $C_{\text{a}}V_{\text{in}}$ is transferred to the large capacitor C_{I} during the first phase. In the second phase, the charge is redistributed between C_{I} and C_{b}. Large capacitance C_{I} is used for both attenuation and integration, thus saving area. The gain and the unity gain frequency, f_u of the integrator are given by the factor $(\frac{C_{\text{a}}}{C_{\text{I}}})(\frac{C_{\text{b}}}{C_{\text{I}}})$ and

$$f_{\text{u}} = \frac{1}{2\pi}\frac{1}{\left[1+\frac{C_{\text{b}}}{C_{\text{I}}}\right]}\frac{C_{\text{a}}}{C_{\text{I}}}\frac{C_{\text{b}}}{C_{\text{I}}}f_{\text{s}}, \tag{28}$$

respectively, where f_{s} is the clock frequency and is equal to the sampling frequency of the ΣΔ modulator.

To avoid long simulation times, f_{hpf} is set at 1 Hz and the circuit is tested for linearity at the same frequency. Lower f_{hpf} can be realized by appropriately selecting the values of capacitances and the clock frequency, at the cost of larger area and power. To obtain a cut-off frequency of 1 Hz, C_{a} = 0.5 pF, C_{I} = 45 pF and C_{b} = 0.2 pF are chosen to realize the scaling coefficient of $5{\cdot}10^{-5}$ that follows from (7) and (28). In the designed modulator, the high-pass cut-off frequency is implemented using ratios of capacitors, which is more accurate and robust to PVT variations as compared to pseudo-resistors or g_m based techniques. The first, the high-pass and the second integrator consume 76.6, 65.4 and 3.7 μW respectively, while the digital blocks consume 0.4 μW. To get an estimate of the noise contributions of the passive components, the thermal noise of the opamps and the quantization noise, a transient noise simulation is run with noise f_{min} and f_{max} being 1 Hz and 200 Hz respectively, after disabling the effect of flicker noise, and is shown in Figure 16a. Assuming that the flicker noise of the opamps can be optimized with available state-of-the-art circuit techniques, the signal energy at the high-pass cut-off frequency region can be acquired with high fidelity. The 3$^{\text{rd}}$ harmonic distortion is at -78 dB for an input signal of 100 mV (peak value) at an input frequency of 1.1 Hz as shown in Figure 16b, which is better than the state-of-the-art performance. Designed and simulated in AMS 0.18 μm CMOS IC technology and taking resistor noise, switched capacitor noise, opamp thermal noise, quantization noise and harmonic distortion into account, the orthonormal HPΣΔ ADC achieves an effective number of bits (ENOB) of 11.02 bits. Table IV summarizes the performance of the designed modulator.

The proposed implementation of the high-pass cut-off frequency is compared with that of a "Harrison amplifier", i.e., the combination of an amplifier and a high-pass filter, as shown in Fig. 15 [6]. Figures 16 and 17 show the performance of the orthonormal HPΣΔ modulator and the Harrison amplifier, respectively. The proposed design is benchmarked against a Harrison amplifier that consists of pseudoresistors designed using PMOS transistors [6] and an ideal amplifier. The high-pass filter is implemented using the pseudoresistors in parallel

Table IV: Performance of the CMOS orthonormal HPΣΔ modulator

Technology	0.18 μm AMS
Supply voltage	1.8 V
Sampling frequency	128 kHz
Signal Bandwidth	1 - 200 Hz
HD_3@f_{in}=1.1 Hz,V_{in} = 100 mVp	-78 dB
SNDR[1]	68.1 dB
ENOB	11.02 bits
Total capacitance	148.4 pF
Total power consumption	146μW

[1] transient thermal noise from noise f_{min} = 1 to f_{max} = 200 Hz; flicker noise disabled

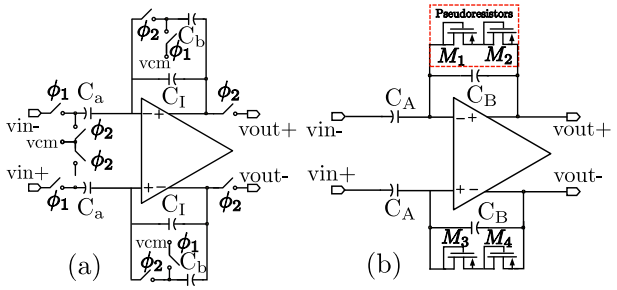
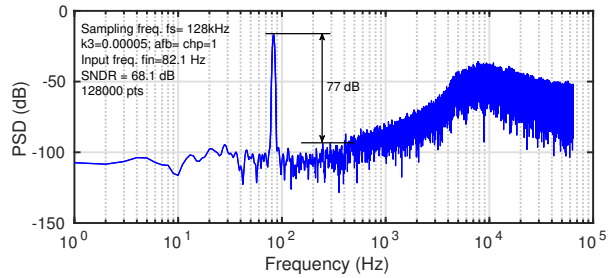
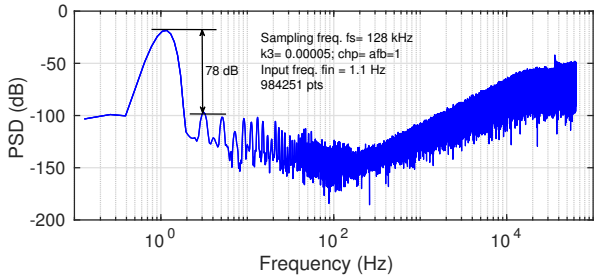


Figure 15: Implementation of the high-pass cut-off frequency a) SC Nagaraj integrator [22] b) Harrison amplifier [6]



(a) Output spectrum for f_{in} = 82.1 Hz



(b) Output spectrum for f_{in} = 1.1 Hz [14]

Figure 16: Orthonormal HPΣΔ circuit simulations

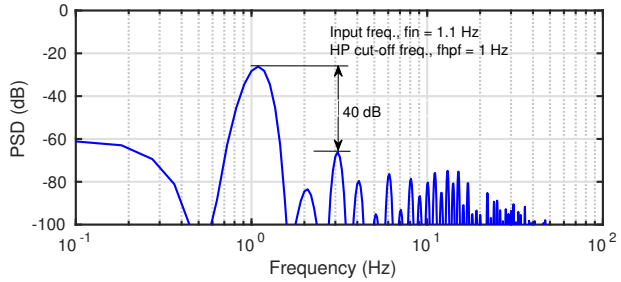
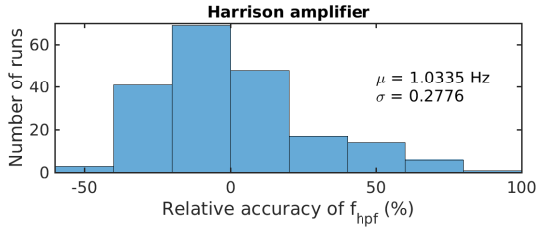
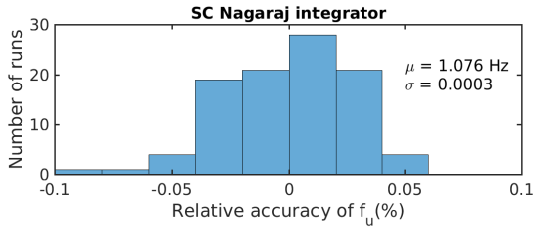


Figure 17: Output spectrum of Harrison amplifier for f_{in}= 1.1 Hz



(a)



(b)

Figure 18: Histogram of the relative accuracies of the high-pass cut-off frequency: (a) Harrison amplifier, (b) SC Nagaraj integrator

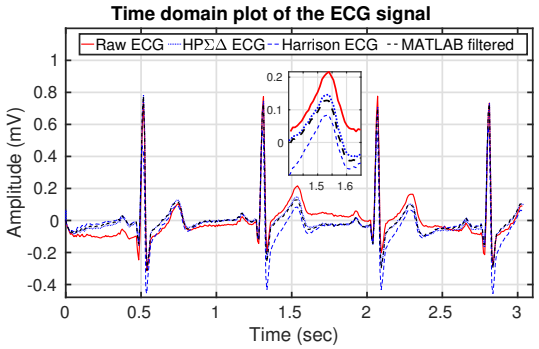


Figure 19: Time-domain ECG signal from the orthonormal HPΣΔ modulator output compared with raw ECG (MIT-BIH), Harrison amplifier and MATLAB filtered output

with the feedback capacitors C_B. The linearity at the high-pass cut-off frequency of the Harrison amplifier is tested and is shown in Fig. 17. The amplifier achieves an HD_3 of about -40 dB for an input amplitude of 10 mV at an input frequency of 1.1 Hz. The relative accuracy of unity gain frequency of the SC integrator is better than 0.1%. Together with the inaccuracies resulting from the ratio of resistances, the accuracy of the proposed method can be better than 1%. Monte Carlo simulations, accounting for process and mismatch variations, comparing the accuracies of the high-pass cut-off frequency set by the SC Nagaraj integrator and the Harrison amplifier, are shown in Figure 18.

A. Testing with pre-recorded ECG signal

The orthonormal HPΣΔ modulator is tested with a pre-recorded ECG signal from the MIT-BIH Normal Sinus Rythym database (nsrdb) numbered as Record 16773 (Signal: ECG1). The designed system is run with 3 seconds of the ECG input signal to observe the effect of baseline wandering and the output is post-processed in MATLAB. The acquired digital signal output is low-pass filtered using a third-order Butter-worth filter and is reconstructed in the analog time domain. Fig. 19 shows the pre-recorded time-domain ECG input signal, the reconstructed signal from the output of the orthonormal HPΣΔ modulator and the signal from the output of the Harrison amplifier, which are benchmarked against a MATLAB high-pass filtered signal of the raw ECG with BW. The distortion components present in the ECG signal acquired using pseudoresistors (with an ideal amplifier having no swing limitations) can be clearly seen in the time-domain. Distortion around the high-pass cut-off frequency of ECG signal can make accurate medical diagnosis a challenge. However, the waveform acquired by the orthonormal HPΣΔ modulator has much better linearity and is closer to the MATLAB filtered waveform. Given that the signal is normal sinus rhythm and assuming that the strength of the beat is fairly uniform, the R-R interval is about 0.8 sec and the amplitude of the P-wave peak of the input ECG signal ranges from -0.054 to 0.058 mV, whereas, the reconstructed ECG peaks vary from 0 to 0.048 mV, which is a much smaller range. The occurrence of the P-wave peak for the input ECG with baseline wander and the reconstructed ECG are tabulated in Table VI. It can be observed that the effect of baseline wandering is greatly reduced in the reconstructed signal.

Table V: Comparison of the implementation of high-pass cut-off frequency (f_{hpf}) with related work

	This work	**[Mohan]**	**[Harrison]**	**[Muller]**	**[Rezaee]**
Year	2017	ISCAS 2013 [9]	JSSC 2003 [6]	JSSC 2012 [10]	JETCAS 2011 [7]
Architecture	2^{nd} HP$\Sigma\Delta$	1^{st} HP$\Sigma\Delta$	amplifier	boxcar ADC	amplifier
Domain	mixed-signal	mixed-signal	analog	digital	analog
Bio-signal	ECG	ECG	neural	neural	neural
HPF technique	SC Nagaraj integrator	g_{m}, current sources	pseudoresistors	IIR-filter (off-chip)	pseudoresistors
Bandwidth [Hz]	1-200	1-200	0.025-7.2k	300-10k	0.5-10k
HD$_3$ [dB]	-78 @$f_{in} = 1.1$ Hz	-62 @$f_{in} = 2.1$ Hz	>-40 @$f_{in} = 1.1$ Hz	-	>-40 @$f_{in} = 1.1$ Hz
Accuracy of f_{hpf}	high	process sensitive	process sensitive	very high	process sensitive
Technology	0.18 μm	0.18 μm	1.5 μm	65 nm	0.18 μm

Table VI: Reduction of baseline wandering

ECG P-wave	1^{st} **(s, mV)**	2^{nd} **(s, mV)**	3^{rd} **(s, mV)**	4^{th} **(s, mV)**
Raw ECG	(0.37, -0.054)	(1.17, 0.024)	(1.93, 0.058)	(2.65, -0.015)
Rec. ECG	(0.38, 0.015)	(1.17, 0.048)	(1.93, 0.012)	(2.66, 0)

B. Comparison with related work

Comparing the performance of the orthonormal HP$\Sigma\Delta$ modulator to the Harrison amplifier, it can be seen that the orthonormal HP$\Sigma\Delta$ topology offers a much better alternative for the implementation of the high-pass cut-off frequency, in terms of linearity and accuracy. Pseudoresistors are used in [6] and [7] for lower area and power consumption at the expense of poor linearity and accuracy of the high-pass cut-off frequency. Due to process (P), voltage (V), and temperature (T) variations and poor circuit structures, pseudoresistors achieve a linearity of about -40 dB and compromise on the accuracy of the implementation of the high-pass cut-off frequency. Although the use of a g_{m} stage in combination with current sources [9] leads to a power efficient solution, the g_{m} of any transistor is inherently non-linear and is less robust to P, V and T variations. Off-chip digital solutions [10] can be used to obtain a highly accurate and linear high-pass cut-off frequency at the expense of power. Table V summarizes the metrics that characterizes the implementation of a high-pass cut-off frequency involving large time constants. For integrated on-chip solutions, the proposed system is among the most promising approaches for applications where good linearity and accuracy of the high-pass cut-off frequency is desired.

VI. Conclusion

In this paper, a state-space based design methodology is proposed to develop HP$\Sigma\Delta$ ADC topologies. By using the state-space synthesis approach, $\Sigma\Delta$ converters with arbitrary signal and quantization noise transfer functions can be synthesized. State-space techniques allow dynamic range optimization of the $\Sigma\Delta$ converters with respect to signal swing and noise through state and noise scaling, respectively. This also minimizes the sensitivity of the topology to component variations [23]. From the intermediate-function analysis, it is seen that the noise from the high-pass integrator are low-pass filtered. Also, from the L_2-norm calculations, it is observed that the orthonormal HP$\Sigma\Delta$ ADC gives better noise performance than the observable HP$\Sigma\Delta$ ADC. Sensitivity analysis is carried out to investigate the impact of coefficient variations and non-idealities of the integrator. Finally, schematic simulations of a circuit designed in AMS 0.18 μm CMOS IC technology verify the findings and match the system level results. The designed orthonormal HP$\Sigma\Delta$ is also tested with a real pre-recorded ECG input signal and successfully reduces baseline wandering.

Appendix

For the orthonormal HP$\Sigma\Delta$ topology (of Fig. 6c), the equations can be written as:

$$\left[u(s)b_1 - a_{\text{fb}}y(s) - c_{\text{hp}}x_3(s)\right]\frac{k_1}{s} = x_1(s), \tag{29}$$

$$x_1(s)\frac{k_2}{s} = x_2(s), \tag{30}$$

$$\frac{k_3}{s}y(s) = x_3(s), \tag{31}$$

and

$$\left[x_1(s)c_1 + x_2(s)c_2\right]k_{\text{q}} + e(s) = y(s), \tag{32}$$

where $u(s)$ and $y(s)$ are the input and the output of the system, respectively, and $x_1(s)$, $x_2(s)$ and $x_3(s)$ are the integrator outputs of the first, second and the high-pass integrator, respectively. After solving the algebraic equations, we obtain the signal transfer function and the quantization noise transfer function given by

$$STF = \frac{k_1b_1s(c_1s + k_2c_2)k_{\text{q}}}{s^3 + k_{\text{q}}k_1(s^2c_1a_{fb} + s(k_2c_2a_{\text{fb}} + k_3c_{\text{hp}}c_1) + k_2k_3c_2c_{\text{hp}})}, \tag{33}$$

and

$$NTF = \frac{s^3}{s^3 + k_{\text{q}}k_1(s^2c_1a_{\text{fb}} + s(k_2c_2a_{\text{fb}} + k_3c_{\text{hp}}c_1) + k_2k_3c_2c_{\text{hp}})} \tag{34}$$

respectively. The poles can be determined by solving the characteristic equation given by

$$s^3 + k_{\text{q}}k_1\left[s^2c_1a_{\text{fb}} + s(k_2c_2a_{\text{fb}} + k_3c_{\text{hp}}c_1) + k_2k_3c_2c_{\text{hp}}\right] = 0 \tag{35}$$

Solving a cubic equation is non-trivial and to calculate the pole located very close to DC, 35 can be approximated to a 2^{nd} order equation and can be written as

$$k_{\text{q}}k_1\left[s^2c_1a_{\text{fb}} + s(k_2c_2a_{\text{fb}} + k_3c_{\text{hp}}c_1) + k_2k_3c_2c_{\text{hp}}\right] = 0 \tag{36}$$

or a 1^{st} order equation given by

$$k_{\text{q}}k_1\left[s(k_2c_2a_{\text{fb}} + k_3c_{\text{hp}}c_1) + k_2k_3c_2c_{\text{hp}}\right] = 0 \tag{37}$$

Assuming that k_3 is very small, the associated term can be made zero. 37 can be written as

$$s \approx -\frac{c_{\text{hp}}k_3}{a_{\text{fb}}}, \tag{38}$$

which defines the location of the high-pass pole.

ACKNOWLEDGMENT

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