Integrated CMOS Current Sensing Systems for Coulomb Counters

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Integrated CMOS Current Sensing Systems for Coulomb Counters

Integrated CMOS Current Sensing Systems for Coulomb Counters

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Front & Back: Block diagram of the current sensor implemented in this work & Infrared photo of the current sensor measuring 5-A DC current.

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To Samira

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Introduction

Not everything that can be counted counts,
and not everything that counts can be counted.

Albert Einstein

Over the past five decades, microelectronics has dramatically changed our lives. In particular, battery-powered portable devices such as computer laptops, smart phones, and tablets have become increasingly integrated into our daily routines. These devices, steadily becoming cheaper, smaller and more powerful, have an amazingly wide range of features, computational power, internet connectivity, GPS, and sensors.

The driving forces behind these remarkable feats of system integration are twofold: 1) technology miniaturization or "More Moore", and 2) technology diversification or "More-than-Moore". In accordance with Moore's law, the number of transistors on a single die has approximately doubled every two years since the early 70's, which in turn has enabled higher memory capacity and faster microprocessors, both at a lower price. Another development is the so-called "More-than-Moore" trend towards incorporating new functionalities such as radio frequency (RF) devices, sensors and actuators, biochips, microelectro-mechanical systems (MEMS), etc., in the microelectronic system.

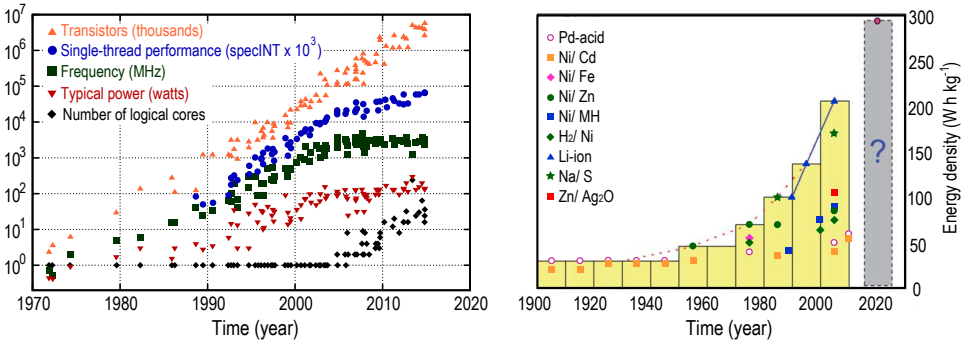

Figure 1.1: Historical trend of (a) microprocessor performance (courtesy of [4]) and, (b) energy density of rechargeable batteries (courtesy of [1]).

Battery technology, however, has not been able to match the pace of IC technology (see Figure 1.1). Over the past 40 years, the energy density of rechargeable batteries has only improved by approximately 5× [1], whereas microprocessor power consumption has increased more, due to higher transistor densities, faster clock frequencies and larger leakage currents in nanoscale CMOS [2–4]. In addition, the introduction of new system capabilities is usually accompanied by higher power consumption. Battery capacity, therefore, has become a limiting factor in the size, computational power, and functionality of battery-powered devices. To deal with this issue, besides optimizing the system's energy/power consumption, a battery management system (BMS), which enables proper and efficient battery use and helps to extend its lifetime, is required [5].

One very critical task of a BMS is to keep track of the battery State-of-Charge (SoC). This is the amount of charge that the battery can supply, and is a vital piece of information for the charging system and the user [6]. An accurate SoC indicator enables efficient charging of the battery by the charger and helps to prevent undesired user experiences, e.g., unexpected system shut-down.

1.1. Coulomb Counting

Coulomb counting is a widely used method to estimate battery SoC. In principle, it involves measuring and integrating the battery's current I_{bat} to determine its net charge flow [7, 8]. Battery behavior, however, is quite complex, and so battery SoC is influenced by many factors, the most important of which are mentioned below [6, 7]:

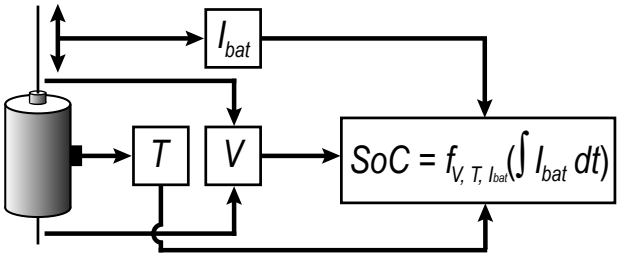

Figure 1.2: Basic principle of a battery SoC indication system based on book-keeping [6].

- **Charging efficiency:** Mainly depending on the SoC, I_{bat} and temperature T, only part of the energy/charge delivered to the battery is stored. For instance, charging efficiency typically drops at high temperatures and/or high charging current.
- **Discharging efficiency:** Mainly depending on the SoC, I_{bat} and T, only part of the charge stored in the battery can be retrieved. For example at low temperatures and/or a high discharge current, an increase in battery internal impedance means that the amount of energy that can be supplied is less than the amount stored.
- **Self-discharge:** Mainly depending on the SoC and T, any battery gradually loses its charge due to internal chemical reactions. Self-discharge cannot be measured by the Coulomb counter since it does not result in an external current.
- **Aging:** Battery aging leads to capacity loss and influences the self-discharge rate and charging/discharging efficiency. Ageing strongly depends on the circumstances under which the battery operates.
- **Storage effect:** Depending on storage time and temperature, some batteries exhibit a temporal and reversible loss in capacity.

In order to take into account the effect of these factors on the SoC, battery voltage V and temperature T are also measured and, together with I_{bat}, fed into an estimation (digital) algorithm. Figure 1.2 shows the basic principle of a book-keeping system, in which the SoC is estimated by a temperature-, voltage- and current-dependent function $f_{V,T,I_{\text{bat}}}(\cdot)$ of the battery's measured charge Q_{bat} $(=\int I_{\text{bat}}\ dt)$. By using an adaptive algorithm based on a mathematical battery model, the function $f_{V,T,I_{\text{bat}}}(\cdot)$ can be continuously corrected to account for the battery's complicated

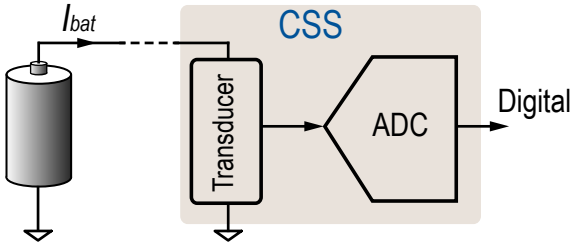

Figure 1.3: Current sensing system (CSS) in the context of a Coulomb counter.

behavior. Some exemplary algorithms used for this purpose are the Kalman filter [9], the extended Kalman filter (EKF) [10], and an EKF combined with neural networks [11].

1.2. Current Sensor Requirements For A Coulomb Counter

A current sensor is a key building block of a Coulomb counting system. Figure 1.3 shows a generic view of a current-sensing system CSS with digital output. It consists of a transducer that converts current into the electrical domain, followed by an analog-to-digital converter (ADC). The overall accuracy of a Coulomb counter-based battery fuel gauge is primarily determined by the accuracy of the CSS [6]. Even a small offset in current measurement can accumulate over an extended period of time and result in a prohibitively large error in the SoC estimation. This is more pronounced in scenarios in which the battery is partially charged/discharged and hence the estimated SoC cannot be reset, e.g., by means of an "end-of-charge" signal generated by the charging system when the battery is full, or by means of an "empty" signal when the battery voltage drops below a certain level [6, 8].

The main error sources of a CSS are offset and gain error. Offset should be well below the battery's self-discharge rate. A conservative self-discharge rate of 1%/month [12] and a typical battery capacity of 5000 mAh in a hand-held device translates into an offset of about 50 μA. In addition, the CSS's current consumption should be well below the battery's self-discharge rate (50 μA). A gain error of less than $\pm 0.5\%$ for currents up to a few Amperes (± 5 A in this work) and over the industrial temperature range ($-40°$C to $+85°$C) is required for an accurate estimation of battery SoC [D. Draxelmayr, J. L. Ceballos, *personal communication*, June 2011]. Although Coulomb counting is robust to current-sensing noise because I_{bat}

is integrated over an extended period of time, the need to monitor battery current in many applications requires a resolution of better than 14 bits (0.01%) in a short conversion time T_{conv}, e.g., 25 ms. This facilitates rapid calibration, as well as the use of the aforementioned digital algorithms to improve the accuracy of the SoC estimation [6, 8]. These requirements are listed in Table 1.1.

Table 1.1: Current sensor requirements.

Current range	± 5 A
Gain error	$< \pm 0.5\%$
Offset	< 50 μA
Current consumption	< 50 μA
Resolution ($T_{\text{conv}} = 25$ ms)	14 bits (0.01%)
Temperature range	-40°C to $+85$°C

It should also be mentioned that an integrated and CMOS-compatible CSS with digital output enables the realization of a small and cost-effective fuel gauge system.

As will be explained in the remainder of this chapter, satisfying the aforementioned requirements has proven to be quite challenging. To the best of the author's knowledge, no CSS available in the market or in the literature comes even close to meeting these specifications. The objective of this thesis is therefore to design a CSS that does meet them. Before describing this objective in more detail, however, we will first review different types of current-sensing techniques and study their feasibility for use in Coulomb counting systems.

1.3. Current-Sensing Techniques

In this section, the suitability of different types of current sensors for the Coulomb counter is briefly evaluated. The discussion is mainly based on the requirements stated in Section 1.2 and is meant as a summary, rather than as an in-depth review. The reader is referred to several review papers, e.g., [13, 14], for more information.

Based on their operating principles, current sensors can be divided into two categories: 1) shunt-based current sensors, and 2) magnetic field sensors.

1.3.1. Shunt-Based Current Sensors

The simplest way to sense current is to measure the voltage drop across a shunt resistor. This method can be used to sense both DC and AC (up to several megahertz) currents, and offers a small and low-cost solution for battery current sensing,

which is, in principle, compatible with standard CMOS processes [13–21].

Inserting a shunt resistor into the current path, however, inevitably introduces extra resistance between the battery and its load, and so involves power loss. To minimize this undesired effect, the value of R_{shunt} is typically chosen to be of the same order of magnitude as the wiring resistance, which, depending on the application, ranges from sub-mΩ values in [13, 15] to a few [16–19] or even tens of mΩ in [20, 21]. For accurate current measurement, four-wire sensing is often used to separate the voltage drop across the dedicated shunt from that across the trace resistance. The lack of electrical isolation inherent to this technique is acceptable for battery current sensing in hand-held devices [13].

CSSs based on *external* shunt resistors can achieve gain errors better than $\pm 0.1\%$ [22, 23]; however, the extra cost and size of this approach is not acceptable for a battery fuel gauge system. Alternatively, a small and low-cost CSS can be implemented by employing *integrated* shunt resistors.

As of 2011 (when this research began), sensors based on integrated shunt resistors only achieved gain errors of $>\pm 3\%$ and current offsets of several milliamperes [16, 17, 20, 21], and hence did not meet our target requirements. This large gain error can be mainly attributed to the large temperature coefficient of resistance (TCR) of the shunt and/or to poor temperature compensation schemes, while their offset is limited by the readout electronics.

To tackle this issue, a recent current sensor employs an in-package shunt made from an alloy with a low TCR ($< 25\text{ppm}/^\circ\text{C}$) [18]. Nevertheless, even with the help of this expensive approach, it only achieves an offset of 50 mA and a gain error of $\pm 0.75\%$ over a ± 10 A current range. An improved version of this product, released in 2016, achieved a gain error of $\pm 0.5\%$ and an offset of 5 mA over the same current range [19]. Another design [15], also released in 2016, uses proprietary techniques to compensate for the shunt TCR, achieving an offset of 9 mA and a gain error of $\pm 1\%$ over a ± 30 A current range.

1.3.2. Magnetic Field Sensors

Current sensors based on magnetic field sensing provide electrical isolation and are widely used in high-current and high-voltage applications. Sensors based on the Faraday's law of induction, Hall effect, magneto-resistance (MR) effect, and fluxgate are the four most commonly used sensors in this class.

Faraday's law states that the electromotive force in any closed loop is proportional to the rate of change of magnetic flux through the loop. Since any current

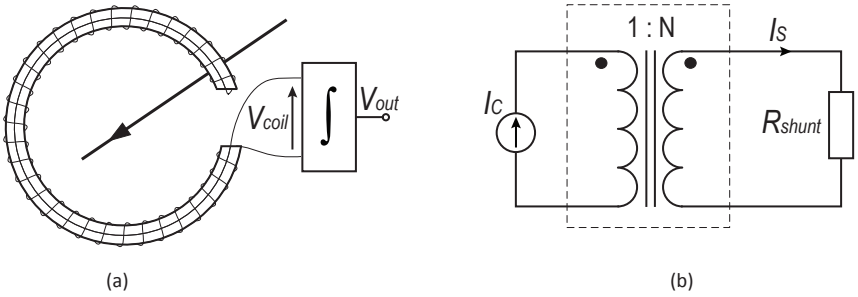

Figure 1.4: Simplified diagram of (a) a Rogowski coil, and (b) a current transformer.

produces a proportional magnetic flux around its conducting wire, this law makes it possible to sense the derivative of current versus time in a galvanically-isolated manner. The two most commonly used sensors of this type are the Rogowski coil and the current transformer (Figure 1.4).

A Rogowski coil is basically an air-cored coil that is uniformly wound around the conducting wire. Its output voltage, after integration, is proportional to the target current. However, since a practical integrator has finite DC gain, offset and flicker noise, and also because the initial value of the current is usually not known, this sensor is not suitable for small (<1 mA) or DC current measurements. They can serve as a high-frequency path in hybrid multipath magnetic sensors and be co-integrated with, e.g., hall effect sensors, in standard CMOS processes [24, 25]. Because of the temperature dependency of the coil permeability and of the readout electronics, however, they show a large gain error of >5% [13, 25]. These coils are widely used in power distribution systems as they offer galvanic isolation and can be used to measure up to megaamperes of current [13, 14].

A current transformer (CT) consists of a single primary turn and multiple (N) secondary turns around a core made out of a high permeable material. The AC magnetic flux in the core, generated by the target current I_c in the primary turn, induces a current $I_s{=}I_c/N$ in the secondary turn, which, for instance, can then be detected by a shunt. However, like Rogowski coils, CTs are not suitable for small (<1 mA) or DC current sensing. An integrated CT with a shunt resistor, reported in [26], exhibited non-linearity of $>\pm 1.5\%$ and current offset of 400 mA over a current range of 0.1 A to 100 A and at room temperature. They are widely used in power conversion applications and power distribution networks [13, 14].

Due to the Hall effect, a magnetic field perpendicular to the direction of electric current flowing through a conductor produces a voltage difference in the conductor

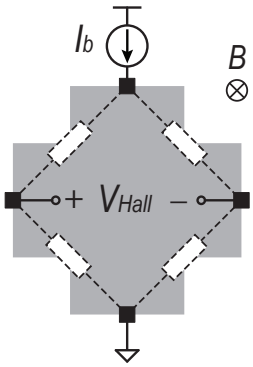

Figure 1.5: Simplified diagram of Hall effect sensors.

transverse to the current. Being compatible with standard CMOS processes [24, 27–29], Hall effect sensors are widely used as integrated magnetic sensors in power conversion systems and motor drives [13, 14, 28].

As shown in Figure 1.5, Hall effect sensors are typically implemented as an n-well plate with four contacts, which can be modelled as a Wheatstone bridge [28]. The perpendicular magnetic field B, emanating from the target current, induces a Hall voltage V_{Hall} at the output of the bridge biased at current I_{b}. This voltage is proportional to both B and I_{b} and has a typical sensitivity of 100 to 400V/AT [28]. The inhomogeneity in the n-well's doping profile, and tolerances in the geometry of the n-well and in the positions of the contacts, lead to bridge imbalance, which, in turn, give rise to an output offset voltage. This offset can be significantly mitigated by using the spinning current technique, which involves periodically changing the direction of I_{b} and averaging the resulting output voltage [27, 28]. Due to their limited sensitivity, however, Hall sensors are not suitable for sensing small (sub-milliampere) currents. In addition, any spread in the spacing between the magnetic sensors and the current-carrying conductor results in a spread in the sensor's sensitivity. This introduces additional challenges in magnetic sensors packaging and mounting. State-of-the-art designs achieve an offset of more than 10 mA [29]. After temperature compensation, their gain errors range from 0.5% to 5% [13, 25].

Current sensors based on fluxgate sensors can be quite accurate (0.001% to 0.5%) and are able to sense currents ranging from the milliampere to kiloampere level [13]. Their operation is based on the nonlinear relation between the magnetic field and magnetic flux density in ferromagnetic materials. As shown in Figure 1.6, such sensors consist of two ferromagnetic cores, each of which is surrounded by an *excitation*

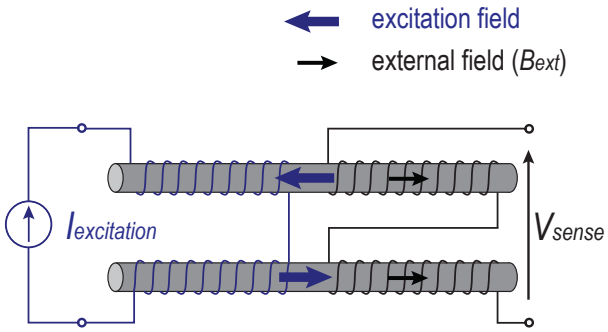

Figure 1.6: Simplified diagram of fluxgate sensors.

and a *sense* coil. The cores are periodically driven into magnetic saturation by applying short (typically several nanoseconds) current pulses to the excitation coil. As the excitation fields in the two cores oppose each other, the absence of an external magnetic field B_{ext} results in a nominally zero sense voltage V_{sense}=0. However, the presence of B_{ext} will cause one core to be driven into saturation earlier than the other, thereby generating a proportional voltage spike on V_{sense}. Due to their use of ferromagnetic materials, however, fluxgate sensors require special backend processing [30, 31]. In addition, large excitation currents are needed to saturate their cores, thus they typically dissipate several tens of milliwatts [30–32]. In [30], an integrated fluxgate sensor achieved an offset of 35 mA and a non-linearity of ±0.1% over a ±5 A range while consuming 56 mA from a 5 V supply.

Magneto-resistive (MR) sensors are based on the fact that the electrical resistance of ferromagnetic materials varies with the magnitude and direction of the applied magnetic field. This type of sensor has been widely used in the read heads of hard disk drives. Anisotropic Magneto Resistance (AMR) and Giant Magneto Resistance (GMR) sensors are the two mostly commonly used MR devices, and can sense currents ranging from milliamperes to kiloamperes [13, 14]. However, they are incompatible with standard CMOS processes as they require ferromagnetic materials.

Besides the above-mentioned drawbacks, any spread in the spacing between a magnetic sensor and the current-carrying conductor leads in a spread in the resulting current sensor's sensitivity. This introduces an additional challenge to the packaging and PCB placement of magnetic sensors. In some cases, a current carrying trace is integrated in the same package as the sensor [29].

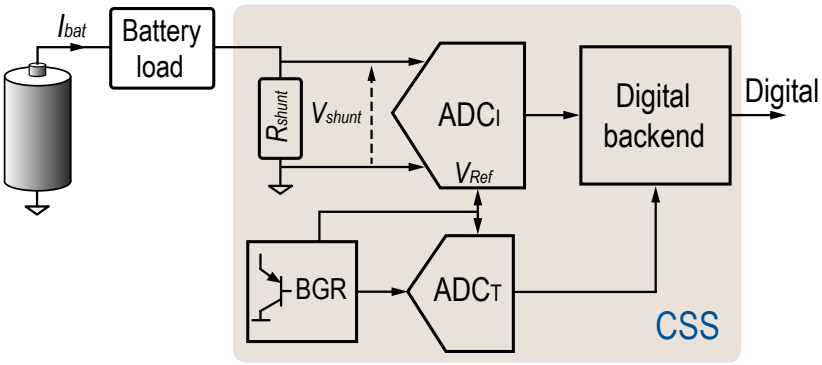

Figure 1.7: Block diagram of the shunt-based CSS implemented in this work.

1.4. Thesis Objective

As discussed in the previous section, magnetic field sensors are not suitable for use in Coulomb counters, because they are power hungry, require post-processing, exhibit limited sensitivity for small current measurement, and their accuracy is impaired by packaging and misalignment. In addition, Rogowski coils and current transformers are not able to measure small or DC currents and are too bulky for use in portable devices.

A shunt-based current sensor, on the other hand, seems to be a promising candidate for use in Coulomb counting systems. Sensors based on external shunt resistors are costly and bulky [22, 23] and hence are not considered for use in this work. Existing sensors based on *integrated* shunt resistors exhibit gain errors of $>\pm 3\%$ and current offset of several milliamperes [16, 17, 20, 21], and hence do not meet the requirements mentioned in Section 1.2. Their large gain error is mainly due to a non-zero shunt TCR and/or poor temperature compensation, while their offset is limited by the readout electronics.

The objective of this thesis is therefore to realize an *integrated shunt-based*, *precision* and *low-cost* CSS for use in the Coulomb counter of portable devices. The block diagram of the CSS designed in this thesis is shown in Figure 1.7. It consists of an integrated shunt resistor and a precision voltage-sensing ADC_I to digitize the voltage drop across the shunt. In order to compensate for the shunt TCR, the system incorporates an on-chip temperature sensor which digitizes the shunt temperature. A single bandgap reference (BGR) both provides the ADCs' reference voltage and also senses the temperature of the shunt. The required calibration and temperature compensation scheme are performed in a digital backend.

1.5. Thesis Organization

The rest of the dissertation is organized as follows. Chapter 2 deals with the shunt resistor, as it plays a key role in determining the overall performance of the CSS. This chapter begins by listing typical shunt resistor non-idealities and limitations, and then studies different ways in which they can be implemented. Finally, two types of integrated resistors will be proposed for use in this work: 1) an on-chip metal resistor, and 2) a resistor made from the lead-frame of an IC package.

Chapter 3 gives a detailed description of the two proposed shunt resistors. The thermal coupling between the shunt and the temperature sensor, which is essential for an accurate shunt temperature compensation, will also be investigated by means of electro-thermal simulation.

Chapter 4 discusses the system-level design of the readout electronics, the ADCs and the BGR. Significant error sources of these building blocks, together with the solutions proposed by the prior art, will be described. In contrast to the prior art, we propose a much simpler solution which essentially only calibrates the non-idealities of the shunt. We show that this solution reduces the effect of many readout electronics' errors to a negligible level without *implicitly* correcting for them.

Three prototype CSSs together with their measurement results are then described. The first one (CSS_1), covered in Chapter 5 and used as a proof-of-concept for ± 5 A current sensing, consists of a 10 mΩ on-chip metal shunt, an ADC and a BGR. This prototype employs a single ADC for both current- and temperature-sensing in a time-multiplexed manner. it exhibits a maximum offset of 16 μA and a maximum gain error of $\pm 0.3\%$ [33], [34]. This level of accuracy is clearly in line with the objective of this thesis, and is achieved by means of an accurate shunt temperature compensation scheme, multiple dynamic error correction techniques, and a simple calibration scheme.

Chapter 6 presents two designs with reduced die area and power consumption, but with improved performance compared to CSS_1. In order to accurately track fast temperature transients in the shunt, two separate ADCs for current- and temperature-sensing were employed. The first design, CSS_2 was based on a 10 mΩ on-chip shunt and is designed for ± 5 A current sensing. In order to eliminate the large die area needed for the on-chip shunt ($> 50\%$ of the total area), another design, CSS_3 employed the 260 $\mu\Omega$ lead-frame resistance of a HVQFN32 plastic package [35, 36]. Although this results in rather small shunt voltages for the target 5 A CSS (leading to excess offset and noise), it demonstrated the feasibility of lead-frame shunts for high current-sensing applications, e.g., automotive. This was

succesfully demonstrated over a ±36 A current range.

Finally, Chapter 7 concludes the thesis, summarizes its original contributions and comments on future work.

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2

Shunt Resistors

As concluded in the previous chapter, the objective of this work is to implement a precision current sensing system (CSS) with an integrated low-cost shunt resistor (Figure 1.7). As the sensing element, the performance of shunt resistor R_{shunt} plays a key role in determining the overall performance of the CSS. Therefore, it is essential to consider different ways in which shunt resistors can be implemented, and then to choose/design the most suitable one(s) for our work.

From system integration and size perspective, shunt resistors can be divided into three categories: 1) off-chip, 2) in-package, and 3) on-chip. Each category offers a unique set of possibilities in terms of shunt performance, size and cost.

This chapter first lists the non-idealities and limitations of shunt resistors. Then, it briefly reviews various categories of resistors and their implementation. Finally, two types of resistors will be proposed for use in this work. These resistors are on-chip and in-package and have been selected on the basis of their small size and low cost.

2.1. Resistor Non-Idealities and Constraints

In the following, resistor non-idealities that can possibly limit current-sensing performance are listed and explained in the following.:

- **Tolerance:** Due to spread in the shunt's geometry and/or its electrical resistivity, its resistance R_{shunt} may differ from the intended value. This problem

is often addressed by either tight control of the fabrication process or by trimming/calibrating the shunt after fabrication [1].

- **Temperature coefficient of resistance (TCR):** Shunt resistance drifts with changes in ambient temperature or Joule heating. At the expense of extra cost, alloys with an extremely low TCR, e.g., Constantan (a copper-nickel alloy with a TCR of $\approx$ 10ppm/°C), can be employed. When using standard IC materials, e.g., copper with a TCR of $\approx$ 3900ppm/°C, a temperature compensation module should be incorporated into the readout circuitry [1].

- **Voltage coefficient of resistance (VCR):** The voltage drop across the shunt may modify the shunt's internal structure, thereby changing its resistance. This phenomenon is quantified as the relative change in resistance per Volt [2].

- **Package stress effect:** The thermal expansion coefficient of the shunt and that of the various materials used to package the shunt are not necessarily the same. Temperature changes can, therefore, cause thermo-mechanical stress (either compressive or contractive) in the shunt, which, in turn, modulates its resistance via the piezoresistive effect [2, 3].

- **Long-term stability:** The slow change in R_{shunt} with time is usually referred to as drift or instability. It depends on many factors, of which ambient temperature, current level, and mechanical stress (e.g., from packaging) are the most important [2].

- **Seebeck effect:** A temperature difference between two junctions of two dissimilar conductors (metal or semiconductor) will generate a voltage. Therefore, errors in the measured shunt voltage V_{shunt} will occur if the connection points of the shunt's two sensing wires are at different temperatures [4].

- **Limited bandwidth:** The shunt's transfer function V_{shunt}/I is influenced by several parasitic effects. Among them, the most notable are 1) the mutual inductance between the current conducting path and the loop created by the shunt's sense wires, and 2) the skin effect, i.e. the non-uniform current distribution within the shunt at high frequencies, and 3) the proximity effect, i.e. the proximity of the shunt to ferromagnetic materials, such as steel, or to a strong magnetic field, which may both alter the current distribution in the shunt and cause systematic errors [1, 5, 6]. As these parasitic effects are

typically only significant at frequencies above a few hundred kilohertz, their detailed description falls beyond the scope of this dissertation. More information can be found in [1, 4, 6].

Besides taking care to minimize the effect of the aforementioned error sources, there are a set of constraints that should also be considered while designing a shunt resistor.

- **Resistor value:** The shunt's resistance R_{shunt} represents a compromise between the power lost in the shunt and the magnitude of the voltage drop V_{shunt}. Lowering R_{shunt} reduces power loss at the expense of V_{shunt}, and consequently, current-sensing offset and resolution.

  In Coulomb counting applications, typical values of R_{shunt} range from a few to tens of mΩ [7–10]. At a peak current of 5 A, this corresponds to several tens to hundreds of milliwatts, which is quite significant. However, portable devices such as cellphones and tablets are usually in low-power/stand-by mode, during which the shunt's power dissipation will be lower than the power dissipated in the continuously-running CSS. The battery's internal resistance, contact resistance and that of the associated wiring should also be taken into account. For instance, in lithium-ion (Li-ion) batteries, which are the most commonly used batteries for portable devices (due to their small size and high capacity features), these resistances will typically be in the order of several tens to hundreds of mΩ [11, 12], and so there is no point in making R_{shunt} any smaller.

  In this work, a shunt with a nominal value of 10 mΩ is chosen, for which a current-sensing offset of a few tens of microamperes corresponds to an ADC offset of several hundred nanovolts, which can be achieved with the help of dynamic offset cancellation techniques [13].

- **Price:** The shunt's fabrication process and the required trimming/calibration steps play a key role in determining the CSS cost. A CMOS-compatible on-chip shunt, or a shunt readily available in a standard IC package together with a simple correction process enables the production of a cost-effective system.

- **Physical size:** A small-sized shunt is critically important for the CSS used in portable devices.

- **Rated power:** This refers to the maximum allowed power that can be continuously applied to the shunt at the maximum specified ambient temperature.

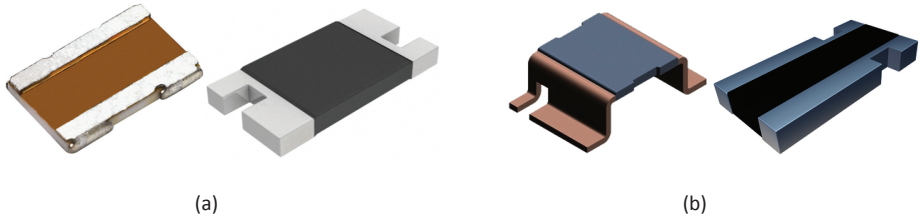

Figure 2.1: Photos illustrating (a) bulk metal foil, and (b) power metal strip resistors (courtesy of [14]).

2.2. Off-Chip Shunt Resistors

This section briefly introduces several commonly used off-chip resistors for current-sensing applications.

2.2.1. Bulk Metal Foil Resistors

Bulk metal foil technology (Figure 2.1) offers the most stable and precise types of resistors [2, 15]. They are made by depositing a several-micrometer-thick layer of a special alloy with low TCR, e.g., Constantan with 10 ppm/°C, on a ceramic substrate, and then etching the resulting foil into the desired resistor pattern. Further improvement of the TCR is achieved by controlling the thermo-mechanical stress of the substrate such that it counteracts the variation of the foil's resistivity with temperature [2].

With strict control of alloy composition and of foil deposition, shunts with a TCR of ±0.2 ppm/°C from −55 to +125°C have been made [2, 15]. In addition, a precise photo etching process and sophisticated trimming yields accurate resistors with absolute tolerances in the order of 10 ppm. These resistors cover a wide range from sub-mΩ to several MΩ [2]. They can also achieve a stability of better than 100 ppm at 70°C and rated power for 10,000 hours. The alloy foil is also etched into an inductance cancelling pattern that enables a fast current step response (1 ns). Errors due to the Seebeck effect are also reduced to the 50 nV/°C level [2].

Due to their sophisticated and tightly-controlled fabrication process, these types of resistors are very expensive, and hence not suitable for low-cost CSS implementation. For instance, a 10 mΩ foil resistor, capable of handling up to 7A, may cost more than 15€ [16].

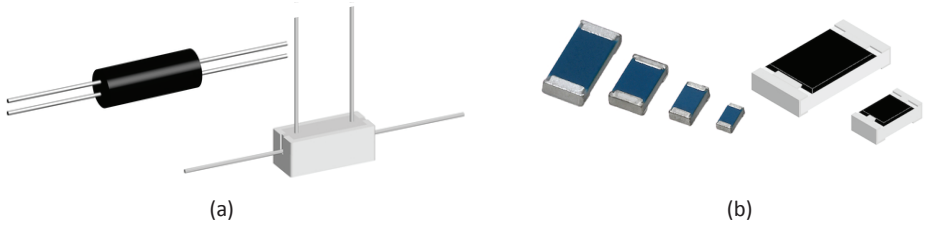

Figure 2.2: Photos illustrating (a) wirewound, and (b) thin film and thick film resistors (courtesy of [14]).

2.2.2. Power Metal Strip Resistors

Widely used in current-sensing applications, power metal strip resistors are made of strip-shaped, low-TCR metal alloys, such as nickel-chrome or manganese-copper with TCRs of several tens to hundreds of ppm/°C [14, 16, 17]. Their values cover a wide range, from sub-mΩ to several MΩ, with a typical absolute tolerance of less than ±0.5%. The error due to the Seebeck effect in a metal strip resistor is significantly larger than that in a metal foil resistor, and is in the range of several μV/°C [2]. Low-inductive implementation of these resistors provides an excellent frequency response up to several tens of megahertz.

These types of resistors are, however, still quite expensive, and therefore not suitable for use in low-cost CSS applications. For example, a 10 mΩ resistor, with a tolerance of ±1%, a TCR of ±50 ppm/°C and capable of handling 5 A, typically costs around 1 € [16].

2.2.3. Wirewound Resistors

A wirewound resistor (Figure 2.2) is often made by winding insulated resistance wire around a cylindrical substrate. By using a low TCR alloy and very tight control of the fabrication process, resistors with initial tolerances of <50 ppm and TCRs of <20 ppm/°C can be realized [2, 18]. The two most commonly used materials are a copper nickel alloy with the addition of manganese (Manganin), and a nickel chromium alloy with the addition of iron. Both can achieve a stability of better than 1500 ppm at 70°C and a rated power for 10,000 hours [2]. Due to their cylindrical geometry, they exhibit large parasitic inductances and capacitances, which results in poor high-frequency behavior, particularly above 50 kHz [2].

Another serious drawback of their geometry is the increased size, bulk and weight of the resulting resistors; they are typically larger than 20 × 5 × 5 mm^3. They are also more expensive than metal strip resistors [14, 16].

2.2.4. Thin Film and Thick Film Resistors

Thin film resistors are made by sputtering a metal film (5 to 25 nm thick) onto a ceramic substrate. Their TCR is controlled by the metal film thickness and is significantly influenced by the shift from optimum film thickness.

Thick film resistors are about 1000× thicker than the thin film resistors. They are fabricated by printing a resistive paste, usually consisting of metal oxides and glass-based materials, onto a ceramic substrate, followed by a high-temperature treatment process.

These types of resistors are less expensive than wirewound or bulk metal foil resistors. Their frequency responses are similar to metal foil resistors. However, thick film resistors suffer from a larger tolerance and are less stable compared to other types of resistors [2, 18].

2.2.5. PCB Copper Trace

The simplest way to realize a shunt resistor is to exploit the resistance of an existing PCB trace [4, 19, 20]. Although this approach enables a very cost-effective implementation without additional power loss, it suffers from the large TCR of the copper trace (∼0.39%/°C), especially since its temperature cannot be accurately sensed, and thus compensated for, by an on-chip temperature sensor.

Ziegler [4], used a stand-alone temperature sensor (LM335 in TO-92 package) to sense the temperature of a PCB trace. The sensor was attached to the copper trace by thermal paste to lower the thermal resistance between it and the trace. However, the remaining thermal resistance still causes an underestimation of the self-heating in the trace. To overcome this issue, a rather complicated correction method was proposed, which requires knowledge of the shunt-to-ambient and the shunt-to-sensor thermal resistances as well as of ambient temperature (obtained by another temperature sensor). This method achieved a current-sensing error of about 2% at a current level of 240 A.

In [20], an indirect temperature compensation scheme is proposed. It involves sensing the thermal drift of a replica copper trace by driving a reference current through it. This approach, however, is not able to compensate for the effect of Joule heating in the shunt, and is therefore limited to low currents (less than 0.5 A in [20]). In addition, the reference current's spread and drift directly limit the resulting current-sensing accuracy.

2.2.6. Remark

Precision off-chip shunt resistors are too large and expensive for use in a low-cost CSS, whereas shunts based on low-cost PCB traces suffer from a large TCR. It can be concluded that off-chip shunt resistors are not suitable for use in a low-cost precision CSS.

2.3. In-Package Shunt Resistor

Incorporating a shunt into an IC package can potentially improve the thermal coupling between the shunt and the on-chip temperature sensor. It can also help to reduce the physical size of the resulting CSS. Several ways to implement such resistors are presented in this section.

2.3.1. Bond Wire

A shunt resistor can be realized by utilizing a bond wire in the package [21, 22]. As shown in Figure 2.3(a), this can be done by connecting a bond wire between two lead-frames. By using a Kelvin connection, the voltage drop across the shunt is picked up and then processed by an on-die readout circuitry [21]. In some applications, e.g., integrated power modules, the target current is inevitably directed toward the die. As shown in Figure 2.3(b), this situation allows the resistance of the existing bond wire in the current path to be used as a shunt without any design overhead [22].

In a standard wire bonding process, the wire resistance spreads up to 20% and can vary significantly with temperature (a gold wire has a TCR of $\sim$0.37%/°C). As such a calibration and temperature compensation module should be included in the readout circuitry. However, the thermal coupling between a bond wire and the die, although better than that of a PCB trace, is still quite poor, and so limits the resulting current-sensing accuracy.

2.3.2. Lead-Frame

The designs reported in [23–25] propose the use from a shunt made of the package lead-frame. As illustrated in Figure 2.4, part of the lead-frame is modified in such a way that the current can flow from pin A^+ to pin A^-. The resulting voltage drop is then picked up by means of two bond wires, connected to the two sensing points S^+ and S^-, and processed by the readout electronics on the die.

The design presented in [24, 25] realizes a total resistance of 1.3mΩ (between

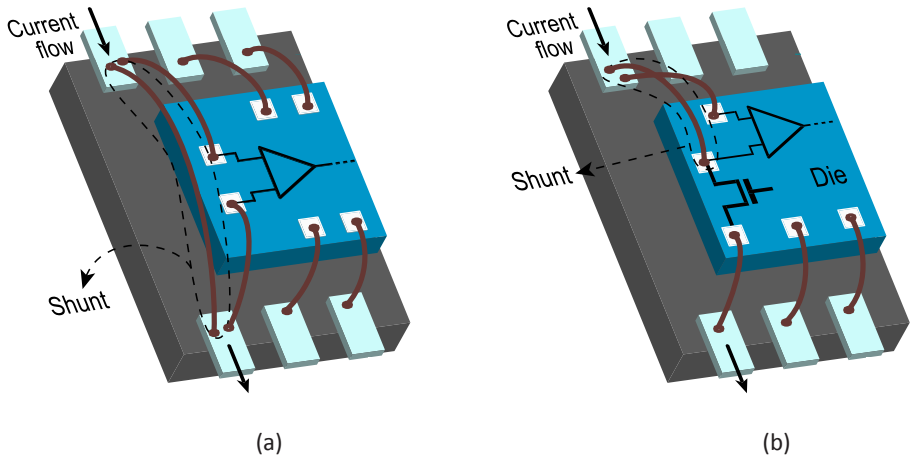

Figure 2.3: Using (a) a dedicated and (b) an existing bond wire for shunt implementation.

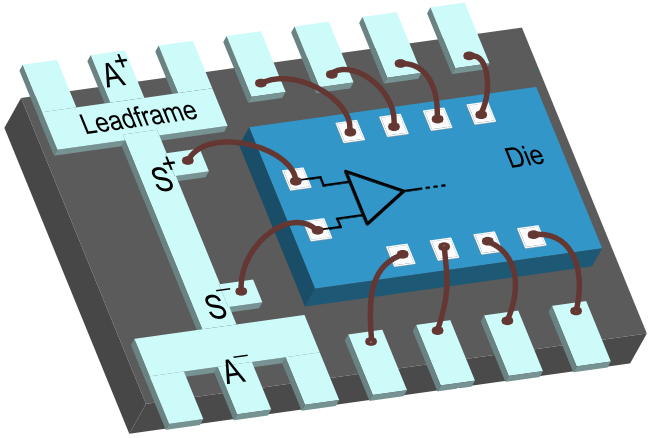

Figure 2.4: IC package lead-frame for shunt implementation.

A^+ and A^-) for up to ±20A current sensing. The resistance between S^+ and S^- is about $667\mu\Omega$ and forms the effective shunt resistance R_{shunt}, while the rest of the lead-frame forms a parasitic resistance which should be minimized. The effect of the lead-frame's large TCR, about $+0.335\%/°C$, is addressed by amplifying V_{shunt} with a gain that is designed to have an equal-but-opposite temperature coefficient. The spread in R_{shunt} is also corrected by trimming the amplifier's gain. However, the resulting gain error is still significant ($> \pm 5\%$) over the temperature range from $-40°C$ to $+85°C$ [25].

A serious drawback of the aforementioned shunt implementations is the physical

distance between the shunt and the die on which the temperature compensation scheme is implemented. This separation results in poor thermal coupling between the shunt and the die, which in turn leads to inaccurate shunt temperature sensing (especially due to the Joule heating effect) and lower current-reading accuracy. To mitigate this, [26] proposes locating the die directly on top of the lead-frame shunt.

Another approach [27], employs a lead-frame with a low TCR. The selected material should also facilitate die attachment and be easy to wire-bond and solder. The exemplary alloys that meet these requirements and provide a TCR of less than 20 ppm/°C are Constantan (copper-nickel), Manganin (copper- nickel-manganese), and Evanohm (copper-nickel-manganese-aluminum-chromium). Stitt [28], proposes using different materials for the lead-frame and for the shunt embedded in the lead-frame. A low TCR alloy is used for shunt implementation and the lead-frame is made of a metal with less electrical resistivity than that used for the shunt. For example, Constantan or Manganin can be used for the shunt, while the lead-frame can be realized with copper or aluminium, whose electrical resistivity is at least ten times lower than that of the shunt. In this way, the problems of shunt thermal drift and parasitic resistance are simultaneously solved. The main drawback of this approach, however, is that it requires a custom package, thus increasing the production cost.

2.3.3. Redistribution Layer

An alternative way of improving the thermal coupling between a shunt and a chip is to implement the shunt in the redistribution layer (RDL) of a chip-scale IC package [29, 30]. The RDL is basically a metal layer, usually copper with a thickness of several micrometers, deposited on the die passivation layer to bridge the die pad and the package solder ball. As shown in Figure 2.5, the RDL can be shaped into a shunt with Kelvin sensing points. An additional benefit of this approach is the smaller shunt foot print, which enables the sensing points to be located closer to each other. This also helps to mitigate the Seebeck voltage caused by possible temperature gradients in the shunt.

2.3.4. Remark

Incorporating a shunt into an IC package lead-frame or an RDL enables the realization of a small-size CSS with a good shunt-temperature-sensor thermal coupling. Custom-designed packages with low TCR, however, lead to much higher production costs and are not considered for use in this work.

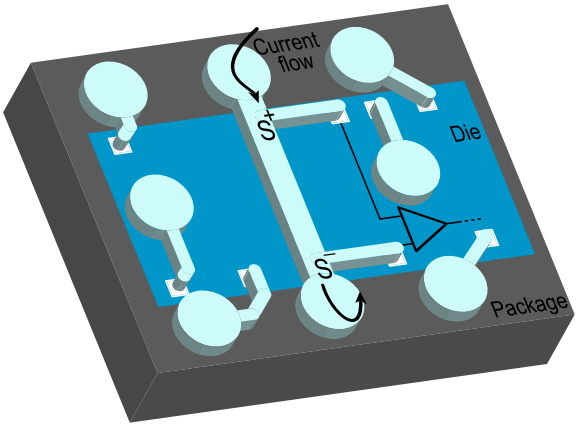

Figure 2.5: Simplified diagram of a shunt built by a redistribution layer (RDL) in a chip-scale package.

2.4. Proposed Shunt Resistor

To minimize production costs, we propose the use of two shunts that are fully compatible with standard CMOS processes and standard IC packaging technology: 1) a shunt made from the metal layers of a CMOS chip, and 2) a shunt made from the heatsink lead-frame of a standard HVQFN32 plastic package.

2.4.1. On-Chip Shunt Resistors

The metal layers of a standard CMOS process can be used to realize a mΩ shunt. As shown in Figure 2.6, the proposed shunt consists of four metal layers (M2 to M5) connected in parallel. Each metal layer occupies a large area ($W = 700$ μm, $L = 400$ μm), in order to reliably handle 5 A currents, and to facilitate low-ohmic contacts to the outside world via eight large (150×150 μm^2) bond pads. The resulting shunt has a nominal value of 10 mΩ, the spread of which (up to ±15%) is corrected by room-temperature calibration. Chapter 4 describes the calibration process in more detail.

The parasitic resistance of the connections between the CSS and the outside world increases the battery-to-load resistance, and the associated Joule heating represents wasted power. As shown in Figure 2.7, the parasitic resistances are minimized **a)** by mounting the chip directly on a PCB [chip-on-board (CoB)], to which the shunt was connected by 32 short (< 1 mm long) and thin (25 μm in diameter) bond wires, and **b)** by packaging the chip in a small ($3 \times 6 \times 0.85$ mm^3) ther-

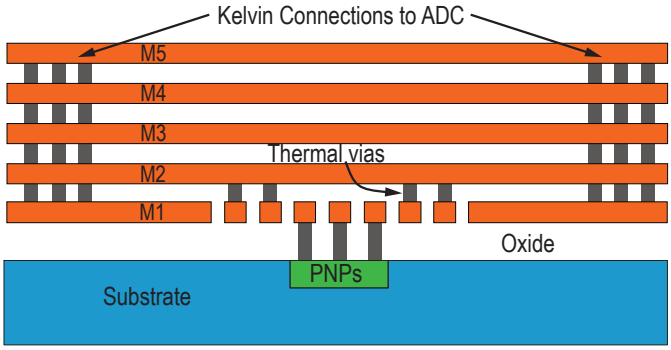

Figure 2.6: Simplified cross-sectional view of the metal shunt and the temperature-sensing PNPs underneath.

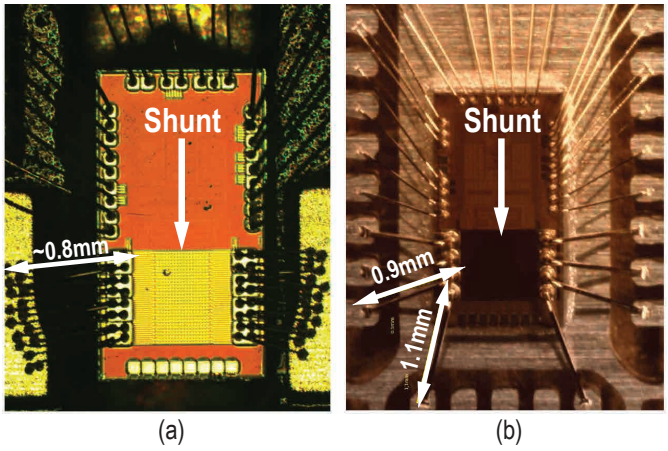

Figure 2.7: Photo of the chip (a) directly bonded to a PCB, and (b) packaged in a HVQFN plastic package.

mally enhanced 32-pin QFN plastic package (HVQFN32), to which the shunt was connected by eight short (∼1 mm long) and thick (50 μm in diameter) bond wires. The total parasitic series resistance, in both cases, is measured to be less than 10 mΩ.

For a typical plastic package with a junction-to-ambient thermal resistance of 100°C/W, passing 5 A through a 10 mΩ shunt will result in a 25°C temperature rise. Considering a worst-case parasitic resistance of 10 mΩ, the self-heating can rise up to 50°C. This, together with ambient temperature variations, results in a significant measurement error, since the shunt has a TCR of about 0.35%/°C. This effect should be counteracted by a temperature compensation scheme. Further

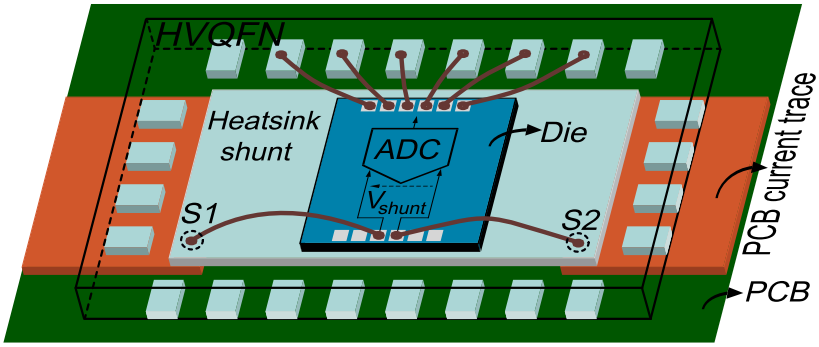

Figure 2.8: Lead-frame shunt in a standard HVQFN32 plastic package.

details of the temperature compensation scheme and thermal coupling between the shunt and the temperature-sensing element is presented in Chapter 3 and 4.

2.4.2. Lead-Frame Shunt Resistor

As shown in Figure 2.8, the lead-frame shunt is made from the heatsink of a small ($3 \times 6 \times 0.85$ mm^3) thermally enhanced 32-pin QFN plastic package (HVQFN32) [31, 32]. The die is glued to the lead-frame and senses the voltage drop V_{shunt} between the Kelvin-contacted points S1 and S2. This approach avoids the costs associated with the design of a custom lead-frame shunt at the expense of a fixed resistance. The resulting shunt, with dimensions of $W \times L \times t = 1.8$ mm $\times$ 4.8 mm $\times$ 0.2 mm, has a nominal value of 260 $\mu\Omega$ at room temperature, whose spread (due to, e.g., spread in the lead-frame thickness or in the location of the Kelvin-contacted points) is corrected by a room-temperature calibration. Although the target 5 A current range results in rather small voltages, this demonstrated the feasibility of a lead-frame shunt, especially for high current-sensing applications, e.g., automotive. In a real product, a custom-designed lead-frame would be used [27].

Compared to an on-chip shunt, whose maximum current is limited by electromigration (see Chapter 3), a lead-frame shunt is quite thick and so its maximum current is mainly limited by the maximum allowable die temperature. Measurements (Chapter 6) show that passing a 36 A current through the lead-frame shunt results in a temperature rise of ~ 50°C[1], which translates into a maximum die temperature of 135°C at the maximum ambient temperature of 85°C. Similar to that of the on-chip shunt, this effect can be counteracted by an on-chip temperature

[1]Some of this self-heating arose in our test PCB and could be improved by a better thermal design.

compensation scheme.

It should be noted that, in this prototype, shifts in the orientation of the heatsink on the PCB, and thus in the exact locations where current enters and leaves the shunt, may cause small changes in the shunt's resistance. Like its spread, this is corrected by room-temperature calibration. However, this implies that the end user must calibrate the sensor after it has been soldered to the PCB, which may not be desirable. A custom lead-frame design would avoid this issue by ensuring that its sensing section, i.e. the section between the Kelvin contacts, is located some distance away from the actual soldering pins of the package, [33].

2.5. Conclusion

In this chapter, different ways of implementing a shunt resistor have been reviewed, and two types have been chosen for use in this work. Precision off-chip resistors are too expensive, whereas the low-cost ones suffer from large TCR and poor thermal coupling to the temperature sensor. In addition, this class of resistors is typically too bulky, and hence not feasible for integration in the portable devices. The in-package shunts offer a compact and potentially low-cost solution; shunts based on a standard package lead-frame and RDL layers are the most promising.

We propose the use of a 10 mΩ on-chip metal shunt resistor. Being compatible with standard CMOS processes and standard packaging technology, this type of shunt can be used for $\pm$5 A current sensing with a gain error of better than $\pm$0.5% (Chapter 5 and 6). On-chip shunts, however, require large silicon area and exhibit a noticeable drift due to electromigration. This problem is solved by employing the lead-frame resistance of a standard package; the heatsink lead-frame of an HVQFN32 offers a 260 $\mu\Omega$ resistor. This is used for $\pm$36 A current sensing with better than $\pm$0.5% gain error (Chapter 6).

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3

Proposed Shunt Resistors

In the previous chapter, we proposed two different types of integrated shunt resistors, 1) a 10 mΩ on-chip metal resistor, and 2) a 260 $\mu\Omega$ lead-frame resistor. Since these resistors suffer from large TCR ($\approx$ 3500ppm/°C), an accurate temperature compensation scheme is essential for accurate current sensing. The choice of the temperature-sensing element and the thermal coupling between the shunt resistor and the temperature sensor are studied in this chapter.

Since they are made from the very thin (a few hundreds of nanometers) metal layers of the CMOS process, the on-chip metal shunt is expected to exhibit noticeable drift due to electromigration at high temperatures and high currents. This effect is experimentally investigated in this chapter.

3.1. Temperature Compensation

At a temperature T, the resistance of a shunt R_{shunt} can be approximated as:

$$R_{\text{shunt}}(T) = R_{\text{shunt}}(T_0) \cdot \Big(1 + \alpha_1 \cdot (T - T_0) + \alpha_2 \cdot (T - T_0)^2\Big) \tag{3.1}$$

where α_1 and α_2 are the resistor's first and second order temperature coefficients, and T_0 is the temperature at which the shunt is calibrated. Since T_0 is sensed by the on-chip temperature sensor, this calibration does not need to be performed in

a temperature-stabilized environment, thus reducing calibration time and cost. According to process data and measurements obtained from two different batches [1], α_1 and α_2 are quite constant for the given process. The measured values of these coefficients for the on-chip shunt are $\alpha_1 \approx +0.33\%/°\text{C}$ and $\alpha_2 \approx -5.6\times10^{-5}\%/°\text{C}^2$, while for the lead-frame shunt they are $\alpha_1 \approx +0.26\%/°\text{C}$ and $\alpha_2 \approx +1.3\times10^{-5}\%/°\text{C}^2$. It will be shown in Chapter 5 and 6 that a first order temperature correction of on-chip shunt results in current-sensing errors of up to 1%, while second order correction keeps errors below 0.35%. The second order coefficient of lead-frame shunt is smaller than that of on-chip shunt, and not correcting for it only increases current-sensing gain error from 0.25% to 0.35%. However, we will use second order correction for both the on-chip and lead-frame shunts.

Unlike [2, 3], in which the effect of the TCR is addressed by amplifying V_{shunt} with a gain that is designed to have an equal-but-opposite temperature coefficient, we opted to directly digitize the shunt's temperature with a smart temperature sensor and then perform a polynomial correction on the digitized value of V_{shunt}. This approach leads to a simpler analog and more digitally-assisted design, which in turn helps to improve accuracy by eliminating the potential error sources of additional analog circuitry.

3.1.1. Temperature Sensors

In order to digitize temperature, a ratio-metric measurement has to be performed. This involves digitizing the ratio between a temperature-dependent signal and a reference signal. The fact that, in a silicon die, nearly all devices' characteristics are temperature-dependent offers many possibilities for implementing such a sensor. Accurate temperature sensors based on resistors (thermistors) [4–6], the thermal diffusivity of the silicon substrate [7–9], MOS transistors [10–14], and bipolar transistors [15–19] have been reported. The type of temperature sensor for this work should be selected based on the following criteria: 1) it should offer sufficient thermal coupling between the shunt and the temperature sensing element, and 2) the sensor must be implemented with the minimum circuit and system overhead.

On-chip resistors with relatively large TCRs ($\sim 0.3\%/°\text{C}$) have been used in a Wheatstone bridge [4] and in Wien bridges [5, 6] as temperature sensing elements. These types of sensors are attractive due to their excellent energy-efficiency [6, 20], and have been used for temperature compensation in MEMS- and crystal-based frequency references [4, 5]. They also have the potential to achieve the highest degree of thermal coupling with the shunt if implemented with a metal resistor laid out

very close to the shunt. However, in order to keep the sensor's power consumption below 50 μA (Table 1.1), the resistor should be in the order of several tens to hundreds of kΩ, which would require a huge area. In addition, due to their relatively large process spread and non-linear temperature dependency, resistor-based sensors require multi-point trimming; e.g., after three-point trimming, the design reported in [5] achieved $\pm$0.12°C from $-$40°C to +85°C. Moreover, the required references for the Wien bridge sensors are derived from a relatively stable frequency reference which is not readily available in a CSS.

The thermal diffusivity of the silicon substrate D is a function of absolute temperature ($D \propto T^{0.9}$) [7]. This property has been utilized to implement temperature sensors based on the thermal delays in the electrothermal filters [7–9]; the temperature is sensed by measuring the time it takes for a heat pulse to travel a certain distance d in a silicon substrate. These sensors can be made very compact (e.g., 1650 μm^2 in [9]) whose accuracy improves with advances in CMOS technology [21] as d is more accurately defined with a better lithography process. However, the thermal diffusivity sensors dissipate several milliwatts and require a relatively accurate frequency reference for thermal delay measurement [8, 9].

Various configurations of MOS transistors have been used for temperature sensing. Probably, the simplest of all is to utilize the temperature-dependency of CMOS gate delay [10, 11, 13]. Due to their large spread, however, their typically require two-point trimming to obtain an inaccuracy of less than 1°C. Another approach is to use the temperature-dependency of gate-source voltage V_{gs} of a diode-connected MOS transistor, biased in the sub-threshold region [22]. However, mainly due to the spread in MOS threshold voltage V_{th} and its variation with gate-body voltage V_{gb}, they typically mandates two-point trimming to reduce the inaccuracy below 1°C. To circumvent this problem, the gate and body terminals can be tied together. This fixed the width of the depletion layer under the channel and cause V_{th} to dynamically change in a well-defined manner [14, 23]. Thereby, this configuration is called DTMOST (dynamic threshold MOST). One state-of-the-art DTMOST-based sensor achieves an inaccuracy of $\pm$0.4°C from $-$40°C to +125°C after one-point trimming [14]. This performance indicates that the DTMOST-based design can be possibly used as the temperature sensor in the CSS.

However, temperature sensors which employ bipolar transistors (available in standard CMOS process) have been proven to be the most accurate reported to date [16, 17, 19]. After a single-point trim, they can achieve an inaccuracy as low as $\pm$0.06°C from $-$70°C to +125°C [18, 19]. In Chapter 4, the choice is made for

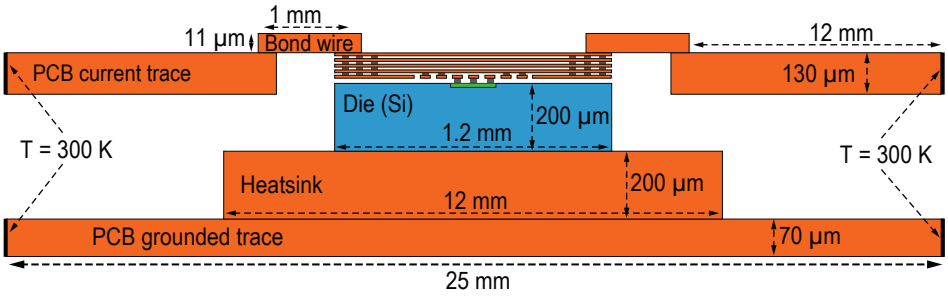

Figure 3.1: A two-dimensional model for electro-thermal simulation of the on-chip shunt with its connection to outside world in COMSOL.

temperature sensors based on the parasitic PNPs available in standard CMOS. This is because 1) they can be merged with the required bandgap reference for the ADC digitizing the shunt voltage V_{shunt}, and 2) they can meet the accuracy and resolution requirements at a power level well within the budget.

In order to enhance the shunt-PNP thermal coupling, the shunt is placed directly above the PNPs. As shown in Figure 2.6, this is achieved by realizing the shunt in the top metal layers (M2 to M5), and reserving M1 for connections to the PNPs. Thermal coupling is further improved by the use of thermal vias between the shunt and an M1 plane surrounding the PNPs.

Measurements show that, compared to a previous implementation [24, 25] in which the PNPs are located besides the shunt, these modifications result in an improvement of 3× in the accuracy of the estimated shunt temperature rise caused by Joule heating. However, the temperature sensor will still under-estimate shunt temperature, since the PNPs are still insulated from the shunt by an oxide layer [26]. According to measurements (Chapter 5), a 5 A current through R_{shunt} causes a temperature rise of around 45°C (obtained by using the same shunt as a thermistor), which the PNPs under-estimate by 1.5°C. Considering that the shunt's TCR of 0.35%/°C, this causes a current-sensing error up to 0.5%. It is therefore necessary to maximize the shunt-PNP thermal coupling. This is the subject of the next section.

3.2. Shunt-Temperature Sensor Termal Coupling

3.2.1. On-Chip Shunt

The thermal coupling between the shunt and the temperature sensor can be investigated with an electro-thermal simulation in COMSOL multi-physics software.

Figure 3.1 illustrates the simulation model, in which the silicon die containing the on-chip shunt, together with the heatsink pad of the HVQFN32 package, the bond wires and PCB traces are included. Since the on-chip metal layers are very thin the distances between them are very small, a three-dimensional simulation of this structure takes too long and often leads to convergence issues and inaccurate results. To avoid these issues, a two-dimensional simulation model is used with the following considerations and boundary conditions.

- The current $I = 5$ A flows into the PCB current trace through their bottom sides.
- The left and right side of the PCB traces are assumed to be at an ambient temperature of 300 K. The length of the PCB traces was chosen such that making them any longer has a negligible effect on the simulation result.
- The dimensions of the different blocks, normal to the heat and the current flow, are adjusted so as to account for the contrast in width (third dimension) compared to that of the shunt (700 μm). For instance, the current-conducting PCB traces, being 18 μm thick and 5 mm wide, are two-dimensionally modelled to be 18 μm $\times$ 5 mm/700 μm $\approx$ 130 μm thick so that the cross-sectional area normal to the heat and the current flow is preserved. As an another example, the thickness of the four bond wires, each with a diameter $d = 50$ μm, is jointly set at $\pi d^2/700$ μm $\approx$ 11 μm. The heatsink, originally measuring 4.8 mm $\times$ 1.8 mm $\times$ 0.2 mm, is also drawn as an area of 4.8 mm $\times$ 1.8 mm/700 μm $\approx$ 12 mm long, so that its heat conducting capability is preserved.
- A convective heat transfer to still air (with a typical coefficient of $h = 5$ W/m^{2}K) is assumed for the top surface (side) of the current-conducting PCB traces. This coefficient, however, should be modified to account for the differences in the third dimension compared to that of the shunt; it is modified to 5 W/m^{2}K $\times$ 5 mm/700 μm $\approx$ 36 W/m^{2}K.

The simulated temperature rise in different metal layers of the on-chip shunt and at the surface of the silicon substrate is plotted in Figure 3.2. Self-heating of around 50°C is shown. The upper metal layers are at slightly higher temperatures as they are more isolated from the substrate, which serves as a heatsink. The average temperature rise of the shunt, calculated by the weighted averaging of metal layers' temperatures (with a weight equal to their electrical conductivity), is about 0.9°C higher than that of the PNP's.

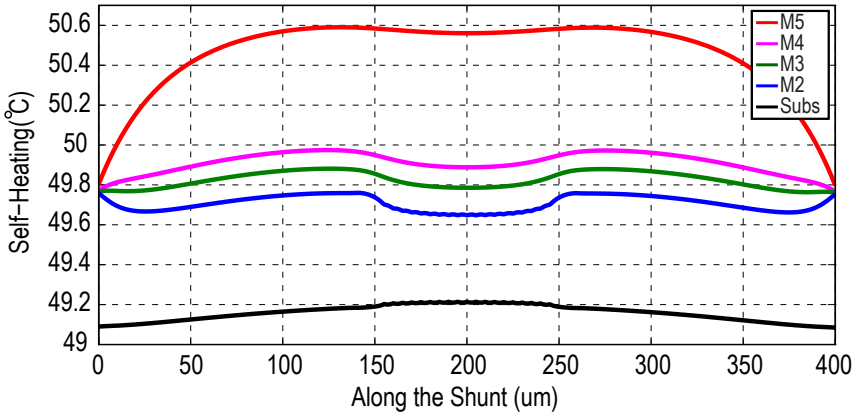

Figure 3.2: COMSOL simulation result: temperature rise in different metal layers of the on-chip shunt (Figure 2.6) and the substrate at 5A current level.

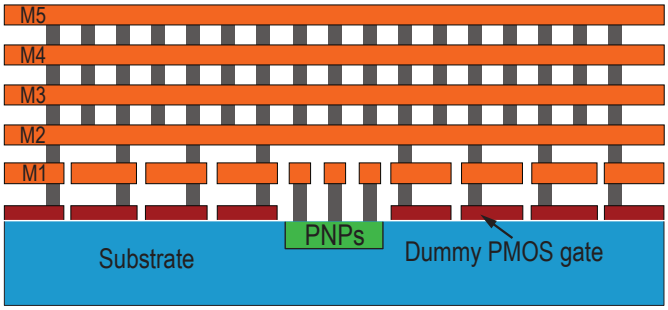

Figure 3.3: Simplified cross-sectional view of the metal shunt with thermal vias to improve its thermal coupling with the PNPs underneath.

This simulation, although not a perfect match with measurements, provides insight into ways of improving the shunt-PNP thermal coupling. As shown in Figure 3.3, the temperature of the upper metal layers can be brought closer to that of the substrate by means of thermal vias placed all over the shunt's metal layers. Additional thermal vias between the shunt and the gates of dummy PMOS devices can also help to reduce the thermal distance between the shunt and the PNPs. The simulation results of this structure is plotted in Figure 3.4, which suggests that the shunt-PNP temperature difference is reduced to 0.12°C, resulting in a current-sensing error of less than 0.05%. This shunt resistor is therefore used in another prototype CSS (presented in Chapter 6).

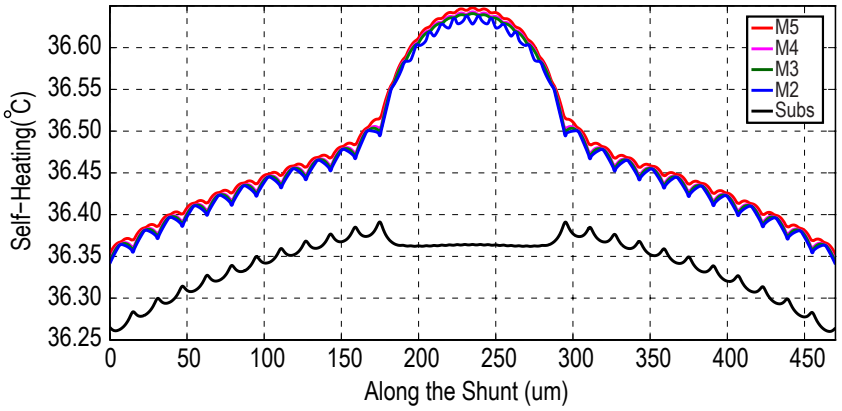

Figure 3.4: COMSOL simulation result: temperature rise in different metal layers of the on-chip shunt (Figure 3.3) and the substrate at a 5A current level.

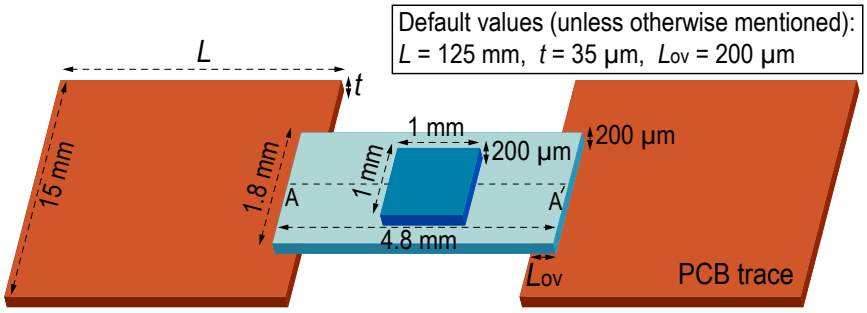

Figure 3.5: COMSOL simulation setup to study the thermal coupling between the lead-frame shunt and the temperature-sensing PNPs located on the surface of the silicon die.

3.2.2. Lead-Frame Shunt

As in the previous section, the thermal coupling between a lead-frame shunt and on-chip PNPs can be investigated. The simulation setup, including the dimensions of the various elements, is shown in Figure 3.5. For the sake of simplicity, only the shunt, silicon die and the current-conducting PCB traces are included in this model. The die was assumed to have a thickness of ~ 200 μm after being back ground to fit into the HVQFN package. A coefficient $h = 5$ W/m^{2}K of convective heat transfer was used for the top surface of the PCB traces, which are assumed to be in perfect thermal contact with the lead frame, and whose far ends are assumed to be at room temperature.

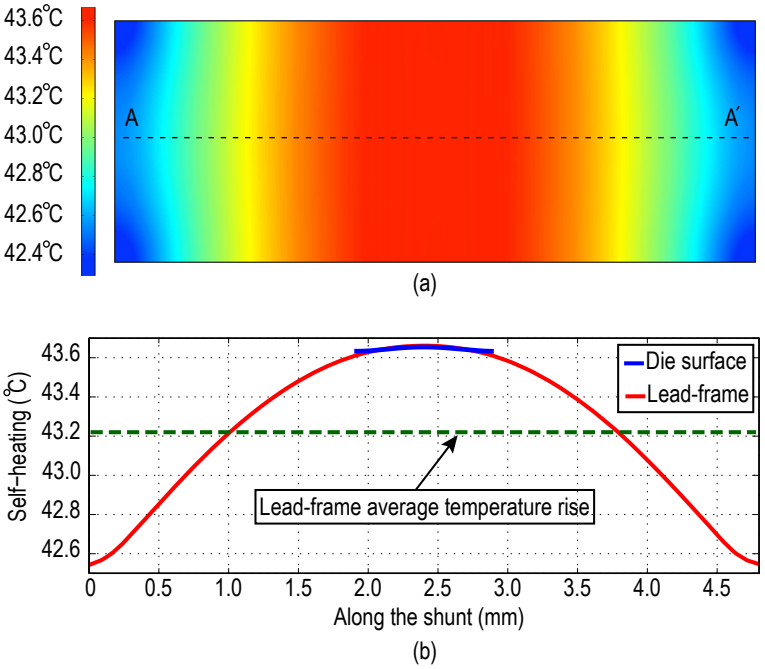

Figure 3.6: COMSOL simulation result: temperature rise at (a) the lead-frame surface, and (b) along the AA' axis at a 36A current level.

The simulated temperature rise on the upper surface of the shunt at $I = 36$A is illustrated in Figure 3.6(a), while the temperature profile along the AA′ axis is shown in Figure 3.6(b). The simulations predict an average temperature rise of about 43°C, which is in good agreement with measurement results. As expected, the self-heating peaks in the middle of the shunt and tapers off towards the points where it is attached to the PCB trace. The simulations also show that the difference between the average temperature of the shunt and that of the PNPs is only about 0.4°C, corresponding to a small 0.1% current-sensing gain error (the measured lead-frame TCR is around 0.26 %/°C as reported in Chapter 6).

As shown in Figure 3.7, even though the shunt's temperature rise and its relative curvature are influenced by the dimensions of the PCB trace, its overlap with the lead-frame, and its ability to conduct heat away from the chip, these factors hardly affect the temperature difference between the shunt and the PNPs. These results indicate that a custom lead-frame shunt can be used as a low-cost and robust shunt in high-current sensing applications.

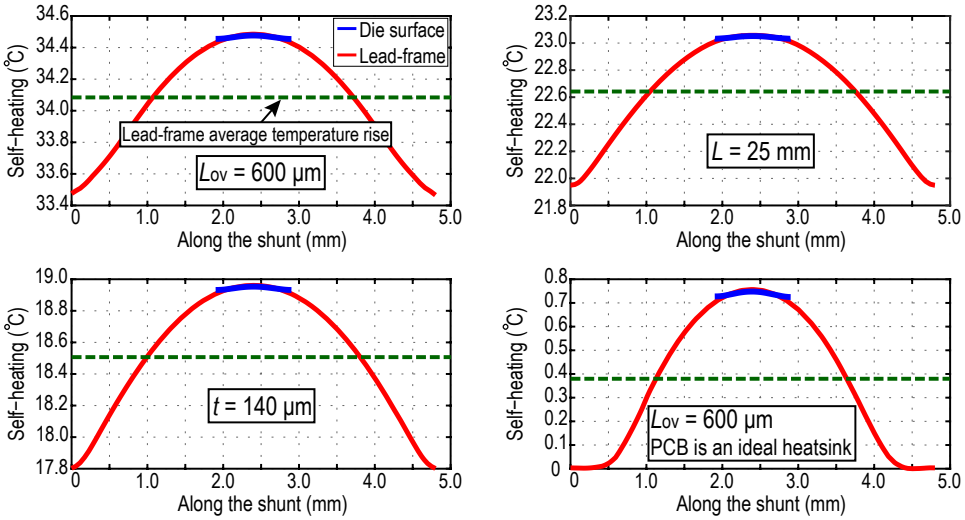

Figure 3.7: COMSOL simulation results showing the self-heating along the AA′ axis at a 36A DC current and under different mechanical setups.

3.3. Electromigration And Stability of On-Chip Shunt

Electromigration (EM) refers to the transport of atoms in (metallic) conductors due to an electric current flow, and the consequential degradation of the metal shunt's stability and reliability. It is therefore necessary to investigate the impact of this phenomenon on the CSS performance. In this section, we present some measurement data showing the resulting drift in a shunt. Before presenting these experimental results, however, it is worth briefly reviewing the mechanism by which EM occurs. A thorough analysis of the physics behind it is, however, beyond the scope of this thesis; the interested reader is referred to the many available textbooks and the literature for an in-depth analysis and discussion (e.g., [27–30]).

At temperatures above absolute zero, a fraction of the metal atoms in a metallic lattice gain enough energy to abandon their sites, thereby creating vacancies which other atoms can occupy. In the absence of an external electric field or electric current, these movements are purely random, resulting in a zero net atomic motion. In the presence of an electric current, however, the atomic motion will be influenced by the moving electrons, hence leading to a non-zero atomic flux. In regions where there is a net depletion of atoms, a void can be formed that can give rise to increased resistance and even an open circuit. A net atomic accumulation, on the

other hand, can result in both metal extrusion and a reduced resistance, which in the worst case will short two neighboring metal lines [29]. Such atomic depletion (or accumulation) causes a progressive local tensile (or compressive) stress, which tends to oppose further the translational motion of atoms and to homogenize atom concentrations throughout the interconnect. However, a failure or a prohibitively large drift in resistance value may occur before the two opposing mechanisms reach an equilibrium.

The rate at which EM occurs is a strong function of the current density J and the temperature T [27, 29, 30]; it roughly doubles for every temperature rise of 10 to 15°C, and it is proportional to J^n, where $1 < n < 2$. EM is also influenced by the interconnect topology, metal microstructure, material and its probable impurity [28–32]. In addition, a DC current leads to a maximum EM rate, whereas in an AC or a pulsed current situation, the effective current density J is reduced [33–35]. This is because for repetitive pulsed currents, the metal interconnect can periodically relax and recover from EM effects during the zero-current intervals. The recovery is even more effective for a bidirectional current, in which the currents flowing in opposite directions can (partially) undo each other's EM effect, and thus lead to a lower drift and longer lifetime.

The EM effect on the performance of the CSS with the proposed on-chip shunt resistor has been explored for an accelerated condition of 5 A DC current and at an ambient temperature of 85°C. Three samples were simultaneously tested for 24 days. It should be noted that this condition is unrealistic and was only chosen to accelerate the EM rate. In a real application, the current through the shunt will periodically change direction during the charging and discharging cycle of the battery, thus reducing the EM effect. In addition, portable devices are usually in low-power/stand-by mode, during which the current value and the temperature are significantly lower.

The resulting drift in the current-sensing gain error is plotted in Figure 3.8. Several tests before and after this measurement at both 25°C and 85°C confirm that the drift is solely caused by the drift in R_{shunt}, as no measurable drift was observed in the characteristics of the readout electronics. This plot shows a maximum drift of 0.13% over the course of 24 days, corresponding to a worst-case drift rate of 2.3 ppm/hour.

Considering that the actual circumstances in which a CSS will be used will be significantly less harsh than this measurement, the proposed on-chip shunt can still offer a reliable solution in a wide variety of practical applications. If required, the

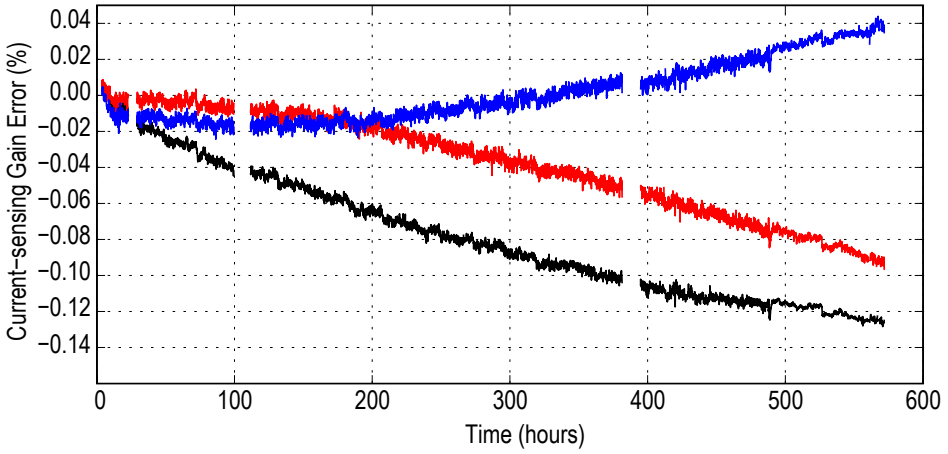

Figure 3.8: Drift in the CSS gain error introduced by the EM effect on R_{shunt} at 5 A DC current and 85°C ambient temperature. The discontinuities in the plots are due to the undesired disruption in the measurement. During the disruptions, however, the 5 A DC current was continuously flowing through the shunt.

drift can be alleviated by: 1) reducing the maximum CSS operating temperature, 2) reducing the maximum current level, or 3) increasing the cross-sectional area of the shunt at the expense of chip area.

3.4. Conclusion

It has been shown that on-die metal layers can be used to realize an on-chip shunt resistor whose temperature can then be accurately sensed by a temperature sensor located directly under it in the silicon substrate. One of the main drawbacks of such shunts, however, is the large silicon area required. This can be circumvented by employing the resistance of the *already available* lead-frame in many *standard* IC packages, e.g., an HVQFN32 plastic package. This costs no extra die area and increases both the shunt's current range and robustness since typical lead-frames are orders of magnitude thicker than on-die metal layers [36, 37].

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4

System-Level Design

The system-level design of the CSS's readout electronics is presented in this chapter. The chosen approach is to explore ways of simplifying the analog portion of the system by means of digital signal processing. It will be shown that, besides simplicity, the main advantage of this approach is to minimize the potential error sources originating from the analog circuitry.

Based on the power budget and accuracy/resolution requirements, possible implementations of the various building blocks are evaluated. Significant error sources of these blocks, together with the solutions employed by prior art, will be discussed. In contrast to prior art, we propose a much simpler solution which essentially only calibrates the non-idealities of the shunt. It is shown that this calibration scheme reduces the effect of many readout electronics' errors to a negligible level without *explicitly* correcting for them.

4.1. Architecture

4.1.1. Generic Block Diagram

Figure 4.1 shows a generic block diagram of a shunt-based CSS. The voltage drop across the shunt resistor V_{shunt} is amplified and then digitized by an ADC. Alternatively, the amplifier can be eliminated and V_{shunt} can be directly interfaced with the ADC. The ADC is provided with a reference voltage V_{Ref}, while a tem-

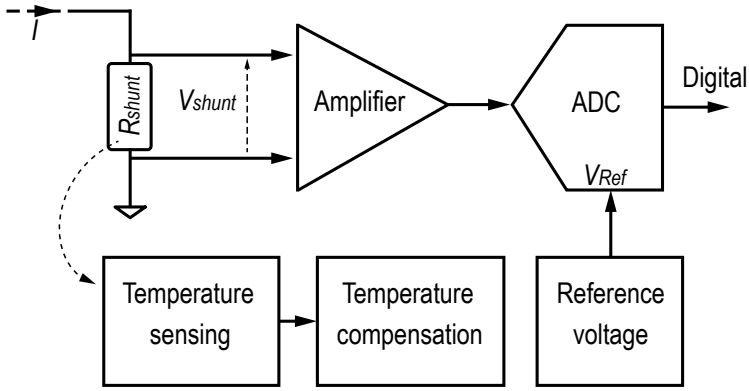

Figure 4.1: A generic block diagram of a shunt-based CSS.

perature sensor measures the shunt's temperature T, in order to compensate for its TCR.

To achieve the targeted current-sensing gain error of better than ±0.5% (Table 1.1), the error introduced by each building block should be much lower than this, e.g., better than ±0.1%. This translates into 1) a gain error of ±0.1% for the amplifier and for the ADC, 2) a spread of ±0.1% for V_{Ref}, and 3) a temperature sensing error of ±0.1% / TCR ≈ ±0.3°C.

The current-sensing resolution σ_I is limited by the resolution of the voltage sensing σ_V and that of the temperature sensing σ_T. In order to achieve the targeted 14-bit current-sensing resolution within a conversion time of 25 ms (Table 1.1), we must ensure that the voltage-sensing ADC also achieves similar resolution. The requirements on the temperature-sensing resolution depend on the actual implementation of the temperature compensation scheme and will be discussed in Section 4.3.

4.1.2. Amplifier and ADC

Trading conversion time for resolution, delta-sigma (ΔΣ) ADCs are the best candidates for digitizing slowly-varying signals with high resolution (e.g., > 12 bits) [1]. By over-sampling their input signals, ΔΣ ADCs allow the use of precision techniques such as dynamic element matching (DEM) and chopping, hence facilitating the accurate digitization of V_{shunt}.

Since switched-capacitor (SC) implementations of ΔΣ ADCs generally achieve higher accuracy than their continuous-time (CT) counterparts [2], we select a SC ΔΣ ADC for use in this work. Unlike CT implementations, the coefficients of a SC filter solely depend on capacitor ratios and are independent of clock frequency and

robust to process variation. This enables a robust loop filter implementation that does not require calibration to ensure modulator stability.

CT $\Delta\Sigma$ ADCs, on the other hand, are attractive due to their inherent anti-aliasing filtering capability and their relatively lower power consumption (typically 2 to 4 times) [2]. Since V_{shunt} is directly sampled in our proposed architecture, aliasing occurs and harmonics at sampling frequencies are folded back to DC, which can potentially cause errors in the estimated SoC. Experimental results, however, suggest that aliasing has a negligible effect on SoC estimation [3], and therefore, is not a major concern. Also, as will be shown in the following chapters, the power consumption of the entire CSS with SC $\Delta\Sigma$ ADCs can be kept well below the power budget (50 μA, see Table 1.1). Thus there is no strong motivation for using a CT $\Delta\Sigma$ ADC at the expense of accuracy and loop filter stability.

In contrast to [4, 5], we have chosen to directly digitize V_{shunt} without any pre-amplification or an *analog* temperature compensation scheme. The reasons for these choices are as follows:

1. Besides simplicity, reducing the number of analog components in the signal chain helps to exclude potential error sources; a pre-amplifier inevitably introduces additional offset and gain error. For instance, in [4, 5], the effect of the lead-frame's large TCR ($\sim 0.335\%/^\circ\text{C}$) is addressed by amplifying V_{shunt} with a gain that is designed to have an equal-but-opposite temperature coefficient. However, the resulting gain error is still significant ($> \pm 5\%$) over the temperature range from -40°C to $+85^\circ$C [5].

2. Since V_{shunt} is quite small, the ADC's integrators can be implemented with *simple and energy-efficient current-reuse* OTAs. As explained in Chapter 6, these OTAs offer small output voltage swing, thus amplifying V_{shunt} would obstruct their use.

4.1.3. Temperature Sensor and Reference Voltage

In Chapter 3, we argued that in order to reduce the complexity of the analog circuitry and to eliminate the associated errors, digital temperature compensation should be used in this work. This involves digitizing the temperature of the shunt and then performing a polynomial correction on the digitized value of V_{shunt}. This can best be achieved by a BJT-based temperature sensor, since these are the most accurate reported to date [6–8]. After a single-point trim, they can achieve an inaccuracy as low as $\pm 0.06^\circ$C from -70°C to $+125^\circ$C [8, 9]. As will be discussed

later in this chapter, they can also satisfy the resolution requirement within the given power budget (Table 1.1).

The required reference voltage V_{Ref} for V_{shunt} digitization can be generated from either BJT- [10–13] or CMOS-based designs [14, 15]. The former have shown to be more accurate than the latter. With only a single-point trim, BJT-based references achieve state-of-the-art 3σ inaccuracy ranging from $\pm 0.03\%$ to $\pm 0.15\%$ [10–13], while MOS-based designs can only achieve an inaccuracy of about $\pm 0.3\%$ (min-max) even with a two-point trim [14, 15].

In conclusion, the bipolar transistors available in standard CMOS process will be used for both generating V_{Ref} and sensing temperature in this work. As an additional benefit, one bipolar core can be used for both purposes [10, 12], which in turn, helps to reduce the design and the calibration complexity as well as the power consumption.

4.1.4. Proposed Architecture

Figure 4.2 depicts a block diagram of the CSS's readout electronics which consist of a bandgap reference (BGR), ADC(s), and a digital backend unit. Figure 4.2(a) shows the first prototype (presented in Chapter 5), which uses a single ADC for both current I and temperature T measurement. To do so, the ADC is operated in incremental mode and is time-multiplexed: with conversion times of 22.5 ms for I and 2.5 ms for T. The reasons for this time-multiplexing choice are:

1. Sensing temperature at 25-ms intervals is expected to be fast enough to compensate for self-heating and ambient temperature changes. This was verified by measurements of actual current transients (see Chapter 5).

2. Most of the time, the system should be configured for current sensing.

A temperature-averaging scheme (TAS) uses the average of two successive T measurements to compensate for each I measurement, resulting in improved accuracy, especially when a current pulse causes dynamic self-heating in the shunt.

As shown in Figure 4.2(b), even better performance could be achieved by using two separate ADCs for I and T (presented in Chapter 6). In this improved prototype, ADC_I digitizes V_{shunt} with respect to the BGR voltage V_{Ref}, and ADC_T uses the BGR's PNPs to sense the shunt's temperature T. Calibration and shunt temperature compensation are performed in the digital backend. Detailed descriptions of these building blocks are presented in the following sections.

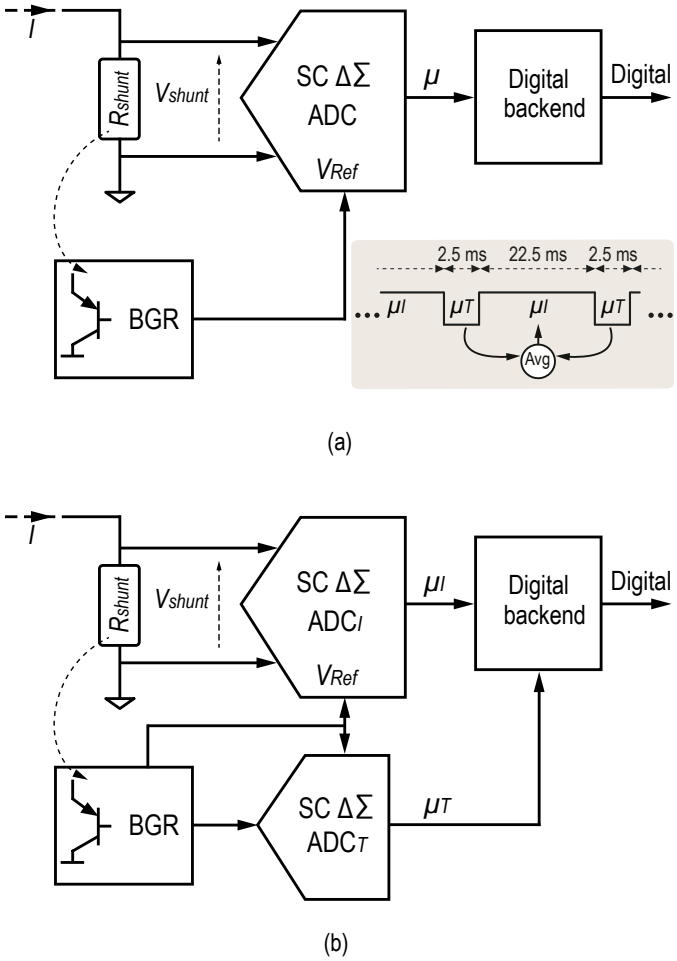

Figure 4.2: Block diagram of the proposed current-sensing system, with (a) a shared time-multiplexed ADC and, (b) dedicated ADCs for I- and T-sensing.

4.2. Bandgap Reference

The operating principle of the bandgap reference (BGR) is presented in this section. Since bipolar transistors are the key components of a BGR, a brief review of their operation and non-idealities will be given. The discussion on the physics of the bipolar transistor is, however, kept relatively simple and restricted to the level needed for our system-level design; for an in-depth analysis, the reader is referred to [1, 16, 17].

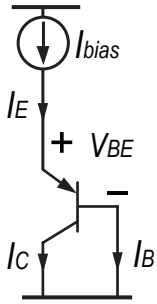

Figure 4.3: A diode-connected substrate PNP transistor.

4.2.1. Bipolar Transistor in CMOS Technology

Standard CMOS processes offer bipolar transistors as parasitic devices. There are two types of these devices available in N-well CMOS technology: substrate or vertical PNP transistors, and lateral PNP transistors [1]. Compared to vertical PNPs, lateral PNPs are more sensitive to process spread [1, 17] and mechanical stress [18], and exhibit more non-idealities in their voltage-current relationship [1, 17, 19]. As a result, substrate PNPs are preferred for use in BGRs and in temperature sensors [1].

4.2.2. Substrate PNP Transistor

The collector terminal of a substrate PNP is formed by the substrate, and hence is grounded. In order to minimize non-idealities, such as base-collector leakage current and Early effect, its base terminal is also tied to ground [1]. Figure 4.3 shows a substrate PNP which is biased via its emitter terminal at I_{bias}. The absolute value of the base-emitter voltage V_{BE} of this PNP transistor, operating in the forward-active region, is written as[1]

$$V_{\text{BE}} = \frac{kT}{q}\ln\Big(\frac{I_C}{I_S}+1\Big) \approx \frac{kT}{q}\ln\Big(\frac{I_C}{I_S}\Big) \qquad (I_S \ll I_C) \tag{4.1}$$

in which, k is Boltzmann's constant, T is the absolute temperature, q is the electron charge, I_C is the PNP's collector current, and I_S is its saturation current. Due to the strong temperature dependency of I_S, V_{BE} is temperature dependent with a coefficient of around -2 mV/°C. The exact value is determined by the absolute

[1]Strictly speaking, for a PNP transistor, the emitter-base voltage $V_{\text{EB}} = -V_{\text{BE}}$ is described by this equation. However, in order to be able to use same set of equations for both NPN and PNP transistors, literature on CMOS temperature sensors and bandgap references typically use V_{BE}.

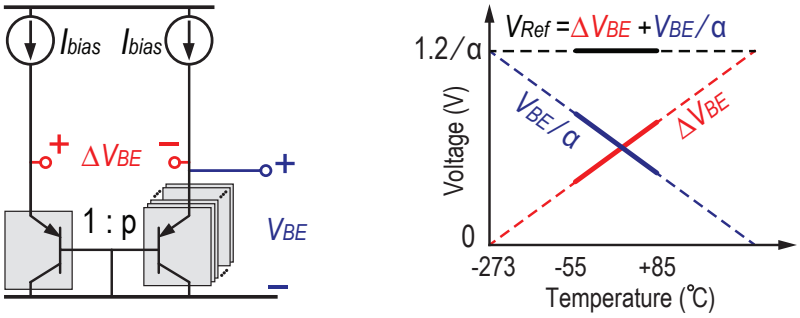

Figure 4.4: Simplified view of the BGR with PTAT, CTAT and reference voltages over temperature.

values of I_C and I_S. The extrapolated value of V_{BE} at 0 K is determined by the silicon bandgap energy and is $V_{g0} \approx 1.2$ V [20]. Decreasing with temperature, V_{BE} is referred to as a complementary-to-absolute-temperature (CTAT) voltage.

The difference between the base-emitter voltages of two PNPs, biased at a 1:p collector current density ratio, can be easily obtained from (4.1):

$$\Delta V_{\mathrm{BE}} = \frac{kT}{q} \ln(p). \tag{4.2}$$

which is a proportional-to-absolute-temperature (PTAT). Being only dependent on the physical constants and on the ratio p, ΔV_{BE} can potentially provide an accurate measurement of temperature [21]. Its temperature coefficient approximately varies from 140 μV/°C to 240 μV/°C for p ranging from 5 to 16.

4.2.3. Operating Principle

As discussed in the previous sections, the function of the bandgap reference (BGR) is both to provide the ADCs' reference voltage V_{Ref} and to sense the temperature T required for the shunt's temperature compensation scheme. In addition, it must operate from a minimum supply voltage of 1.35 V (the specified range is 1.5 V ± 10%). Due to these constraints, we opted for a dynamic BGR design [10, 22–24]. As shown in the simplified diagram of Figure 4.4, the BGR is designed to only generate a CTAT voltage V_{BE} and a PTAT voltage ΔV_{BE} from a pair of substrate PNPs biased at a 1:p current-density ratio. As will be explained, p is equal to 16 and 10 in the prototype chips described in Chapter 5 and 6, respectively. These voltages are then sampled and linearly combined at the input switched-capacitor sampling branch of the two ADCs to generate a dynamic reference voltage:

$$V_{\mathrm{Ref}} = \Delta V_{\mathrm{BE}} + \frac{V_{\mathrm{BE}}}{\alpha} \approx \frac{1.2V}{\alpha}, \tag{4.3}$$

where the weighting factor α is chosen such that the temperature dependency of these two voltages cancel each other and, as a result, V_{Ref} becomes temperature-independent. The factor α depends on the ratio p and is approximately equal to 8 and 10 for $p = 16$ and 10, respectively[2]. This results in reference voltages of 150 mV and 120 mV. This is compatible with V_{shunt}, which is typically in the order of tens of millivolts even as R_{shunt} varies over process and temperature. Digitizing V_{shunt} against V_{Ref}, ADC_I produces a digital output:

$$\mu_I = \frac{V_{\mathrm{shunt}}}{V_{\mathrm{Ref}}} = \frac{R_{\mathrm{shunt}}(T) \cdot I}{V_{\mathrm{Ref}}}. \tag{4.4}$$

In order to obtain the temperature information, ADC_T digitizes ΔV_{BE} with respect to V_{Ref}:

$$\mu_T = \frac{\Delta V_{\mathrm{BE}}}{V_{\mathrm{Ref}}}. \tag{4.5}$$

The temperature T in degrees Celsius can then be calculated by linearly scaling μ_T [6]:

$$T = A \cdot \mu_T - B \tag{4.6}$$

in which, $A \approx 623$ and $B \approx 273$.

Having briefly reviewed the basic principles of the substrate PNPs and the BGR circuitry, we will introduce the PNP non-idealities and its impact on the system performance in the section.

4.2.4. Non-idealities

PNP non-idealities introduce errors in both V_{Ref} and the temperature sensor, thus impairing current-sensing accuracy. In order to develop an effective calibration process to mitigate the effects of such errors, the important non-idealities will be briefly reviewed, together with solutions from literature. For in-depth reviews of bipolar transistor non-idealities, the interested reader is referred to the many available textbooks and the literature (e.g., [1, 16, 17]).

[2]This is described in more detail in Chapter 5 and 6, respectively.

Spread in Saturation Current

Mainly due to the tolerance in the base doping concentration and dimensions of the PNP, the saturation current I_S exhibits a spread ΔI_S [1]. This causes an error in V_{BE}:

$$\begin{aligned} V_{\mathrm{BE}} &= \frac{kT}{q}\ln\Big(\frac{I_C}{I_S+\Delta I_S}\Big) = \frac{kT}{q}\ln\Big(\frac{I_C}{I_S}\Big) - \frac{kT}{q}\ln\Big(1+\frac{\Delta I_S}{I_S}\Big) \\ &\approx \frac{kT}{q}\ln\Big(\frac{I_C}{I_S}\Big) - \frac{kT}{q}\,\frac{\Delta I_S}{I_S} \qquad (\Delta I_S \ll I_S) \end{aligned} \tag{4.7}$$

As described in [1], the relative spread $\Delta I_S/I_S$ is nearly temperature-independent, resulting in a PTAT error in V_{BE} and hence in V_{Ref} [21]. This error can be significantly reduced by performing a single PTAT trim at room temperature [21]. This has been done in several ways by:

1. adjusting the emitter area or bias current of the PNP by means of binary-scaled components [21],
2. trimming the bias current by using a $\Delta\Sigma$ DAC to obtain high trimming resolution [6], or
3. digitally adding a PTAT correcting term to V_{BE} [1, 7–9].

As will be explained in Section 4.4, ΔI_S, is not explicitly corrected in this work; its effect is absorbed during the calibration of the shunt and so is significantly suppressed.

V_{BE} Curvature

The saturation current I_S is a strong and non-linear function of the absolute temperature:

$$I_S(T) = CT^{\eta} exp\Big(\frac{-qV_{g0}}{kT}\Big) \tag{4.8}$$

where C is a constant and $\eta \approx 4$ [1, 17]. As a result of this temperature dependency, V_{BE} becomes slightly non-linear over temperature [17]:

$$V_{\mathrm{BE}}(T) = V_{g0} - \lambda T + c(T) - c(0) \tag{4.9}$$

in which, λ is the slope of V_{BE} at a reference temperature T_r, and $c(T)$ represents the non-linearity or curvature. Assuming that the PNP's bias current exhibits a temperature dependency as $I_{\mathrm{bias}} \propto T^m$, this curvature can be written as [1, 17]:

$$c(T) = \frac{k}{q}(\eta - m)\Big(T - T_r - T\ln\Big(\frac{T}{T_r}\Big)\Big). \tag{4.10}$$

This curvature is roughly parabolic and can amount to several millivolts over the military temperature range (−55°C to +125°C) [1, 19].

Various techniques have been developed to reduce the effect of $c(T)$. In [1], Pertijs presentes an excellent summary and comparison of these techniques. We briefly discuss some of them.

One way of minimizing $c(T)$ is by adjusting the temperature dependency of the BJT's bias current I_{bias}. By means of a translinear loop implemented in a BiCMOS process [25], $I_{\mathrm{bias}} \propto T^m$ can be generated, where $3 < m < 4$. The design reported in [26] proposes to null the second-order curvature by adjusting the temperature dependency of a biasing resistor. This is done by properly combining two resistors with different TCRs and trimming them to tackle their spread.

An alternative technique is to implement a temperature-dependent gain (applied to ΔV_{BE}) using the ratio of resistors with different TCRs [27–29]. This, however, requires the resistors to be trimmed. This approach has also been implemented in a digitally assisted way, in which the output of a digital temperature sensor is used to control a resistive DAC [30].

Another approach is to add a compensating voltage to V_{Ref} with an opposing curvature. This compensating voltage can be generated 1) from a weak inversion-biased MOS [31], 2) with a temperature-dependent weighted linear combination of V_{BE} and ΔV_{BE}, in which, the operating temperature range can be divided into several segments in a piecewise linear way,[32], or 3) by means of a temperature-dependent current density ratio p [11, 33–35].

Another way of reducing $c(T)$ is to include a temperature sensor to obtain the die temperature, and then digitally correct for curvature via a lookup table [10] or a polynomial function [13, 22].

In this work, however, the effect of V_{Ref} curvature is absorbed during the calibration of the shunt and so is significantly suppressed (see Section 4.4).

Finite Current Gain β_F

Since substrate PNPs are biased via their emitter terminals, their finite common-emitter current gain β_F influences the collector current I_C:

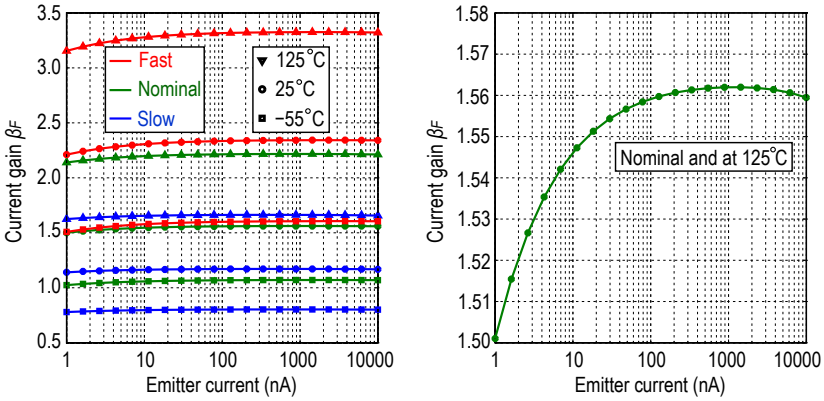

Figure 4.5: Simulated value of current gain β_F of the PNP in the process used. The emitter area of the PNP is 10 μm^2.

$$I_C = \frac{\beta_F}{\beta_F + 1} I_E \tag{4.11}$$

and hence V_{BE} is:

$$V_{\mathrm{BE}} = \frac{kT}{q} \ln\Big(\frac{I_{\mathrm{bias}}}{I_S} \frac{\beta_F}{\beta_F + 1}\Big). \tag{4.12}$$

Changing with I_{bias}, T and process variations, the finite β_F leads to a spread in V_{BE}. In addition, it can also impair the accuracy of ΔV_{BE}, as the two PNPs may have different β_F because they operate at different current density. The simulated value of β_F for a PNP in the process used, with an emitter area of 10 μm^2, is plotted in Figure 4.5. It shows a significant variation (from 0.75 to 3.4) over I_{bias}, T and process corners.

One way to reduce the effect of finite current gain β_F is to sense the PNP's base current I_B, and then, in a feedback loop, regulate its I_E such that the collector current I_C is at the desired level [25]. In another approach, the base current of an auxiliary PNP is added to the emitter current of the main PNP [36]. This helps to boost the effect current gain to $\beta_F(\beta_F + 2)$. A much simpler and more effective technique is to generate a bias current that is $(\beta_F + 1)/\beta_F$ times larger than the intended PNP's I_C [1]. This will be explained in more detail in the following section.

Spread in Current Density Ratio

The spread in I_{bias} (due to current-mirror mismatch) and I_S of the two PNPs leads to an error Δp in their current density ratio p. This, in turn, modifies ΔV_{BE}:

$$\Delta V_{\mathrm{BE}} = \frac{kT}{q}\ln(p+\Delta p) \approx \frac{kT}{q}\ln(p) + \frac{kT}{q}\frac{\Delta p}{p} \qquad (\Delta p \ll p). \tag{4.13}$$

The relative error $\Delta p/p$ can be assumed to be temperature-independent [1]. This results in a PTAT error in ΔV_{BE}.

This error can be suppressed by using dynamic element matching (DEM) [1, 6, 7, 21]. in [1], Pertijs shows that, in a complete DEMing cycle, the first-order effect of this error term can be cancelled and the residual second-order error will be upper-bounded by $(kT/q)(\Delta p/p)^2/2$. For instance, a large spread of $\Delta p/p = 1\%$ leads to a residual error of less than 130 nV in ΔV_{BE} at room temperature. For $p = 10$, the resulting error in V_{Ref} and in the temperature sensor will be less than 0.00011% and 0.01°C, respectively.

As will be explained in Section 4.4, the spread in p, is not explicitly corrected in this work; its effect is absorbed during the calibration of the shunt and so is significantly suppressed.

4.2.5. Proposed Design

So far we have reviewed the fundamentals of substrate PNPs, the effect of their non-idealities and the solutions proposed by prior art. The basics of the BGR and the temperature sensor have also been introduced. In this section, a simplified circuit diagram of the BGR together with simulation results over temperature and process variations will be presented. The latter allows the relative effect of different error sources to be evaluated, which will be helpful in establishing an effective calibration scheme.

Figure 4.6 shows a simplified circuit diagram of the BGR, consisting of a bias circuit and a bipolar core [1]. The bias circuit generates a PTAT current I_{bias} with the help of an opamp and two auxiliary PNPs, which are also biased at a 1:p current-density ratio:

$$I_{\mathrm{bias}} = \frac{\Delta V_{\mathrm{BE,bias}}}{R} \qquad (R_\beta = 0). \tag{4.14}$$

This current is mirrored to the bipolar core and used to bias two PNPs at equal emitter currents to generate V_{BE} and ΔV_{BE}.

In [1], it has been shown that by adding a resistor in series with the base terminal of the biasing PNP (Figure 4.6), the β_F-dependency of V_{BE} can be eliminated as the bias current is then:

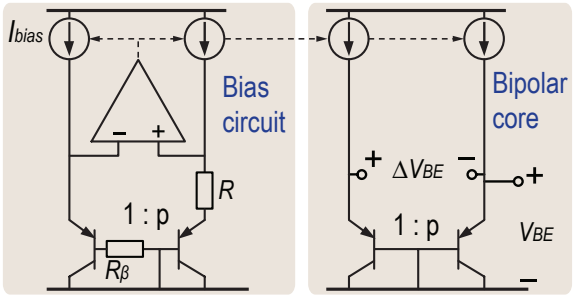

Figure 4.6: Simplified view of the BGR consisting of a PTAT bias current generator and a bipolar core.

$$I_{\text{bias}} = \frac{\beta_F + 1}{\beta_F} \frac{\Delta V_{\text{BE,bias}}}{R} \qquad (R_\beta = R). \tag{4.15}$$

Assuming that the two BJTs have the same β_F, this bias current ensures that the BJTs' collector current $I_C = \Delta V_{\text{BE}}/R$.

The simulation results of such a BGR, with $p = \alpha = 10$ and $R = 230$ kΩ which results in $I_{\text{bias}} = 260$ nA at room temperature, are shown in Figure 4.7. It is assumed that the current sources and the PNPs are dynamically matched and hence p does not spread. It can be seen that, for both $R_\beta = 0$ and $R_\beta = R$, V_{Ref} suffers from process spread, which can be up to ±1% if no trimming is used. This is mainly due to the spread in the saturation current I_S, leading to a large spread in V_{BE}. Also due to the curvature of V_{BE}, V_{Ref} exhibits a corresponding curvature of about ±0.2%.

When β_F-compensation is enabled ($R_\beta = R$), this PTAT spread can be significantly suppressed by performing a single PTAT trim at room temperature [21]. This reduces the spread down to ±0.01%, with almost constant curvature over the process corners[3] (see Figure 4.7). This observation is in close agreement with the theory presented in Section 4.2.4. The resulting reference voltage when using the β_F-compensation technique can then be obtained by combining (4.3) and (4.9), and by assuming a first-order temperature compensation between V_{BE} and ΔV_{BE}

[3] Measurements of three different batches revealed that the curvature has less than ±0.03% variation [22, 23, 37]. This assertion is also supported by much larger data sets obtained from a precision bandgap reference implemented in the same process [13].

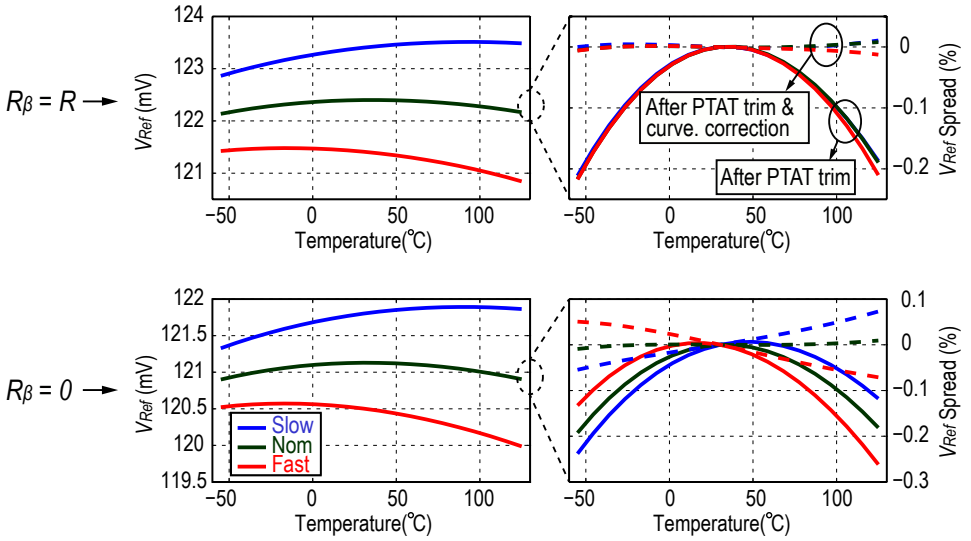

Figure 4.7: Corner simulations of V_{Ref} and its spread before (left) and after (right) PTAT trimming and curvature correction, with (top) and without (bottom) β_F-compensated I_{bias}.

$$V_{\mathrm{Ref}}(T) = \Delta V_{\mathrm{BE}} + \frac{V_{\mathrm{BE}}}{\alpha} \approx \frac{V_{g0}}{\alpha}\left(1 + \delta\frac{T}{T_c}\right) + \frac{c(T) - c(0)}{\alpha}$$
$$= V_{\mathrm{Ref0}}\left(1 + \delta\frac{T}{T_c}\right) + \frac{c(T) - c(T_c)}{\alpha} \tag{4.16}$$

where V_{Ref0} is the nominal value of V_{Ref} measured at room temperature T_c, and δ represents the PTAT error term measured at T_c. After compensating for the curvature by means of a fixed second-order polynomial, the total error of V_{Ref} reduces to $< \pm 0.01\%$.

Without the β_F-compensation technique ($R_\beta = 0$), the resulting spread in V_{Ref} is not fully PTAT. This is mainly due to the temperature-dependency of β_F [1, 6]. As shown in Figure 4.7, after applying a PTAT trim and a second-order curvature correction, the spread is now limited to $\pm 0.06\%$. In fact, simulation indicates that the spread is a linear function of temperature, which requires two-point trimming in order to be suppressed to below $\pm 0.01\%$. As a result, the reference voltage can be empirically expressed as

$$V_{\mathrm{Ref}}(T) \approx \frac{V_{g0}}{\alpha}\left(1+\delta_0+\delta_1\frac{T}{T_c}\right)+\frac{c(T)-c(0)}{\alpha}$$
$$= V_{\mathrm{Ref0}}\left(1+\delta_0+\delta_1\frac{T}{T_c}\right)+\frac{c(T)-c(T_c)}{\alpha} \tag{4.17}$$

in which, δ_0 and δ_1 represent the linear spread in V_{BE}, and hence also in V_{Ref}.

4.3. ADC

The operating principles of ADC_I and ADC_T are presented in this section. The resolution requirement of each ADC determines the size of the input sampling capacitors, the order of the loop filters and the sampling frequency.

4.3.1. Operating Principle

Figure 4.8 shows a simplified single-ended diagram of both ADC's first integrators. In ADC_I, capacitor C_{S1} samples V_{shunt}, while the capacitors $C_{S2} = C_{S1}$ and C_{S3} $(= C_{S2}/\alpha)$ sample $\pm\Delta V_{\mathrm{BE}}$ and $\pm V_{\mathrm{BE}}$, respectively. The sampled voltages are then accurately combined in the charge domain to generate the voltage V_{Ref} [22, 23, 37]. The modulator's feedback is established by using the output bit-stream bs_I to control the polarity of the feedback voltages $\pm\Delta V_{\mathrm{BE}}$ and $\pm V_{\mathrm{BE}}$. This conversion results in an output bit-stream bs_T with an average value μ_I:

$$\mu_I = \frac{C_{S1}\cdot R_{\mathrm{shunt}}(T)\cdot I}{C_{S2}\cdot\Delta V_{\mathrm{BE}}+C_{S3}\cdot V_{\mathrm{BE}}} = \frac{R_{\mathrm{shunt}}(T)\cdot I}{V_{\mathrm{Ref}}} = \frac{V_{\mathrm{shunt}}}{V_{\mathrm{Ref}}}. \tag{4.18}$$

To determine the temperature T, the input sampling capacitors C_{S4} and C_{S5} in ADC_T perform charge balancing[4]. When bs_T is 0, C_{S4} samples $+\Delta V_{\mathrm{BE}}$ and when bs_T is 1, C_{S5} $(= C_{S4}/\alpha)$ samples $-V_{\mathrm{BE}}$. This results in an average value of bs equal to:

$$\mu_T = \frac{C_{S4}\cdot\Delta V_{\mathrm{BE}}}{C_{S4}\cdot\Delta V_{\mathrm{BE}}+C_{S5}\cdot V_{\mathrm{BE}}} = \frac{\Delta V_{\mathrm{BE}}}{V_{\mathrm{Ref}}}. \tag{4.19}$$

The temperature T in degree Celsius can then be calculated using the linear relation given in (4.6).

[4] In the single-ADC architecture, the sampling switches connected to C_{S1} are disabled, while the capacitors C_{S2} and C_{S3} perform the charge balancing.

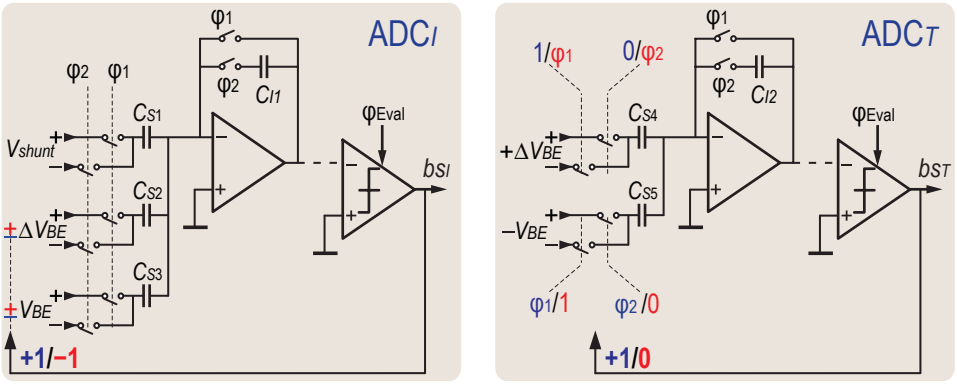

Figure 4.8: A simplified singled-ended digram of ADC_I and ADC_T's first integrators and feedback loop.

4.3.2. Resolution

As explained in Chapter 2, current sensing is performed by dividing the measured shunt voltage V_{shunt} by the temperature-compensated shunt value

$$I = \frac{V_{\text{shunt}}}{R_{\text{shunt}}(T)}. \tag{4.20}$$

The current-sensing resolution σ_I can be expressed in terms of both the voltage-sensing resolution σ_V and the temperature-sensing resolution σ_T as:

$$\sigma_I^2 = \left(\frac{\partial I}{\partial V_{\text{shunt}}}\right)^2 \cdot \sigma_V^2 + \left(\frac{\partial I}{\partial T}\right)^2 \cdot \sigma_T^2. \tag{4.21}$$

Assuming a first-order temperature dependency of R_{shunt}:

$$R_{\text{shunt}}(T) = R_{\text{shunt}}(T_0) \cdot \Big(1 + \alpha_1 \cdot \Delta T\Big), \tag{4.22}$$

in which, $\Delta T = T - T_0$, σ_I can be written as

$$\sigma_I^2 = \left(\frac{1}{R_{\text{shunt}}(T)}\right)^2 \cdot \sigma_V^2 + \left(I \cdot \frac{\alpha_1}{1 + \alpha_1 \cdot \Delta T}\right)^2 \cdot \sigma_T^2. \tag{4.23}$$

Although, the worst-case σ_I occurs at the lowest temperature and the highest current level, the resolution requirement during calibration is the most stringent – 14-bit current sensing resolution at a 3A calibration current and at ambient

room temperature. Assuming $R_{\text{shunt}} = 8.5\ \text{m}\Omega$[5] at room temperature with 20°C self-heating at 3A, and $\alpha_1 = 0.35\%/°\text{C}$, σ_I during the calibration process can be written as:

$$\begin{aligned}\sigma_I &= \sqrt{\left(\frac{1}{9.1\ \text{m}\Omega}\right)^2 \cdot \sigma_V^2 + \left(3\ \text{A} \cdot \frac{0.35\%/°\text{C}}{1 + 0.35\%/°\text{C} \times 20°\text{C}}\right)^2 \cdot \sigma_T^2} \\ &\approx \sqrt{(110\ \Omega^{-1})^2 \times \sigma_V^2 + (0.009\ \text{A}/°\text{C})^2 \times \sigma_T^2} \end{aligned} \tag{4.24}$$

In order to provide 14-bit current-sensing resolution in a 25 ms conversion time, we must ensure that $\sigma_V < 2\ \mu\text{V}$ and $\sigma_T < 24\ \text{mK}$ (assuming the same contribution of σ_V and σ_T in σ_I).

The resolution of a $\Delta\Sigma$ ADC is limited by its thermal and quantization noise. For a given conversion time, the input-referred thermal noise of a SC $\Delta\Sigma$ ADC is dominated by the value of its first integrator's sampling capacitors (kT/C-noise) and the modulator's sampling frequency F_S, while its quantization noise is determined by the order of its loop filter L, quantizer's number of bit n, and F_S [1, 2, 38].

Pertijs in [1] and Schreier in [2, 38] present a detailed design-oriented estimation of the thermal noise and the quantization noise in SC $\Delta\Sigma$ ADCs. After some simplifying assumptions, the results of these calculations are applied to ADC_I and ADC_T in the following subsections.

4.3.3. ADC_I Thermal Noise Estimation

The input-referred thermal noise of ADC_I is mainly determined by that of the first integrator's OTA, of the switches' on-resistance R_{on} and of the BGR. These noise sources result in a charge noise across the input sampling capacitors and then are sampled at the end of each clock phase ϕ_1 and ϕ_2. In an energy-efficient design, R_{on} is chosen to be much smaller than the inverse of the OTA's transconductance. This is to ensure that the settling of the sampling capacitors is dominated by g_m, which determines the ADC's power consumption. Under the condition $R_{\text{on}} \ll g_m^{-1}$, the switches can be disregarded in our noise calculation [1, 2, 38]. To further sim-

[5] This is after considering that R_{shunt} spreads by ±15% and that σ_I is worse at the lower shunt value. It should also be mentioned that this calculation is only performed for a CSS employing the on-chip metal shunt resistor. The 260-$\mu\Omega$ lead-frame resistor is not considered optimal for ±5A current-sensing as it leads to unrealistically stringent requirements on ADC_I's offset and resolution; in this work, it is only used to demonstrate high-current capability.

plify the analysis, the PNPs can also be ignored. This is because besides introducing noise, the PNPs also limit the thermal-noise bandwidth (due to the resistance seen from their emitter terminals), and hence eliminating the PNPs from the noise analysis leads to a minor error in the calculated integrated noise [1]. The OTA's flicker noise can also be ignored as it is suppressed by means of the correlated double-sampling technique (see Chapter 5).

The power spectral density (PSD) of the OTA's input-referred noise can be written as

$$S_{Vn,OTA}(f) = \frac{16kT}{3g_m}\left(1 + \frac{g_{m,X}}{g_m}\right) = \frac{16kT}{3g_m}\xi, \tag{4.25}$$

in which, g_m is the transconductance of the OTA's input differential pair, while $g_{m,X}$ represents the thermal noise contribution of the other pairs, the value of which depends on the implementation of the OTA. In addition, $\xi = (1 + g_{m,X}/g_m)$, is the noise figure of the OTA.

The total charge noise sampled by the three sampling capacitors in one clock period (consisting of two sampling phases) of ADC$_I$ can be estimated as [38]:

$$q_{n,I} = \sqrt{2 \cdot \frac{4kT}{3}\xi \cdot \left(C_{S1} + C_{S2} + C_{S3}\right)}. \tag{4.26}$$

The total signal charge sampled in N clock cycles is

$$q_I = 2N \cdot C_{S1} \cdot V_{\text{shunt}} = G \cdot V_{\text{shunt}}. \tag{4.27}$$

The input-referred rms noise of ADC$_I$ in N clock periods is therefore

$$\sigma_V = \frac{\sqrt{N} \cdot q_{n,I}}{G} = \sqrt{\frac{1}{N}\frac{2\xi}{3}\frac{kT}{C_{S1}}\left(1 + \frac{C_{S2} + C_{S3}}{C_{S1}}\right)}. \tag{4.28}$$

This expression can be simplified by taking into account that $C_{S2} = C_{S1}$ and $C_{S3} \ll C_{S1}$. In addition, N can be expressed in terms of the conversion time T_{conv} and the sampling clock frequency F_S of ADC$_I$:

$$N = T_{\text{conv}} \cdot F_S, \tag{4.29}$$

therefore,

$$\sigma_V \approx \sqrt{\frac{4\xi}{3}\frac{kT}{C_{S1}F_S}\frac{1}{T_{\text{conv}}}}. \tag{4.30}$$

Note that noise analysis for a fully differential topology would yield to same expression (see (22) and (33) in [38]).

4.3.4. ADC$_T$ Thermal Noise Estimation

In [1], Pertijs calculates the resulting standard deviation in μ_T due to the sampled thermal noise during N clock periods as

$$\sigma_{\mu_T} = \frac{\sqrt{N}\cdot q_{n,T}}{N\cdot\left(Q_{\Delta V_{\text{BE}}} + Q_{V_{\text{BE}}}\right)}. \tag{4.31}$$

in which, $q_{n,T}$ is the sampled noise charge by the input sampling capacitors, while $Q_{\Delta V_{\text{BE}}}$ and $Q_{V_{\text{BE}}}$ are the signal charge sampled by C_{S4} and C_{S5}, all in one clock period. By ignoring the PNPs, $q_{n,T}$ can be written:

$$q_{n,T} = \sqrt{\frac{8kT}{3}\xi\cdot\left(C_{S4}+C_{S5}\right)} \approx \sqrt{\frac{8kT}{3}\xi\cdot C_{S4}}. \tag{4.32}$$

The sampled charge signal are:

$$Q_{\Delta V_{\text{BE}}} = 2C_{S4}\cdot\Delta V_{\text{BE}}, \qquad \text{and} \qquad Q_{V_{\text{BE}}} = 2C_{S5}\cdot V_{\text{BE}}. \tag{4.33}$$

Substituting (4.29), (4.32) and (4.33) in (4.31) yields the resulting output-referred temperature noise:

$$\sigma_T \approx A\cdot\frac{\alpha}{V_{g0}}\sqrt{\frac{8\xi}{3}\frac{kT}{C_{S4}F_S}\frac{1}{T_{\text{conv}}}}. \tag{4.34}$$

Equations (4.30) and (4.34) suggest that, for a given T_{conv}, the effect of the thermal noise can be reduced by increasing either the sampling capacitors or the sampling frequency F_S, both of which lead to a proportional increase in power consumption. For instance, reducing the effect of thermal noise by 2× entails a 4× increase in power consumption.

4.3.5. Quantization Noise

In an energy-efficient ΔΣ ADC design, resolution is mainly determined by thermal noise rather than by quantization noise. This is because reducing the former leads to a quadratic increase in the ADC's power consumption, while the latter can be mitigated by increasing the order of the modulator's loop filter L, its quantizer's number of bit n, or slightly increasing F_S [1, 2, 38], all of which come at the expense of a minor increase in power consumption. To sufficiently suppress the quantization error, the design parameters are determined based on the following observations:

- **Quantizer's number of bits n**: Quantization noise can be proportionally suppressed by increasing the number of bits n. However, a single-bit quantizer ($n = 1$) is attractive because it is simple and linear: 1) the quantizer is realized with a single comparator, 2) it can be combined with an inherently linear single-bit DAC, which in contrast to multi-bit DAC, needs no data-weighted averaging (DWA) to cope with DAC non-linearity [2]. A single-bit quantizer ADC is therefore considered for use in this work.

- **Order of the loop filter L**: A modulator with a first-order loop filter ($L = 1$) and a 1-bit quantizer is prone to idle tones, especially for DC inputs; high-energy tones can appear in the signal bandwidth and corrupt the signal quality [2]. In addition, the detection limit of a first-order modulator $\epsilon_{\Delta\Sigma,1}$ is ultimately limited by the DC gain of the integrator's OTA A_0 [1]

$$\epsilon_{\Delta\Sigma,1} \geq \frac{V_{\text{Ref}}}{A_0}. \tag{4.35}$$

  This implies that in order to achieve a detection limit below 50 μA × 10 mΩ = 500 nV (offset requirement) with V_{Ref} = 120 mV, the OTA should provide more than 105 dB of DC gain. This requires either a gain-boosted single-stage or a two-stage OTA, thus complicating the OTA design. These issues can be alleviated by using higher-order loop filters. Thus, $L = 2$ is a suitable choice for our purpose. Firstly, it helps to eliminate the idle tones [2]. Secondly, the detection limit $\epsilon_{\Delta\Sigma,2}$ is determined by the product of the two integrator OTAs' DC gain as

$$\epsilon_{\Delta\Sigma,2} \geq \frac{V_{\text{Ref}}}{A_{0,1} \cdot A_{0,2}}, \tag{4.36}$$

suggesting that the OTAs, each with a relaxed DC gain of 55 dB, satisfy the requirement. Although further increasing L helps to reduce the required OTAs' DC gain and F_S, it comes at the cost of a more complicated loop filter and loop stability. Moreover, the required 55 dB DC gain can be easily achieved with a single-stage OTA (e.g., cascode), and, as it becomes clear later on in this section, the quantization error can be sufficiently suppressed with a reasonable F_S. As a result, modulators with second-order loop filters are preferred for use in our CSSs.

In order to sufficiently suppress the out-of-band quantization noise of a second-order $\Delta\Sigma$ ADC, one has to use a decimation filter with an order of at least three [2]. Using this decimation filter means that the modulator's input samples do not contribute equally to the final decimated result as their contributions depend on when they occur relative to the start of a conversion. This may result in the erroneous measurement of the net charge flow associated with short current pulses. In order to circumvent this problem and to be able to accurately measure the battery net charge flow Q_{bat}, equally-weighted current samples should be integrated [3, 39], meaning that a sinc^1 decimation filter should be used for ADC_I.

To illustrate this point, we will do a MATLAB simulation, in which, the charge Q_{bat} corresponding to a short current pulse (with duration of $T_{\text{on}} = 10\ \mu\text{s}$, as shown in Figure 4.9) is measured by a second-order $\Delta\Sigma$ ADC_I with three different types of decimation filters, namely, sinc^1, sinc^2, and sinc^3. Without loss of generality, a sampling frequency $F_S = 100$ kHz and a conversion time $T_{\text{conv}} = 25$ ms are assumed for ADC_I in this simulation. The moment at which the pulse starts t_0 is swept over the entire duration of the conversion, and the resulting ratios between the estimated and the actual Q_{bat} are plotted in Figure 4.9. As shown, the sinc^1 decimation filter always results in correct Q_{bat}, whereas the sinc^2 and sinc^3 filters underestimate Q_{bat} for t_0 close to 0 and T_{conv} (and overestimates Q_{bat} for t_0 around $T_{\text{conv}}/2$). In fact, as expected, these plots take the time-domain shapes of the employed decimation filter. The same results are obtained for a first-order $\Delta\Sigma$ ADC_I, implying that the order of the loop filter does not impact the measured Q_{bat}.

Achieving a resolution of better than 15 bits (in $T_{\text{conv}} = 25$ ms) for ADC_I with a sinc^1 decimation filter requires a relatively large sampling frequency; $F_S > 2^{16}/\ T_{\text{conv}} = 2.6$ MHz [1]. However, as will be discussed in the next subsection, using a third-order decimation filter (e.g., sinc^3) can help to greatly reduce

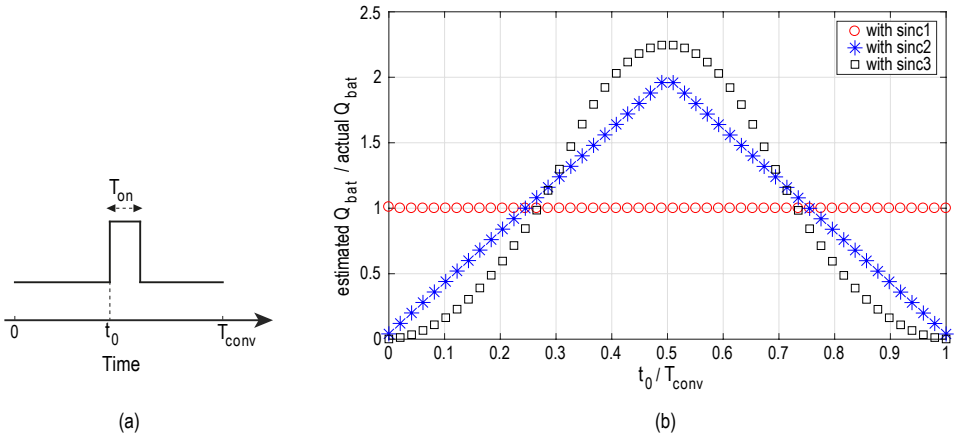

Figure 4.9: (a) Short current pulse used in MATLAB simulation and, (b) the ratio between the estimated and the actual Q_{bat} associated with a current pulse occurring at various t_0.

the required F_S to 100 kHz. The significantly smaller F_S required by the sinc^3 filter results in lower ADC$_I$ power consumption. This motivates the use of sinc^3 decimation filters, despite the fact that this may cause errors if the current flow contains many short transients.

- **Sampling frequency** F_S: This is determined in conjunction with the sampling capacitors to simultaneously meet the thermal and quantization noise requirements. It was earlier calculated that the voltage- and temperature-sensing resolution should satisfy $\sigma_V < 2$ μV and $\sigma_T < \sqrt{2} \times 24$ mK $= 34$ mK[6]. In order to leave some margin for the noise sources ignored in our calculation as well as for the quantization noise, we may rewrite (4.30) and (4.34) as

$$\sigma_V \approx \sqrt{\frac{kT}{C_{S1}F_S}\frac{4\xi}{3}\frac{1}{T_{\text{conv}}}} < 1\ \mu\text{V}, \tag{4.37}$$

$$\sigma_T \approx A \cdot \frac{\alpha}{V_{g0}}\sqrt{\frac{kT}{C_{S4}F_S}\frac{8\xi}{3}\frac{1}{T_{\text{conv}}}} < 17\ \text{mK}. \tag{4.38}$$

[6]Temperature averaging scheme (TAS) relaxes σ_T by $\sqrt{2}$.

Considering $A \approx 611$, $\alpha = 10$, $V_{g0} \approx 1.2$ V, and $T = 320$ K[7], (4.37) and (4.38) become:

$$\frac{C_{S1} \cdot F_S \cdot T_{\text{conv}}}{\xi} > 5.9 \times 10^{-9}, \tag{4.39}$$

$$\frac{C_{S4} \cdot F_S \cdot T_{\text{conv}}}{\xi} > 1.05 \times 10^{-9} \tag{4.40}$$

For the single-ADC architecture (Figure 4.2(a)), the conversion times for the current and temperature measurements are 22.5 ms and 5 ms, respectively. In addition, as will be explained in Chapter 5, the first integrator is built around a folded cascode OTA, for which it can be assumed that the excess noise factor $\xi = 1.5$. Choosing, for instance, $C_{S1} = C_{S4} = 5$ pF, and $F_S = 100$ kHz satisfies the noise requirements[8].

For the double-ADC architecture (Figure 4.2(b)), $T_{\text{conv}} = 25$ ms for both current- and temperature-sensing. As explained in Chapter 6, the integrators use current-reuse OTAs, in which there is no dominant noise source other than the input MOS devices, thus $\xi = 1$. In this case, the noise requirement is met by setting $C_{S1} = 3$ pF, $C_{S4} = 1$ pF, and $F_S = 100$ kHz.

To summarize, second-order SC feedforward $\Delta\Sigma$ ADCs with single-bit quantizers running at 100 kHz (see Figure 4.10) are considered for use in the CSS. These modulators with their input-referred thermal noise were behaviorally simulated in MATLAB. The power spectral densities (PSDs) of the ADCs' output bitstream are plotted in Figure 4.11. The PSDs show that the ADCs are thermal-noise limited up to several hundred Hz, confirming that current-sensing resolution is limited by thermal noise in a 25-ms conversion time.

[7] 20°C self-heating at ambient room temperature.
[8] In the single-ADC architecture, C_{S4} is actually C_{S2}.

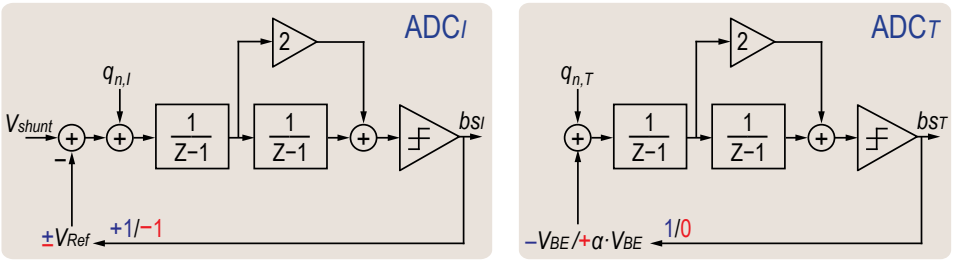

Figure 4.10: Block diagrams of ADC_I and ADC_T with input-referred thermal noise.

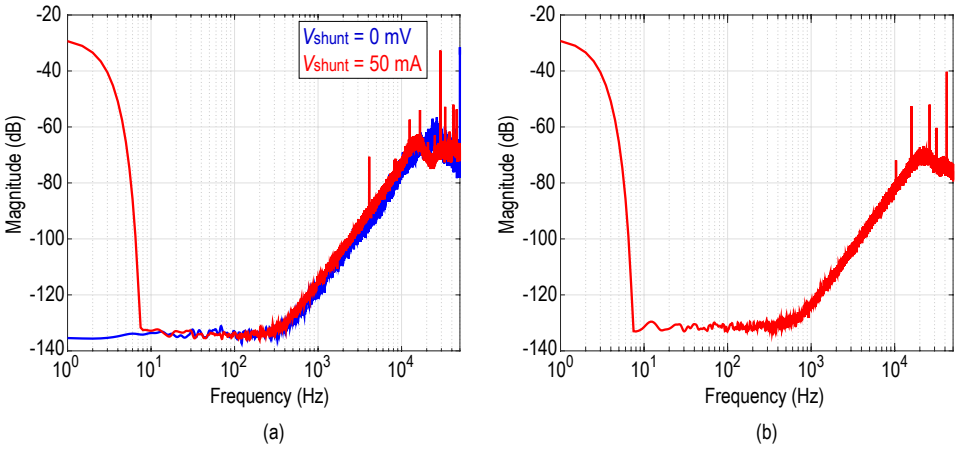

Figure 4.11: Power spectral densities (PSDs) of (a) ADC_I, and (b) ADC_T output bitstreams at DC currents of 0 and 5A.

4.4. Calibration[9]

This section describes the calibration process and the digital backend computation used in the CSS. Unlike previous precision temperature sensors [6, 7, 9], BGRs [10, 13], and CSSs [12, 22, 37, 40], neither the PTAT error in V_{BE} nor its curvature is explicitly corrected. In addition, unlike [6, 7, 9, 10], the mismatch between the ADC's sampling capacitors is also not corrected. Instead, the spread in R_{shunt} and other static errors are corrected by a room-temperature calibration, while the shunt's non-linear TCR and V_{BE} curvature are corrected by a fixed polynomial established by a batch calibration. In this section, it will be shown that this approach effectively

[9]This section is derived from a journal publication by the author: S. H. Shalmany, D. Draxelmayr, K. A. A. Makinwa, "A ±36 A Integrated Current-Sensing System with 0.3% Gain Error and 400 μA Offset from −55°C to +85°C," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1034−1043, Apr. 2017.

compensates for all major sources of error. Additionally, it significantly simplifies both the circuit implementation and the calibration of the CSS, thus reducing its production cost.

Alternatively, as in our previous work [22, 23, 37], the curvature and the spread of V_{Ref} can be separately obtained by a batch and individual calibration, respectively, and then corrected in the digital backend with the help of the known die temperature T. At the start of the process, however, an accurate V_{Ref}, and hence an accurate T is not yet available. Therefore an iterative process is used, in which, the initial value of V_{Ref} ($= V_{\mathrm{Ref0}}$) is used to estimate T, which is then used to correct V_{Ref}, from which an improved estimate of T is determined, etc. [23]. However, this process requires more calibration time and more complex digital computation.

4.4.1. Calibration Process

There are two sets of calibration data. The shunt's resistance at the calibration temperature $R_{\mathrm{shunt}}(T_0)$ is unique for each device and is referred to as individual calibration data, meaning that it is obtained by calibrating individual devices. All the other parameters (V_{Ref0}, A, B, α_1, α_2, and T_0) are common to all devices and are referred to as batch-calibration data, meaning that they are obtained by calibrating several devices and then averaging the results.

The batch-calibration data is obtained by characterizing several samples over temperature T as follows:

1. Determining V_{Ref0}, A, and B: a known external voltage is applied to ADC_I, while the CSS produces $\mu_T(T)$ and $\mu_I(T)$. By substituting $\mu_I(T)$ in (4.18), $V_{\mathrm{Ref}}(T)$ can be obtained, the room-temperature value of which is defined as V_{Ref0}. During the rest of the calibration, the simplifying assumption is made that $V_{\mathrm{Ref}}(T) = V_{\mathrm{Ref0}}$. By substituting $\mu_T(T)$ in (4.6) and using a linear fit, A and B can be obtained.

2. Determining α_1, α_2, and T_0: a known current I is passed through the shunt[10], while the CSS measures $\mu_T(T)$ and $\mu_I(T)$. From (4.6), the shunt's temperature can be obtained, the room-temperature value of which is denoted as T_0. By substituting I, V_{Ref0}, and $\mu_I(T)$ into (4.18), $R_{\mathrm{shunt}}(T)$ is obtained. The temperature coefficients α_1 and α_2 are then determined by fitting $R_{\mathrm{shunt}}(T)$ to a second-order polynomial.

[10] In this work, the calibration current was chosen 3 A for the on-chip shunt and 5 A for the lead-fame shunt.

After obtaining the batch-calibrated data, all the chips are then individually calibrated at room temperature as follows:

1. Determining the shunt resistance $R_{\text{shunt}}(T_0)$ at room temperature: a known current I is passed through the shunt, while the ADC measures $\mu_T(T_1)$ and $\mu_I(T_1)$. It should be noted that the shunt temperature T_1 will probably not be equal to the T_0 from the previous step. This is due to the spread in the shunt's self-heating and ambient temperature variations (in order to save the calibration time and cost, this calibration step is done in an unstabilized room-temperature environment).

   By substituting $\mu_T(T_1)$ into (4.6), the shunt temperature T_1 can be calculated. $R_{\text{shunt}}(T_1)$ can also be calculated by putting I, V_{Ref0} and $\mu_I(T_1)$ into (4.18). Finally, $R_{\text{shunt}}(T_0)$ can be approximated by using (3.1),

$$R_{\text{shunt}}(T_0) \approx R_{\text{shunt}}(T_0') \cdot \left(1 + \alpha_1 \cdot (T_0 - T_0') + \alpha_2 \cdot (T_0 - T_0')^2\right) \tag{4.41}$$

   It should be noted that this last step is necessary as α_1 and α_2 for a given shunt will depend on T_0. In other words, for a single shunt with given resistor values at different temperatures, the TCRs α_1 and α_2, obtained from a second-order polynomial fitting, change with the chosen calibration temperature T_0.

In normal operation, I is then measured by substituting the calibration data and the ADCs' output $\mu_T(T)$ and $\mu_I(T)$ into (4.6), (3.1) and (4.18).

4.4.2. Calibration Evaluation

In this section, the effect of uncorrected error sources on the CSS accuracy will be analyzed. Following that, we present the results of a Monte Carlo simulation in MATLAB, which are in very close agreement with this analysis.

First these error sources are introduced as follows.

1. In ADC_I, the two sampling capacitors C_{S1} and C_{S2} are nominally equal; their mismatch, however, can be regarded as a gain error δ_g applied to the ADC_I's reference voltage

$$\frac{C_{S2}}{C_{S1}} = 1 + \delta_g. \tag{4.42}$$

2. Any mismatch between C_{S2} and C_{S3} leads to a spread in the α factor of ADC_I

$$\frac{C_{S2}}{C_{S3}} = \alpha \cdot (1 + \delta_{\alpha I}). \tag{4.43}$$

3. The same holds for the mismatch between C_{S4} and C_{S5} in ADC_T

$$\frac{C_{S4}}{C_{S5}} = \alpha \cdot (1 + \delta_{\alpha T}). \tag{4.44}$$

4. As shown in (4.13), the spread in the PNP's current density ratio, Δp, leads to a PTAT error in ΔV_{BE}

$$\Delta V_{\mathrm{BE}} = \frac{kT}{q} \ln(p) \cdot \Big(1 + \delta_p\Big) \tag{4.45}$$

where $\delta_p \approx \dfrac{1}{\ln(p)} \dfrac{\Delta p}{p}$.

5. Since analyzing the effect of curvature is rather cumbersome, we will ignore its effect for the moment, and assume that V_{BE} exhibits no curvature. Nevertheless, $c(T)$ will be taken into account in a follow-up MATLAB simulation, where it will be shown that it has a negligible effect on the CSS accuracy. This is because $c(T)$ is constant for a given design, even over different batches [12, 13], and so it introduces a constant non-linearity in the measured T and R_{shunt}. The impact of this non-linearity on the CSS accuracy can then be alleviated by appropriately adjusting α_1 and α_2.

6. Assuming that the β-compensation technique is not used in the bipolar core, V_{BE} and hence V_{Ref} exhibits an error which is a linear function of the absolute temperature. Therefore, for the purpose of our analysis V_{BE} can be written as

$$V_{\mathrm{BE}}(T) \approx V_{g0}\Big(1 + \delta_0 + \delta_1 \frac{T}{T_c}\Big) - \lambda T. \tag{4.46}$$

Although (4.46) incorrectly indicates that, at the absolute temperature, V_{BE} deviates from the bandgap voltage V_{g0}, it is justified to use this approximation in a *limited* temperature range, e.g., from $-55°\mathrm{C}$ to $+125°\mathrm{C}$.

For the sake of simplicity in our analysis, we assume that all the introduced error terms are independent from each other and exhibit zero mean values. The independence assumption, however, does not completely hold true for δ_g and $\delta_{\alpha I}$,

in which C_{S2} contributes to both. However, since $\delta_{\alpha I}$ is dominated by the small sampling capacitor C_{S3} ($\ll C_{S2}$), these two error terms may be assumed to be independent.

At the presence of these errors, ADC$_I$'s output can be obtained by rewriting (4.18) [11]

$$\mu_I'(T) = \frac{C_{S1}\cdot R_{\text{shunt}}(T)\cdot I}{C_{S2}\cdot \Delta V_{\text{BE}} + C_{S3}\cdot V_{\text{BE}}}$$
$$\approx \alpha\,\frac{R_{\text{shunt}}(T)\cdot I}{V_{g0}\big(1-\delta_{\alpha I}+\delta_g+\delta_0\big)+\Big(\alpha\frac{k}{q}\ln(p)\delta_p+\lambda\delta_{\alpha I}+\frac{V_{g0}}{T_c}\delta_1\Big)T} = \frac{R_{\text{shunt}}(T)\cdot I}{{V_{\text{Ref0}}}'}. \tag{4.47}$$

where, in order to have a first-order temperature cancellation on the reference voltage, it is assumed that $\alpha\frac{k}{q}\ln(p)=\lambda$. In the rest of the thesis, the *prime* symbol, $'$, is used to indicate the *measured* value of the corresponding parameter which is corrupted by the error sources. Similarly, ADC$_T$'s output can be expressed as

$$\mu_T'(T) = \frac{C_{S4}\cdot \Delta V_{\text{BE}}}{C_{S4}\cdot \Delta V_{\text{BE}} + C_{S5}\cdot V_{\text{BE}}}$$
$$\approx \frac{\alpha\frac{kT}{q}\ln(p)}{V_{g0}}\Big(1+\delta_{\alpha T}+\delta_p-\delta_0-\frac{\lambda T}{V_{g0}}\big(\delta_{\alpha T}+\delta_p\big)-\frac{T}{T_c}\delta_1\Big). \tag{4.48}$$

During the first step of the calibration process, V_{Ref0} is obtained by taking the average of the reference voltage of ADC$_I$s measured at room temperature. Assuming that N samples are measured, and considering that the error terms have a zero mean value, V_{Ref0} can be calculated from (4.47) as

$$V_{\text{Ref0}} = \frac{1}{N}\sum_{i=1}^{N} {V_{\text{Ref0},i}}' \approx \frac{V_{g0}}{\alpha} \tag{4.49}$$

which is equal to its nominal value. It can also be shown that the parameters A and B, obtained by averaging the linear fit of (4.48), are equal to their nominal values

[11] The expression is simplified by disregarding the second-order effects and by using the approximation $1/(1+\delta)\approx 1-\delta$ for $\delta \ll 1$.

as

$$A = \frac{V_{g0}}{\alpha \frac{k}{q} \ln(p)}, \qquad \text{and} \qquad B = -273.15°C. \tag{4.50}$$

By combining (4.48) and (4.50), the measured shunt calibration temperature T_0' in Kelvin is

$$T_0' = A\mu_T'(T_0) \approx T_0\Big(1 + \delta_{\alpha T} + \delta_p - \delta_0 - \frac{\lambda T_0}{V_{g0}}\big(\delta_{\alpha T} + \delta_p\big) - \frac{T_0}{T_c}\delta_1\Big) \tag{4.51}$$

Averaging the measured calibration temperature (4.51) results in[12]

$$T_0'' = \frac{1}{N}\sum_{i=1}^{N} T_{0,i}' \approx T_0 \tag{4.52}$$

which is equal to the nominal temperature T_0.

Similarly, it can be shown that α_1 and α_2 are not influenced by the uncalibrated error terms as their effects are averaged out[13]. However, the individual calibration data will be impacted since they are obtained by measurements on each sample.

By using (4.47) and (4.49), the *measured* shunt value at the *measured* calibration temperature $R_{\text{shunt}}'(T_0')$ is obtained as

$$\begin{aligned} R_{\text{shunt}}'(T_0') &= \frac{\mu_I'(T_0) \cdot V_{\text{Ref0}}}{I_{\text{bat}}} \\ &\approx \frac{R_{\text{shunt}}(T_0)}{\big(1 - \delta_{\alpha I} + \delta_g + \delta_0\big) + \Big(\alpha \frac{k}{q} T_0 \ln(p)\delta_p + \lambda T_0 \delta_{\alpha I}\Big)\frac{1}{V_{g0}} + \frac{T_0}{T_c}\delta_1}. \end{aligned} \tag{4.53}$$

The shunt resistor value at average calibration temperature $R_{\text{shunt}}'(T_0'')$ is then calculated to be:

$$R_{\text{shunt}}'(T_0'' = T_0) = R_{\text{shunt}}'(T_0') \cdot \Big(1 + \alpha_1 \cdot (T_0 - T_0')\Big) \tag{4.54}$$

[12] For the sake of simplifying the analysis, we assume that all devices are at the same calibration temperature T_0.

[13] It is confirmed by MATLAB simulation; hand calculation is non-trivial.

where, in order to simplify the analysis, only the first-order TCR is considered. The key to mitigating the effect of all the uncalibrated errors lies in (4.51) and (4.53). These two calibration data points collectively absorb all the error terms and significantly mitigate their impact during the normal operation of the CSS. This important conclusion will be clarified further in the remainder of this section.

During normal operation, when an unknown current I flows through the shunt at an unknown temperature T, the two ADCs produce outputs $\mu'_I(T)$ and $\mu'_T(T)$ given by (4.47) and (4.48), respectively. The reported current by the CSS, I', can then be written as

$$\begin{aligned} I'(T) &= \frac{\mu'_I(T) \cdot V_{\text{Ref0}}}{R'_{\text{shunt}}(T)} \\ &= \frac{\mu'_I(T)\dfrac{V_{g0}}{\alpha}}{R'_{\text{shunt}}(T_0) \cdot \Big(1 + \alpha_1 \cdot (A\mu'_T(T) - T_0)\Big)} \end{aligned} \tag{4.55}$$

The CSS gain error is

$$\epsilon(T) = \frac{I'(T) - I}{I}. \tag{4.56}$$

The sensitivity of this gain error to each error term over temperature can be obtained as

$$S_{\delta_i}^{\epsilon(T)}(T) = \frac{\partial \epsilon(T)}{\partial \delta_i}. \tag{4.57}$$

These sensitivities are calculated in Appendix A and are plotted in Figure 4.12. Considering the effects of shunt self-heating, the calibration temperature is assumed to be 40°C in this plot. As shown, the error sources are significantly suppressed. For instance, the sensitivity to the capacitor mismatch is at most 0.2, meaning that the effect of this mismatch is suppressed by $> 5\times$. With a reasonable layout, the capacitor mismatch can be easily bounded to $\pm 0.3\%$ (3σ), leading to $< \pm 0.05\%$ error in the current sensing. It should be noted that, the effect of this mismatch in the single-ADC design is even less pronounced as $\delta_{\alpha I} = \delta_{\alpha T}$ and $S_{\delta_{\alpha I}}^{\epsilon(T)} \approx -S_{\delta_{\alpha T}}^{\epsilon(T)}$ (they significantly mitigate each other's effect). The errors originated from the BGR are mitigated by $> 20\times$; up to $\pm 1\%$ process spread in V_{BE} and up to $\pm 1\%$ mismatch in the ratio p will cause a negligible error ($< \pm 0.05\%$) in the current sensing.

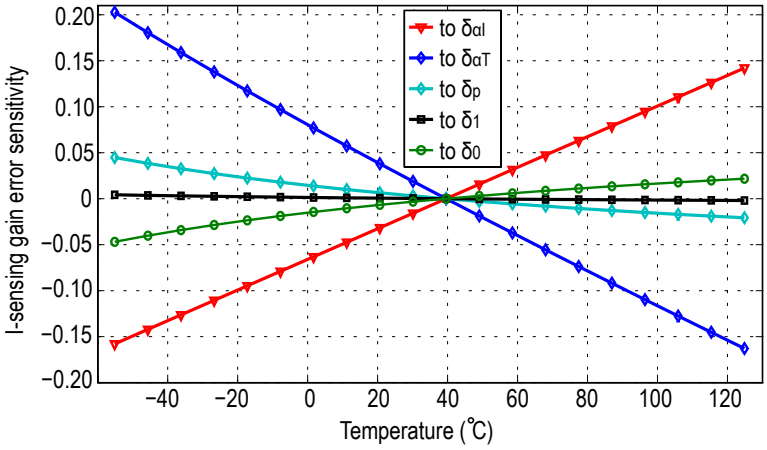

Figure 4.12: The sensitivity of the current sensing error with respect to different error sources.

So far, for the sake of simplifying our analysis, $c(T)$ and the shunt's second-order TCR α_2 have been overlooked. In order to evaluate their effects and to verify the validity of our analysis, we present a Monte Carlo simulation in MATLAB (10,000 runs) with the following conditions:

- V_{BE} is taken from circuit s corner simulation which includes the curvature $c(T)$ (besides the spread up to $\pm 1\%$).
- The spread in the ratio p is assumed to have a Gaussian distribution with a 3σ value of 1%.
- The mismatches among various capacitors are assumed to be Gaussian with a 3σ value of 0.3%.
- R_{shunt} has a Gaussian distribution with a 3σ value of 15%.

After applying the proposed calibration scheme, the resulting current-sensing gain errors are plotted in Figure 4.13. It is in accordance with the calculation result shown in Figure 4.12, in which the maximum errors occur at the two temperature ends $-55°$C and $+125°$C. This simulation also shows a maximum 3σ error of $\sim$ 0.083%, which is very close to the calculation result ($\sim$ 0.089%).

It can be qualitatively explained that the effect of $c(T)$ propagates up to the point where α_1 and α_2 are determined. As a result, α_1 and α_2 will be slightly modified so as to account for the effect of $c(T)$. In short, the shunt's TCR absorbs $c(T)$ and suppresses its effect on the accuracy of the CSS[12].

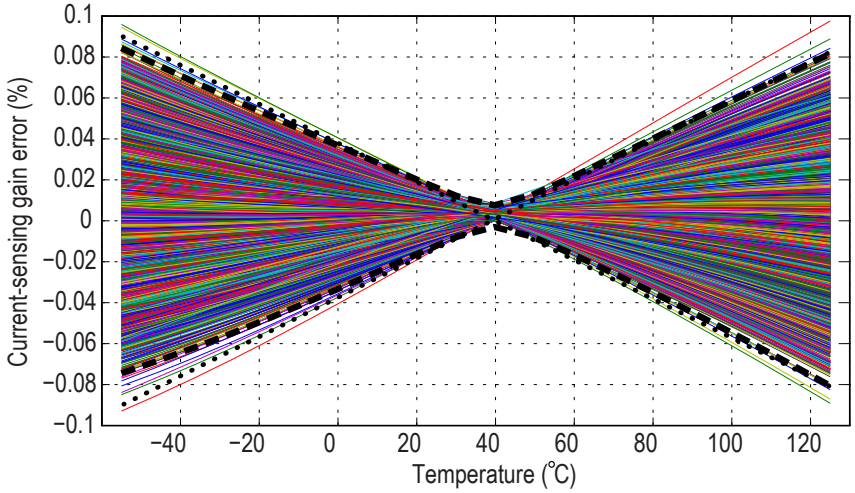

Figure 4.13: The simulated current-sensing gain error over temperature (the dashed and the dotted lines indicate the simulated and the calculated $\pm 3\sigma$ values, respectively).

4.5. Conclusion

The system-level design of the CSS readout electronics has been presented. A bandgap reference (BGR) built from the substrate PNPs available in a standard CMOS process is shown to be an optimal choice for generating both the reference voltage and the temperature information required by the CSS. Driven by resolution requirements, the current- and temperature-sensing ADCs have been implemented as second-order SC $\Delta\Sigma$ modulators.

Significant error sources of the BGR and the ADCs, together with the solutions utilized by prior art, have been reviewed. In contrast to the these, we propose a much simpler solution which corrects: 1) the spread of R_{shunt} by room temperature calibration, and 2) the shunt's non-linear TCR and V_{BE} curvature with a fixed polynomial established by a batch calibration. It has been shown that this approach effectively compensates for all the major sources of error. It significantly simplifies both the circuit implementation and the calibration of the CSS, and thus reduces its production cost.

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5

Implementation I, Proof of Concept

5.1. Introduction[1]

The design and performance of a proof-of-concept 5 A CSS with a 10 mΩ on-chip metal shunt (shown in Figure 2.6) is presented in this chapter. The objective of this prototype is to *experimentally* evaluate 1) the feasibility of using the metal layers of a silicon die as a shunt resistor (proposed in Chapter 2), 2) the thermal coupling between the shunt and the temperature-sensing PNPs (Chapter 2), and 3) the calibration scheme, developed in Chapter 4, in which only the shunt's spread and its TCR are calibrated.

As shown in Figure 4.2(a), in this prototype (CSS_1) a single ADC is used for both current I and temperature T measurement. To do so, the ADC is operated in incremental mode and is time-multiplexed. A temperature-averaging scheme (TAS) uses the average of two successive T measurements to compensate for each I measurement (Figure 5.1), resulting in improved accuracy, especially when a current pulse causes dynamic self-heating in the shunt. The selected multiplexing scheme

[1] This chapter is derived from a journal publication by the author: S. H. Shalmany, D. Draxelmayr, K. A. A. Makinwa, "A ±5 A Integrated Current-Sensing System with ±0.3% Gain Error and 16 μA Offset from −55°C to +85°C," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 800−808, Apr. 2016.

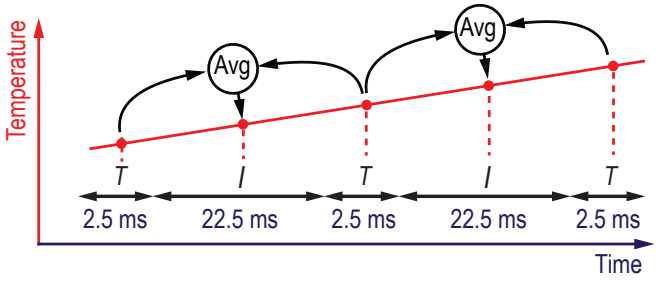

Figure 5.1: The temperature averaging scheme (TAS) used in the single-ADC architecture.

ensures sufficient resolution for the T measurements (24 mK_{rms}) and allows I to be monitored at 40 S/s, which is fast enough to compensate for thermal transients (as will be shown in Section 5.5). After temperature compensation, the CSS achieves ∼14-bit resolution, which is mainly limited by the noise associated with both the I (for currents below 3 A) and T (for currents above 3 A) measurements.

5.2. Dynamic Bandgap Reference

5.2.1. Operating Principle

Figure 5.2 shows the schematic of the BGR. Its bias circuit generates a PTAT current $I_{\text{bias}} = 1.4\ \mu\text{A}$ (at 45°C) with the help of an opamp (single-ended folded cascode with a PMOS input pair, as in [1]) and two auxiliary PNPs which are also biased at a 1:16 current-density ratio (emitter area of a unit PNP $A_E = 10\ \mu\text{m}^2$). This current is then mirrored to the bipolar core, and used to bias two PNPs at equal emitter currents $4I_{\text{bias}}$ to generate V_{BE} and ΔV_{BE}. It should be noted that in contrast to the common use of scaled emitter currents [2, 3], this work uses PNPs with scaled emitter areas. This approach results in equal PNP transconductances, which, in turn, minimizes the total bias current required to ensure accurate settling when V_{BE} and ΔV_{BE} are sampled. In addition, in contrast to [2, 3] which used a current density ratio of $p = 5$, the choice of $p = 16$ in this design results in larger ΔV_{BE}, which in turns makes it more robust to circuit non-idealities (opamp's offset), while still ensuring almost the same β_F for the the two PNPs (see Figure 4.5).

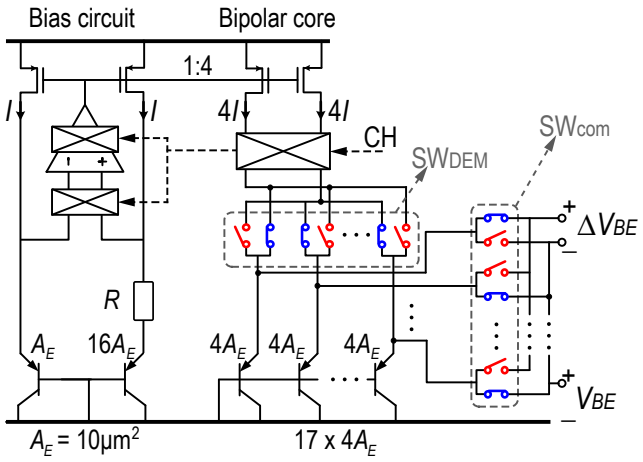

Figure 5.2: Simplified schematic of the bandgap reference consisting of a bias circuit and a bipolar core with dynamic error correction techniques.

5.2.2. Precision Techniques

To decrease the spread in I_{bias}, and hence in V_{BE}, the opamp's offset is reduced by chopping, while an accurate ΔV_{BE} is achieved by applying dynamic element matching (DEM) to the PNPs and chopping the current sources of the bipolar core [2, 3].

The voltage drop across the DEM switches (SW_{DEM}), if added to V_{BE} and ΔV_{BE}, will introduce significant errors in both V_{Ref} and T. Calculations show that switches with an on-resistance R_{on} of only 25 Ω (or R_{on} variation by 25 Ω with process and the supply voltage) will introduce errors of $\sim 0.1\%$ and $\sim 0.3°\text{C}$ in V_{Ref} and T, respectively. One way of mitigating such large errors is to use wide MOS switches with sufficiently low R_{on}; however, these will introduce large leakage currents, especially at high temperatures. To mitigate the effect of relatively large R_{on} ($\approx 1\,\text{k}\Omega$), the DEM switches are Kelvin-connected [4]. The base-emitter voltages of the PNPs are directly sampled via the switches (SW_{com}), which can be swapped to generate V_{BE} and ΔV_{BE}. Since these voltages are sampled by a SC $\Delta\Sigma$ ADC, the resistance of the switches SW_{com} is not critical as long as the ADC's input circuit settles sufficiently.

As pointed out in Chapter 4, the spread in the PNP's saturation current I_S leads to a PTAT spread in V_{BE} and hence in V_{Ref} [5]. Over process and temperature, this spread can be as large as $\pm 1\%$ [6]. Also since V_{BE} has a nonlinear temperature characteristic or curvature, V_{Ref} exhibits a corresponding curvature error of about

±0.2% [6, 7]. The effects of these non-idealities are absorbed in the shunt calibration data and significantly suppressed (see Section 4.4).

5.3. ADC

CSS_1 employs a second-order switched-capacitor feed-forward ΔΣ ADC. The circuit and the timing diagram of the ADC are shown in Figure 5.3, in which capacitors C_{S1} (= 5 pF) sample V_{shunt}, while capacitors C_{S2} (= 5 pF) and C_{S3} (= $C_{S2}/8$) sample $\pm\Delta V_{\text{BE}}$ and $\pm V_{\text{BE}}$, respectively. The sampled voltages are then accurately combined in the charge domain to generate the voltage $V_{\text{Ref}} = V_{\text{BE}} + \Delta V_{\text{BE}}/8 \approx$ 150 mV. The modulator's feedback is established by using the output bitstream *bs* to control the polarity of the feedback voltages $\pm\Delta V_{\text{BE}}$ and $\pm V_{\text{BE}}$. This conversion results in an output bit-stream *bs* with an average value of μ_I as stated in Equation (4.18). In addition, unlike [2, 3, 8, 9], the mismatch between sampling capacitors is not corrected with DEM. Instead, its effect is absorbed in the shunt calibration data and significantly suppressed (see Chapter 4).

As a precautionary measure, in CSS_1, V_{Ref} is designed to be slightly larger than 120 mV. This is to cope with unexpectedly large spread in R_{shunt}, i.e., if the metal resistance appears to be significantly larger than what is modelled in the process design kit (PDK). Measurements, however, show that the metal resistor is well-modelled, and therefore V_{Ref} was designed to be 120 mV in the follow-up designs presented in Chapter 6

To determine the temperature T, the sampling switches connected to C_{S1} are disabled, while the capacitors C_{S2} and C_{S3} perform the charge balancing. When *bs* is +1, C_{S3} samples $-V_{\text{BE}}$ and when *bs* is 0, C_{S2} is sampling $+\Delta V_{\text{BE}}$.

As explained in Chapter 4, the value of the ADC's input sampling capacitors and its sampling frequency (F_S = 100 kHz) is chosen to satisfy the resolution requirements. The first integrator uses correlated double-sampling (CDS) to suppress its offset and $1/f$ noise. Further suppression is achieved with low frequency chopping (CHL), i.e. by averaging the results of two conversions, each with a different polarity of input. The resulting input impedance is $1/(C_{S1}{\cdot}2F_S) = 1$ MΩ, which is eight orders of magnitude larger than R_{shunt}, and hence has a negligible (0.01 ppm) effect on the current-sensing gain error. The first and second integrators are based on folded-cascode OTAs, which draw 18 μA and 1.6 μA, respectively.

5.3.1. Timing

The frequency of the various dynamic error correction signals in the BGR and

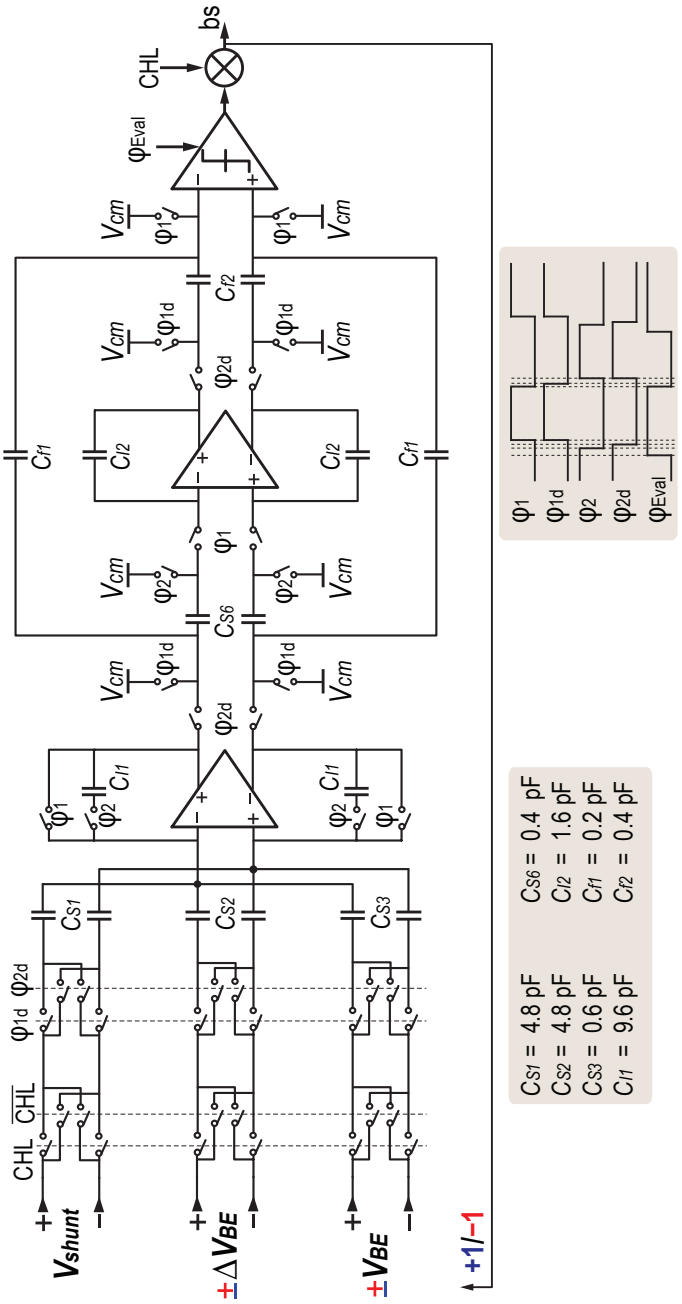

Figure 5.3: Simplified diagram of the second-order switched-capacitor ΔΣ ADC used in the CSS.

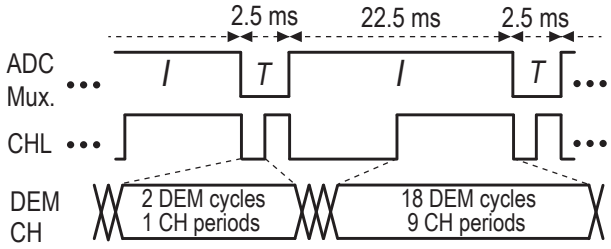

Figure 5.4: (a) ADC multiplexing and temperature-averaging scheme, and (b) timing diagram of different signals in the ADC and the BGR.

in the ADC (DEM, CH, and CHL) was chosen to avoid extra errors due to their interaction. As shown in Figure 5.4(b), the frequency of the CHL signal is adjusted such that its period is equal to each I and T measurement period. Furthermore, the frequency of the CH and DEM is chosen to be 2× (18×) and 4× (36×) higher than that of the CHL during the T and I measurements, respectively.

5.3.2. Low-Leakage Sensor Frontend

To avoid introducing additional current-sensing errors, the switches connected to R_{shunt} should be designed to minimize the leakage current due to their finite off-resistance [4, 7]. As shown in Figure 5.5, this leakage current I_{leak} is provided by I and flows through the on-resistance R_{on} of the input switches. Assuming that the four input switches are matched, the resulting voltage drop across R_{on} will cause a differential error $V_e = 2R_{\text{on}} \cdot I_{\text{leak}}$ in the sampled voltage across C_{S1}. This translates into a current-sensing error $I_e = 2R_{\text{on}}/R_{\text{shunt}} \cdot I_{\text{leak}}$. Since R_{on} is on the order of several kΩ and R_{shunt} is only 10 mΩ, I_e is about 6 orders of magnitude larger than I_{leak}. To make matters worse, I_{leak} is a nonlinear function of V_{shunt} (or I). This error is especially significant (up to 0.5%) at high temperatures (> 125°C) and negative I, when I_{leak} is in the nA range.

To tackle this issue, the input switches were realized as low-leakage high-threshold voltage NMOS transistors whose off-resistance is ∼ 15× higher than that of normal NMOS transistors. As shown in Figure 5.6, since a super cut-off MOS switch exhibits significantly less leakage [10, 11], the gates of the "off" switches are driven by the lowest available voltage, i.e. by ground when $I > 0$, and by ${R_{\text{on}}}^{+}$ when $I < 0$. The polarity of I needed for this minimum selection scheme is obtained from the ADC's output [4, 7]. Simulations show that this scheme reduces the worst-case

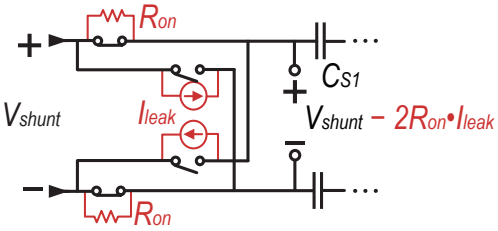

Figure 5.5: Leakage sources in the sensor frontend.

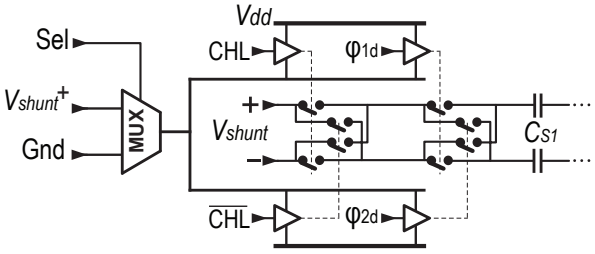

Figure 5.6: Simplified schematic of the low-leakage sensor frontend.

gain error due to I_{leak} by more than 60 times to $< 0.01\%$.

5.4. Layout

The floor-plan and the layout of the ADC are critical for achieving a voltage offset on the order of 100 nanovolts and below. A simplified view of the employed layout floor-plan is shown in Figure 5.7. Due to the shunt's self-heating, large temperature gradients are created in the die. In order to mitigate their effects on the readout performance, the BGR and the ADC are symmetrically laid out along the xx′ axis (which is normal to the shunt's current direction). Different clock phases are generated in the digital domain (with digital supply and ground −dvdd and dvss), while the rest of the circuitry operates at analog supply and ground −avdd and avss. The following measures are taken in routing the digital and analog signals:

1. The digital signals are distributed on the second metal layer (M2) and are completely shielded by means of *continuous* grounded planes of M1 and M3 to protect the sensitive analog signals routed on M4 and M5. It should be noted that in order to minimize the area of the return current loop, and hence its interference with the analog signals, the ground shielding plans should not

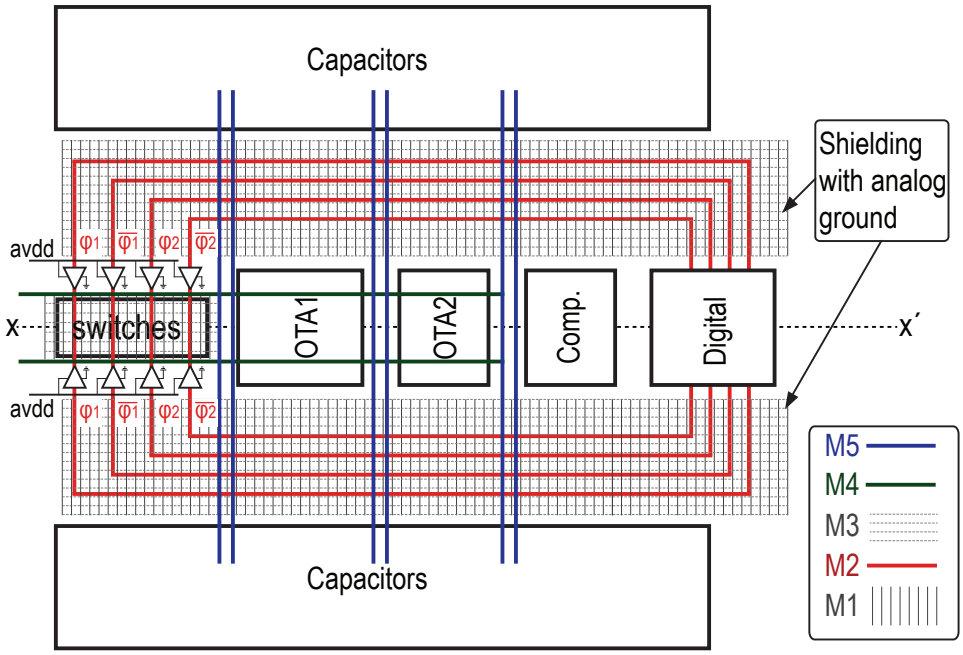

Figure 5.7: Simplified view of the ADC layout floor-plan.

be breached along the digital route [12]. In addition, an on-chip decoupling capacitor ($C_{decap} \sim 20$ pF in this work) helps to reduce the area of the digital return current loop.

These points are better illustrated in Figure 5.8, in which a digital inverter drives an analog buffer over a long line (on M2). The input parasitic capacitance of the buffer and that of the digital line is modelled by C_p. The falling edge of the digital signal V_ϕ to zero, leads to C_p being charged to dvdd, with current primarily provided by C_{decap}. As any current will return to its source, a loop is formed which radiates a magnetic field whose magnitude is proportional to the loop area. One key to minimizing this interference is to reduce the area of the return current loop[2]. As shown in Figure 5.8(a), this can be done by: a) placing C_{decap} as close as possible to the digital circuitry, b) not breaking the grounded shield layer, which otherwise forces the return current to form a larger loop as illustrated in Figure 5.8(b), or c) bridging avss and dvss to help close the loop. In this work, avss and dvss are already connected together at the PCB level (by using a shared PCB ground plane); however,

[2]Reducing dvdd and C_p also helps to lower the radiation.

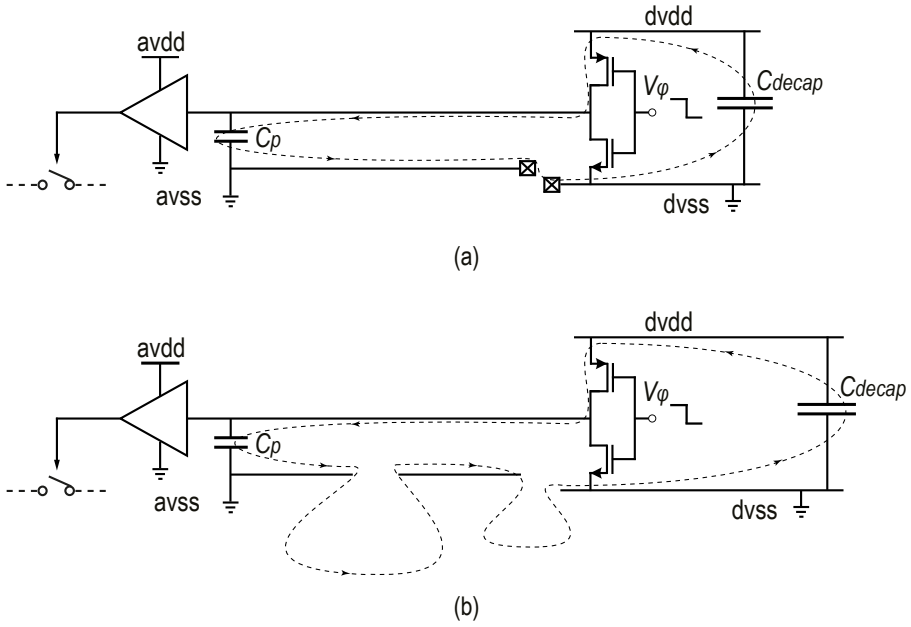

Figure 5.8: Return current of a digital line, (a) proper layout to minimize the loop area, and (b) a layout with a potentially large magnetic interference.

this path leads to a large return current loop. A better approach is to leverage their loose connection via the relatively high-ohmic substrate. In a process with a deep N-well option, these two grounds on the die can be isolated from each other. However, in this work, we choose not to separate them on the die, but instead enhance their connection by using a large number (more than 300) of closely positioned analog and digital substrate contacts (separated by the minimum allowed layout rules) around the digital clock generation block. This helps to minimize the current loop area.

2. The digital signals are routed differentially (e.g., ϕ_1 and $\overline{\phi_1}$ run together) in order to minimize the analog ground perturbation induced by the clocks.

3. The digital signals are also routed symmetrically along the xx′ axis so as to suppress their residual impacts on the sensitive analog signals.

4. The digital signals pass through analog buffers before being applied to the switches so as to isolate the analog switches from the digital supply/ground noise.

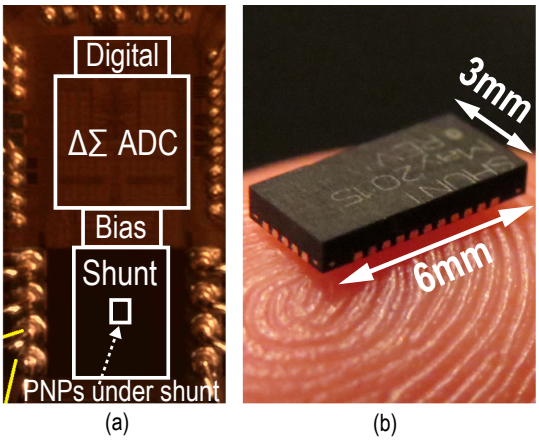

Figure 5.9: (a) Die micrograph, and (b) HVQFN package.

5. In order to achieve a higher level of immunity to interferences, the *differential* analog signals are routed adjacently.

6. The low-frequency choppers (CHL) are placed as close as possible to their input analog signal sources. This is because the CHL cannot cancel out any offset-like error induced beforehand.

5.5. Experimental Results

CSS_1 was realized in a standard 0.13 μm CMOS process (Figure 5.9). It occupies 1.15 mm^2 and draws 55 μA from a 1.5 V supply. The ADC and the BGR consume 25 μA and 20 μA, respectively, and 10 μA is dissipated in digital and auxiliary circuitry. For flexibility, the digital backend and sinc^3 decimation filter were implemented off-chip. 24 chips, 12 of which were directly bonded to PCB and 12 of which were packaged in HVQFN package, were characterized from -55°C to $+85$°C in steps of 20°C.

The ADC's output PSDs in the voltage- and the temperature-sensing configuration show that it is kT/C-noise limited up to a bandwidth of 400 Hz (Figure 5.10). Note that the tones at 50-Hz harmonics in the voltage-sensing mode are caused by the finite main-line rejection of the current source used in the experiment. The voltage-sensing resolution is measured around 1.5 μV_{rms} in a 22.5 ms conversion time, while the temperature sensor achieves 22 mK_{rms} resolution in a 2.5 ms conversion time, both of which are $\sim$0.5 bit worse than the simplified calculations in Chapter 4. As expected, this is because the BGR and the frontend switches are

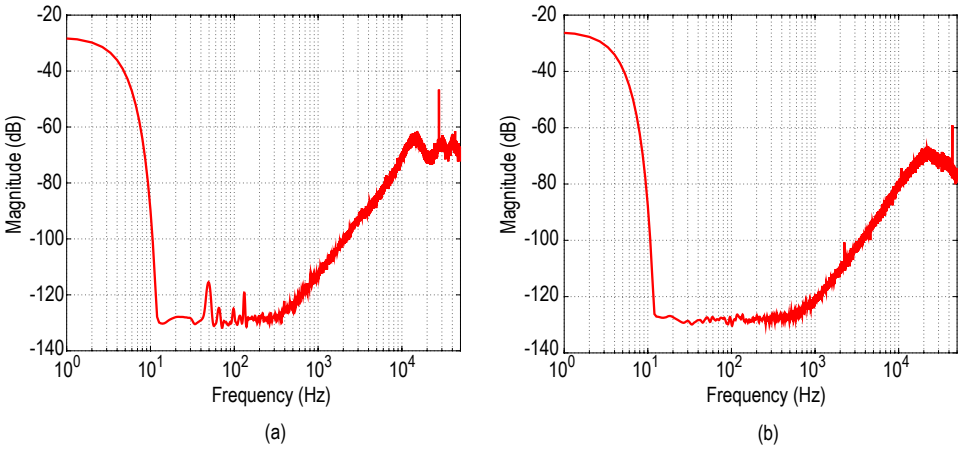

Figure 5.10: Power spectral density (PSD) of the ADC's output bitstream at DC currents of 5A in, (a) the current-sensing mode, and (b) the temperature-sensing mode.

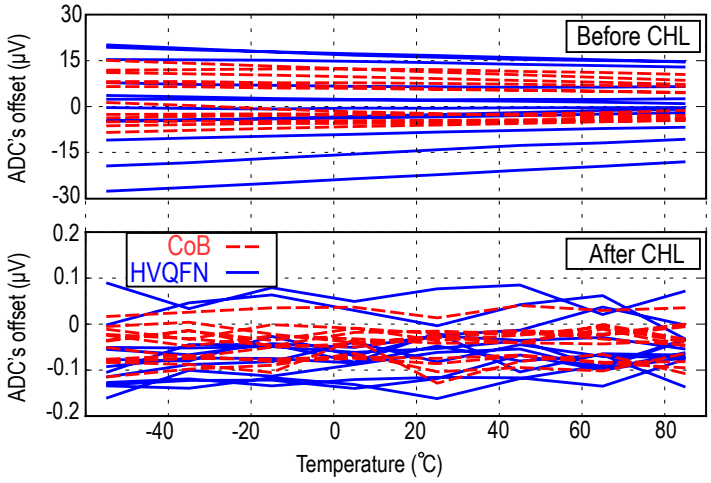

Figure 5.11: ADC's offset over temperature, before (top) and after (bottom) using the CHL.

ignored in the noise calculation, as well as the residual quantization noise.

The ADC's offset was measured by disconnecting the shunt from the current sources; as shown in Figure 5.11 it is less than 30 μV (3 mA) from -55°C to $+85$°C, and drops below 160 nV (16 μA) after low-frequency chopping.

The parameters obtained from the batch calibration (the average of all 24 samples) are shown in Table 5.1. The shunt TCR α_1 and α_2 are modified by $\sim$0.5% and $\sim$1.5%, respectively, to account for the BGR nonlinearity. Figure 5.12 shows the

Table 5.1: Batch-calibration data.

Parameter	Value
V_{Ref0}	150.47 [mV]
A	623.85 [1/°C]
B	−272.35 [°C]
T_0	36.58 [°C]
α_1 (Shunt only)	0.3321 [%/°C]
α_2 (Shunt only)	-5.585×10^{-5} [%/°C^2]
α_1 (Shunt and BGR combined)	0.3305 [%/°C]
α_2 (Shunt and BGR combined)	-5.661×10^{-5} [%/°C^2]

spread and the curvature in the BGR voltage and shunt value versus temperature, after the batch calibration, but before the nonlinearity correction. The measured curvature of V_{Ref} is about 0.5%, while the spread among chips in the same package is about ±0.06%. The resulting curvature in the temperature sensor's output is about 0.6°C, with less than ±0.3°C spread among chips in the same package. Compared to the CoB samples, however, the curvature of the HVQFN samples differs slightly ($\sim 0.25\%$). This may be due to the thermo-mechanical stress induced by the plastic package, which, due to the piezojunction effect, changes both the minority carrier mobility and intrinsic carrier concentration in the base of the PNPs and hence modifies V_{BE} (and V_{Ref}) [13, 14]. This may be exacerbated by the fact that the dies were back ground (from $\sim$ 740 μm to $\sim$ 200μm thick) to fit into the HVQFN package. The nonlinearities of R_{shunt} versus temperature in the two packages also differ by about ±0.15%. This can again be attributed to the electro-mechanical stress of the HVQFN package and the piezoresistivity of the metal resistor [15]; depending on the package construction and its mounting on the board, a temperature-dependent mechanical stress is applied to the silicon die, hence introducing extra nonlinearity in R_{shunt}.

Measurements show that R_{shunt} spreads by about ±3% within a batch. After calibration and digital temperature compensation, the CSS achieves a gain error of less than ±0.6% for a ±5 A range, from −55°C to +85°C (Figure 5.13). However, a systematic gain error remains since the PNPs are somewhat insulated from the shunt by an oxide layer, and therefore the actual temperature is underestimated. Since this error is proportional to I^2, and I is (approximately) known, it can be corrected by multiplying the ADC's output by a linear function of I^2. The associated

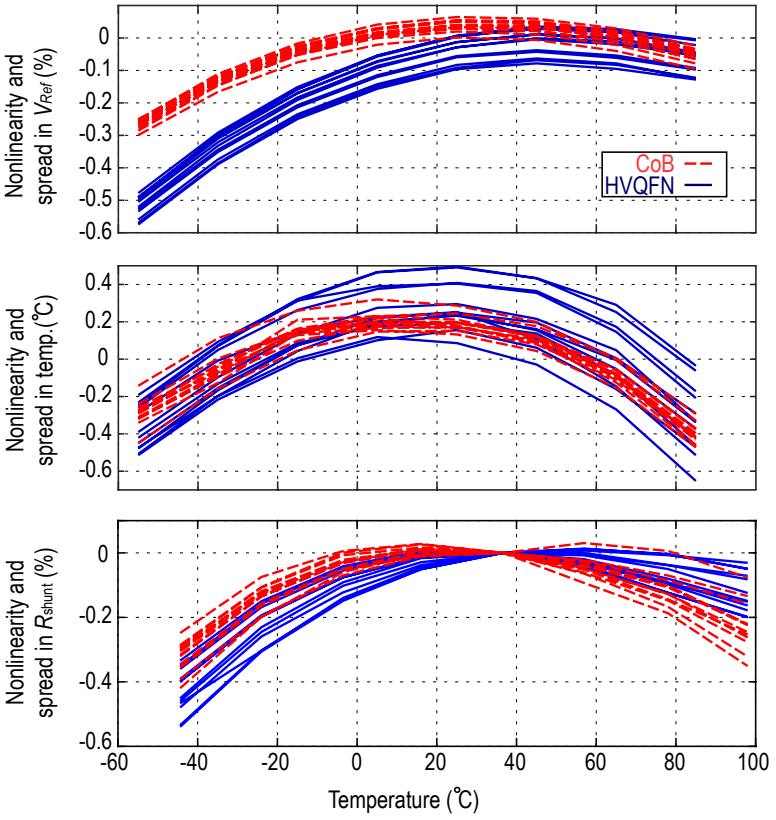

Figure 5.12: Spread and curvature in V_{Ref}, the temperature sensor, and the shunt nonlinearity after batch-calibration in HVQFN-packaged chips (solid lines) and CoB (dashed lines).

coefficients were determined by batch calibration and found to be almost identical for the CoB and HVQFN packaged chips. This residual self-heating compensation (RSHC) reduces the gain error of the CSS to ±0.3% from −55°C to +85°C (Figure 5.13). As shown in Figure 5.14, applying a first order temperature correction increases the gain error by 3× to 1%. This confirms that second order temperature correction is necessary to achieve an accurate current sensing.

The batch-calibration data for the results shown in Figure 5.12 and Figure 5.13 are determined by averaging the data obtained from all 24 devices. To demonstrate the impact of averaging in obtaining the batch-calibration data, Figure 5.15 shows the current-sensing gain error, for the case when this data is obtained by measurements on one sample. The data is then used to calibrate all 24 samples. It can

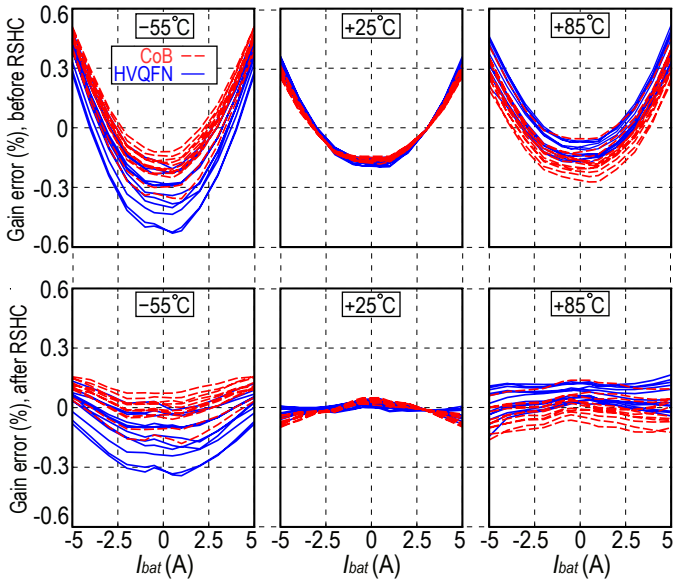

Figure 5.13: Current-sensing gain error at three ambient temperature points, before (top), and after (bottom) residual self-heating compensation.

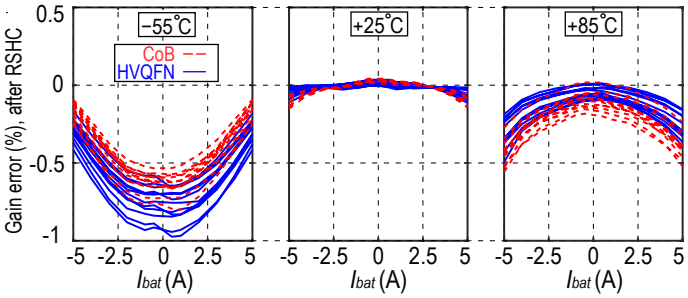

Figure 5.14: Current-sensing gain error at three ambient temperature points with first-order temperature compensation and after RSHC.

be seen that the gain error is then slightly larger, but is always less than ±0.5%. The increase is mainly due to the difference in the V_{Ref} curvature of the CoB and HVQFN devices.

As presented in Chapter 3, the accelerated electromigration test (with a 5 A DC current, and at an ambient temperature of 85°C) shows a maximum drift of 0.13% over the course of 24 days, corresponding to a worst-case drift rate of 2.3 ppm/hour. Considering that the actual circumstances, in which a CSS will be used, will be significantly less harsh than this measurement, the proposed on-chip shunt can still

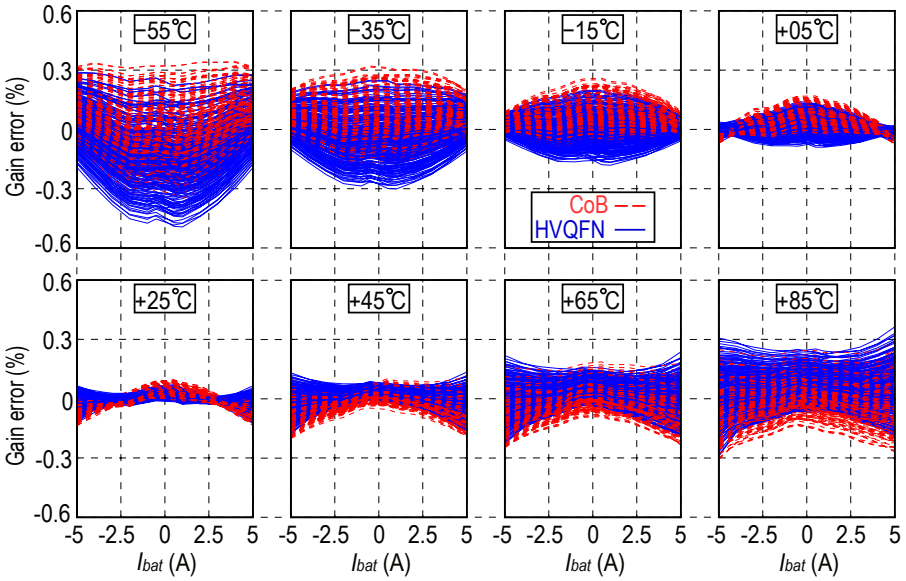

Figure 5.15: Current-sensing gain error at eight ambient temperature points, in which the batch calibration data is obtained by measurements on *one* sample.

offer a reliable solution in a wide variety of practical applications. If required, the drift can be alleviated by: 1) reducing the maximum CSS operating temperature, 2) reducing the maximum current level, or 3) increasing the cross-sectional area of the shunt at the expense of chip area.

The dynamic accuracy of the shunt temperature compensation was evaluated with a 0.1A-to-5A step. As shown in Figure 5.16, this causes a temperature rise of about 40°C. Without TAS, the gain error settles within 1 s to −0.04%, and to 0.33% with and without RSHC, respectively. Enabling TAS reduces the settling time significantly at the expense of slightly more gain error in the first I measurement after the current step. The corresponding improvement in the charge domain (the area under the curve) is $\sim 2.5\times$ after enabling TAS. Note: better performance can be achieved by employing a double-ADC architecture which allows the continuous measurement of I and T (see Chapter 6).

Compared to the state-of-the-art (Table 5.2), the proposed CSS achieves significantly better current-sensing accuracy, achieving a gain error of ±0.3% over a wide current range (±5 A) as well as an offset of only 16 μA.

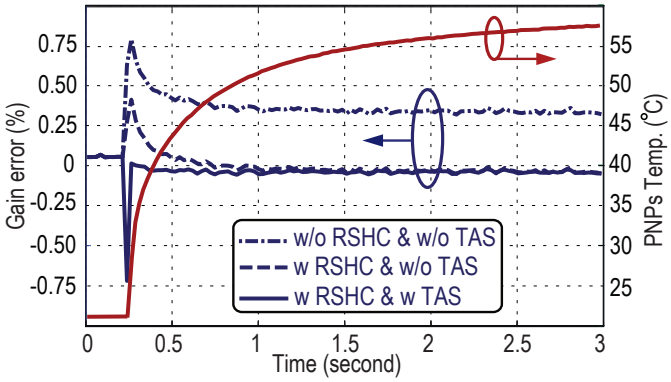

Figure 5.16: Transient temperature and gain error measurement for a 0.1-to-5A current step driven through the shunt (at room temperature).

Table 5.2: Performance summary and comparison with the-state-of-the-art.

	CSS_1	[16]	[17]	[18]	[19]
R_{shunt} [mΩ]	**10**	25	4	38	3
I-range [A]	**±5**	±1.9	±7	±2.5	±2
Gain error [%]	**±0.3**	> ±3	±3	±5	±5
Offset [μV]	**0.16**	15.6	44	760	30
Offset (I) [mA]	**0.016**	0.625	11	20	10
T-range [°C]	**−55 to 85**	0 to 50	−40 to 125	0 to 70	−40 to 85

5.6. Conclusion

The circuit realization and the experimental results of the first prototype CSS with a 10 mΩ on-chip metal shunt resistor have been presented in this chapter. For currents ranging from −5 A to +5 A and over the temperature range of −55°C to +85°C, it exhibits 16 μA offset and a ±0.3% gain error for devices packaged in the HVQFN plastic package and devices directly bonded to the PCB. The error sources in the BGR are effectively suppressed by using chopping and dynamic element matching, while the ADC is made accurate by using correlated-double sampling, system-level chopping and a low-leakage frontend design.

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6

Implementation II

6.1. Introduction[1]

In this chapter, two improved versions of the CSS described in Chapter 5 are presented. In the previous design, the insulating oxide between the metal shunt and the substrate PNPs in CSS_1 gave rise to errors in the estimated T, which were then corrected by an extra calibration step. In a new design (CSS_2), thermal vias between the shunt and the gates of dummy PMOS devices improve (by $\sim 2\times$) the thermal coupling between the shunt and the substrate and reduce shunt self-heating, while preserving galvanic isolation. In Chapter 2, it was shown that the main limitations of an on-chip metal shunt are its large area and long-term drift. The latter can be alleviated by reducing the current range and/or the maximum operating temperature. Although this is acceptable for some applications, a superior solution is to use a lead-frame shunt. This extends the current-sensing range without increasing the die area. This chapter also describes the implementation of CSS_3 which employs the lead-frame of a standard HVQFN32 package as a shunt with a nominal value of 260 $\mu\Omega$ at room temperature.

Compared to CSS_1, in which a single ADC was time-multiplexed between current

[1] This chapter is derived from a journal publication by the author: S. H. Shalmany, D. Draxelmayr, K. A. A. Makinwa, "A ±36 A Integrated Current-Sensing System with 0.3% Gain Error and 400 μA Offset from −55°C to +85°C," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1034−1043, Apr. 2017.

I and temperature T measurements (see Figure 4.2(a)), these new designs use two dedicated ADCs (shown in Figure 4.2(b)). This enables continuous I and T sensing, leading to a faster and more accurate response to large current transients. In addition, by using an energy-efficient current-reuse OTA and fringe capacitors, the readout's power consumption and area are reduced by about 4× and 2× compared to CSS_1, for the same performance.

6.2. Readout Electronics

The circuit diagrams of the readout's building blocks are similar to those in CSS_1. This section, therefore, will very briefly review the operating principles of the readout's building blocks, while mainly emphasizing their improvements.

6.2.1. Bandgap Reference

The simplified circuit diagram of the BGR is shown Figure 6.1. The bias circuit generates a PTAT current $I = 260$ nA (at 27°C) with the help of an opamp and two auxiliary PNPs biased at a 1:p (= 10) current-density ratio (emitter area of a unit PNP $A_E = 10\ \mu m^2$). This current is then mirrored (1:8) to the bipolar core, and used to bias two other PNPs also at a 1:10 current density ratio to generate V_{BE} and ΔV_{BE}. These voltages are then sampled and linearly combined in the $\Delta\Sigma$ ADCs to generate a dynamic reference voltage

$$V_{Ref} = \Delta V_{BE} + \frac{V_{BE}}{\alpha} \approx \frac{V_{g0}}{\alpha} = V_{Ref0}, \tag{6.1}$$

in which the ratio α (= 10), realized by the ADCs' sampling capacitors, results in $V_{Ref} = 120$ mV.

To decrease the spread in I, and hence in V_{BE}, the opamp's offset is reduced by chopping, while ΔV_{BE} is made accurate by dynamically matching both the current sources and the PNPs [1, 2]. In order to prevent the voltage drop across the DEM switches (SW_{DEM}) from corrupting V_{BE} and ΔV_{BE} and then causing significant errors in V_{Ref} and T, Kelvin-connected switches are used [2].

Compared to the design of CSS_1 which generates a PTAT current of 1.4 μA in the bias circuitry, this design generates only 260 nA, while still ensuring the PNPs are biased in the flattest region of current gain β. In addition, the power consumption of the auxiliary amplifier (folded cascode) is reduced from 8.4 μA to about 1.6 μA. By reducing the total capacitive load of the bipolar core from 5.6 pF to 4.1 pF, and significantly reducing the layout parasitic capacitance, the current consumption of the bipolar core is reduced from 11.2 μA to 4.2 μA. Compared to

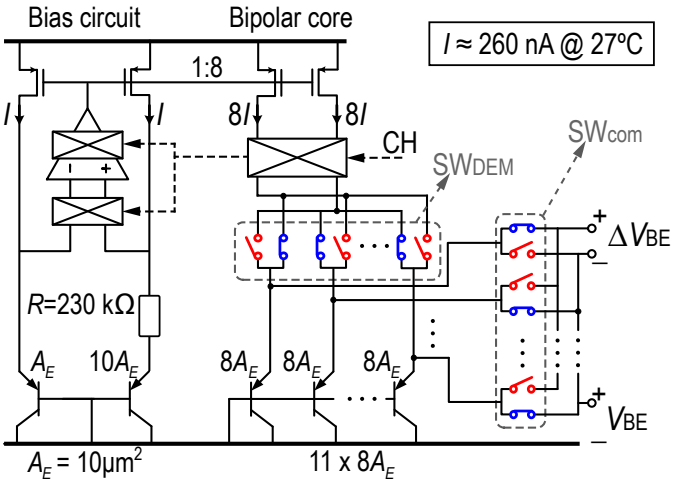

Figure 6.1: Simplified schematic of the BGR consisting of a bias circuit and a bipolar core.

the power consumed in CSS_1, these improvements reduce the BGR's total current consumption by $\sim 4\times$ to 6.5μA.

6.2.2. ADCs

The CSS employs two second-order SC feed-forward $\Delta\Sigma$ ADCs; ADC_I digitizes V_{shunt} and ADC_T digitizes T. Figure 6.2 shows a simplified diagram of ADC_I in which capacitor C_{S1} (= 3 pF) samples V_{shunt}, while capacitors C_{S2} (= 3 pF) and C_{S3} (= 300 fF), sample and accurately combine ΔV_{BE} and V_{BE}, respectively, to generate V_{Ref} [3]. The modulator's feedback is established by using the output bitstream bs_I to control the polarity of the feedback voltages $\pm\Delta V_{\mathrm{BE}}$ and $\pm V_{\mathrm{BE}}$. As explained in Chapter 5 the leakage current of ADC_I's input sampling switches is suppressed by using low-leakage high-V_{th} NMOS transistors whose gates are driven by the lowest available voltage.

Figure 6.3 shows a simplified diagram of ADC_T, in which T is digitized by charge-balancing ΔV_{BE} against $-V_{\mathrm{BE}}/10$. When bs_T is 0, C_{S4} (= 1 pF) samples $+\Delta V_{\mathrm{BE}}$, and when bs_T is +1, C_{S5} (= 100 fF) samples $-V_{\mathrm{BE}}$. This results in an average value of bs_T stated in (4.19). The temperature T in degrees Celsius is then obtain by the linear scaling expressed in Equation (4.6).

Both ADCs are operated at a sampling frequency F_S = 100 kHz. To mitigate the first integrators' offset and $1/f$ noise, CDS and low-frequency chopping (CHL) are used. All four integrators employ current-reuse amplifiers with fringe capacitors.

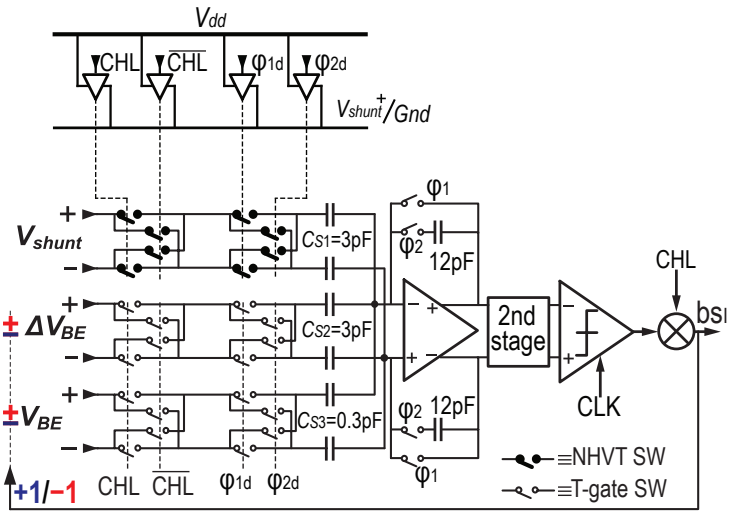

Figure 6.2: Simplified schematic of the current-sensing ADC (ADC_I).

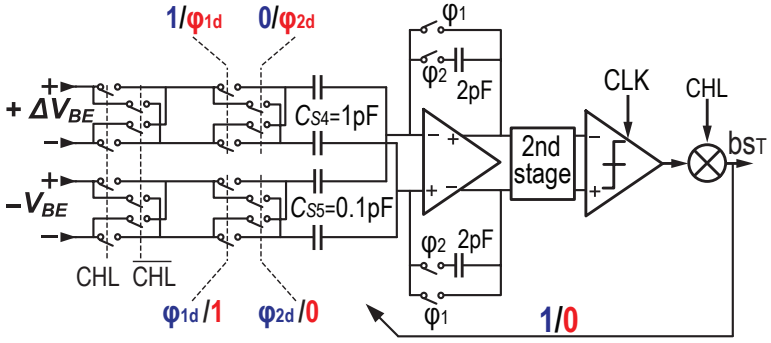

Figure 6.3: Simplified schematic of the temperature-sensing ADC (ADC_T).

Current-Reuse OTA

In a current-reuse OTA, both NMOS and PMOS contribute to the OTA's transconductance while sharing the same bias current. Unlike the folded-cascode OTAs, their telescopic implementations also eliminate the need for an extra output branch. In addition, their input-pair devices are the only dominant noise sources, resulting in the OTA noise factor $\gamma = 1$. These make current-reuse OTAs potentially $\sim 4\times$ more power-efficient than the folded-cascode OTAs, and hence attractive for use in power-constraint applications.

In [4], Chae proposes the use of two-transistor inverters, shown in Figure 6.4(a),

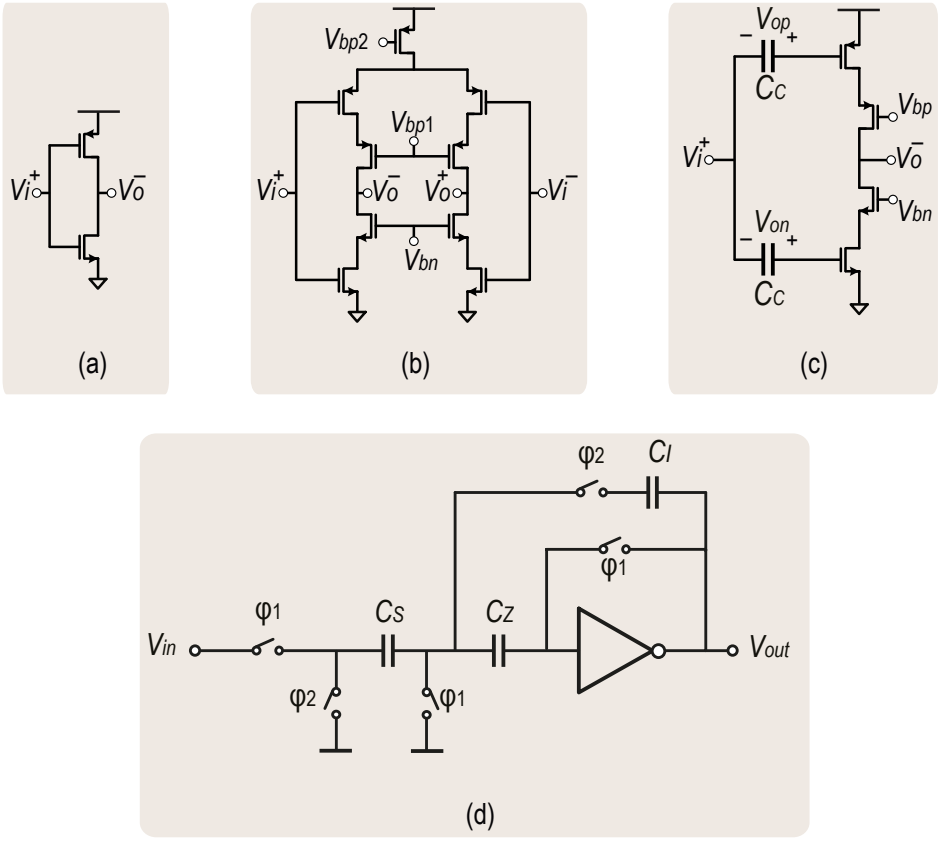

Figure 6.4: Current-reuse OTAs presented in (a) [4], (b) [5], and (c) [6]. (d) A simplified single-ended version of the integrator.

to design power-efficient sub-1V SC $\Delta\Sigma$ ADCs. An integrator is then built around two inverters in a pseudo-differential configuration. A simplified single-ended version of the integrator is shown in Figure 6.4(d), in which an auto-zeroing capacitor C_Z is used to mitigate the effect of the inverter's offset and flicker noise as well as the supply variation. Not being biased with a fixed current source, this structure facilitates class-AB operation and is, therefore, very power-efficient. This simple OTA, however, suffers from a number of drawbacks, namely: 1) limited DC gain, 2) a relatively poor power supply rejection ratio(PSRR), and 3) sensitivity to PVT variations, i.e., the devices' bias current and their operational region are strongly dependent on the supply voltage.

As shown in Figure 6.4(b), using a current-starved cascode inverter, [5] boosts

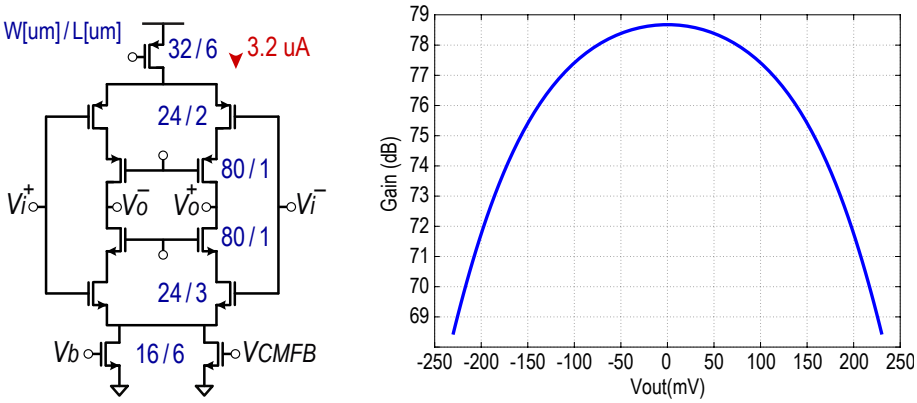

Figure 6.5: ADC_I first integrator's current-reuse OTA and its DC gain at +125°C, fast process corner, and V_{dd} = 1.5 V − 10%.

both the OTA's DC gain and its tolerance to PVT variations. This, however, comes at the expense of the output voltage swing and the loss of class-AB operation. These issues are addressed in [6] by eliminating the PMOS tail current source, and instead separating the common-mode voltage of the PMOS and the NMOS input pairs by means of two dedicated auto-zeroing capacitors (see Figure 6.4(c)). During the auto-zeroing phase, these capacitors sample the bias voltages V_{op} and V_{on} for a well-defined input bias current level. Doing so retains the class-AB operation at a defined input quiescent current. Although this OTA provides high DC PSRR, it suffers from a relatively poor AC PSRR, particularly at frequencies beyond the its sampling frequency. In addition, in the three above-mentioned topologies, the auto-zeroing capacitors contribute to the input-referred noise. This is minimized in [6] by choosing $C_Z = 3C_S$, which comes at the cost of excess die area.

By taking advantage of the small-swing input voltage of the CSSs, which does not require class-AB OTAs with high output voltage swing, we propose the use of the current-starved cascode current-reuse OTA shown in Figure 6.5 [7]. This OTA eliminates the need for the explicit auto-zeroing capacitors and can provide a relatively better PSRR. Its limited output voltage swing and hence nonlinear DC gain, however, can introduce error in the ADCs' characteristics. For instance, the worst-case DC gain of this OTA versus the output swing is plotted in Figure 6.5, exhibiting more than 6dB variation over a ±200 mV output range[2].

The effect of this worst-case non-linearity on ADC_I is behaviouraly simulated in MATLAB over different values of V_{shunt}. Histograms of the first integrator's output

[2]This occurs at a fast process corner, +125°C, and V_{dd} = 1.5 V − 10%.

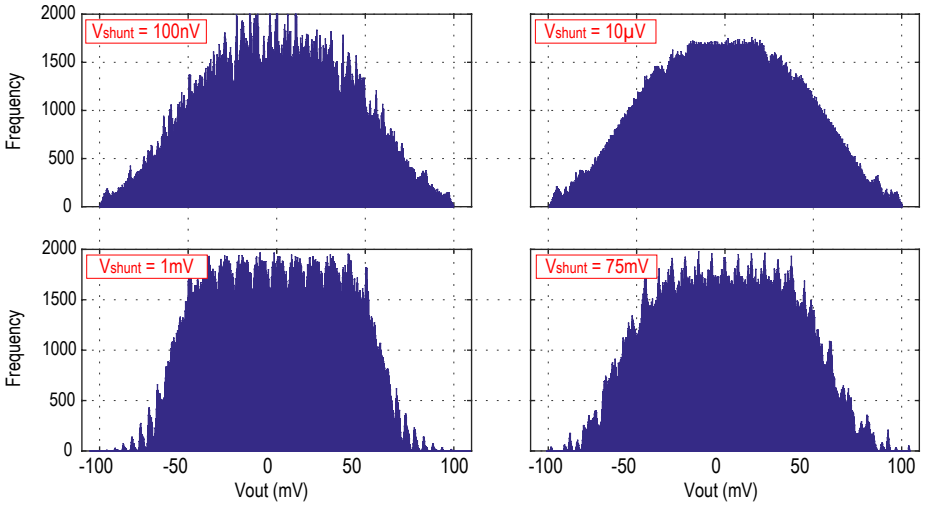

Figure 6.6: Histograms of ADC_I's first integrator's output swing for different V_{shunt} (a thermal noise with a density of 300 nV/$\sqrt{\mathrm{Hz}}$ was considered at the ADC_I's input).

are plotted in Figure 6.6, showing a maximum value of around 100 mV. It should be noted that the output voltage swing can be controlled by properly sizing the integration capacitor (C_{I1} = 12 pF). As shown in Figure 6.7, the resulting error versus V_{shunt} is well below a conservative error budget of 50-nV offset and 0.1% gain error. The scaled versions of this OTA are used in ADC_T and at the second integrators. A similar simulation for ADC_T shows a maximum temperature-sensing error of 2 mK. These confirm the feasibility of the proposed current-reuse OTAs for use in the CSSs.

6.3. Measurement results

The CSSs were realized in a standard 0.13 μm CMOS process (Figure 6.8). They occupy 0.85 mm^2 (CSS_2 with on-chip shunt) and 0.4 mm^2 (CSS_3 with lead-frame shunt) and draw 13 μA from a 1.5 V supply. BGR, ADC_I and ADC_T consume 6.5 μA, 4.3 μA, and 2.2 μA, respectively. For flexibility, the digital backend and decimation filter were implemented off-chip.

The ADCs' output PSDs show that they are kT/C-noise limited up to a bandwidth of 400 Hz (Figure 6.9). Note that the rise in the thermal noise floor and the tones at 50-Hz harmonics in ADC_I at I = 5 A are caused by the current source used

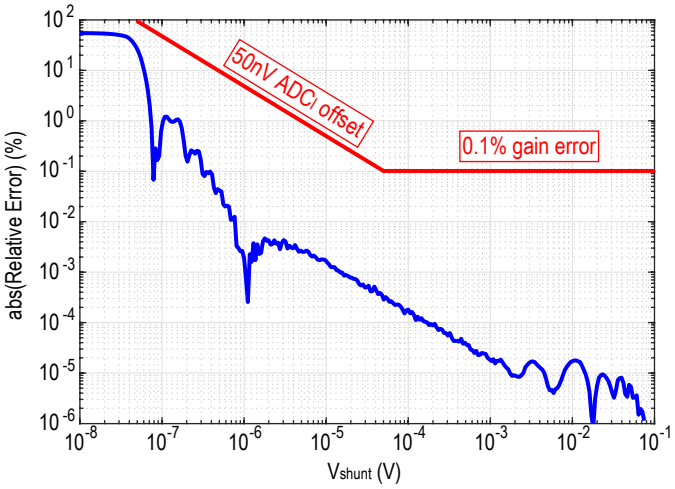

Figure 6.7: ADC_I's relative error due to non-linearity and finite DC gain of its first integrator's OTA.

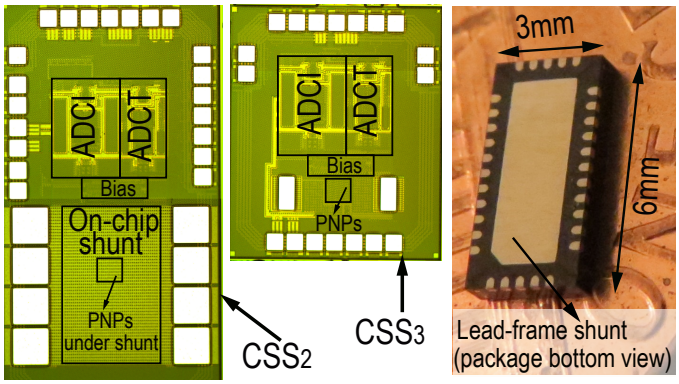

Figure 6.8: Chip micrograph and HVQFN package.

in the experiment[3]. In a conversion time T_{conv} of 18 ms, ADC_I and ADC_T achieve 1.4 μV_{rms} and 10 mK_{rms} resolution, respectively.

Fifteen HVQFN-packaged samples of CSS_2 and five samples of CSS_3 were tested from -55 to $+85$°C. Before using CHL, the measured offset of both CSSs' ADC_I is less than 6 μV (Figure 6.10). After using CHL, the offset drops below 40 nV (4 μA) and 110 nV (400 μA) in CSS_2 and CSS_3, respectively. The larger offset for CSS_3 can be attributed to its bond wires of the lead-frame shunt, forming a relatively larger input ground loop and making CSS_3 more susceptible to external

[3]This is confirmed by applying a low-noise external voltage to the ADC_I's input.

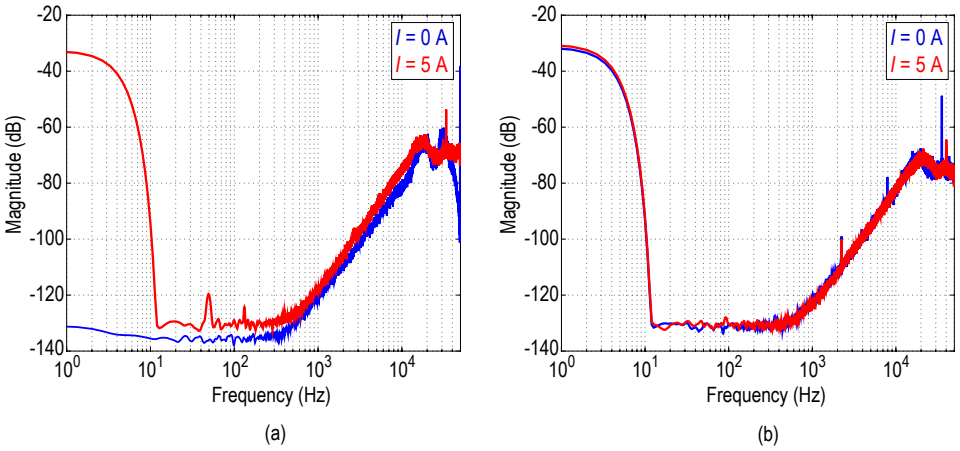

Figure 6.9: Power spectral density (PSD) of (a) ADC_I, and (b) ADC_T output bitstream at DC currents of 0 and 5A.

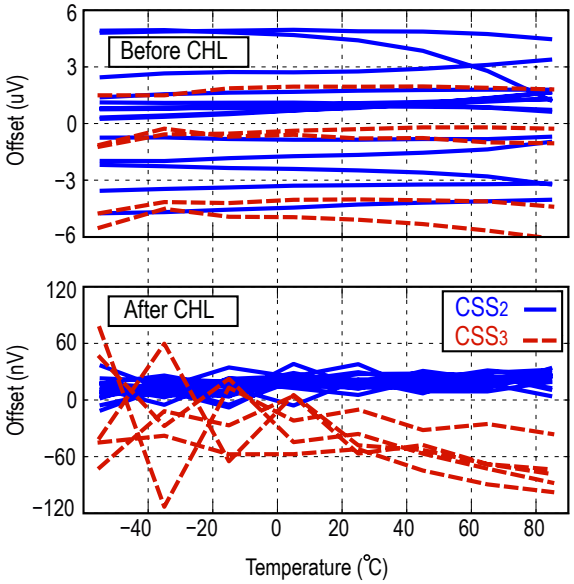

Figure 6.10: ADC_I's offset over temperature, before (top) and, after (bottom) using CHL.

interference. Compared to CSS_1, CSS_2 shows 4× lower offset. This is believed to be because of more carefully following the layout guidelines explained in Chapter 5 for CSS_2. The ADCs' input sampling capacitors also show a maximum spread of up to ±0.05%, which as explained in Chapters 4, does not need to be explicitly corrected.

The parameters obtained from the batch calibration are available in Table 6.1.

Table 6.1: Batch-calibration data.

Parameter	Value (on-chip shunt)	Value (lead-frame shunt)
V_{Ref0}	121.12 [mV]	121.35 [mV]
A	611.435 [1/°C]	610.262 [1/°C]
B	−274.92 [°C]	−274.83 [°C]
T_0	32.83 [°C]	27.48 [°C]
α_1	0.3362 [%/°C]	0.2578 [%/°C]
α_2	-5.619×10^{-5} [%/°C^2]	$+1.31\times10^{-5}$ [%/°C^2]

Figure 6.11 illustrates the nonlinearities and the spread of V_{Ref} and the temperature sensor, as well as the nonlinearity of the calibrated R_{shunt}, after the batch calibration but before the nonlinearity correction. The variation of V_{Ref} is about 1%, while the spread among chips is about ±0.1%. The resulting curvature in the temperature sensor's output is about 1°C, with a spread of less than ±0.3°C. As described in Section 4.4.2, the spread of V_{Ref} and the temperature sensor are absorbed in the shunt calibration process, while their nonlinearity, together with the shunt's TCR, are digitally compensated by a *single* second-order polynomial, as they are quite stable in the process used [2, 8]. After a linear temperature compensation, the on-chip R_{shunt} exhibits a distinct second-order curvature of about 0.2% and a spread of ±0.15%, while the lead-frame shunt has negligible nonlinearity but a spread of ±0.15%.

Measurements show that the on-chip shunt spreads by up to ±2.5%. After calibrating it (at +3 A and at room temperature) and with temperature compensation, CSS_2 achieves a ±0.3% gain error from −55 to +85°C, and over a ±5 A range (Figure 6.12). This figure clearly shows the effect of the improved shunt-PNP thermal coupling compared to that in CSS_1; there is no need to use the residual self-heating compensation (RSHC) scheme in CSS_2 as it only marginally improves the gain error to ±0.25%. After calibrating the lead-frame shunt (at +5 A and at room temperature) and with temperature compensation, CSS_3 achieves a similar gain error of ±0.3% over a ±36 A range (Figure 6.14). It is worth mentioning that the gain error of both CSSs is dominated by the spread in the shunts' TCR (±0.15%, shown in Figure 6.11). As shown in Figure 6.13 and 6.15, applying a first-order temperature correction results in noticeably larger gain errors compared to applying a second-order one. This confirms that second-order temperature correction is necessary to achieve an accurate current sensing.

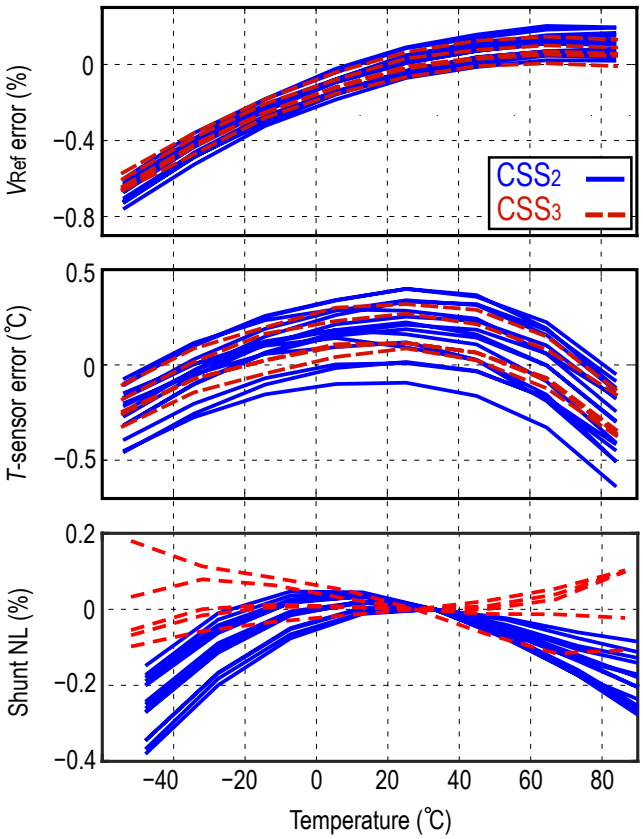

Figure 6.11: Error in V_{Ref} (top), the temperature sensor (middle), and the nonlinearity in the shunt resistor (bottom).

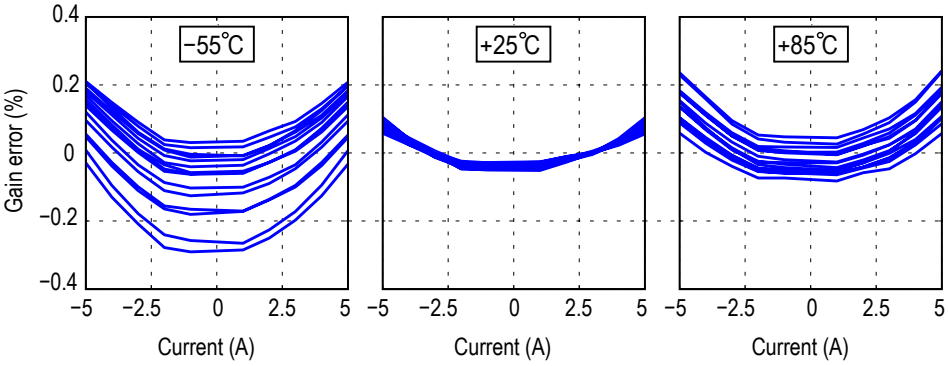

Figure 6.12: CSS_2 (with on-chip shunt) gain error at three ambient temperatures.

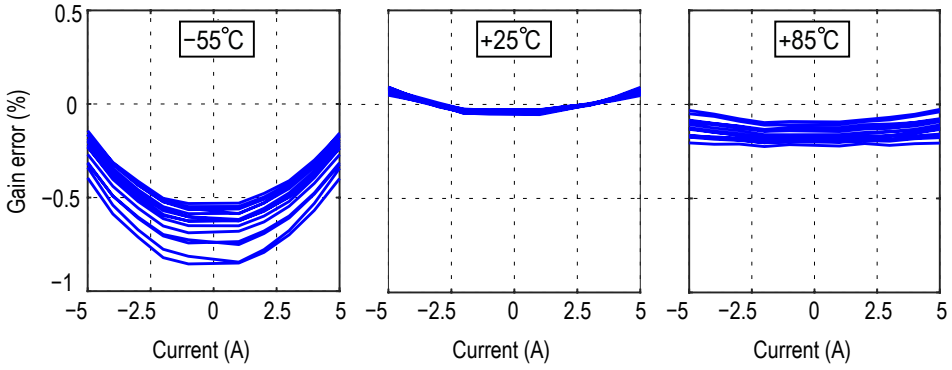

Figure 6.13: CSS_2 (with on-chip shunt) gain error with first-order temperature compensation.

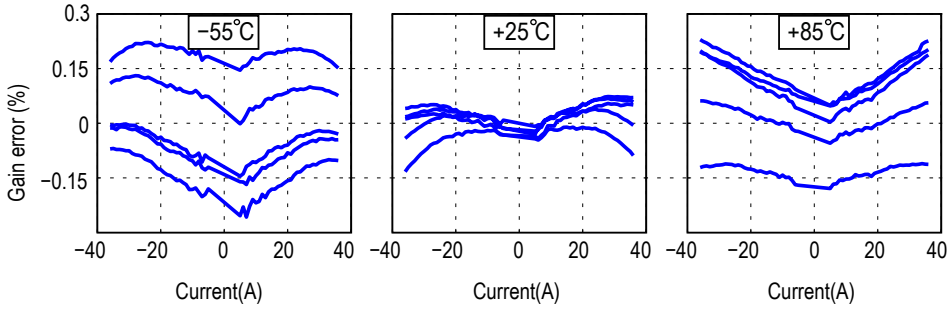

Figure 6.14: CSS_3 (with lead-frame shunt) gain error at three ambient temperatures.

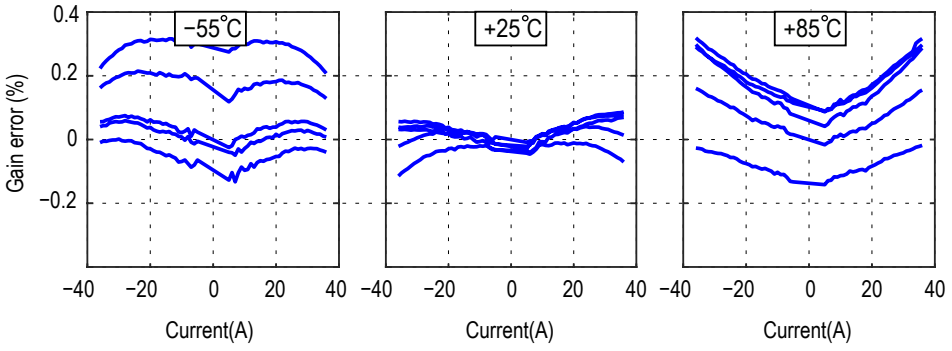

Figure 6.15: CSS_3 (with lead-frame shunt) gain error with first-order temperature compensation.

The batch-calibration data for the results shown in Figure 6.12 are determined by averaging the data obtained from all 15 samples of CSS_2. To demonstrate the robustness of the proposed calibration method, Figure 6.16 shows the current-sensing

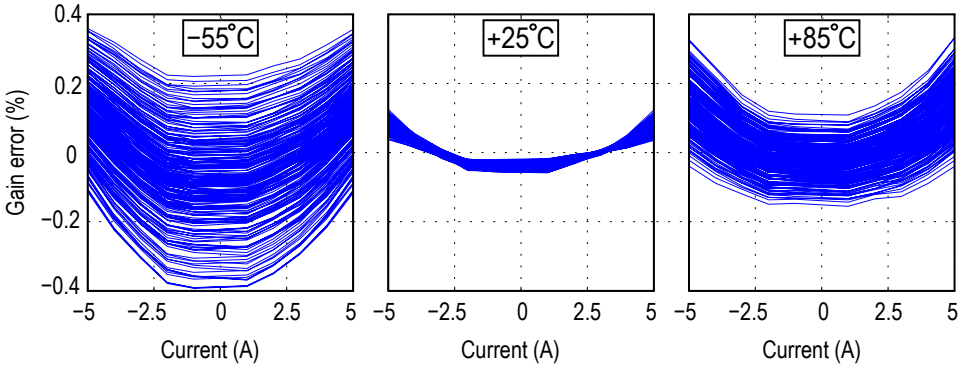

Figure 6.16: CSS_2 (with on-chip shunt) gain error at three ambient temperatures, in which the batch-calibration data are obtained from measurements on *one* sample.

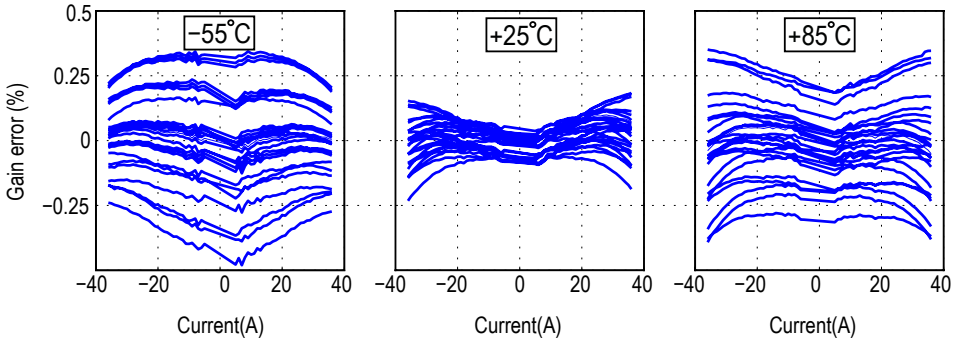

Figure 6.17: CSS_3 (with lead-frame shunt) gain error at three ambient temperatures, in which the batch-calibration data are obtained from measurements on *one* sample.

gain error, for the case when this data are obtained by measurements on one sample. The data is then used to calibrate all 15 samples. It can be seen that the gain error is then slightly larger, but is always less than ±0.4%. Applying the same calibration process to CSS_3 results in a maximum gain error of ±0.5% (see Figure 6.17).

The dynamic accuracy of both CSSs was evaluated with a 5 A step and at T_{conv} = 18 ms (Figure 6.18). Over a 9 s measurement time, this causes a temperature rise of ∼20°C and ∼1°C in CSS_2 and CSS_3, respectively. Unlike CSS_1, which shows an additional error of up to 0.7% in transient, both CSSs maintain their accuracy throughout the current step. This demonstrates the advantage of the dual-ADC design, which enables continuous current and temperature sensing.

A performance summary and a comparison with the state-of-the-art are shown in Table 6.2. Compared to [9–12], CSS_2 improves the offset by $> 100\times$ and the

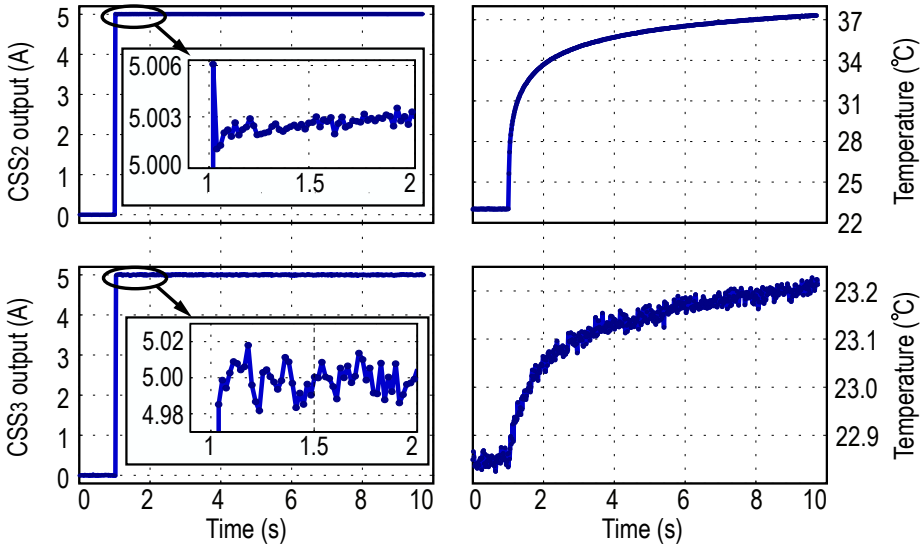

Figure 6.18: Transient temperature and gain error measurement for a 5 A current step driven through the shunt at room temperature in CSS_2 (top), and CSS_3 (bottom).

accuracy by $> 10\times$. In addition, compared to our CSS_1, it achieves $4\times$ lower offset and a similar gain error despite using a simpler calibration scheme and $4\times$ lower power. Compared to [12, 13], CSS_3 represents a significant increase in current handling capability ($> 2\times$), accuracy ($> 10\times$) and dynamic range ($> 25\times$). The large gain error in [9–13] is mainly due to the shunt TCR and poor temperature compensation, while the offset is limited by the readout electronics. To improve gain error, recently a stand-alone current sensor employing an in-package shunt made from alloy with a low TCR (< 25ppm/°C) has been reported [14]. Nevertheless, even with the help of this expensive custom shunt, it only achieves an offset of 50 mA and a gain error of $\pm 0.75\%$ over a ± 10 A current range. An improved version of this product, released after the conclusion of our research in the year 2016, shows a gain error of $\pm 0.5\%$ and an offset of 5 mA over the same current range [15]. Another design [16], also released in 2016, uses proprietary techniques to compensate for the shunt TCR, achieving an offset of 9 mA and gain error of $\pm 1\%$ over a ± 30 A current range. However, despite the use of a standard (high-TCR) lead-frame shunt, CSS_3 achieves $> 10\times$ lower offset and $> 2\times$ better accuracy compared to [14–16]. These results demonstrate that by combining precision readout electronics and good thermal design, an accurate fully integrated CSS can be realized with the help of a standard lead-frame shunt.

Table 6.2: Performance summary and comparison with the-state-of-the-art.

	R_{shunt} [mΩ]	I-range [A]	Gain error [%]	Offset [μV]	Offset [mA]	T-range [°C]
CSS_2	10	±5	0.3	0.04	0.004	−55 to 85
CSS_1	10	±5	0.35	0.16	0.016	−55 to 85
[9]	3	±2	> 5	30	10	−40 to 85
[10]	25	±1.9	> 3	15.6	0.625	0 to 50
[11]	38	±2.5	> 5	760	20	0 to 70
[12]	4	±7	3	44	11	−40 to 125
CSS_3	0.26	±36	0.3	0.12	0.4	−55 to 85
[13]	1.3	±15	> 3	−−	−−	−40 to 85
[14]	2	±10	0.75	100	50	−40 to 125
[15]	2	±10	0.5	10	5	−40 to 125
[16]	0.30	±30	1	2.7	9	−40 to 85

6.4. Conclusion

The design and the experimental results of two prototype CSSs are presented: 1) CSS_2 with a 10 mΩ on-chip metal R_{shunt}, and 2) CSS_3 with a 260 $\mu\Omega$ lead-frame R_{shunt}. By using an energy-efficient design methodology and fringe capacitors, the power consumption and the area of the readout electronics are reduced by about 4× and 2× compared to that in CSS_2. In addition, over a ±5 A current range, CSS_2 reduces the maximum offset to only 4 μA and the maximum gain error to ±0.3%. In order to eliminate the large die area needed for the on-chip shunt (> 50% of the total area) and to enhance the shunt reliability, CSS_3 makes use of the lead-frame resistance of a HVQFN32 plastic package. For currents ranging from −36 A to +36 A and over a temperature range of −55°C to +85°C, CSS_3 exhibits a maximum offset of 400 μA and a maximum gain error of ±0.3%. Compared to the state-of-the-art (see Table 6.2), this level of performance represents a significant increase in current handling capability, accuracy (> 2×) and dynamic range (> 10×) despite the use of a standard lead-frame shunt.

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7

Main Findings and Future Work

In this thesis, a number of precision low-cost integrated shunt-based current-sensing systems (CSSs) have been described. Low cost is achieved by the use of chip-compatible shunts: 1) a 10-mΩ on-chip metal shunt resistor for a $\pm$5-A CSS, and 2) a 260 $\mu\Omega$ lead-frame shunt of standard HVQFN32 plastic package for a $\pm$36 A CSS implementation. Compared to the state-of-the-art [1–8], these CSSs significantly improve the current-sensing gain error and offset despite the use of these high-TCR shunts (see Table 6.2). This level of performance is enabled by: 1) nanovolt-offset ADCs, 2) good thermal coupling between the shunt and the temperature sensor, and 3) a calibration scheme which explicitly calibrates the shunt's spread and its TCR, while substantially mitigating the effect of several critical error sources of the readout electronics. It should be noted that the various parameters for shunt temperature compensation are obtained from a batch calibration (see 4.4).

The main findings and future work of this thesis are outlined in the following sections.

7.1. Main Findings

The main findings of this work are listed below:

- The metal layers of a silicon die can be used to realize the shunt resistor of

a low-cost integrated current-sensing system. The shunt's spread is corrected with a room temperature calibration while its large temperature coefficient of resistance (TCR $\approx 0.35\%/°C$) is counteracted by a digital temperature compensation scheme. This involves measuring the shunt's temperature with an on-die temperature sensor (PNPs of the bandgap circuitry) and then correcting for its known TCR in the digital domain.

- Good thermal coupling between the shunt and the temperature sensor is essential to accurately measure and thus compensate for the shunt's Joule heating. In order to ensure good thermal coupling, PNPs are positioned directly under the shunt, and thermal vias from all the shunt's metal layers are connected to the gates of dummy PMOS transistors.

- The lead-frame of a package can be used to implement the shunt resistor. Compared to the on-chip metal shunt, this costs no extra die area and increases both the shunt's current range (± 36 A in this work) and robustness since typical lead-frames are orders of magnitude thicker than on-die metal layers.

- Many significant error sources in the presented CSSs do not need to be explicitly calibrated. Neither the PTAT error and the curvature in V_{BE} nor the mismatches among the ADC's sampling capacitors are explicitly corrected. Instead, R_{shunt} spread and other static errors are corrected with a room temperature calibration, whereas the shunt's nonlinear TCR and V_{BE} curvature are corrected with a fixed polynomial established by a batch calibration. It is shown that this approach effectively compensates for all the major sources of error. It significantly simplifies both the circuit implementation and the calibration of the CSS, and thus reduces its production cost.

- Implementing a low-offset (< 100 nV) ADC requires a precision layout floorplan. In this work, the BGR and the ADC are symmetrically laid out normal to the shunt's current direction with the system-level chopper as close as possible to the signal source. Symmetric and differential routing of the clock signals in a shielded clock channel with low-area return current loops also helps to minimize the digital interference with the sensitive analog signals.

7.2. Future work

Several items are suggested as future work based on this thesis:

- The robustness of the lead-frame shunt to electromigration should be experimentally investigated and compared to that of an on-chip metal shunt.
- The package stress effect on the lead-frame shunt and the potential ageing of R_{shunt} needs to be studied. This effect can be particularly important for lead-frame shunt since it is directly soldered to the board.
- A custom lead-frame shunt could be designed 1) to realize a larger shunt resistance and achieve better offset and resolution, or 2) to ensure that the sensing section, i.e., the section between the Kelvin contacts, is located at some distance from the actual soldering pins of the package [9]. This will help to prevent shifts in the orientation of the heatsink on the PCB from causing changes in $R_{\text{shunt}}(T_0)$, therefore avoiding the need for the end-user to calibrate R_{shunt} after mounting the samples on a PCB.
- The robustness of the proposed calibration scheme to errors in the PNP's current density ratio Δp could be experimentally validated.
- By taking advantage of the fact that V_{shunt} is quite small (tens of millivolts), especially when using a small-value lead-frame shunt, a continuous-time $\Delta\Sigma$ modulator based on an open-loop g_m-C first integrator could be used to implement ADC_I. Thanks to its anti-aliasing filtering effect, this topology should be more power-efficient than its SC counterpart, and is expected to exhibit good linearity since its input voltage will be quite small.

This list motivates further research on precision low-cost integrated shunt-based current-sensing systems.

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A

Appendix

In this Appendix, the sensitivity of the current-sensing accuracy with respect to various error sources, presented in Section 4.4.2, is calculated.

Combining (4.47), (4.53), (4.54) and (4.55) leads to:

$$I'(T) = I \times \left[1 - \left(\alpha \frac{k}{q} \ln(p)\delta_p + \lambda\delta_{\alpha I} + \frac{V_{g0}}{T_c}\delta_1\right)\frac{(T - T_0)}{V_{g0}}\right] \times \left[\frac{1 + \alpha_1 \cdot (T - T_0)}{\left(1 + \alpha_1 \cdot (T_0 - A\mu'_T(T_0))\right) \times \left(1 + \alpha_1 \cdot (A\mu'_T(T) - T_0)\right)}\right]. \tag{A.1}$$

The CSS gain error is

$$\epsilon(T) = \frac{I'(T) - I}{I}. \tag{A.2}$$

Assuming that these terms are much smaller than 1 ($\delta_i \ll 1$), the resulting current-sensing inaccuracy due to each error term is calculated as:

$$\epsilon^{\delta_g}(T) = 0, \tag{A.3}$$

$$\epsilon^{\delta_{\alpha I}}(T) = \frac{\lambda\big(T - T_0\big)}{V_{g0}}\delta_{\alpha I}, \tag{A.4}$$

$$\epsilon^{\delta_{\alpha T}}(T) = 1 - \frac{1 + \alpha_1\big(T - T_0\big)}{\Big(1 - \alpha_1 T_0\Big(1 - \frac{\lambda T_0}{V_{g0}}\Big)\delta_{\alpha T}\Big)\Big(1 + \alpha_1\big(T - T_0\big) + \alpha_1 T\Big(1 - \frac{\lambda T}{V_{g0}}\Big)\delta_{\alpha T}\Big)}, \tag{A.5}$$

$$\epsilon^{\delta_0}(T) = 1 - \frac{1 + \alpha_1(T - T_0)}{\Big(1 + \alpha_1 T_0\delta_0\Big)\Big(1 + \alpha_1(T - T_0) - \alpha_1 T\delta_0\Big)}, \tag{A.6}$$

$$\epsilon^{\delta_1}(T) = 1 - \frac{\Big(1 - \frac{T - T_0}{T_c}\delta_1\Big)\big(1 + \alpha_1(T - T_0)\big)}{\Big(1 + \frac{\alpha_1 T_0^2}{T_c}\delta_1\Big)\Big(1 + \alpha_1\big(T - T_0\big) - \frac{\alpha_1 T^2}{T_c}\delta_1\Big)}, \tag{A.7}$$

and,

$$\epsilon^{\delta_p}(T) = 1 - \frac{\Big(1 - \alpha\frac{k}{q}\big(T - T_0\big)\ln(p)\frac{1}{V_{g0}}\delta_p\Big)\Big(1 + \alpha_1\big(T - T_0\big)\Big)}{\Big(1 - \alpha_1 T_0\Big(1 - \frac{\lambda T_0}{V_{g0}}\Big)\delta_p\Big)\Big(1 + \alpha_1\big(T - T_0\big) + \alpha_1 T\Big(1 - \frac{\lambda T}{V_{g0}}\Big)\delta_p\Big)}, \tag{A.8}$$

The sensitivity of this gain error to each error term over temperature is expressed as:

$$S_{\delta_i}^{\epsilon(T)}(T) = \frac{\partial\epsilon(T)}{\partial\delta_i}, \tag{A.9}$$

which results in the following expressions:

$$S_{\delta_g}^{\epsilon(T)}(T) = 0, \tag{A.10}$$

$$S_{\delta_{\alpha I}}^{\epsilon(T)}(T) = \frac{\lambda\big(T - T_0\big)}{V_{g0}}, \tag{A.11}$$

$$S_{\delta_{\alpha T}}^{\epsilon(T)}(T) = \frac{\alpha_1 T\Big(1 - \dfrac{\lambda T}{V_{g0}}\Big)}{1 + \alpha_1\big(T - T_0\big)} - \alpha_1 T_0\Big(1 - \frac{\lambda T_0}{V_{g0}}\Big), \tag{A.12}$$

$$S_{\delta_0}^{\epsilon(T)}(T) = \alpha_1\Big(T_0 - \frac{T}{1 + \alpha_1\big(T - T_0\big)}\Big), \tag{A.13}$$

$$S_{\delta_1}^{\epsilon(T)}(T) = \frac{1}{T_c}\Big(\frac{\alpha_1 T^2}{1 + \alpha_1\big(T - T_0\big)} - \alpha_1 T_0^2 - \big(T - T_0\big)\Big), \tag{A.14}$$

and,

$$S_{\delta_p}^{\epsilon(T)}(T) = \frac{\alpha_1 T\Big(1 - \dfrac{\lambda T}{V_{g0}}\Big)}{1 + \alpha_1\big(T - T_0\big)} - \alpha_1 T_0\Big(1 - \frac{\lambda T_0}{V_{g0}}\Big) + \frac{\alpha\dfrac{k}{q}\big(T - T_0\big)\ln(p)}{V_{g0}}, \tag{A.15}$$

These sensitivities versus temperature are plotted in Figure 4.12.

Summary

Coulomb counting is a widely used method to estimate battery state-of-charge (SoC). It involves measuring and integrating the battery's current to determine its net charge flow.

As explained in Chapter 1, the overall accuracy of a Coulomb counter is primarily determined by the accuracy of its current-sensing system (CSS). The offset of this CSS should be well below the battery's self-discharge rate ($\approx 50\ \mu$A for hand-held device). A gain error of less than $\pm 0.5\%$ for currents up to a few Amperes and over the industrial temperature range ($-40°$C to $+85°$C) is required to facilitate an accurate estimation of battery SoC. A resolution of better than 14 bits (0.01%) over a 25-ms conversion time is needed for rapid calibration. In addition, an integrated and CMOS-compatible CSS with digital output enables the realization of a small and cost-effective fuel gauge system. Finally, in order to minimize the power overhead, the power consumption of the CSS should be kept below the battery self-discharge rate. Based on their operating principles, current sensors are divided into two categories: 1) magnetic field sensors, and 2) shunt-based current sensors. Magnetic field sensors are generally not suited for use in Coulomb counters. Rogowski coils and current transformers are not suitable for DC and/or small (sub-milliampere) current measurement. Fluxgates and magneto-resistors, which are able to measure small DC currents, require backend processing due to their use of ferromagnetic materials. In addition, fluxgates require large excitation currents to saturate their cores, and therefore dissipate several tens of milliwatts. Hall-effect sensors draw similar amounts of current, but are at least CMOS-compatible. Due to their limited sensitivity, however, Hall sensors are not suitable for sensing small (sub-milliampere) currents. On the other hand, shunt-based sensors, which sense current by measuring the voltage drop across a shunt resistor are widely used in Coulomb counters. Their simplicity results in greater accuracy and resolution, making them amenable to integration. CSSs based on *external* shunt resistors can achieve gain errors better than $\pm 0.1\%$; however, the extra cost and size of this approach is not acceptable for a battery fuel gauge system. As of 2011 (when this research began), sensors based on *integrated* shunt resistors only achieved gain errors of $>\pm 3\%$ and current offsets

of several milliamperes. Their gain error is mainly due to inadequate compensation of the shunt resistor's spread and temperature coefficient of resistance (TCR), while their current offset is limited by the readout electronics. To improve the gain error to better than 1%, several designs realized the shunt from low-TCR (< 20 ppm/°C) alloys, such as Constantan, Manganin, or Evanohm. However, a custom process is still needed to accommodate the shunt, which increases production costs. The objective of this thesis is therefore defined as realizing an *integrated*, *precision* and *low-cost* shunt-based CSS for use in the Coulomb counter of portable devices.

In Chapter 2, different ways of implementing a shunt resistor are reviewed, and two types are chosen for use in this work. It is explained that precision off-chip resistors are too expensive, whereas the low-cost ones suffer from large TCR and poor thermal coupling to the temperature sensor. In addition, they are typically too bulky, and hence not feasible for integration in portable devices. The in-package shunts offer a compact and potentially low-cost solution; shunts based on a standard package lead-frame and RDL layers are the most promising of this kind. We propose the use of 1) a 10 mΩ on-chip metal shunt resistor, and 2) the heatsink lead-frame of an HVQFN32 to implement a 260 $\mu\Omega$ resistor. Although the lead-frame shunt results in rather small shunt voltages for the target 5 A CSS (leading to excess offset and noise), it demonstrates the feasibility of lead-frame shunts for high current-sensing applications, e.g., automotive. Being compatible with standard CMOS processes and standard packaging technology, the former is used for $\pm$5 A current sensing, while the latter is used for $\pm$36 A current sensing, both with a gain error of better than $\pm$0.5%.

Chapter 3 deals with shunt temperature compensation. The effect of the shunt TCR is counteracted by a digital temperature compensation scheme which involves measuring the shunt's temperature and then correcting for its known TCR in the digital domain. It is discussed that the substrate PNPs available in standard CMOS processes is an optimal choice for the CSS's temperature sensing element. These PNPs are also reused to generate the required CSS's reference voltage. The thermal coupling between the shunt and the temperature sensor, which is essential for an accurate shunt temperature compensation, is studied and enhanced by means of electro-thermal simulation in COMSOL. Due to electromigration, however, the on-chip shunt resistor exhibits significant (0.1%) drift after long-term (24 day) testing at high temperatures (+85°C) and currents (5 A DC). This can be mitigated by reducing the current density and temperature of the shunt, either by increasing its area, or by reducing its maximum operating current and/or temperature. Another

drawback of the on-chip shunt is the large silicon area required. These two problems are circumvented by employing the resistance of the *already available* lead-frame in many *standard* IC packages, e.g., an HVQFN32 plastic package. This costs no extra die area and increases both the shunt's current range and robustness since typical lead-frames are orders of magnitude thicker than on-die metal layers.

Chapter 4 presents the system-level design of the readout electronics, the ADCs and the bandgap reference (BGR). The substrate PNPs are used in the BGR to sense shunt's temperature and to generate the CSS's reference voltage. Driven by the resolution requirements, the ADCs are chosen as second-order switched-capacitor $\Delta\Sigma$ modulators. Significant error sources of these two building blocks, together with the solutions proposed by the prior art, are explained. In contrast to the prior art, we propose a much simpler solution which essentially only calibrates the non-idealities of the shunt. We show that this calibration scheme reduces the effect of many readout electronics errors to a negligible level without *explicitly* correcting for them. This significantly simplifies both the circuit implementation and the calibration of the CSS, thus reducing the production cost.

Three prototype CSSs together with their measurement results are described in this dissertation. The first one (CSS_1), covered in Chapter 5, consists of a 10 mΩ on-chip metal shunt, an ADC and a BGR. It employs a single ADC for both current and temperature sensing in a time-multiplexed manner. This design, realized in a standard 0.13-μm CMOS process, occupies 1.15 mm^2 and draws 55 μA from a 1.5-V supply. For currents ranging from -5 A to $+5$ A and over a temperature range of -55°C to $+85$°C, it exhibits a maximum offset of 16 μA and a maximum gain error of $\pm 0.3\%$. This level of accuracy is clearly in line with the objective of this thesis, and is achieved by means of an accurate shunt temperature compensation scheme, multiple dynamic error correction techniques, and a simple calibration scheme.

Chapter 6 presents the other two designs, which achieve an improved performance with a reduced die area (by 2×) and power consumption (by 4×), compared to CSS_1. In order to accurately track fast temperature transients in the shunt, two separate ADCs for current and temperature sensing are employed. The first design (CSS_2) is based on a 10 mΩ on-chip shunt, while the second one (CSS_3) employs the 260 $\mu\Omega$ lead-frame resistance of a HVQFN32 plastic package. Both designs are realized in a standard 0.13 μm CMOS process and draw 13 μA from a 1.5 V supply. For currents ranging from -5 A to $+5$ A and over a temperature range of -55°C to $+85$°C, CSS_2 exhibits a maximum offset of 4 μA and a maximum gain error of $\pm 0.3\%$. Over the same temperature range and for currents ranging from -36 A

to +36 A, CSS_3 exhibits a maximum offset of 400 μA and a maximum gain error of $\pm 0.3\%$. Compared to the state-of-the-art, this level of performance represents a significant increase in current handling capability, accuracy and dynamic range despite the use of a standard on-chip and lead-frame shunts.

Finally, Chapter 7 concludes the thesis, summarizes its original contributions and comments on future work. The future work proposed includes: 1) experimentally investigating the robustness of the lead-frame shunt to electromigration, 2) customizing the lead-frame to adjust its resistance value, 3) employing continuous-time $\Delta\Sigma$ ADCs in the CSS to further reduce its power consumption, and 4) combining the integrated shunts with beyond-the-rail ADCs to realize integrated high-side CSSs.

Compared to the prior art, the presented *integrated* shunt-based CSSs significantly improve current sensing accuracy, and are well-suited for use in the Coulomb counter of portable devices.

Samenvatting

Coulomb tellen is een veelgebruikte methode voor het inschatten van de batterijlading (SoC). Dit houdt in het meten en integreren van de stroom door de batterij om de netto batterijlading te bepalen.

Zoals uiteengezet in Hoofdstuk 1 wordt de algehele nauwkeurigheid van een Coulomb teller voornamelijk bepaald door de nauwkeurigheid van zijn stroommeting systeem (CSS). De offset van deze CSS moet lager zijn dan de zelfontlading van de accu ($\approx 50\ \mu$A voor een draagbaar apparaat). Een versterkingsfout van minder dan $\pm 0.5\%$, voor stromen tot een paar ampere en over het industriele temperatuurbereik ($-40°$C to $+85°$C), zijn vereist voor een nauwkeurige inschatting van de batterijlading. Een resolutie van beter dan 14 bits (0.01%) in een meettijd van 25-ms is nodig voor een snelle kalibratie. Bovendien maakt de geintegreerde en CMOS-compatibele stroommeter met digitale uitgang de realisatie van een kleine en kosteneffectieve batterijladingsmeter mogelijk. Tot slot, om vermogensverlies te minimaliseren, moet het stroomverbruik van de stroommeter beneden het vermogensverlies van de zelfontlading van de batterij gehouden worden. Op basis van hun operationele beginselen, worden stroomsensoren onderverdeeld in twee categorieen: 1) magnetische veld sensoren, en 2) shunt gebaseerde Stroomsensoren. Magnetische veld sensoren zijn over het algemeen niet geschikt voor gebruik in Coulomb tellers. Rogowski spoelen en stroomtransformatoren zijn niet geschikt voor DC en/of kleine (sub-milliampere) stroommeting. Fluxgates en magneto-weerstanden, die kleine DC stromen kunnen meten, vereisen nabewerking als gevolg van hun gebruik van ferromagnetische materialen. Daarnaast vereisen fluxgates grote excitatie stromen om hun kern te verzadigen, en verbruiken daarom enkele tientallen milliwatten. Hall-effect sensoren verbruiken een vergelijkbare hoeveelheid energie, maar zijn ten minste wel CMOS-compatibel. Vanwege hun beperkte gevoeligheid zijn Hall-sensoren echter niet geschikt voor het meten van kleine (sub-milliampere) stromen. Aan de andere kant worden shunt gebaseerde sensoren, die de stroom meten doormiddel van de spanningsval over een shunt weerstand, veel gebruikt in Coulomb tellers. Hun eenvoud leidt tot grotere nauwkeurigheid en resolutie, waardoor ze zich goed lenen voor integratie in een IC. Stroommetingen op basis van externe shunt

weerstanden kunnen fouten behalen van minder dan ±0.1%; echter zijn de extra kosten en omvang van deze aanpak niet acceptabel voor een batterijladingsmeter. Vanaf 2011 (wanneer dit onderzoek begon), behaalden sensoren op basis van geintegreerde shunt weerstanden winstfouten van >±3% en stroom-offsetten van enkele milliampere. Hun winstfout is voornamelijk te wijten aan onvoldoende compensatie ten gevolge van de shunt weerstandspreiding en zijn temperatuur coefficient (TCR), terwijl hun stroom-offset wordt beperkt door de uitlezing elektronica. Ter verbetering van de winstfout tot beter dan 1% realiseerde verschillende ontwerpen de shunt van lage-TCR legeringen, zoals Evanohm, Constantaan en Manganine. Een aangepast proces is echter nog steeds nodig om deze shunts te realiseren, waardoor de productiekosten omhoog gaan. Het doel van deze thesis is dan ook gedefinieerd als: het realiseren van een geintegreerde, precisie en betaalbare shunt-gebaseerde CSS voor gebruik in de Coulomb teller van draagbare apparaten.

In Hoofdstuk 2 worden verschillende manieren van het realiseren van een shunt weerstand besproken, en twee typen worden gekozen voor gebruik in dit werk. Er wordt uitgelegd dat precisie off-chip weerstanden ofwel te duur zijn, of lijden onder grote TCR en slechte thermische koppeling tussen shunt en temperatuursensor hebben. Daarnaast zijn ze meestal te omvangrijk, en dus niet uitvoerbaar voor integratie in draagbare apparaten. De in-behuizing shunts bieden een compacte en potentieel betaalbare oplossing; shunts op basis van een bedradingsframe van een standaard behuizing en RDL lagen zijn de meest veelbelovende van deze soort. Wij stellen het gebruik voor van 1) een 10 mΩ op-de-chip metalen shunt weerstand, en 2) de warmtekoppel-bedradingsframe van een HVQFN32 om een 260 $\mu\Omega$ weerstand te realiseren. Hoewel de bedradingsframe shunt resulteert een in vrij kleine shunt spanningen voor doelstromen binnen 5 A (leidend tot een grotere meetfout en overtollige ruis), demonstreert het de haalbaarheid van bedradingsframeshunts voor hoge stroommetings-toepassingen, zoals bijvoorbeeld de auto-industrie. Omdat deze compatibel zijn met standaard CMOS-processen en standaard verpakkingstechnologie, wordt de voormalige gebruikt voor stroommetingen tot ±5 A, terwijl de laatste gebruikt wordt voor stroommetingen tot ±36 A, beide met een winstfout beter dan ±0.5%.

Hoofdstuk 3 behandelt shunt temperatuurcompensatie. Het effect van de shunt TCR wordt gecompenseerd door een digitale temperatuur-compensatieregeling, waarbij de shunt de temperatuur meet en vervolgens in het digitale domein corrigeert voor de TCR van de shunt weerstand. Er wordt besproken dat substraat PNPs, die beschikbaar zijn in standaard CMOS-processen, een optimale keuze zijn voor de

temperatuur meter van de CSS. Deze PNPs zijn ook hergebruikt voor het genereren van de vereiste referentie spanning voor de CSS. De thermische koppeling tussen de shunt en de temperatuursensor, die essentieel is voor een nauwkeurige shunt temperatuurcompensatie, is bestudeerd en verbeterd doormiddel van elektro-thermische simulaties in COMSOL. Als gevolg van de electro-migratie, ondervind de op-de-chip shunt weerstand aanzienlijke (0.1%) drift na het testen over lange termijn (24 dagen) bij hoge- temperaturen (+85°C) en stromen (5 A DC). Dit kan opgelost worden door vermindering van de stroomdichtheid en/of de temperatuur van de shunt, hetzij door vergroting van haar oppervlak, of door het reduceren van haar maximale bedrijfsstroom en/of temperatuur. Een ander nadeel van de op-de-chip shunt is het verbruik van het grote silicium oppervlak. Deze twee problemen worden omzeild door gebruik te maken van de, in vele *standaard* IC behuizingen *reeds beschikbare*, bedradingsframe, bijvoorbeeld in een HVQFN32 plastic behuizing. Dit kost geen extra silicium oppervlak en vergroot zowel het stroombereik en de robuustheid van de shunt, aangezien typische bedradingsframes ordes van grootte dikker zijn dan on-de-chip metaal-lagen.

Hoofdstuk 4 presenteert het systeemniveau ontwerp van de uitlezing elektronica, de ADCs en de bandgap referentie (BGR). De substraat PNPs worden gebruikt in de BGR om de shunttemperatuur te meten en voor het genereren van de CSS referentie spanning. Gedreven door de resolutie vereisten, zijn tweede-orde geschakelde-condensator $\Delta\Sigma$ modulatoren gekozen als de ADCs. Significante tekortkomingen van deze twee bouwstenen, samen met de, door de prior-art, voorgestelde oplossingen worden toegelicht. In tegenstelling tot de prior-art, stellen wij een veel eenvoudigere oplossing voor die in wezen alleen de niet-idialiteiten van de shunt kalibreert. We tonen aan dat deze kalibratie methode het effect van veel uitlees-elektronica fouten tot een verwaarloosbaar niveau reduceert, zonder deze *expliciet* te corrigeren. Dit vereenvoudigt zowel de implementatie van het circuit als de kalibratie van de CSS aanzienlijk, waardoor de productiekosten verminderd worden.

Drie prototype CSSs samen met hun meetresultaten worden beschreven in dit proefschrift. De eerste (CSS_1), behandeld in in Hoofdstuk 5, bestaat uit een 10 mΩ op-de-chip metalen shunt, een ADC en een BGR. Het maakt gebruik van een enkele ADC voor zowel de stroom- als de temperatuurmeting in een tijds-multiplexde wijze. Dit ontwerp, gerealiseerd in een standaard 0.13-μm CMOS proces, neemt 1.15 mm^2 in en trekt 55 μA van een 1.5-V spanningsbron. Voor stromen varierend van -5 A tot $+5$ A en over een temperatuurbereik van -55°C tot $+85$°C vertoont het een maximale afwijking van 16 μA en maximale winstfout van $\pm 0.3\%$. Dit niveau van

nauwkeurigheid is duidelijk in overeenstemming met de doelstelling van deze thesis, en wordt bereikt door middel van een nauwkeurige compensatieregeling van de shunttemperatuur, meerdere dynamische foutcorrectie technieken en een eenvoudige kalibratie-regeling.

Hoofdstuk 6 presenteert de andere twee ontwerpen, die verbeterde prestaties met een verminderd IC oppervlak (2×) en verminderd energieverbruik (4×), in vergelijking met CSS_1, bereiken. Om nauwkeurig snelle temperatuur transienten in de shunt bij te houden zijn twee aparte ADCs, een voor het meten van de stroomsterkte en een voor de temperatuurmeting, tewerkgesteld. Het eerste ontwerp (CSS_2) is gebaseerd op een 10 mΩ op-de-chip shunt, terwijl de tweede (CSS_3) een 260 $\mu\Omega$ bedradingsframe weerstand van een plastic HVQFN32 behuizing gebruikt. Beide modellen zijn gerealiseerd in een standaard 0.13 μm CMOS proces en trekken 13 μA van een 1.5 V spanningsbron. Voor stromen binnen een bereik van -5 A tot $+5$ A en over een temperatuurbereik van $-55°$C tot $+85°$C, vertoont (CSS_2) een maximale afwijking van 4 μA en een maximale winstfout van $\pm 0.3\%$. Over hetzelfde temperatuurbereik, maar voor stromen varierend van -36 A tot $+36$ A, vertoont (CSS_3) een maximale afwijking van 400 μA en een maximale winstfout van $\pm 0.3\%$. Vergeleken met de state-of-the-art vertegenwoordigen deze prestaties een aanzienlijke stijging in het stroombereik, de nauwkeurigheid en het dynamisch bereik, desondanks het gebruik van een standaard op-de-chip en bedradingsframe shunt.

Ten slotte concludeert Hoofdstuk 7 de thesis en geeft een overzicht van de oorspronkelijke bijdragen en bespreekt toekomstige werkzaamheden. De voorgestelde toekomstige werkzaamheden bedragen: 1) experimenteel onderzoek naar de robuustheid van de bedradingsframe shunt en naar electro-migratie, 2) het aanpassen van het bedradingsframe om zijn weerstandswaarde aan te passen, 3) implementeren van een continue-tijd $\Delta\Sigma$ ADC in de CSS om het verbruikte vermogen te verminderen, en 4) de geintegreerde shunts combineren met een voorbij-de-rails ADC om een hooge-kant geintegreerde CSS te realiseren.

In vergelijking met de prior art, zijn de gepresenteerde *geintegreerde* shunt gebaseerde CSSs een aanzienlijk verbetering op de stroommetingsnauwkeurigheid, en zijn zeer geschikt voor gebruik in de Coulomb teller van draagbare apparaten.

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List of Publications

Journal Papers

[1] **S. H. Shalmany**, D. Draxelmayr, K. A. A. Makinwa, "A ±36 A Integrated Current-Sensing System with 0.3% Gain Error and 400 μA Offset from −55°C to +85°C," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1034−1043, Apr. 2017.

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[1] **S. H. Shalmany**, D. Draxelmayr, K. A. A. Makinwa, "A ±36A Integrated Current-Sensing System with 0.3% Gain Error and 400μA Offset from −55°C to +85°C," *Symp. on VLSI Circuits Dig. of Tech. Papers*, pp. 96−97, 2016.

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Saleh Heidary Shalmany received the B.S.E.E degree from Tehran University in 2008, and the M.S.E.E degree (*cum laude*) from TUDelft in 2010. From 2010 to 2011, he was a researcher with TUDelft and NXP Semiconductors. From 2011 to 2016, he pursued his Ph.D. at TUDelft and in collaboration with Infineon Technologies.

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