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Impact of Photovoltaic Technology and Feeder Voltage Level on the Efficiency of Façade Building-Integrated Photovoltaic Systems

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Abstract

Façade building-integrated photovoltaics is a technology that transforms a passive façade into a distributed, renewable electrical generator by the inclusion of solar cells in the building envelope. Partial shading due to nearby objects is a typical problem for façade building-integrated photovoltaics as it strongly reduces the output power of the installation. Distributed maximum power point tracking by means of embedded converters and a common direct current bus has been proposed to alleviate this issue. However, the bus voltage plays an important role in converter topology selection and overall efficiency, although this is not being covered in literature. Also the influence of the solar cell technology on the output voltage of the module is not studied before, although it strongly influences the converter topology selection and the losses. In this paper, a methodology is described to investigate the influence of the voltage level and solar cell technology by taking conversion losses in the converters and the cabling into account. The methodology is applied to two case study buildings for which four different cell technologies are considered. It is shown that overall

high efficiencies are obtained, regardless of the voltage level. However, the loss distribution changes significantly with the voltage. This aspect can be used advantageously to reduce thermal stresses on the embedded converter. Furthermore, the overall system efficiency is typically higher when the voltage step-up is lower.
Keywords: BIPV; DC/DC converters; MLC; LVDC.

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1. Introduction

1.1. Motivation

Building-Integrated PhotoVoltaics (BIPV) is a technology where PV cells are an integral part of the building skin and serve as a replacement for conventional building modules [1, 2]. As BIPV serves simultaneously as a building envelope material and a power generator, savings in material and electricity costs can be obtained [3]. BIPV is promoted by the EU through the Strategic Energy Technology (SET) plan [4] and the Energy Performance of Buildings Directive (EPBD) [5]. From 2020 on, all new public buildings in the EU are required to be Near Zero Energy Buildings (NZEBs), meaning that they have a very high energy performance. Generating sufficient energy to cover the building's energy demand can be very challenging for high rise buildings in a dense urban context with a limited roof surface [6]. Façade BIPV systems offer a solution to this problem by using the large vertical surfaces as a distributed generator.

Partial shading due to nearby objects is a typical problem for façade BIPV. Distributed Maximum Power Point Tracking (MPPT) by Module-Level Converters (MLCs) can reduce the negative effects of partial shading on the performance of the installation [7]. The use of MLCs also enhances the design freedom of architects, as PV modules with different electrical ratings can be used. Furthermore, cost reductions are expected by integrating the converter into the BIPV frame. However, this integration also introduces several new challenges for the MLC design. A high compactness, a long lifetime and the ability to work

at high ambient temperatures are required [8]. Ravyts et. al. have shown that commercially available MLCs cannot be used for façade BIPV applications as electrical, thermal or dimensional limits imposed by the BIPV module are not respected [9].

In this work, the use of DC/DC MLCs is considered, where all converters are coupled in parallel to a common DC bus. Compared to DC/AC MLCs, that employ an AC bus, fewer converter components are required which allows a higher power density and possibly a higher reliability. Although nowadays AC is still widely employed, using a Low Voltage DC (LVDC) system has several advantages. First, there is a better compatibility with DC loads and generators such as LED lighting, PV generation and battery storage. A lower amount of conversion steps is required which in turn leads to less conversion losses [10]. Second, more power can be transferred through the same cable as there is no reactive current or skin effect present [11, 12]. The correct functioning of LVDC grids has been showcased by a number of demonstrators for industrial [13] and office buildings [14].

Several DC voltage levels are in use nowadays. The IEC 60038 defines the limit of LVDC at 1500 V. Telecom operators use 48 V systems [15], which is also being considered for commercial buildings [16]. Furthermore, 48 V is used for rural electrification [17]. The more electric aircraft will work with a bipolar DC bus of 270 V [18]. Borcherding et al. considered a 650 V bus for industrial applications [19]. In the Netherlands, the use of a bipolar 350 V bus is preferred [20] whereas datacenters employ a bipolar 190 V DC bus [10]. The use of LVDC for BIPV applications was first introduced by Liu et al., where a 200 V DC bus was used [7]. In this paper, a bipolar LVDC backbone of +380 V/0/-380 V is proposed as the system backbone in the building. A bipolar system offers the advantage of having two voltage levels to which high power (e.g. elevators) or low power (e.g. lighting) loads can be connected. Furthermore, a lower cable cross section for a given power is needed in comparison to a unipolar network [15].

Technical design challenges for the safe application of BIPV systems are

discussed in [21]. Fire, heat and noise protection towards the end users is discussed. Safety concerns related to electrical hazards can also be a reason for using a lower DC voltage. In [22], the touch voltage that users can experience in LVDC grids during earth faults is discussed. Assuming a midpoint-grounded bipolar grid ($+V_{DC}/0/\text{-}V_{DC}$), the maximum touch voltage is $V_{DC}/2$. Under dry skin conditions, voltages below 120 V are considered safe for humans [22]. When an earth fault occurs in DC systems where $V_{DC} \leqslant 240$ V, human safety is guaranteed.

In previous work, a direct connection to the 380 V pole was always considered for BIPV MLCs [23, 24]. In this work, a voltage balancing converter is assumed to be placed between the LVDC backbone and the BIPV feeder. Hence, the DC voltage level, V_{DC}, at which the system is operated, is a degree of freedom. Due to the different dimensions compared to standard 60 or 72 cell c-Si PV modules, BIPV modules are typically custom designed. Another degree of freedom is the PV technology used and the way of interconnecting the cells. By changing to different cell sizes or PV materials, the electrical output characteristics of the BIPV module will differ [9].

The conversion efficiency of step-up converters is strongly dominated by the required gain. For a given converter, the losses will increase if the ratio between input and output voltage increases. By lowering V_{DC} and choosing PV technologies with higher output voltages, the efficiency of the MLC can in principle increase. Due to the high ambient temperatures in the module frame, reducing the losses in an embedded MLC is beneficial to increase its lifetime. Furthermore, by reducing the gain, simpler topologies with less components can be used which is favorable for the power density, the cost and the lifetime of the MLC. However, decreasing the DC voltage level to which the MLC has to boost comes at the expense of increased losses in the cabling and in the Voltage Balancing Converter (VBC). Given the aforementioned trade-offs between the required step-up due to the difference in voltage level between the PV generator and the DC grid, the objective of this paper is to develop a system model to quantify the losses in function of two major degrees of freedom that a BIPV

designer has, namely the PV technology and the DC bus voltage level. The main research questions of this paper can be formulated as:

- Is a unipolar or a bipolar system preferred from a cost and efficieny perspective and where should the VBC be located in the BIPV feeder?
- Under which conditions can a regular boost topology be used for the MLC, instead of the more advanced but also more costly, high step-up converters?
- What is the impact of derating the MLC on the energy production of the BIPV module and can a certain derating be adviced?
- To what extent is the cable a limiting factor for reducing the DC bus voltage in terms of losses, dimensions and voltage increase?
- How are the losses and the conversion efficiency affected by reducing the DC bus voltage and/or choosing a different PV technology and how are the losses distributed over the different conversion steps?

This will be evaluated by calculating the losses and efficiency of two case study buildings for which different PV technologies and voltage levels are considered. Ravyts et al. highlighted the advantages of a DC bus over an AC bus [8], but the location of the VBC and the unipolar or bipolar character of the string have not been addressed. In other work, typically only one PV technology is evaluated for a building [25, 26]. This paper will consider the implementation of multiple PV technologies and compare the outcomes. To the author's best knowledge, the impact of the DC bus voltage on the losses in a BIPV system has not been investigated before.

1.2. Paper structure

This paper is organised as follows: In section 2, the methodology is explained and the different building blocks of the simulation framework are highlighted. Sections 3 - 8 explain in detail the assumptions and calculations of each block,

that represent physical components of the studied system. In section 9, the system performance of two case study buildings is evaluated. Section 10 presents the conclusions. A Nomenclature section is included before the References section.

2. Methodology

To investigate the impact of the DC bus voltage level and the PV technology on the BIPV system efficiency, two case study buildings are evaluated. The case studies are based on façades of actual buildings, however no BIPV elements are present in real life. One floor level is composed of multiple curtain wall elements next to each other, as shown in Fig. 2. Every curtain wall module consists of a transparent and an opaque part. The opaque part, in real life a regular construction material, is assumed to be functioning as a PV generator. From the module dimensions, the electrical parameters can be calculated as a function of the chosen PV technology. The actual electrical output of the PV generator is a function of the solar irradiance and module temperature. This power is transferred by the MLC, the cable and the VBC towards the LVDC backbone in the building. Each of these steps includes losses that depend on the DC voltage level and the PV voltage. Therefore, the losses of each power transfer are modeled as a function of the PV technology and the DC bus voltage. Those two variables are also essential design choices a BIPV designer needs to make for a specific installation. For a given case study building and input profile, the proposed methodology allows to calculate the overall system efficiency as a function of the PV technology and the DC system voltage.

The methodology is represented as a block diagram in Fig. 1 and is implemented accordingly in the actual code.

3. Electrical system configuration

Different options exist for the network layout of the BIPV installation. They will differ in cost and efficiency which will be investigated in this section.

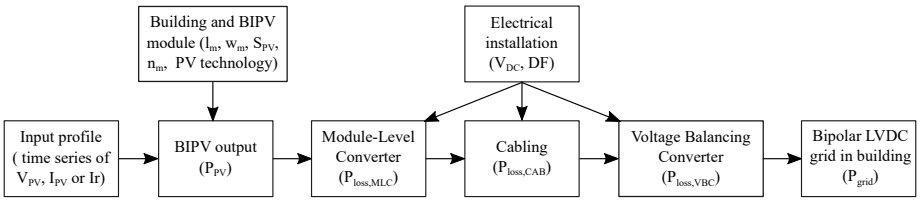


Figure 1: Implemented methodology framework. Based on the power flow within the system and the degrees of freedom a designer has, the losses are calculated in each conversion step.

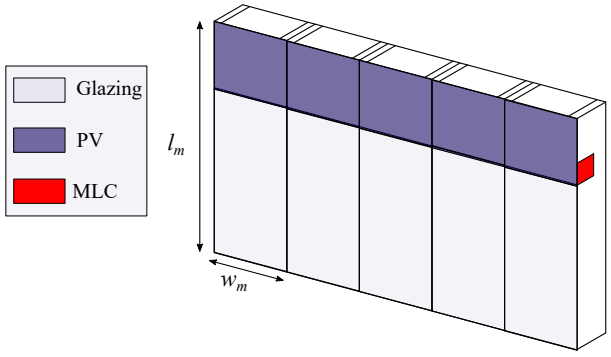
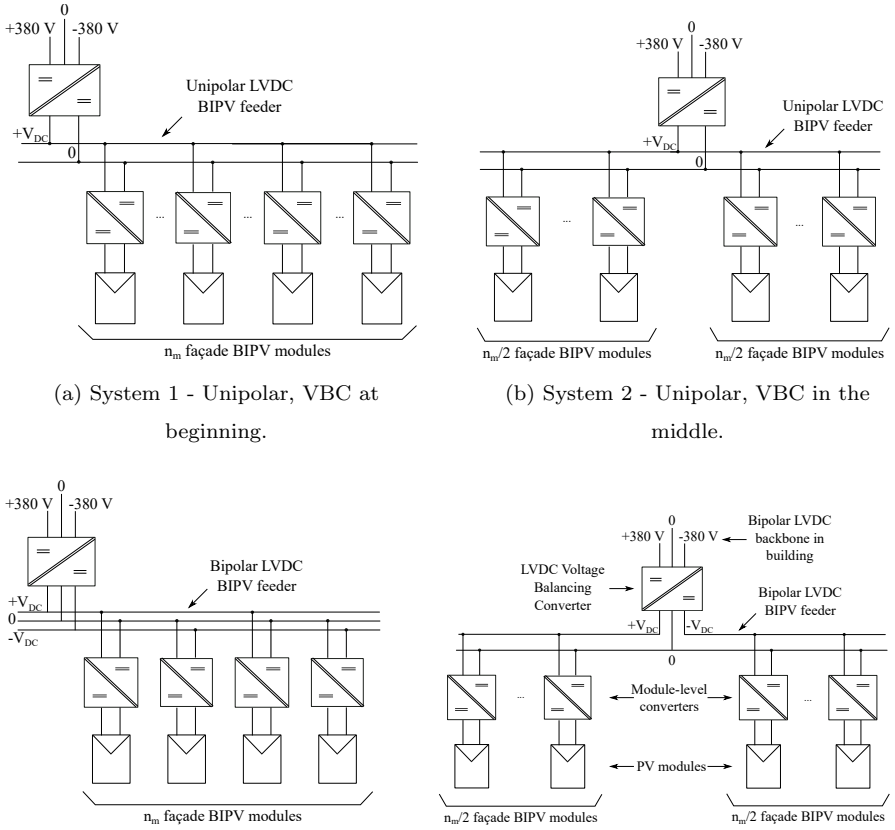


Figure 2: Façade structure using BIPV curtain wall elements. Every curtain wall element consists of glazing and of a PV generator. The MLC is an integral part of the BIPV module and is installed in the module frame.



(a) System 1 - Unipolar, VBC at beginning.

(b) System 2 - Unipolar, VBC in the middle.

(c) System 3 - Bipolar, VBC at beginning.

(d) System 4 - Bipolar, VBC in the middle.

Figure 3: Four possibilities for the system lay-out considering a unipolar or bipolar system and the location of the VBC.

Four possibilities are shown in Fig. 3: a unipolar or bipolar system is considered and the VBC was evaluated to be placed at the beginning or in the middle of the BIPV feeder. The four systems were evaluated by four Key Performance Indicators (KPIs) that relate to the cost and losses. The results are shown in Table 1. First, the gain of the VBC G_{VBC} is considered. Bipolar systems have a clear advantage over unipolar systems, as twice V_{DC} is available at the VBC terminals [15, 27, 28]. This leads to a reduction of the required gain by a factor two, which is in turn beneficial to reduce the VBC losses. Second, the cable

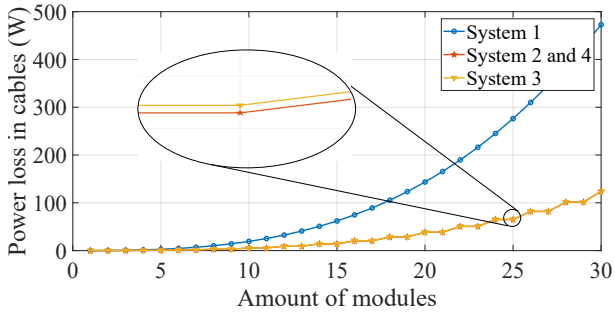


Figure 4: Cable losses as a function of the amount of modules for different network configurations (R = 0.1 Ω and I_{MLC} = 0.5 A). A magnification has been included to highlight the minor difference between system 3 and systems 2/4.

length l_{CAB} is considered. Here it can be noticed that system 3 requires 50% more cable, which increases the total cost of the system. Third, the losses in the cable $P_{loss,CAB}$ are considered, assuming equal output current of all MLCs. The cable resistance per module is denoted as R and the MLC output current as I_{MLC}. The losses are graphically represented as a function of the amount of modules, n_m, in Fig. 4. System 1 clearly has the highest cable losses, whereas the other three systems have similar losses. The extra term in the loss equation of system 3 is a consequence of the current through the 0 V pole. Note in Fig. 4 that this extra term only leads to a minor increase of the cable losses. Fourth, the maximum current that can be present in the cables, $I_{CAB,max}$, is considered. This occurs when all MLCs generate the maximum output current, $I_{MLC,max}$. As such, $I_{CAB,max}$ should preferably be as low as possible since the cable cross section and the price increases with the required ampacity. Note that $I_{CAB,max}$ is twice as high for system 1, compared to the other three systems. In conclusion, a bipolar system, where the VBC is placed in the middle of the feeder, offers several advantages in terms of cost and efficiency and is therefore used in the remainder of this manuscript.

4. Input profile

At our test site a BIPV prototype has been installed to evaluate thermal and

Table 1: Evaluation of four different network layout options, based on the required gain at the VBC G_{VBC}, the required cable length l_{CAB}, the losses in the cabling $P_{loss,CAB}$ and the required cable ampacity $I_{CAB,max}$.

System	G_{VBC}	l_{CAB}	$P_{loss,CAB}$	$I_{CAB,max}$
1	$\frac{760}{V_{DC}}$	$2n_m w_m$	$2RI_{MLC}^2 \sum_{k=1}^{n_m} k^2$	$n_m I_{MLC,max}$
2	$\frac{760}{V_{DC}}$	$2n_m w_m$	$4RI_{MLC}^2 \sum_{k=1}^{n_m/2} k^2$	$\frac{n_m I_{MLC,max}}{2}$
3	$\frac{760}{2V_{DC}}$	$3n_m w_m$	$4RI_{MLC}^2 \sum_{k=1}^{n_m/2} k^2 + \frac{n_m R I_{MLC}^2}{2}$	$\frac{n_m I_{MLC,max}}{2}$
4	$\frac{760}{2V_{DC}}$	$2n_m w_m$	$4RI_{MLC}^2 \sum_{k=1}^{n_m/2} k^2$	$\frac{n_m I_{MLC,max}}{2}$

System 1: Unipolar, VBC at beginning; System 2: Unipolar, VBC in middle

System 3: Bipolar, VBC at beginning; System 4: Bipolar, VBC in middle

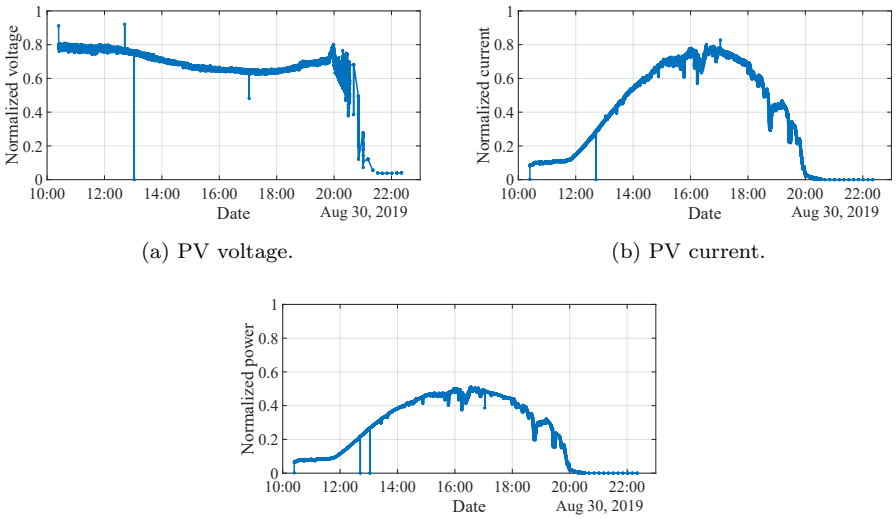
electrical aspects of BIPV curtain wall modules. The test set-up and measured results have been presented in [29, 30]. Voltage, current and power measurements are taken every two seconds using a Femtogrid PO310 power optimizer on a south-west oriented, vertically inclined, 60-cell c-Si PV module.

For the input profile, August 30 2019 was selected as a suitable day for comparison purposes. As there was little impact of clouds, the profile is relatively smooth. The measured voltage, current and power are normalized with respect to the Standard Test Conditions (STC) values of the PV module ($I_{MPP,STC}$ = 8.694 A and $V_{MPP,STC}$ = 37.97 V). The normalized voltage, current and power profile over the course of the day are shown in Fig. 5 and will be used as input to compare the different voltage levels and PV technologies.

5. PV generator

5.1. Cell technology

A façade BIPV module is typically a custom engineered product and the PV technology gives a sense of freedom to the designer. The different PV technologies also result in different voltages and currents at the output of the PV generator. It is expected that technologies with a higher output voltage are



(a) PV voltage.

(b) PV current.

(c) PV power.

Figure 5: Normalized voltage, current and power measurements on August 30 2019. The measurements have a 2 seconds resolution and are taken on a south-west oriented, vertically inclined, 60-cell c-Si PV module.

beneficial to reduce conversion losses. The cell technology is thus an important parameter to evaluate.

The most widely employed PV material is monocrystalline Silicon (c-Si) of which the dimensions and electrical properties of one cell are listed in Table 2, based on a commercially available products. Variations on this technology exist if the shape of regular [31], half [32], quarter or shingled [33] solar cells, where the cells are cut in smaller pieces. The reduced cell dimensions lead to a lower current, as the generated current is proportional to the cell surface. When PV modules using half or quarter cells are designed for the Building Applied PV (BAPV) market, cell strings are placed in parallel to achieve similar electrical parameters as traditional c-Si modules [32]. In contrast, this work assumes a series connection of all cells to exploit the advantage of the higher output voltage.

Another possible PV material that will be investigated is thin film CIGS.

Table 2: Electrical and dimensional cell parameters of the investigated PV technologies.

	c-Si RC	c-Si HC	c-Si SC	CIGS
$V_{oc,STC}$ (V)	0.652	0.683	0.670	0.600
$I_{sc,STC}$ (A)	9.047	5.165	1.920	2.590
$V_{MPP,STC}$ (V)	0.549	0.576	0.552	0.500
$I_{MPP,STC}$ (A)	8.553	4.775	1.818	2.380
l_{cell} (mm)	157	157	157	5
w_{cell} (mm)	157	79	28.5	1587
Reference	[31]	[32]	[33]	[34]

Although the market share of CIGS is limited, this technology offers advantages in terms of cost. The high flexibility can be an advantage for BIPV applications. The dimensions of the used thin film cells are also included in Table 2 and are based on a commercial product [34]. Note that the length of the cells is very low and the width very high compared to c-Si. This is done to limit resistive losses in the solar cell.

Four possible cells are considered: c-Si Regular Cells (RC), c-Si Half Cells (HC), c-Si Shingled Cells (SC) and thin film Cadmium Indium Germanium Sulfide (CIGS). Their cell properties are listed in Table 2. The short-circuit current, open-circuit voltage, MPP current and voltage at Standard Test Conditions (STC) are respectively denoted as $I_{sc,STC}$, $V_{oc,STC}$, $I_{MPP,STC}$ and $V_{MPP,STC}$.

5.2. By-pass diodes and partial shading

In BIPV applications, shading due to nearby objects needs to be taken into account [35]. Since a PV module is made of series-connected cells, all cells share the same current. The current flowing through a cell is proportional to its illumination thus, when one cell of the module is shaded whereas the other cells are not, either the current of the module is limited to the current of the shaded cell, significantly reducing the PV module power output, or the shaded cell works in reverse bias, allowing a high current to flow, but dissipating

a significant amount of power due to the reverse voltage. When the reverse voltage across the shaded cell becomes too high, reverse breakdown can occur. Energy is dissipated in the reverse biased cell, which will lead to a hot spot and possible permanent damage. To prevent this from happening and to reduce the probability that a shaded cell gets strongly reverse biased, by-pass diodes are placed. When the reverse voltage across the substring containing the shaded solar cell is larger than the forward voltage of the by-pass diode, the by-pass diode will start conducting, thereby limiting the voltage across the shaded cell and providing an alternative path for the current to flow.

By-pass diodes are an effective method of protecting solar cells against damage due to reverse bias. The PV module power output can,however, significantly reduce under partial shading due to the loss of voltage of the substring bridged by the activated by-pass diode, and the the by-pass diode. Hence, the input voltage of the power converter is reduced accordingly, and the step-up ratio has to increase in order to maintain the desired output voltage. This aspect will be of importance in section 6 for selecting a suitable converter topology. For commercial c-Si modules, by-pass diodes are placed across every 20...24 series-connected cells [36].

The performance of CIGS and CdTe thin film modules under partial shading conditions has been investigated in [37]. Compared to c-Si, an improved performance under partial shading conditions is highlighted due to the different module lay-out. Nevertheless, extreme partial shading can lead to cell defects [37]. For commercial CIGS modules, only one by-pass diode is placed across the entire module. In these modules, cells are formed as strips across the entire width of the module. They are usually divided into smaller pieces, forming multiple parallel strings, in order to avoid reliability issues related to reverse break-down. An interesting consequence is that the output voltage remains high in case of partial shading, since the unaffected strings operate normally, maintaining their forward voltage [38]. In general, a higher cell granularity is beneficial to reduce the consequences of partial shading.

An alternative for by-pass diodes that has been proposed in literature is the

use of differential power processing [39, 40]. A converter is connected across a group of cells that allows to divert the mismatch current between two cells or groups of cells. This is particularly beneficial in case of partial shading, where more of the power still produced by the partially shaded string can be retained.

5.3. Temperature coefficient

The electrical parameters of a PV cell are measured at STC, where it is subjected to an irradiance of 1000 W/m^2 and operate at a temperature of 25 °C. In practice, the solar cells operate at higher temperatures, at which the saturation current increases, the voltage decreases correspondingly, and the photo current increases slightly due to the reduction in electronic bandgap. The combination negatively influences their output power, and in particular the voltage at the maximum power point, i.e. the operating point of the PV module. This is linearly approximated by the temperature coefficients of short-circuit current α_{Isc} and voltage β_{Voc}, β_{Vmpp}. Typical values for modern c-Si PV modules are α_{Isc} = +0.04...0.06 %/K, β_{Voc} = -0.24...-0.34 %/K, and β_{Vmpp} = -0.33...-0.45 %/K, resulting in a temperature coefficient of the maximal power of -0.29...-0.41 %/K. For CIGS, α_{Isc} = +0.01...0.04 %/K, β_{Voc} = -0.30...-0.31 %/K and β_{Vmpp} = -0.2...0.3 %/K. Hence, the typical operating voltage of a PV system is considerably lower than the value based on STC. This phenomenon is also visible in Fig. 5a, where the V_{MPP} is between 60 to 80% of the STC value. In the remainder of this paper, mainly β_{Vmpp} is the parameter of interest. For c-Si, β_{Vmpp} = -0.39 %/K and for CIGS β_{Vmpp} = -0.25 %/K will be used. The MPP voltage for a given temperature T (in °C) can be calculated:

$$V_{MPP,T} = V_{MPP,STC}(1 + \beta_{Vmpp}(T - 25)) \tag{1}$$

In [41], the module temperatures of an experimental BIPV façade test set-up are reported. Operating temperatures near 100 °C are reported measured at the back of the PV module. In [30], operating temperatures near 75 °C have been measured. In this study, a maximum working temperature of 100 °C is assumed.

This temperature dependence will be of importance for the converter selection in section 6.

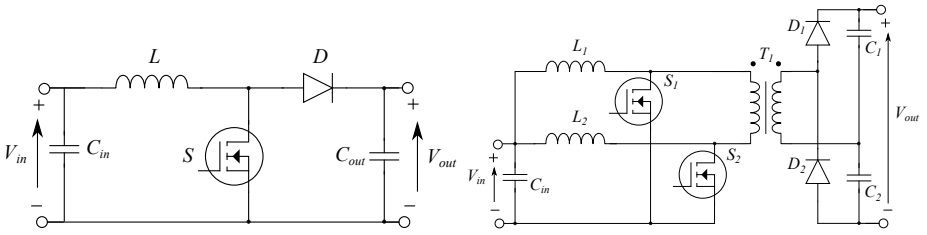
5.4. Calculation of electrical parameters

The BIPV module electrical parameters can be calculated from the module length l_{mod}, the module width w_{mod}, the surface dedicated to PV S_{PV} (in% of the total surface) and the PV technology. Using the cell dimensions as listed in Table 2, the total amount of PV cells, n_{cell}, can be easily calculated for the three c-Si cases by multiplying the maximum amount of cells along the width ($n_{cell,x}$) by the maximum amount of cells along the length ($n_{cell,y}$). It is assumed that all cells are series connected such that they produce the highest possible output voltage. For the CIGS cells, the length of the cells is assumed constant but the width is adapted to the width of the modules, which means that $n_{cell,x} = 1$. The cell current is dependent on the total cell surface and thus needs to be scaled according to the new cell width. This is done by multiplying $I_{sc,STC}$ and $I_{MPP,STC}$ with w_{mod}/w_{cell}. Using the normalized voltage and current profiles, the output voltage and current of the PV module are simulated over the course of a day.

6. Module-Level Converter

6.1. Topology selection

The MLC is the interface between the PV module and the LVDC grid. It is responsible for the Maximum Power Point Tracking (MPPT) and the voltage step-up. The required converter topology will depend on the ratio of the input and output voltages. If the maximum required gain is below five, a regular boost converter topology can be used [42]. If the required gain is higher, the parasitics lead to strong deviations from the ideal gain, and the efficiency quickly drops. More advanced topologies using switched inductors [43], switched capacitors [44], coupled inductors [45], voltage multiplier cells [46] or transformers [23, 24, 47] are then required. However, these solutions require more components, which



(a) Boost converter. (b) Isolated interleaved boost converter.

Figure 6: Circuit topology of the two studied converters. The isolated topology allows for higher voltage gains due to the presence of the transformer.

leads to a lower power density, a higher cost and reduced reliability. Besides, high step-up ratios have a lower efficiency due to the increased conduction losses. The above mentioned aspects are of utmost importance in BIPV applications where the converter is frame-integrated and replacement is difficult.

In this work, two different topologies are considered: a boost converter, depicted in Fig. 6a and an Isolated Interleaved Boost Converter (IIBC), depicted in Fig. 6b. The boost converter is in practice not used for gains above five, as the parasitics strongly decrease the efficiency. In [48], a boost converter was designed for a BIPV application using a 48 V DC bus. The gain of the IIBC can be increased beyond five by adapting the turns ratio of the transformer n_{tr}. The IIBC was considered for BIPV applications using a 200 V DC bus in [7]. A detailed analysis of the working principle of the IIBC is presented in [49].

The topology for a given case depends on the maximum voltage gain $G_{max} = V_{DC}/V_{PV,min}$ and is thus a function of the PV and DC bus voltages. The minimum input voltage for which the converter still needs to operate is denoted with $V_{PV,min}$. For c-Si this is assumed to be 1/3 of the V_{MPP} at 100 °C to take into account temperature effects and output voltage reductions when partial shading occurs and by-pass diodes get activated. For CIGS, only the temperature effect is taken into account as there is typically only one by-pass diode placed per module. Furthermore, the output voltage remains more constant due to the

non-shaded parallel cell strings.

$$G_{max} = \frac{V_{DC}}{V_{PV,min}} = \begin{cases} \dfrac{3V_{DC}}{V_{MPP,STC} + \beta_{Vmpp}(100-25)}, & \text{for c-Si} \\ \dfrac{V_{DC}}{V_{MPP,STC} + \beta_{Vmpp}(100-25)}, & \text{for CIGS} \end{cases} \tag{2}$$

When G_{max} is below five, a regular boost converter can be used. When G_{max} is higher than five, an IIBC is required.

6.2. Loss model

The origin and calculation of losses in power electronics converters is treated in detail in [42]. A detailed boost converter loss model is used that was experimentally validated in [50]. The IIBC loss model is built up similarly but includes also transformer losses [51]. The component selection and calculation of the losses will be discussed below. Both topologies are assumed to work in Continuous Conduction Mode (CCM).

The inductor current ripple ΔI defines the required minimal inductance to operate in CCM. The converter needs to work up to 10% of $I_{MPP,STC}$. Thus, to ensure CCM for the boost converter, $\Delta I = 0.2 I_{MPP,STC}$. For the IIBC, $\Delta I = 0.1 I_{MPP,STC}$ as the current is always split between both legs. The required inductance can be calculated based on the input voltage V_{in}, the DC bus voltage V_{DC}, the inductor current ripple ΔI and the switching frequency f_s:

$$L = \frac{V_{in}\delta}{\Delta I f_s} = \frac{V_{in}V_{DC} - V_{in}^2}{V_{DC}\Delta I f_s} \tag{3}$$

This quadratic function has its maximum value at $V_{in} = V_{DC}/2$. The required inductance thus depends on $V_{in,min}$ and $V_{in,max}$ and the position of these values with respect to $V_{DC}/2$. $V_{in,min}$ is calculated as in Eqn. (2) and $V_{in,max}$ is assumed to be equal to $V_{oc,STC}$. The calculation is slightly different for the boost (Eqn. (4)) and the IIBC (Eqn. (5)), since the transformer turns ratio n_{tr}

needs to be taken into account:

$$L = \begin{cases} \dfrac{V_{in,max}V_{DC} - V_{in,max}^2}{V_{DC}\Delta I f_s}, & \text{if } V_{in,max} < \dfrac{V_{DC}}{2} \\ \dfrac{V_{DC}^2}{4V_{DC}\Delta I f_s}, & \text{if } V_{in,min} < \dfrac{V_{DC}}{2} < V_{in,max} \\ \dfrac{V_{in,min}V_{DC} - V_{in,min}^2}{V_{DC}\Delta I f_s}, & \text{if } V_{in,min} > \dfrac{V_{DC}}{2} \end{cases} \tag{4}$$

$$L = \begin{cases} \dfrac{V_{in,max}V_{DC} - 2n_{tr}V_{in,max}^2}{V_{DC}\Delta I f_s}, & \text{if } V_{in,max} < \dfrac{V_{DC}}{4n_{tr}} \\ \dfrac{V_{DC}^2}{8n_{tr}V_{DC}\Delta I f_s}, & \text{if } V_{in,min} < \dfrac{V_{DC}}{4n_{tr}} < V_{in,max} \\ \dfrac{V_{in,min}V_{DC} - 2n_{tr}V_{in,min}^2}{V_{DC}\Delta I f_s}, & \text{if } V_{in,min} > \dfrac{V_{DC}}{4n_{tr}} \end{cases} \tag{5}$$

A suitable inductor is selected from the Bourns 1140 series for which the manufacturer provided the required data to calculate the losses. The DC winding losses, AC winding losses and core losses are included in the inductor loss model:

$$P_{L,DC} = R_{L,DC}I_{L,DC}^2 \tag{6}$$

$$P_{L,AC} = R_{L,AC}I_{L,AC,rms}^2 \tag{7}$$

$$\frac{R_{L,AC}}{R_{L,DC}} = \Delta\left(\frac{sinh(2\Delta) + sin(2\Delta)}{cosh(2\Delta) - cos(2\Delta)} + \frac{2(n^2-1)}{3}\frac{sinh(\Delta) - sin(\Delta)}{cosh(\Delta) + cos(\Delta)}\right) \tag{8}$$

Eqn. (8) is referred to as Dowell's equation [52] and takes the proximity and skin effect into account. The above equation requires the computation of the skin depth δ' and the penetration ratio Δ:

$$\delta' = \sqrt{\frac{\rho_{Cu}}{\pi\mu_{Cu}f_s}} \tag{9}$$

$$\Delta = \frac{d}{\delta'} \tag{10}$$

ρ_{Cu} is the resistivity of copper being 1.68*10^{-8} Ωm and μ_{Cu} is the permeability of copper. Since the relative permeability of copper, $\mu_{r,Cu} \approx 1$, $\mu_{Cu} \approx \mu_0$ = 4π*10^{-7} H/m. The wire diameter is denoted with d.

The core losses are caluclated using the Steinmetz equation with coefficients $k = 0.00244306$, $\alpha = 1.97498$ and $\beta = 2.53187$, as received from the manufacturer for this core type.

$$P_{L,core} = k f_s^{\alpha} B_p^{\beta} V_{core,L} \tag{11}$$

where B_p is the peak flux AC density in Tesla, given by:

$$B_p = \frac{V_{in} \cdot \delta}{2 \cdot n_L \cdot A \cdot f_s} \tag{12}$$

with n_L the number of turns of the inductor and A the cross section of the core.

For the switches, both conduction and switching losses are taken into account. The possible switches are listed in Table 3. GaN High Electron Mobility Transistors (HEMTs) were selected as they have a superior performance compared to Si MOSFETs in terms of on resistance $R_{DS,on}$ and switching speed, leading to lower losses in the switches [53, 54]. A suitable component is selected from Table 3 by comparing the maximum voltage across the switch $V_{S,max}$ in the given configuration with the rated drain-source voltage $V_{DS,rated}$. $V_{S,max}$ depends on the converter's output voltage and the topology and the expressions are given in Table 4.

$$P_{S,cond} = R_{DS,on} I_{S,rms}^2 \tag{13}$$

$$P_{S,sw} = \frac{V_{DS,max} \cdot I_{on} \cdot t_{on} \cdot f_s}{2} + \frac{V_{DS,max} \cdot I_{off} \cdot t_{off} \cdot f_s}{2} + \frac{Q_{oss} V_{DS,max} f_s}{2} \tag{14}$$

To estimate t_{on} and t_{off}, the method presented in [55] is followed:

$$t_{on} = \frac{R_G (Q_{GD} + Q_{GS})}{V_{dr} - V_{pl}} \tag{15}$$

$$t_{off} = \frac{R_G(Q_{GD} + Q_{GS})}{V_{pl}} \tag{16}$$

where R_G is the gate resistance, here considered to be 10 Ω. Q_{GD}, Q_{GS} and V_{pl} are respectively the gate-drain charge, the gate-source charge and the Miller plateau voltage, which are all given in component datasheets. The GaN components are driven with a voltage $V_{dr} = 5$ V.

For the diode, both conduction and switching losses are taken into acccount:

$$P_{D,cond} = V_F \cdot I_{D,avg} + R_F \cdot I_{D,rms}^2 \tag{17}$$

$$P_{D,sw} = \frac{I_{rr} t_{rr} V_{r,max} f_s}{2} \tag{18}$$

V_F and R_F are respectively the forward voltage drop and the on resistance of the diode. The expressions for the average $I_{D,avg}$, RMS current $I_{D,rms}$ through the diode and the maximum reverse voltage $V_{r,max}$ depends on the topology and is given in Table 4. The diodes that can be selected are given in Table 5. A suitable diode is selected from Table 5 by comparing the maximum voltage across the diode $V_{r,max}$ in the given configuration with the rated reverse blocking voltage $V_{r,rated}$. The maximum voltage over the diode is again a function of the output voltage and the topology. The expressions are listed in Table 4.

The transformer loss model includes conduction losses in both windings and core losses and the calculation method is based on [51, 56].

First, a transformer core is selected from Table 6. Based on the power rating of the transformer S_T, the minumum required characteristic length a_{ch} of the transformer can be calculated [56].

$$a_{ch} = (\frac{S_T}{15.10^6})^{1/3} \tag{19}$$

with

$$S_T = V_{T,p,rms} I_{T,p,rms} + V_{T,s,rms} I_{T,s,rms} \tag{20}$$

When a suitable core is found, the amount of secondary turns can be calculated. The maximum flux swing density ΔB_{max} is set to 0.1 T to limit core losses. The effective core area A_e can be found in Table 6 and the maximum duty cycle δ_{max} is set to 80%.

$$n_{tr,s} = \frac{V_{DC}\delta_{max}}{2A_e\Delta B_{max}f_s} \tag{21}$$

$$n_{tr,p} = \frac{n_{tr,s}}{n_{tr}} \tag{22}$$

From the primary and secondary peak currents in the windings (see Table 4), the wire cross section of the primary A_p and secondary A_s can be calculated using a maximum current density of 5 A/mm^2 [51]. To avoid skin effect losses, the use of Litz wire is assumed. The length of each winding can be calculated using the Mean Length of a Turn (MLT), which is also given in Table 6. The resistance R_p and R_s can be found using Pouillet's law:

$$R_p = \frac{n_{tr,p}MLT\rho_{Cu}}{A_p} \tag{23}$$

$$R_s = \frac{n_{tr,s}MLT\rho_{Cu}}{A_s} \tag{24}$$

$$P_{T,cond} = R_pI^2_{T,p,rms} + R_sI^2_{T,s,rms} \tag{25}$$

The core losses can be found by multiplying the specific core losses P_{Fe} by the effective core volume V_e, listed in Table 6. For N87 material operated at 100 kHz and a flux swing density of 0.1 T, $P_{Fe} = 50.10^3$ W/m^3 [57].

$$P_{T,core} = P_{Fe}V_e \tag{26}$$

Film capacitors using PolyPropylene (PP) are assumed since they have the lowest dissipation factor ($\tan(\delta) = 0.05\%$) [58], from which the Equivalent Series

Table 3: Overview of GaN HEMT properties required for the transistor loss calculation [59, 60, 61, 62].

Type	$V_{DS,rated}$ (V)	$R_{DS,on}$ (mΩ)	Q_{GD} (nC)	Q_{GS} (nC)	V_{pl} (V)	Q_{oss} (nC)
EPC2022	100	4	2.4	3.4	1.4	71
EPC2033	150	8	3.2	3.8	1.4	90
EPC2034C	200	10	2.0	3.8	1.1	96
PGA26E07BA	600	110	2.6	0.9	1.7	45

Resistance (ESR) and the losses can then be calculated:

$$R_{ESR} = \frac{\tan(\delta)}{\omega C} \tag{27}$$

$$P_C = R_{ESR} I_{C,rms}^2 \tag{28}$$

The total power loss in the MLC, $P_{loss,MLC}$ is the sum of the losses in the constituting components.

6.3. Converter derating

A PV installation where the total installed PV power exceeds the inverter power is a practice which is referred to as oversizing (from a PV perspective) or derating (from inverter perspective). The reasoning behind oversizing is that the generated PV power almost never reaches the rated STC output power. In [67], a 260 W PV module coupled to a 215 W micro-inverter is analyzed. The PV output power is below 215 W for approximately 99.5% of the time. The initial investment cost can be reduced by installing an inverter with a lower power rating, which in turn leads to a faster return on investment. When the available PV power exceeds the inverter power rating, the inverter will curtail the current and part of the available energy is lost. Oversizing is adviced by string inverter manufacturers [68] as well as MLC manufacturers [67]. The

Table 4: Overview of voltages and currents for the MLC loss calculation as a function of the input current I_{in}, the duty cycle δ and the inductor current ripple ΔI.

	Boost	IIBC
$I_{L,DC}$	I_{in}	$I_{in}/2$
$I_{L,AC,rms}$	$\frac{\Delta I}{2\sqrt{3}}$	$\frac{\Delta I}{2\sqrt{3}}$
$I_{S,rms}$	$\sqrt{\delta(I_{in}^2 + \frac{1}{3}(\frac{\Delta I}{2})^2)}$	$I_{in}\sqrt{\frac{3}{4} - \frac{\delta}{2}}$
$V_{S,max}$	V_{DC}	$\frac{V_{DC}}{2n_{tr}}$
$I_{D,rms}$	$\sqrt{(1-\delta)(I_{in}^2 + \frac{1}{3}(\frac{\Delta I}{2})^2}$	$\sqrt{(1-\delta)(\frac{I_{in}}{2n_{tr}})^2 + \frac{1}{3}(\frac{\Delta I}{4n_{tr}})^2}$
$I_{D,avg}$	$I_{in}(1-\delta)$	$\frac{I_{in}(1-\delta)}{2n_{tr}}$
$V_{D,max}$	V_{DC}	$V_{DC}/2$
$I_{C,rms}$	$\sqrt{I_{D,rms}^2 - (I_{in}(1-\delta))^2}$	$\sqrt{I_{D,rms}^2 - (\frac{I_{in}(1-\delta)}{4n_{tr}})^2}$
$I_{T,p,rms}$	NA	$\frac{I_{in}\sqrt{2(1-\delta)}}{2}$
$V_{T,p,rms}$	NA	$\frac{V_{DC}}{2n_{tr}}$
$I_{T,s,rms}$	NA	$\frac{I_{in}\sqrt{2(1-\delta)}}{2n_{tr}}$
$V_{T,s,rms}$	NA	$\frac{V_{DC}}{2}$

Table 5: Overview of diode properties required for the transistor loss calculation [63, 64, 65, 66].

Type	$V_{r,rated}$ (V)	$I_{F,rated}$ (A)	V_F (V)	R_F (mΩ)	t_{rr} (ns)	I_{rr} (A)
STTH802	200	8	0.73	21	17	5.5
STTH1003S	300	10	0.86	24	28	5.7
STTH8R04	400	8	0.83	34	25	5.5
STTH15RQ06-Y	600	9	0.9	107	35	6.0

Table 6: Overview of transformer core properties required for the transistor loss calculation [56].

Type	a_{ch} (mm)	A_e (mm^2)	MLT (mm)	V_e (mm^3)
RM10	28.5	83	52	3470
RM12	37.6	146	61	8320
RM14	42.2	198	71	13900

'ideal' amount of oversizing is however strongly dependent on the geographical location and economical factors such as feed-in tariffs.

For this paper, oversizing is taken into account and specified by the Derating Factor (DF). Note that this paper focuses on effiency, which is influenced by the DF. For example the cable cross section and thus the cable losses will depend on the total installed MLC power. Cost aspects are only considered from a qualitative point-of-view. The DF is a number between 0 and 1 and defined as:

$$DF = 1 - \frac{I_{MLC,max}}{I_{MPP,STC}} \tag{29}$$

A DF of 20% for a PV module with $I_{MPP,STC} = 10$ A, would mean that an MLC with a maximum current rating of 8 A is installed. The DF is an important degree of freedom for the system design. To make an informed choice on the used DF, electrical measurements on four PV mini-modules, consisting of 9 PV cells were analyzed. The first two mini-modules were installed on the BIPV testsite in Leuven, Belgium and are vertically tilted (90°). The last two are installed on the roof of EnergyVille, Genk, Belgium and tilted at 35°. An overview of their electrical parameters is given in Table 7. Note that only mini-module one and two (90°tiled) are of interest for this paper, as the focus is on façace BIPV applications. Mini-modules three and four are however included to highlight the difference between both inclinations.

The actual V_{MPP} and I_{MPP} were measured over the timespan of one year,

Table 7: Overview of 9 cell mini-module properties, which are used for evaluating the derating factor.

Number	Location	Tilt (°)	Type	$V_{MPP,STC}$ (V)	$I_{MPP,STC}$ (A)
1	1	90	Bifacial c-Si	4.919	8.379
2	1	90	Monofacial c-Si	4.470	7.780
3	2	35	Bifacial c-Si	4.854	8.275
4	2	35	Monofacial c-Si	4.380	8.120

from 1 October 2018 up to 30 September 2019. The total available energy from the mini-modules can be found by multiplying the voltage and current and integrating over the entire year. An inverter with no derating (DF = 0) can capture all the energy, assuming that the irradiance does not exceed 1000 W/m^2. This value is denoted by E_0.

$$E_0 = \int_{t_0}^{t_{end}} V_{MPP} I_{MPP} dt \tag{30}$$

When derating is applied, a certain percentage of the total available energy will be lost due to clipping as the converter will limit the PV current, Eqn. (31). The remaining energy is calculated by setting all current values above the inverter rating, equal to the inverter rating. The voltage profile is not changed.

$$I_{DF} = \begin{cases} I_{MPP}, & \text{if } I_{MPP} \leq I_{MLC,max} \\ I_{MPP}(1 - DF), & \text{if } I_{MPP} > I_{MLC,max} \end{cases} \tag{31}$$

$$E_{DF} = \int_{t_0}^{t_{end}} V_{MPP} I_{DF} dt \tag{32}$$

The results are shown in Fig. 7 where the remaining energy is calculated as E_{DF}/E_0. It can be seen that the same DF leads to a large difference in remaining energy between the 35°and 90 °tilted panels. Due to the less favourable position towards the sun, high irradiance events and thus high currents, occur less often for the latter. Here, derating has less impact on the produced energy. A second

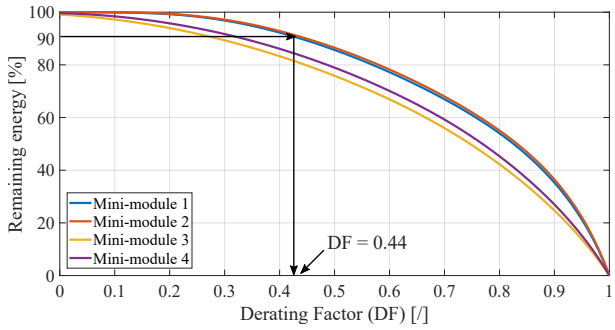


Figure 7: Remaining energy as a function of the derating factor for the four considered mini-modules. The required derating to maintain 90% of the energy is indicated.

difference is visible between the monofacial and bifacial mini-modules where the difference is more pronounced for the 35°tilted mini-module. Bifacial modules are able to absorb sunlight coming from both the front and back of the cell, which leads to a higher current generation. In this paper, the interest is on finding a suitable DF for a Belgian building. From Fig. 7, it can be seen that still 90% of the energy is available when a DF of 44% is applied for the 90°inclined modules. In the remainder of the manuscript, a DF = 40% will be assumed.

Note that the approach is conservative in the sense that it will lead to an underestimation of the remaining energy. Indeed, when the PV module is operated outside of the MPP point by reducing the current, the voltage will increase. All the curves in Fig. 7 are thus pessimistic estimates.

7. Cabling

The generated PV power is first conditioned by the MLC and then transported towards the VBC using cables. Also in the cables, losses occur which is dependent on the used system and the cable cross section; both will be discussed separately.

Table 8: Overview of cable properties for calculating the required cable cross section and losses [69].

S (mm^2)	$R_{DC,20}$ (mΩ/m)	$R_{DC,70}$ (mΩ/m)	$I_{CAB,rated,30}$ (A)	$I_{CAB,rated,70}$ (A)
1.5	12.10	14.46	23	13.57
2.5	7.41	8.86	32	18.88
4.0	4.61	5.51	42	24.78
6.0	3.08	3.68	54	31.86

7.1. Cable selection

For a given case, a cable needs to be selected. An overview of cable properties is presented in Table 8. S is the cable cross section, $R_{DC,20}$ and $R_{DC,70}$ are the resistance per meter at respectively 20 °C and 70 °C. $I_{CAB,rated,30}$ and $I_{CAB,rated,70}$ is the rated cable current assuming an ambient temperature of respectively 30 °C and 70 °C. The required cable cross section will primarily be determined by the total power of the installation and the DC voltage level, as they determine the maximum cable current:

$$I_{CAB,max} = \frac{n_m I_{MLC,max}}{2} = \frac{n P_{MLC,max}}{2 V_{DC}} \tag{33}$$

A cable manufacturer specifies the rated (maximum) current $I_{CAB,rated}$ in the datasheet for an ambient temperature of 30 °C. The cable is assumed to be integrated in the BIPV frame together with the MLC. Ambient temperatures up to 70 °C in the frame of curtain wall modules have been reported by [30]. The datasheet values thus need to be recalculated to 70 °C. For the resistance, this is done using Pouillet's law. For the rated cable current, a temperature correction factor k_T needs to be applied. For 70 °C, $k_T = 0.59$ [69]. The expression for selecting a cable based on the ampacity becomes:

$$I_{CAB,max} < k_T I_{CAB,rated} \tag{34}$$

Also the voltage increase along the cable, ΔV_{CAB} is considered and should not exceed a given limit, ΔV_{max} when the installation is working under full power. This is expressed by the factor k_V. Typically a maximum difference of 10% with respect to the nominal voltage is allowed, so $k_V = 0.1$. The voltage increase ΔV_{CAB} is calculated in a worst case scenario using the DC cable resistance at 70 °C, $R_{DC,70}$, the width of the modules w_m and the maximum output current of the MLCs $I_{MLC,max}$.

$$\Delta V_{max} > \Delta V_{CAB} \tag{35}$$

$$k_V V_{DC} > 2 w_m R_{DC,70} I_{MLC,max} \sum_{k=1}^{n_m/2} k \tag{36}$$

A third aspect that a system designer might want to take into account for selecting a cable size, is the amount of losses. The system can be designed in such a way that, under full power, the cable losses do not exceed a specific percentage of the total installed power. This is expressed by the factor k_P.

$$n k_P P_{MLC,max} > 4 R I_{MLC,max}^2 \sum_{k=1}^{n/2} k^2 \tag{37}$$

Equations (33) - (37) were evaluated as a function of n_m and $P_{MLC,max}$ for four different bipolar systems: +48 V/0/-48 V, +100 V/0/-100 V, +190 V/0/-190 V and +380 V/0/-380 V. A maximum cable cross section of 6 mm^2 and a module width $w_m = 1$ m are assumed. Figure 8 shows the minimal required voltage level for a given installation. 48 V systems can only be used for relatively small installations where the amount of modules and the power per module are limited. Increasing the voltage level allows to serve larger installations. Note the region in the right upper corner which requires a higher DC bus voltage (>380 V) under the given constraints.

The three different limits were also investigated separately for a +100 V/0/-100 V system, and the result is shown in Fig. 9. The maximum current through the wires is the most stringent limitation over the considered range.

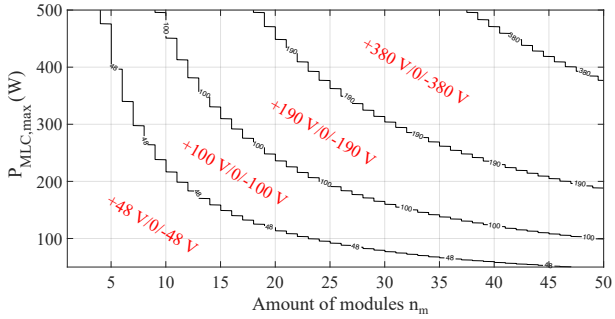


Figure 8: Minimum required voltage level as a function of n_m, $P_{MLC,max}$ for $k_T = 0.59$,$k_V = 0.1$,$k_P = 0.02$ and a maximum cable thickness of 6 mm^2.

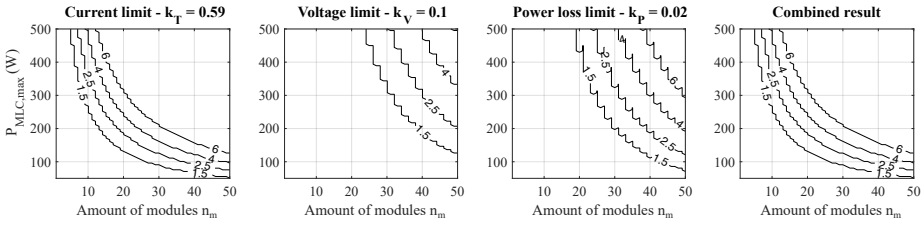


Figure 9: Separate and combined results for cable selection in a +100 V/0/-100 V system as a function of the total amount of modules in the system (n_m) and the maximum MLC output power ($P_{MLC,max}$). The lines indicate the transition from one cable cross section to another.

Once the cable cross section is determined for a given case, the cable power loss $P_{loss,CAB}$ is calculated:

$$P_{loss,CAB} = 4 w_m R_{DC,70} I_{MLC}^2 \sum_{k=1}^{n_m/2} k^2 \tag{38}$$

8. Voltage balancing converter

The function of the VBC is to balance the bipolar BIPV feeder and to perform the required voltage boost from the BIPV feeder to the remainder of the LVDC grid in the building, which is here assumed to be at +380 V/0/-380 V. Note that, when a BIPV feeder voltage of +380 V/0/-380 V is considered, the

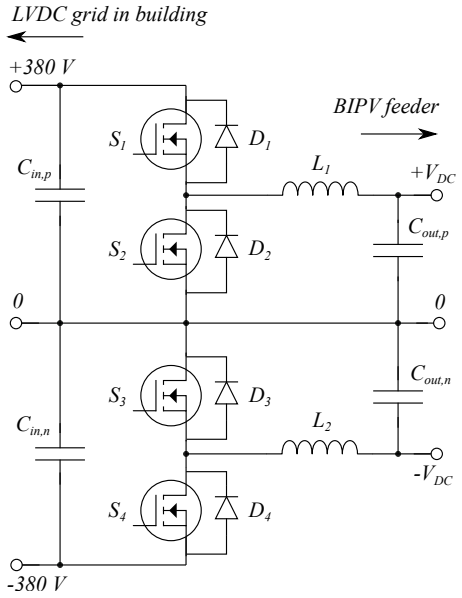


Figure 10: Three-level boost converter topology, used as a VBC to couple the BIPV feeder with the LVC grid inside the building.

VBC is not strictly required. The step-up function is then omitted but the balancing is still performed.

A full bridge three-level converter is a topology that is able to perform these functions and the circuit topology is shown in Fig. 10. An experimental prototype and efficiency results were presented in [28, 27]. The loss model will not be included here as it is similar to the derivations in section 6. For the exact loss model, [27] can be consulted. The VBC efficiency results as a function of the power level are summarized in Fig. 11. Four different BIPV feeder voltage levels (+48 V/0/-48 V, +100 V/0/-100 V, +190 V/0/-190 V and +380 V/0/-380 V) are plotted and the LVDC grid voltage is +380 V/0/-380 V. Note that the efficiency is strongly impacted when the ratio between input and output voltage increases. The losses in the VBC are denoted as $P_{loss,VBC}$

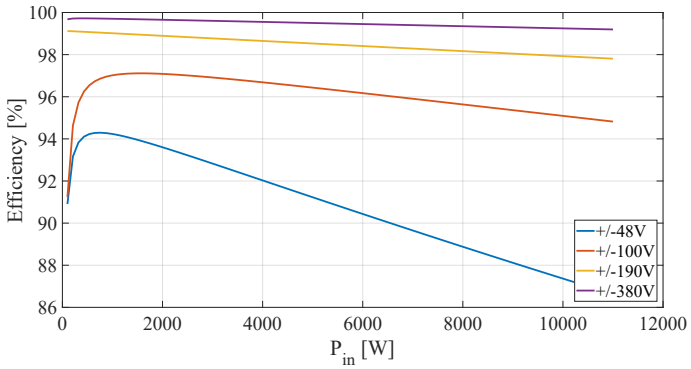


Figure 11: Modeled conversion efficiency of the VBC for different input voltages and a fixed output voltage of +380/0/-380 V. The efficiency drops significantly when lower DC feeder voltages are considered.

Table 9: Overview of building properties that are used as an input for the case studies.

Building	Aramis	South tower
Location	Diegem, Belgium	Brussels, Belgium
Coordinates	50.8877, 4.4590	50.8376, 4.3361
n_m	42	22
w_m (m)	1.4	1.8
l_m (m)	4	4
S_{PV}	0.2	0.4

9. Case studies

To investigate the efficiency as a function of the BIPV feeder voltage level and the used PV technology, two case study buildings were selected. Both buildings are located in Belgium and have no BIPV modules installed. An overview of relevant properties is given in Table 9.

For both buildings, three voltage levels (100 V, 190 V and 380 V) and four PV technologies (c-Si RC, c-Si HC, c-Si SC and CIGS) are considered. Note that the 48 V system is not included as the cable cross section would exceed the boundary conditions as discussed in section 7. In total, 18 different cases

are investigated. The STC voltage and current are listed in Tables 10 and 11.

To compare the cases with one another, several KPIs are used. The minimal output voltage of the PV panel, taking into account temperature and activated by-pass diodes, is denoted with V_{min}. From V_{DC} and V_{min}, the maximum gain G_{max} and the corresponding MLC topology can be determined. P_{tot} is the total installed PV power and S the required cable cross section. The energy generated by the PV generator is denoted with E_{PV} and the energy which is injected into the grid with E_{grid}. The losses in the MLC, the cabling and the VBC are designated by, respectively, $E_{loss,MLC}$, $E_{loss,CAB}$ and $E_{loss,VBC}$. They are calculated through numerical integration of the calculated power losses $P_{loss,MLC}$, $P_{loss,CAB}$ and $P_{loss,VBC}$.

The system efficiency, η_S, is calculated every time sample and is given by:

$$\eta_S = \frac{n_m P_{PV} - n_m P_{loss,MLC} - P_{loss,CAB} - P_{loss,VBC}}{n_m P_{PV}} \tag{39}$$

The result is shown in Figs. 13 and 17 where it is calculated for August 30, 2019 using the input data shown in Fig. 5. The peak efficiency η_P is defined as the maximum of η_S over the given profile. The total conversion efficiency η_T is calculated using the total produced energy and the losses:

$$\eta_T = \frac{E_{grid}}{E_{PV}} \tag{40}$$

An overview of the outcomes is given in Tables 10 and 11.

9.1. Results and discussion

When inspecting the results that are shown in Tables 10 and 11, and displayed in Figs. 12-19, several conclusions can be drawn.

The main difference between both examined buildings is in the total power level of the installation. Due to the larger BIPV modules of the South Tower, the total installed power P_{tot} is higher. As a consequence, 48 or 100 V systems are excluded given the boundary conditions on the cable cross section. Furthermore, the PV voltages are also higher due to the larger module dimensions for the South Tower case. Note also that the total installed PV power P_{tot} differs

Table 10: Overview of the simulation outcomes for the Aramis building. Both the total losses as the intermediate results are given.

Case	1	2	3	4	5	6	7	8	9	10	11
V_{DC} (V)	100	190	380	100	190	380	190	380	100	190	380
PV type	c-Si RC	c-Si RC	c-Si RC	c-Si HC	c-Si HC	c-Si HC	c-Si SC	c-Si SC	CIGS	CIGS	CIGS
V_{STC} (V)	21.96	21.96	21.96	46.08	46.08	46.08	135.24	135.24	80.00	80.00	80.00
I_{STC} (A)	8.55	8.55	8.55	4.78	4.78	4.78	1.82	1.82	2.10	2.10	2.10
V_{min} (V)	5.18	5.18	5.18	10.90	10.90	10.90	31.90	31.90	65.00	65.00	65.00
G_{max}	19.3	36.7	73.3	9.2	17.5	35.0	6.0	11.9	1.5	2.9	5.8
MLC	IIBC	IIBC	IIBC	IIBC	IIBC	IIBC	IIBC	IIBC	boost	boost	IIBC
P_{tot} (W)	7889	7889	7889	9241	9241	9241	10338	10338	7056	7056	7056
S (mm^2)	6.0	1.5	1.5	6.0	2.5	1.5	2.5	1.5	4.0	1.5	1.5
E_{PV}(MJ)	72.0	72.0	72.0	84.3	84.3	84.3	94.2	94.2	64.4	64.4	64.4
E_{grid} (MJ)	67.9	67.5	63.9	79.6	79.9	77.4	87.9	85.7	61.2	60.0	55.7
$E_{loss,tot}$ (MJ)	5.3	4.9	8.3	6.0	5.0	7.2	7.0	8.9	4.0	4.8	8.8
$E_{loss,MLC}$ (MJ)	3.4	3.8	7.9	3.8	3.8	6.7	5.6	8.3	2.4	3.8	8.5
$E_{loss,CAB}$ (MJ)	0.7	0.7	0.2	0.9	0.6	0.2	0.8	0.3	0.8	0.6	0.1
$E_{loss,VBC}$ (MJ)	1.2	0.4	0.2	1.2	0.6	0.3	0.6	0.3	0.9	0.4	0.2
η_P (%)	93.2	93.8	90.7	93.6	94.7	93.4	93.8	92.9	94.5	93.9	89.8
η_T (%)	92.7	93.2	88.5	92.9	94.0	91.5	92.6	90.6	93.7	92.6	86.3

Table 11: Overview of the simulation outcomes for the South Tower building. Both the total losses as the intermediate results are given.

Case	12	13	14	15	16	17	18
V_{DC} (V)	190	380	190	380	380	190	380
PV type	c-Si RC	c-Si RC	c-Si HC	c-Si HC	c-Si SC	CIGS	CIGS
V_{STC} (V)	60.39	60.39	126.72	126.72	347.76	160.00	160.00
I_{STC} (A)	8.55	8.55	4.78	4.78	1.82	2.70	2.70
V_{min} (V)	14.20	14.20	29.90	29.90	82.00	130.00	130.00
G_{max}	13.3	26.6	6.4	12.7	4.6	1.5	2.9
MLC	IIBC	IIBC	IIBC	IIBC	boost	boost	boost
P_{tot} (W)	11359	11359	13326	13326	13894	9504	9504
S (mm^2)	2.5	1.5	4.0	1.5	1.5	2.5	1.5
E_{PV}(MJ)	103.7	103.7	121.5	121.5	127	86.7	86.7
E_{grid} (MJ)	99.7	98.7	116.5	115.6	121.9	83.9	81.7
$E_{loss,tot}$ (MJ)	5.1	5.4	6.4	6.4	5.5	3.7	5.3
$E_{loss,MLC}$ (MJ)	3.3	4.7	4.4	5.5	4.6	2.3	4.8
$E_{loss,CAB}$ (MJ)	0.7	0.3	0.6	0.4	0.4	0.5	0.2
$E_{loss,VBC}$ (MJ)	1.1	0.4	1.4	0.5	0.5	0.9	0.3
η_P (%)	95.4	95.6	95.2	95.6	96.5	96.2	95.2
η_T (%)	95.1	94.8	94.8	94.7	95.7	95.7	93.9

strongly due to the different PV efficiencies in terms of power generation per unit area in W/m^2. For the same façade, a difference of 46% in terms of power rating can be achieved. For one floor level of the Aramis building this comes down to an increase of more than 3280 (Watt-peak) Wp of installed PV power between CIGS and c-Si SC. For the South Tower, the difference is even more pronounced due to the larger modules, being 4390 Wp.

Figs. 12 and 16 highlight the total energy loss $E_{loss,tot}$ of every case. It can be concluded that reducing the DC bus voltage below 380 V is beneficial for the total losses in every case. The total losses remain within the same order of magnitude but comparing cases 9 (CIGS at 100 V) and 11 (CIGS at 380 V), the losses can be halved by going from 380 V to 100 V. The best performing system in terms of total losses for the Aramis and South Tower building are respectively case 9 (CIGS at 100 V) and case 17 (CIGS at 190 V). The systems with the highest total losses are respectively case 8 (c-Si SC at 380 V) and case 15 (c-Si SC at 380 V). Investigating the system efficiency η_S in Figs. 13 and 17 highlights that, when the converters are working under full power, the best performing system is case 7 (c-Si SC at 190 V) for the Aramis building and case 16 (c-Si SC at 380 V) for the South Tower building. The worst performing systems in terms of efficiency are case 11 (CIGS at 380 V) and case 18 (CIGS at 380 V). The difference between the cases with highest/lowest efficiency and lowest/highest total losses are a consequence of the different PV efficiencies, as a different power per unit area is generated by different PV technologies. As discussed above, CIGS and c-Si SC have respectively the lowest and highest efficiency per unit area. To calculate the system efficiency η_S, not only the total losses but also the total generation is taken into account. Hence, the notable difference between the cases.

The overall loss distribution, shown in Figs. 14 and 18, is similar for all cases: By far, the majority of the losses is situated in the MLC, $E_{loss,MLC}$. The cable losses $E_{loss,CAB}$ and VBC losses $E_{loss,VBC}$ are much lower. When V_{DC} increases, the difference between $E_{loss,MLC}$ and the sum of $E_{loss,CAB}$ and $E_{loss,VBC}$ becomes more distinct. In contrast, reducing V_{DC} is always ben-

eficial from the MLC point of view as $E_{loss,MLC}$ decreases. As discussed in sections 1 and 2, the MLC is preferably embedded in the frame of the curtain wall module for reasons of cost. This is challenging as it becomes increasingly difficult to maintain the MLC or replace it in case of failure. Furthermore, the expected ambient temperatures in the frame are relatively high, which is detrimental for the lifetime of the electronics. The MLC components will experience a total temperature which is equal to the sum of the ambient temperature and the temperature increase due to the losses in the component. As $E_{loss,MLC}$ decreases for lower V_{DC}, so will the component temperature. From this perspective, reducing V_{DC} is an effective method to increase MLC lifetime. Note that the increased losses in the VBC are less severe. In contrast to the MLCs, which are frame-embedded, the VBC is placed inside the building. This also means that there are no strict boundary conditions on its dimensions or on the lifetime as it is much easier to access and repair the VBC in case of a failure.

However, reducing V_{DC} too much is not always beneficial when the total conversion efficiency η_T is considered. From the three considered voltages, the optimum is always found at 190 V. When going from 190 to 100 V, the reduction of losses in the MLC is lower than the increase of losses in the cables. The sole exception to this is case 9, where 100 V is the optimal DC bus voltage. Overall, a DC bus of 190 V has a superior performance in terms of system efficiency.

Another aspect which is important for the embedment of the MLC, is the topology. It was highlighted in sections 1 and 6 that a boost converter is beneficial in terms of size, as no transformer is required, and in terms of reliability and cost as it has a lower component count. As discussed in section 5, CIGS has the advantage of a better tolerance against partial shading. Due to the larger cell granularity, the voltage does not collapse that rapidly. This in turn leads to the possible use of boost converters in cases 9, 10, 16, 17 and 18, as G_{max} is in these cases below five. Besides the effect on size, cost and reliability, it can also be seen from Tables 10 and 11 that CIGS has the highest total conversion efficiency η_T for both buildings (cases 9 and 17).

Although two Belgium buildings have been used as case studies, it is impor-

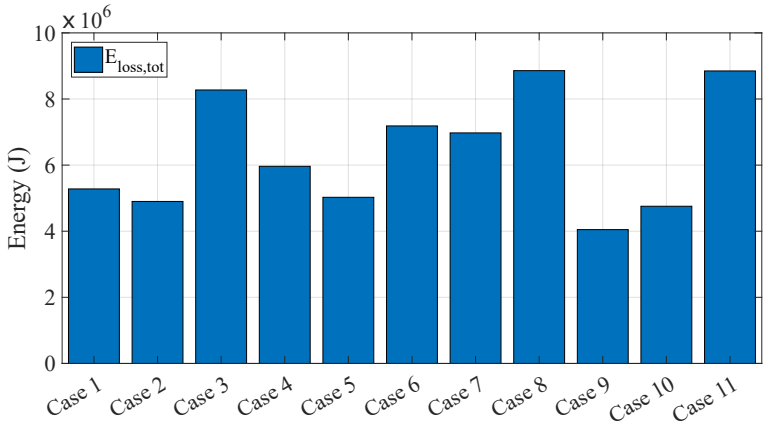


Figure 12: Total energy loss for different cases of the Aramis building, evaluated on August 30, 2019.

tant to note that the methodology, the developed loss model and conclusions can easily be extended to other countries.

10. Conclusions

The PV technology and the DC bus voltage are two important parameters when designing BIPV electrical installations. Conversion efficiency, cost and lifetime are strongly impacted by these choices. The focal point of this paper was the effect on losses and the overall efficiency. A methodology was presented that allows to calculate the losses in every conversion step for a given building, based on recorded electrical measurements of a prototype BIPV curtain wall element. First, the electrical installation was studied and a bipolar system with VBC in the middle turned out to be the best solution. Detailed loss models were provided for the MLC, the cabling and the VBC. Special attention was given to the amount of converter derating and its impact on the reduced energy generation. From BIPV measurements, it was shown that a derating factor of 0.4 allows to gather more than 90% of the energy on a yearly basis. Cable boundary conditions on voltage drop, ampacity and losses allowed to define an upper limit for the amount of modules and the MLC power level for a given

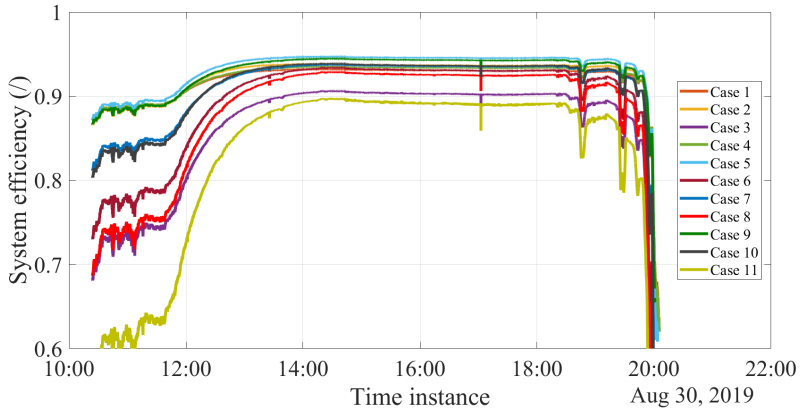


Figure 13: System efficiency η_S as a function of time for the Aramis building for different PV types and DC bus voltages (cases 1-11).

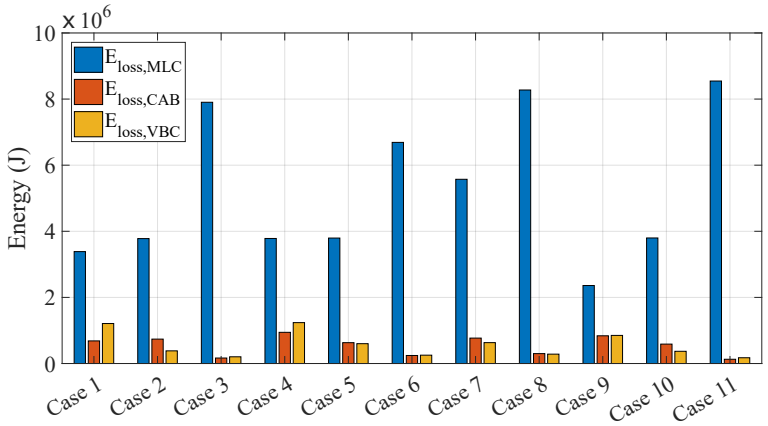


Figure 14: Loss distribution for different cases of the Aramis building, evaluated on August 30, 2019.

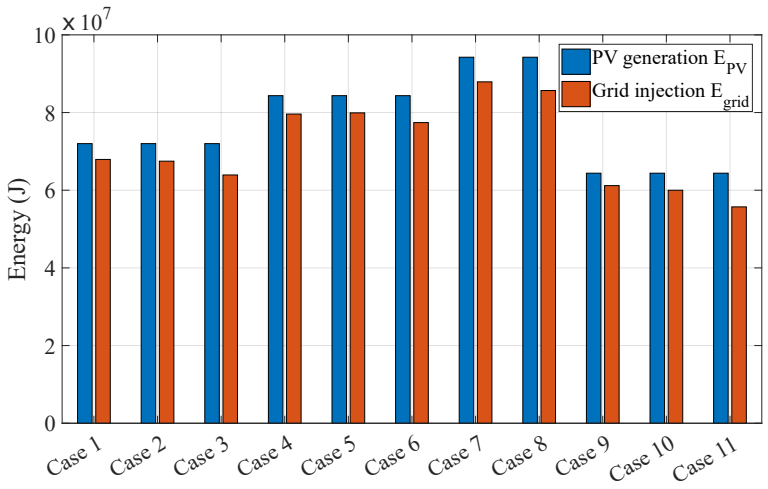


Figure 15: PV generation and grid injection for different cases of the Aramis building, evaluated on August 30, 2019.

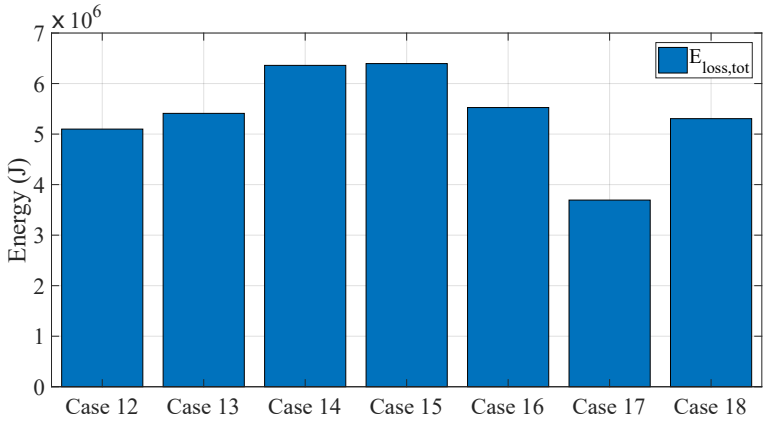


Figure 16: Total energy loss for different cases of the South Tower building, evaluated on August 30, 2019.

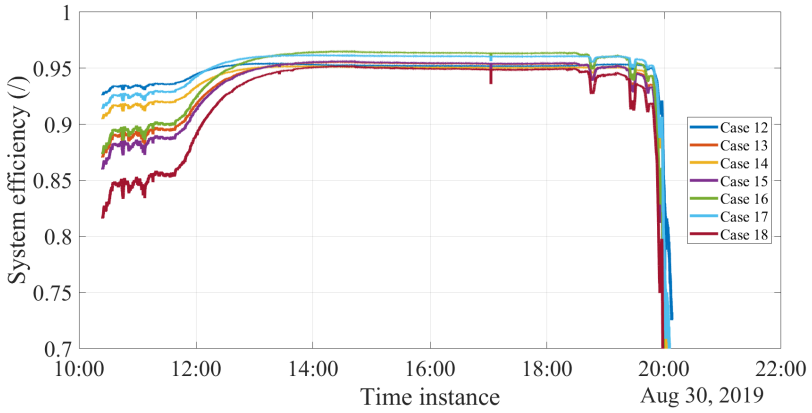


Figure 17: System efficiency η_S as a function of time for the South Tower building for different PV types and DC bus voltages (cases 12-18).

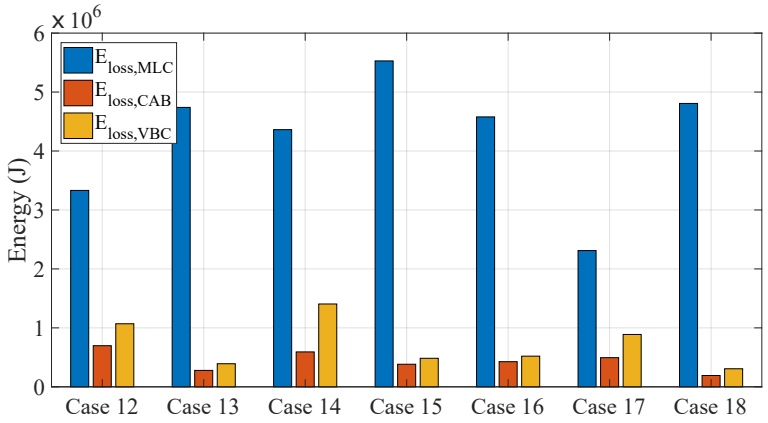


Figure 18: Loss distribution for different cases of the South Tower building, evaluated on August 30, 2019.

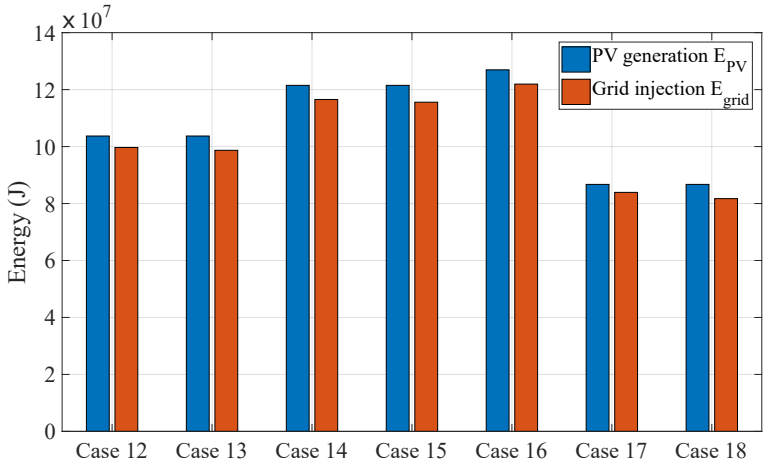


Figure 19: PV generation and grid injection for different cases of the South Tower building, evaluated on August 30, 2019.

voltage. Furthermore, it was shown that the current limit is the most stringent.

Two PV technologies with different internal cell geometries and three voltage levels were evaluated over the course of a day for two case study buildings. Efficiencies in the order of 90% or higher are achieved when the total energy production is regarded, and more than 96% can be achieved with careful optimization of the converters and cabling. When the difference between V_{PV} and V_{DC} reduces or when simpler MLC topologies can be used, the efficiency typically increases. Moreover, the loss distribution is strongly affected by reducing the voltage level. This is beneficial for the lifetime of the MLCs, given that they are preferably frame-embedded and thus difficult to maintain.

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Nomenclature

Abbreviations

AC	Alternating Current
BAPV	Building-Applied Photovoltaics
BIPV	Building-Integrated Photovoltaics
c-Si	Monocrystalline Silicon
C	Capacitor
CCM	Continuous Conduction Mode
CdTe	Cadmium Telluride
CIGS	Cadmium Indium Germanium Sulfide
D	Diode
DC	Direct Current
DF	Derating Factor
EPBD	Energy Performance of Buildings Directive
ESR	Equivalent Series Resistance
GaN	Gallium Nitride
HC	Half Cell
HEMT	High Electron Mobility Transistor
IIBC	Isolated Interleaved Boost Converter
KPI	Key Performance Indicator
L	Inductor
LVDC	Low-Voltage Direct Current
MLC	Module Level Converter
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracker
NA	Not Applicable
NZEB	Near Zero Energy Buildings

PV	Photovoltaics
PP	PolyPropylene
RC	Regular Cell
S	Switch
SC	Shingled Cell
SET	Strategic Energy Technology
STC	Standard Test Conditions
T	Transformer
VBC	Voltage Balancing Converter

Symbols

Symbol	Unit	Meaning
α		Steinmetz coefficient
α_{Isc}	%/K	Short circuit current temperature coefficient
β		Steinmetz coefficient
β_{Vmpp}	%/K	MPP voltage temperature coefficient
β_{Voc}	%/K	Open circuit voltage temperature coefficient
δ		Duty ratio
δ'	m	Skin depth
δ_{max}		Maximum duty ratio
Δ		Penetration ratio
ΔI	A	Inductor current ripple
ΔB	T	Flux swing density
ΔV_{CAB}	V	Voltage increase along the cable
ΔV_{max}	V	Maximum allowed voltage increase along the cable
η_S		System efficiency
η_P		Peak efficiency
η_T		Total conversion efficiency
μ_0	H/m	Permeability of free space
μ_{Cu}	H/m	Copper permeability
$\mu_{r,Cu}$		Copper relative permeability
ρ_{Cu}	Ωm	Copper resistivity
ω	rad/s	Angular frequency
a_{ch}	m	Characteristic transformer dimension
A_e	m^3	Effective transformer core volume
A_p	m^2	Transformer primary winding cross section
A_s	m^2	Transformer secondary winding cross section
B	T	Magnetic flux density
C	F	Capacitance
d	m	Wire diameter

E_0	J	Available energy with no derating
E_{DF}	J	Available energy for a given DF
E_{grid}	J	Grid injected energy
$E_{loss,tot}$	J	Total energy loss
$E_{loss,CAB}$	J	Cable energy loss
$E_{loss,MLC}$	J	MLC energy loss
$E_{loss,VBC}$	J	VBC energy loss
E_{PV}	J	PV generated energy
f_s	Hz	Switching frequency
G_{max}		Maximum voltage gain
G_{VBC}		VBC voltage gain
$I_{C,rms}$	A	Capacitor RMS current
$I_{CAB,max}$	A	Maximum cable current
$I_{CAB,rated,T}$	A	Rated cable current at temperature T
$I_{D,avg}$	A	Diode average current
$I_{D,rms}$	A	Diode RMS current
I_{DF}	A	Current taking a given DF into account
$I_{F,rated}$	A	Rated diode forward current
I_{in}	A	MLC input current
$I_{L,AC,rms}$	A	Inductor AC RMS current
$I_{L,DC}$	A	Inductor DC current
I_{MLC}	A	MLC output current
$I_{MLC,max}$	A	Maximum MLC output current
$I_{MPP,STC}$	A	Maximum Power Point current under STC
I_{on}	A	Transistor turn-on current
I_{off}	A	Transistor turn-off current
Ir	W/m^2	Irradiance
I_{rr}	A	Diode reverse recovery current
$I_{S,rms}$	A	Transistor RMS current
$I_{sc,STC}$	A	Short circuit current under STC

$I_{T,p,rms}$	A	Transformer primary RMS current
$I_{T,s,rms}$	A	Transformer secondary RMS current
k		Steinmetz coefficient
k_P		Cable loss factor
k_T		Cable temperature correction factor
k_V		Cable voltage factor
L	H	Inductance
l_{CAB}	m	Required cable length of one façade
l_{cell}	m	Length of one solar cell
l_m	m	Length of one BIPV module
MLT	m	Mean Length of a Turn
n_{cell}		Amount of PV cells in one entire BIPV module
$n_{cell,x}$		Amount of PV cells along the width of the BIPV module
$n_{cell,y}$		Amount of PV cells along the length of the BIPV module
n_L		Amount of inductor turns
n_m		Amount of BIPV modules along the façade
n_{tr}		Transformer turns ratio
$n_{tr,p}$		Transformer primary turns
$n_{tr,p}$		Transformer secondary turns
P_C	W	Capacitor loss
$P_{D,cond}$	W	Diode conduction loss
$P_{D,sw}$	W	Diode switching loss
P_{Fe}	W/m^3	Specific core loss
$P_{L,AC}$	W	Inductor AC loss
$P_{L,core}$	W	Inductor core loss
$P_{L,DC}$	W	Inductor DC loss
$P_{loss,CAB}$	W	Cable power loss
$P_{loss,MLC}$	W	MLC power loss
$P_{loss,VBC}$	W	VBC power loss
$P_{MLC,max}$	W	Maximum MLC output power

P_{PV}	W	PV output power
$P_{S,cond}$	W	Transistor conduction loss
$P_{S,sw}$	W	Transistor switching loss
$P_{T,cond}$	W	Transformer conduction loss
$P_{T,core}$	W	Transformer core loss
Q_{GD}	C	Transistor gate-drain charge
Q_{GS}	C	Transistor gate-source charge
Q_{oss}	C	Transistor output charge
R	Ω	Cable resistance per BIPV module
$R_{DC,T}$	Ω/m	Cable resistance per meter at temperature T
$R_{DS,on}$	Ω	Transistor on-resistance
R_{ESR}	Ω	Capacitor equivalent series resistance
R_F	Ω	Diode on-resistance
R_G	Ω	Gate resistance
$R_{L,AC}$	Ω	Inductor AC resistance
$R_{L,DC}$	Ω	Inductor DC resistance
R_p	Ω	Transformer primary resistance
R_s	Ω	Transformer secondary resistance
S	m^2	Cable cross section
S_{PV}		Normalized PV dedicated surface of the curtain wall module
S_T	W	Transformer total power rating
$tan(\delta)$		Loss tangent
t_{off}	s	Transistor turn-off time
t_{on}	s	Transistor turn-on time
t_{rr}	s	Diode reverse recovery time
$V_{core,L}$	m^3	Inductor core volume
$V_{D,max}$	V	Diode maximum reverse voltage
V_{DC}	V	Feeder DC voltage
V_{dr}	V	Gate driver voltage
$V_{DS,max}$	V	Transistor maximum blocking voltage

$V_{DS,rated}$	V	Rated transistor blocking voltage
V_e	m^3	Effective core volume
V_F	V	Diode forward voltage drop
V_{in}	V	MLC input voltage
$V_{in,max}$	V	Maximum MLC input voltage
$V_{in,min}$	V	Minimum MLC input voltage
$V_{MPP,STC}$	V	Maximum Power Point voltage under STC
$V_{MPP,T}$	V	Maximum Power Point voltage at temperature T
$V_{oc,STC}$	V	Open circuit voltage under STC
V_{out}	V	MLC output voltage
V_{pl}	V	Miller plateau voltage
V_{PV}	V	PV output voltage
$V_{PV,min}$	V	Minimum PV output voltage
$V_{r,max}$	V	Maximum diode reverse voltage
$V_{r,rated}$	V	Rated diode reverse voltage
$V_{S,max}$	V	Transistor maximum blocking voltage
$V_{T,p,rms}$	V	Transformer primary RMS voltage
$V_{T,s,rms}$	V	Transformer secondary RMS voltage
w_{cell}	m	Width of one solar cell
w_m	m	Width of one BIPV module
Wp		Peak PV output power under STC conditions

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