# Through Package Via: A bottom-up approach

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# Through Package Via

A Bottom-up Approach

# THROUGH PACKAGE VIA

## A BOTTOM-UP APPROACH

**Proefschrift**

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
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door

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*To my dear family and Yunran*

# CONTENTS

# 1

# INTRODUCTION

*Today, the manufacturing of integrated circuits, two dimensional (2D) down-sizing following the "Moore's Law" is no longer yielding the required cost-effective integration of functionalities. This leads to an enhanced and accelerated development of three-dimension (3D) fabrication technologies in wafer manufacturing (front-end) and microelectronic packaging (back-end). Due to the increasing need for a higher degree of integration inside a microelectronic package, conventional front-end technologies are now being introduced in the back-end. The merge of these technologies is often referred to as the mid-end. As an emerging trend, the mid-end becomes the drive for creating innovative products and broadening the product portfolio of microelectronic packaging.*

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## 1.1. 3D PACKAGING AND SYSTEM INTEGRATION: AN OVERVIEW

A microelectronic package bridges the gap between micro/nanoscale devices and macro applications. Furthermore, it protects the often extremely small and sensitive features on the chip from light, force, moisture, chemicals, heat, dust, etc. As the need to integrate more functionalities at a smaller footprint increases, electronic packages with multiple chips and components are developed which increases the complexity inside a single package. In the high-end products, two-dimensional (2D) packaging is being replaced by three-dimensional (3D) packaging. Hence, 3D packaging and system integration are becoming one of the main driving forces in the semiconductor industry. To achieve higher packaging density, the manufacturing dimensions of interconnections inside a package are continuously shrinking down. The reduced feature size leads to the introduction of wafer-level fabrication technologies (front-end)into the microelectronic packaging (back-end) manufacturing. This trend merges the so-called front-end and back-end technologies, often referred to as mid-end, and creates opportunities for new packaging technologies [1–4].

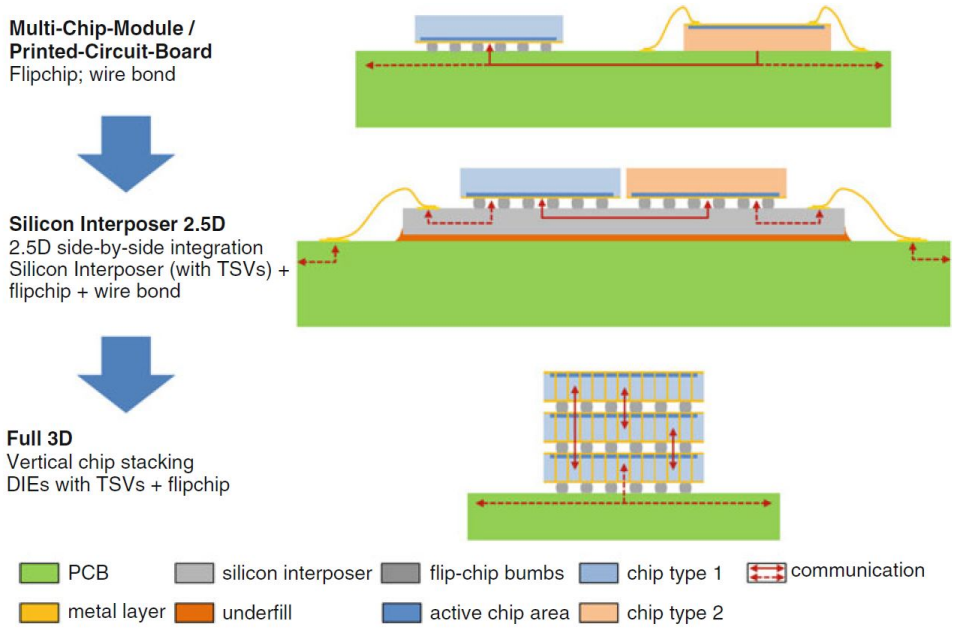


Figure 1.1: Illustration of the development from 2D packaging approach towards 3D packaging approach. Figure adapted from [2].

The development of electronic packaging concept from 2D to 2.5D and 3D are shown in Figure 1.1. To realize a multiple chip module, a conventional 2D system-in-package (SiP) places chips and components side by side on a substrate. Taking one step further, the 2.5D approach utilizes an intermediate substrate, such as a silicon interposer, to bring the interconnection between chips closer. The corresponding size reduction leads to a reduction in cost and increase in performance. The full 3D packaging is more

advanced and enables the stacking of functional chips and components in the vertical direction [5]. Reducing the footprint even more, 3D packaging approach leads to a further reduction of cost per function and an increase in performance.

Main conventional technologies for realizing the interconnection between the chip and its package are wire-bonding, and flip-chip. Wire-bonding utilizes an Au, Al, or Cu wires to make bonds from one contact pads to another [8]. Conventionally, wire-bonding is a flexible packaging technology however is limited in wire density, wire swinging, and loop shape induced drawbacks. Flip-chip utilize solder balls to make a direct connection from the chip to the package [9]. Flip-chip technology can provide high I/O counts and is suitable for 3D integration. However, solder bumps are limited in their aspect ratios which are not suitable for high-aspect-ratio and high density interconnects. Both wire-bonding and flip-chip have developed new technologies to fulfill the requirement of 3D packaging, such as the vertical wire and the Cu pillar.

3D integration technologies, such as chip stacking using through-silicon vias (TSV) and package stacking or package-on-package (POP) using through-mold vias (TMV), are already commercialized technologies [6, 7]. TSV has realized the vertical interconnection on the chip level which uses front-end technologies. TMV, on the other hand, has realized the vertical interconnection on the package level which uses the back-end technologies. TSV is based on the silicon process and is not fully compatible with creating interconnection through package while the current TMV technology is limited in aspect-ratio. Hence, a high-aspect-ratio 3D chip-to-package interconnection technology is needed for a higher integration density with relatively low packaging complexity and higher design flexibility. For example, for RF applications, a given substrate thickness is required for antenna integration. The conventional approach is using the stacking of multiple interconnection layers to realize the substrate thickness leading to complex structures, time-consuming in fabrication, and challenging in reliability. Through package vertical interconnection technologies have the potential to overcome these limitations.

## 1.2. THROUGH PACKAGE VIA TECHNOLOGIES

The state of the art high-aspect-ratio vertical chip-to-package interconnect technologies include through silicon via (TSV) [6, 10–14], through mold via (TMV) [7, 15–18], tall copper pillars (TCP) [19–21] and vertical wires (VWB) [8, 22, 23]. These technologies provide high-aspect-ratio (HAR) interconnections that connect the embedded chips or components to the package level. However, they still have their limitations.

### 1.2.1. THROUGH SILICON VIAS (TSV)

A through-silicon via generally consists of a through-hole in the silicon substrate, a passivation layer covering the through-hole sidewalls, and copper filling using a plating process. TSV process is categorized into three different types depending on the insertion point in the IC fabrication process flow. When TSV is formed before the IC processes, the process is called TSV first. When TSV is formed during the IC process, it is called TSV middle, as shown in Figure 1.2. The third type is called TSV last process where TSVs are fabricated after completing the IC processes. The choice of which type of TSV process to

use depends on the final application of the chip, and the electrical or mechanical properties of the vias. There are several key processes in the TSV fabrication, including deep reactive ion etching (DRIE), the deposition of a dielectric layer, a barrier layer, and a seed layer, the via filling, the chemical mechanical polishing (CMP), and Cu revealing process. The cross-sectional images of TSVs under the scanning electron microscope (SEM) are shown in Figure 1.3. TSVs can be fabricated through wafers with integrated circuits that connect the circuit on the front to the backside or through bare wafers without active areas which are used as an interposer.

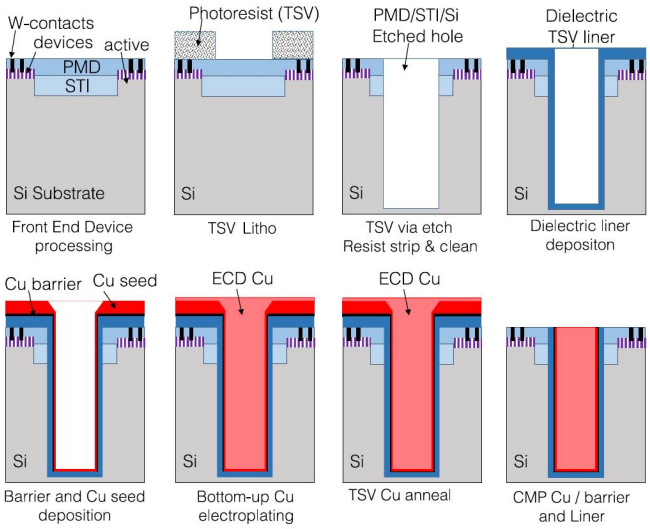


Figure 1.2: Schematic illustration of the main process steps of via-middle TSV fabrication after the front-end process. Figure adapted from [5].

Although TSV is a key technology for the realization of 3D integration and a lot of knowledge has been developed, it still has challenges in reliability and cost which prevent it from being widely adopted in various applications. Challenges especially lie in the process of high-aspect-ratio and high-density via forming where both the DRIE etching of silicon and the conformable Cu filling processes become more difficult and time-consuming. Much research work has been devoted to the influence of via profile and passivation layer[24], the chemical additives in the plating bath [25–27], and the electrical current during Cu plating to the quality of the fabricated TSVs [28]. Stress developed during wafer thinning for revealing the TSVs can also induce wafer breaking which limits the process yield [29]. Furthermore, the CTE mismatch of Cu and Si leads to reliability issues during operation of the device. Although TSV is widely used for creating a via through the silicon chip, its technologies are not one to one suitable for forming a via through the encapsulated package due to significant differences in materials and form factor of a 3D package compared to a silicon substrate. In most of the applications in 3D packing and system integration, a vertical interconnection is required to go through the polymer-based substrate materials such as epoxy molding compound (EMC).

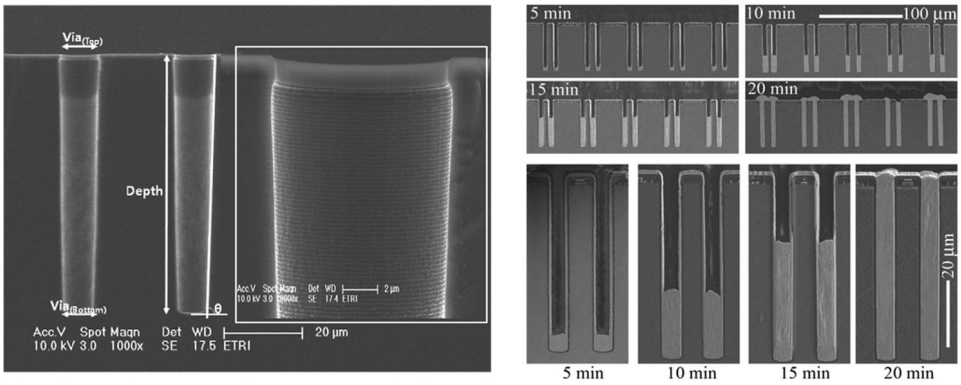


Figure 1.3: SEM images of TSVs. (a) Deep reactive ion etching of silicon (Bosch process). (b) The cross-sectional images showing the bottom-up Cu filling process at a different time frame. Figure adapted from [30].

### 1.2.2. THROUGH MOLD VIAS (TMV)

Through-mold via (TMV) technology was first introduced by Amkor in 2008 [7]. TMV is a via forming technology which is similar to TSV. TMV also has process steps of creating a hole through the substrate and filling the hole with conductive metal [15, 18]. However, the substrate is silicon in TSV, while the substrate is EMC instead in TMV. A schematic illustration of Package-on-Package (PoP) utilizing TMVs is shown in Figure 1.4. In the TMV process, laser drilling is the used technique to open through holes inside the EMC layer [16, 31, 32]. But, EMC is a composite material which contains a large number of fillers. Compare with the epoxy, the silica fillers have a higher melting point which can escape from the drilled hole and interfere with the incoming laser beam and reducing the laser power reaching the bottom. This makes the laser drilling non-uniform and requires extra cleaning. Since the laser drilling is a thermal process, the heat generated during ablation can cause the degradation of the EMC material and even damage the embedded chip. Also, accurate alignment of the drilling site with the underneath metal pad is required, which is challenging due to the non-transparent optical properties of EMC. In addition, the roughness of the drilled hole is largely influenced by the fillers, and a chemical process is needed to smooth the surface in case of large roughness [33].

Different filling techniques can be used in TMV technology. One of them is Cu plating which is similar to TSV however on a much rougher surface. SEM images of laser-drilled high-aspect-ratio through-mold holes plated with a layer of Cu on the inner surface is shown in Figure 1.5 (a), showing a rough sidewall of the laser-drilled holes which largely depends on the filler size of the EMC. With smaller filler size, the roughness of the sidewall profile can be reduced. However, finner filler dimensions will increase the overall cost of the package. Alternatively, a drilled hole can be filled with solder paste [7, 34]. An SEM image of solder filled TMV after reflow is shown in Figure 1.5 (b). But, a drawback of this method is that it is not suitable for high-aspect-ratio through-package vias and thus

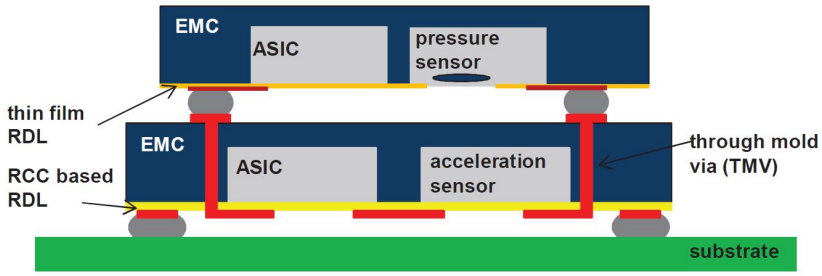


Figure 1.4: Illustration of a package utilizing TMVs. Figure adapted from [15].

is limited in the Via density.

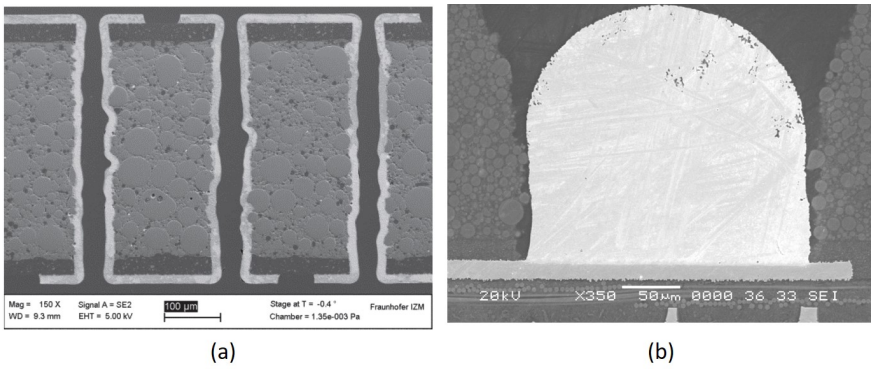


Figure 1.5: SEM images of TMVs. (a) TMVs with Cu coating, figure adapted from [15]. (b) A TMV filled with sold ball [7].

### 1.2.3. TALL COPPER PILLARS (TCP)

In tall Cu pillar (TCP) technology, a thick photoresist is used as the mold for Cu plating, as shown in Figure 1.6. Through-holes are created inside the thick resist layer by lithographical processes. From a Cu seed layer on the bottom substrate, the Cu pillars are plated inside the through-holes in the resist mold. To reach a pillar height above 100 µm, multiple spin coating of resist is required. After the plating process, both the resist and the seed layer are removed. Single dies can be flipped onto the wafer with TCPs and placed on the side of TCPs. The Cu pillars are taller than the placed dies. After the over-molding, the top side of the wafer is then ground back to expose the Cu pillars.

Both TSV and TMV are a top-down approach to create vertical interconnections. Unlike TSV and TMV, tall copper pillar (TCP) technology is a bottom-up approach. The advantage of a bottom-up approach is that the etching or laser drilling of the substrate material is not needed which avoids the corresponding process issues. The bottom-up method also involves less process induced damages which can improve the reliability [19–21].

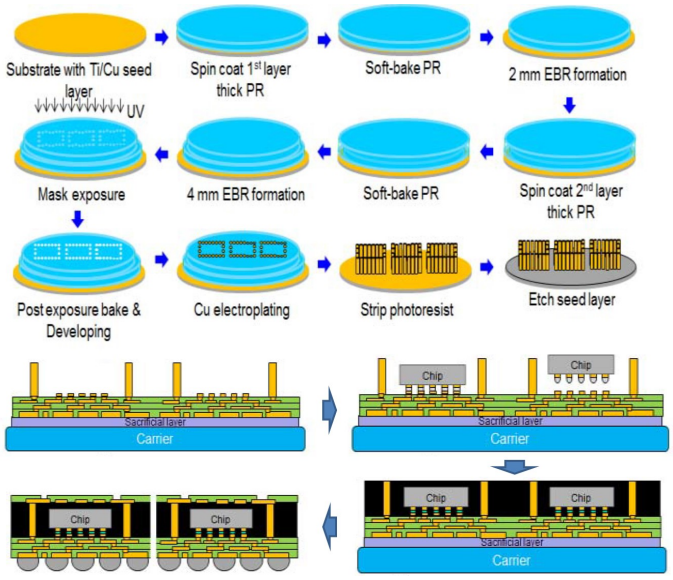


Figure 1.6: The wafer-level fabrication process of tall copper pillars and the steps of assembly and molding. Figures adapted from [35].

Although TCP is a promising alternative to TMV, it has several limitations. Since the plating process starts from the bottom seed layer in the via, the process becomes less efficient when the via goes deeper. Thus for creating high-aspect-ratio TCPs, it becomes more difficult and time-consuming. Furthermore, the height of the pillars is limited by the thickness of the photoresist which makes it challenging to reach a pillar height above 200 µm and more. Additionally, plated tall Cu pillars can suffer from mechanical defects, such as cracks, and other reliability issues.

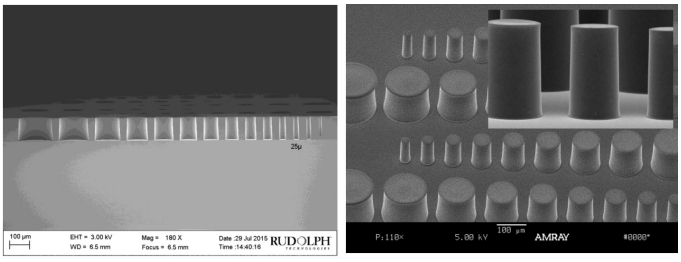


Figure 1.7: SEM images of tall Cu pillars. (a) The thick photoresist mold used for Cu plating. (b) The plated Cu pillars after photoresist removal. Figures adapted from [21].

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### 1.2.4. VERTICAL WIRE-BONDS (VWB)

Vertical wire-bonds (VWB) technology is another bottom-up candidate for through package via formation. VWB employs an optimized wire-bonding technology to form a vertical wire. Instead of bonding at two ends, a vertical wire bond at the surface of the substrate and is pulled straight up and cut off at the desired height [8, 22, 23]. A big advantage of vertical wire technology is that it does not require lithography and other front-end processes. However, a vertical wire occupies a larger surface area at the bottom compared to the diameter of the wire which limits the density of the wires that can be implemented. The cut off cross-section of the wire usually possesses a non-flat tip that needs back-grind after over-molding to create a smooth contact surface for further processing. Also, wire swinging can happen during molding, especially for HAR wires, due to a low stiffness of the wires at molding temperatures.

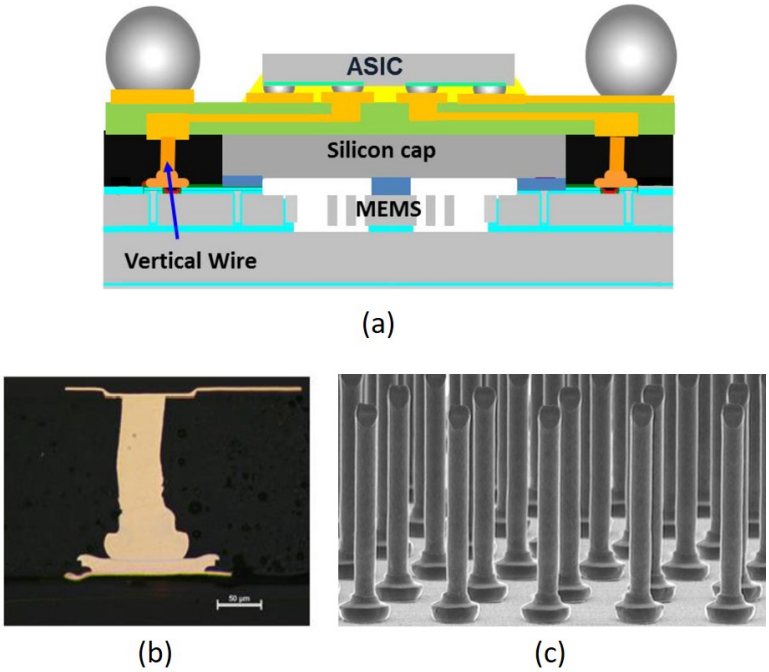


Figure 1.8: Through package vertical interconnection made of vertical wire bonds. (a) The application of vertical wire bonds in a MEMS WLCSP packaging process. (b) The cross-sectional view of a vertical wire bond interconnection after molding. (c) The SEM image of high-aspect-ratio vertical wire bond array. Figures adapted from [8, 22, 35].

### 1.2.5. MOTIVATION FOR A NOVEL THROUGH PACKAGE VIA TECHNOLOGY

The state of the art chip-to-package vertical interconnection technologies including TSV, TMV, TCP, VWB technologies have enabled a large variety of applications of 3D integration in microelectronic packaging. However, these technologies each has its own limitations. Briefly, TSV is limited in cost, reliability, and substrate material. TMV is limited

in its process induced damages, aspect-ratio, density, the capability of creating finner feature size, and the quality of EMC material. TCP is limited in maximum pillar height and aspect-ratio and its mechanical reliability. VWB is limited due to wire swinging and the ratio between the bottom diameter and the wire diameter.

As the need for 3D integration in microelectronic packaging keeps increasing, not only electrical vertical interconnection is needed, but also more functions such as optical, mechanical, and micro-fluidic need to be integrated which requires "composite" via forming technologies to cover multi-physical application domains. Thus new via forming technology which provides a packaging solution that is low-cost, flexible process ability, suitable for high-aspect-ratio, high density, with a large applicable range of dimensions, and capable of providing multi-physical interconnection is highly demanded.

## 1.3. A BOTTOM-UP APPROACH: THROUGH-POLYMER VIA (TPV) TECHNOLOGY

Through-Polymer Via (TPV) technology, first introduced in 2015 [36], is a promising new via forming technology which can potentially fulfill the requirement of the new 3D integration era of low-cost, with flexible process ability, suitable for high-aspect-ratio and high density, with a large applicable range of dimensions, capable of providing multi-physical interconnection [37].

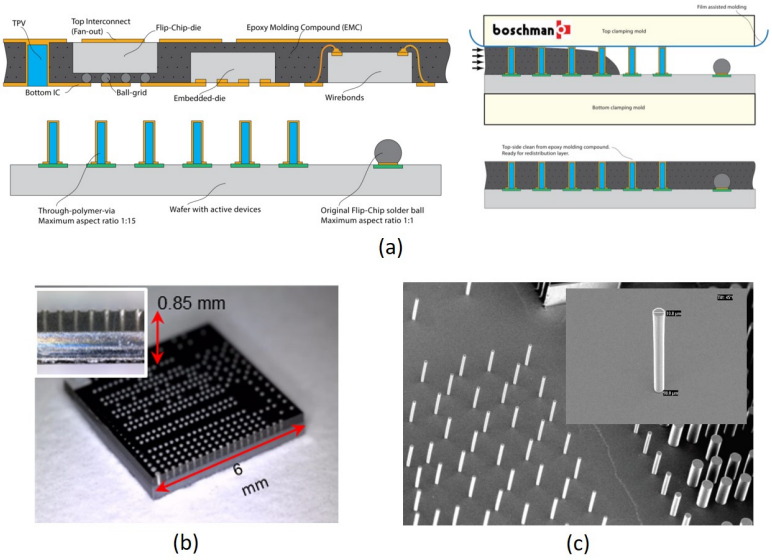


Figure 1.9: A graphic introduction of TPV technology (a) The schematic illustration of TPV application in through package vertical interconnection and the film assisted molding process. (b) A molded package demonstrating high density TPVs . (c) The SEM image of high-aspect-ratio TPVs. Figures adapted from [36].

Similar to TCP and VWB technologies, TPV is also a bottom-up via forming method

without process-induced damage. One of the Key features of TPV technology is that it employs film assisted molding to keep the top surface of the pillar clean from EMC. Due to the elastic nature of the polymer pillar, it can be slightly compressed during the film assisted molding where the head of the TPVs can dent into the top film without damaging the pillars. In such a way, the top side of the TPV is protected by the film. This results in clean pillar heads right after the molding process enabling further processing without the need for grinding. In TPV process, the polymer is structured by lithographic patterning enabling a broad range of form factors to target specific applications. Furthermore, lithographic patterning is very scalable to high-volume manufacturing.

Unlike TSV, TMV, TCP, and VWB technologies, TPV forms a "composite" via other than the pure metal. The "P" means a polymer which is an important element of the TPV technology. TPV utilizes a polymer "skeleton" to achieve high-aspect-ratio, high density, and a large range of dimensions and an optional coating layer to enable the conductivity or other physical functions. The polymer used can reach thickness up to millimeters and is optically transparent. Combining the polymer core with a functional coating can yield many advantages, including improved mechanical strength, fast speed of functional coating, dimension depends on the polymer material, and flexible to the choices of substrate materials.

Polymer materials which can form high-aspect-ratio pillars are required for the TPV process. A very promising material is SU-8, an epoxy-based negative photoresist. SU-8 can form HAR structures and is widely used in the MEMS application for its excellent mechanical properties. The epoxy-based nature makes SU-8 a mechanically and thermally very stable material after fully cross-linked which makes it ideal for being used as the polymer "skeleton" in TPV technology.

## 1.4. OUTLINE OF THE THESIS

### 1.4.1. SCOPE OF THE RESEARCH

The microelectronics industry is moving towards three-dimensional (3D) integration of multiple heterogeneous devices to meet the need for increased functionalities (More-than-Moore), miniaturization, cost reduction, and better performance. The increasing complexity of multi-functional applications requires novel and robust approaches for achieving high-density vertical-interconnections (vias) to connect multiple devices and systems in an out-of-plane direction. The advantages that vertical interconnects can offer for 3D integration are shorter electric length, lower power consumption, lower signal loss, faster communication speed, smaller form factor, thinner package, higher I/O density, and lower parasitic effects. Through-Polymer Via (TPV) technology is unique in its broad range of potential applications. Since a TPV structure is based on polymers which are optically transparent and mechanically strong and stable, its application is not only limited in electrical vertical interconnections but also suitable for applications in optical, microfluidic, thermal and mechanical domains. TPV technology has the potential of becoming a key technology for heterogeneous 3D integration.

This research work focuses on developing low-cost, large-scale, and parallel fabrication process of Through-Polymer Vias (TPVs). Multiple applications carriers are defined which demands different functionalities of TPVs, including electrical, optical, and

mechanical functions. For each application, the fabrication process and the challenges differ. A general process guideline for TPV manufacturing based on wafer-level fabrication using cleanroom facilities is obtained from this research. Four special process cases with different materials and techniques are developed. The characterization of the mechanical strength of the metalized TPVs is carried out. And in the end, a 122 GHz radar system-in-package with on package antenna array is developed and tested to demonstrate the application of the TPVs.

### 1.4.2. THESIS OUTLINE

The outline of this thesis is given below,

Chapter 2 comprises the first part of this thesis. It presents the process guidelines of fabricating through-polymer vias. This chapter starts with introducing SU-8 as the structural material used in TPV fabrication and the lithography process. Other materials, such as SUEX, will also be introduced and the process-related differences of the materials will be highlighted. In addition, this chapter also shows how the fabrication process is optimized to be cleanroom compatible.

Chapter 3 discusses the 4 process cases of TPV technology developed with 4 different application carriers, namely, antenna-in-package (AiP) for mm-wave radar, optical encoder system-in-package, PCB display panel, 1 x 1 mm QFN package with exposed die area. The mask design, process flow, and fabrication results are explained as well as the challenges for each process flow.

Chapter 4 presents the mechanical characterization of TPVs. Shear tests on uncoated and metalized TPVs were carried out to characterize the mechanical strength of TPVs when under lateral forces. The influence of different metal coating thicknesses, different pillar diameters, different shear heights to the mechanical strength of the pillars is discussed. The shear process of uncoated TPVs in a 3D FEM model is simulated and geometrical features are analyzed to explain the measured shear response results.

Chapter 5 focuses on the application of TPVs in a 122 GHz radar system in package (SiP) and presents corresponding RF simulation and functional test results. A radar SiP that contains a commercial TRX system on chip (SoC) with its antenna array integrated on top of the epoxy molding compound (EMC) surface of an 8 x 8 mm QFN realized by TPV technology is designed, modeled, manufactured and tested.

Chapter 6 summaries the results of this research work about Through-polymer Via technology and gives recommendations for future research activities to bring Through-polymer Via technology to commercial products.

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# 2

# THROUGH-POLYMER VIA (TPV) PROCESS GUIDELINES

*Conventional SU-8 polymer process guidelines are not well optimized for the TPV processes. To develop a scalable TPV fabrication flow, it should be compatible with a cleanroom environment. In this work, a TPV process guideline is generated based on cleanroom process flowcharts. In this chapter, the process details and the obtained know-how from coating SU-8 towards the final molding process are discussed.*

## 2.1. INTRODUCTION

Cleanroom processes enable high-volume production of microelectronic devices. Hence, the development of a cleanroom-compatible TPV process is key for potential cost-effective high-volume manufacturing. Like in many cleanroom processes, also in TPV fabrication, photolithography plays an important role. In conventional photolithography, the use of photo-resist (PR) is temporary as a masking layer for material processing such as etching. The thickness of PRs used in such processes is usually in the range of several micrometers. However, the TPV process requires the permanent use of thick PR layers above 100 µm. The knowledge and know-how based on the conventional cleanroom process (CMOS and MEMS) are not completely transferable to the TPV process. Modifications and new techniques are required to improve the process quality and efficiency. Also, because of the permanent nature of SU-8, protecting the equipment from SU-8 contamination is required. The process details and the obtained know-how of the cleanroom compatible TPV process are discussed in this chapter.

## 2.2. POLYMER MATERIALS

The polymer material used in TPV is SU-8 negative photoresist [1, 2]. SU-8 is an epoxy-based negative photoresist that has broad applications in the LIGA process [3–5], MEMS [6–10] and microfluidics [11–13]. It has stable mechanical and thermal properties and was usually applied for permanent purposes.

The SU-8 monomer, also known as EPON SU-8 resin, is a novolac resin which contains 8 epoxy groups and was firstly developed by Shell Chemicals. The EPON SU-8 resin can reach a very high degree of crosslinking which leads to beneficial properties such as excellent thermal stability, chemical resistance, and mechanical strength. Based on the EPON SU-8 resin, the first SU-8 negative photoresist compositions were developed and patented by IBM in 1989. The SU-8 photoresist combines the advantages of the SU-8 resin and the ability of photolithography and is widely used in microfabrication as a structural material, such as in MEMS, microfluidic applications. The chemical formulation of the EPON SU-8 resin monomer is shown in Figure 2.1 (a). Several commercially available polymer materials are suitable for the application in TPV technology. These include the SU-8 2000 series from Kayaku Advanced Materials [14], Inc.(KAM), was known as MicroChem Corp, the HARE SQ 50 series from KemLab Inc, and the GM1075 series from Gersteltec Sarl. Also, a dry film resist of SU-8, also known as SUEX, is available at DJ MicroLaminates, Inc [15]. Although these products might use different additives and solvent, they are all based on the same SU-8 epoxy.

The SU-8 negative photoresist is a mixture of EPON SU-8 resin, a photoinitiator, organic solvent, and other additives. Triarylsulfonium hexafluoroantimonate salt is usually used as the photoinitiator for SU-8 which can absorb UV radiation and generate a low concentration of a strong acid. The generated $H^+$ triggers the crosslinking of the SU-8 epoxy group and its crosslinking reaction is further amplified by applying heat. The epoxide rings are opened by the $H^+$ from the acid and new carbon-oxygen bonds are formed between the epoxy groups. The chemical formulation of triarylsulfonium hexafluoroanimonate salt is shown in Figure 2.1 (b) and the procedure of acid generation and crosslinking reaction are shown in Figure 2.2. To enable spin coat processing, the

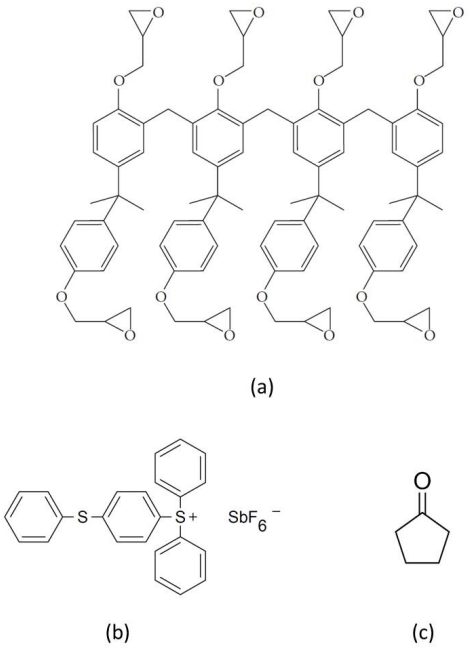


Figure 2.1: The chemical formulations of the compositions in SU-8 negative photoresist. (a) The chemical formulation of EPON SU-8 resin monomer, showing 8 epoxy groups at the ends of the polymeric chains, (b) the chemical formulation of triarylsulfonium hexafluoroantimonate salt, the photoinitiator, (c) the chemical formulation of cyclopentanone, the solvent used in SU-8 2000 series from Kayaku Advanced Materials, Inc.

EPON SU-8 resin is dissolved in an organic solvent such as propylene glycol methyl ether acetate (PGMEA), cyclopentanone, or gamma-butyrolactone (GBL).

The EPON SU-8 resin has a low molecular weight of around 7000 ±1000 Da that leads to high solubility and fine feature resolution. Because of the high solubility, the mixture of solvent and the solids can reach very high viscosity. For example, the viscosity of SU-8 2075 is around 22000 cSt with 73.5% solids which results in a film thickness up to 500 µm with a single spin coating process. And as for the SU-8 TF 6000 series, the film thickness can reach a lowest of 400 nm and can be exposed with nanometer resolution features.

The triarylsulfonium hexafluoroantimonate salt has low absorption of UV light above a wavelength of 360 nm. However, the absorption of shorter wavelength UV light increases and peaks at around 300 nm. The low UV absorption of the SU-8 photoresist above 360 nm wavelength enables the exposure of very thick films up to mm range to form high-aspect-ratio (HAR) structures. However the high absorption of shorter wavelength (below 360 nm) UV light induces a non-uniform photoacid generation along the thickness direction of the film. The shallow surface region of the SU-8 photoresist film then absorbs most of the short wavelength UV light and generates a higher concentration of photoacid. The higher concentration of acid can diffuse and triggers a larger area of crosslinking than the design intended and this translates to the “mushroom head” or “T-topping” of the HAR SU-8 structures. Thus for applications that prefer a well-

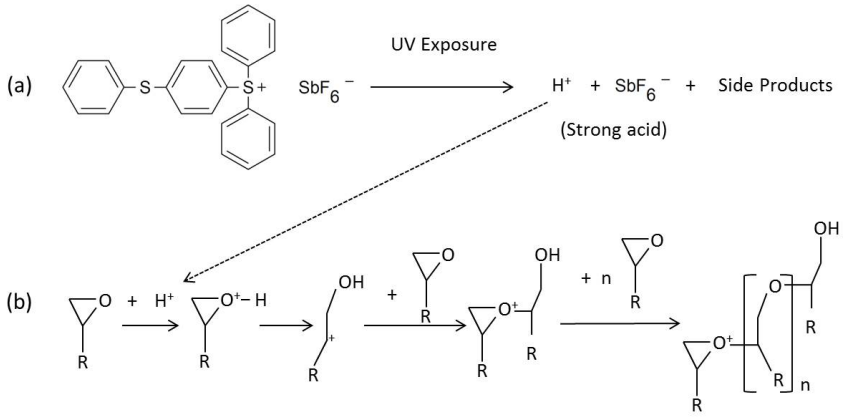


Figure 2.2: The procedure of the crosslinking reaction of the SU-8 epoxy groups. (a) The acid generation reaction during UV exposure. (b) The crosslinking reaction trigger by the acid during the post exposure baking process.

controlled vertical sidewall profile of the HAR SU-8 structures, such as the applications in MEMS and microfluidics, a high-pass optical filter is recommended to filter out the shorter wavelength below 360 nm. Hence, the possibility of thick film coating and the excellent transparency for UV light above 360nm wavelength makes SU-8 suitable for constructing HAR structures with fine feature sizes.

Due to the large proportion of aromatic functional groups and the high density of epoxy groups, fully cross-linked SU-8 has high thermal stability (Tg>200 °C), excellent mechanical strength and high resistance to chemicals which can withstand nitric acid, acetone, NaOH at 90 °C and, to some extends, oxygen plasma.

The Young's modulus of SU-8 is in the range of 4.02 to 4.95 GPa, and the Poisson ratio of SU-8 is 0.22. Compared to aluminum and copper which has young's modulus of 69 GPa and 117 GPa respectively, SU-8 is softer and more flexible. SU-8 has a thermal expansion coefficient (CTE ) of around $52\times10^{-6}$/K and thermal conductivity of 0.2 W/mK. As for substrate materials, silicon has a CTE around $2.6\times10^{-6}$/K at room temperature, and PCB material, such as FR-4 laminate, has a CTE near $14\times10^{-6}$/K. The thermal expansion mismatch between the SU-8 polymer and the substrate can cause high internal stress which can lead to delamination or cracking of the SU-8 structures. Thus, during the lithography process of SU-8, sudden heating or cooling should be avoided. The physical properties of SU-8 are summarized in Table 2.1.

## 2.3. LITHOGRAPHIC PROCESS OF THICK SU-8

Although X-ray lithography has shown better results in fabricating HAR SU-8 structures [5, 16], the cost and scalability of X-ray lithography can not compare with UV lithography. As for the TPV application, UV lithography is preferred for its lower cost and compatibility with conventional technologies. Other lithographic techniques such as hologram exposure [17, 18], drawing lithography [19], tilted exposure [20, 21], focused ion beam

Table 2.1: The physical properties of SU-8 [13]

| Material properties of SU-8 | |
|---|---|
| Appearance | Pale yellow to clear |
| Odor | Faint to mild |
| Young's modulus | 4.02–4.95 GPa |
| Poisson ratio | 0.22 |
| Friction coefficient | 0.19 |
| Glass temperature (Tg) | 50°C–55°C, uncross-linked; >200°C, cross-linked |
| Degradation temperature (Td) | appr.380°C |
| Boiling point | 204°C |
| Flash point | 100°C |
| Autoignition temperature | 455°C |
| CTE | $52 \times 10^{-6}$/K |
| Thermal conductivity | 0.2 W/(m·K) |
| Specific heat | 1500 J/(kg·K) |
| Vapor pressure | 0.3 mmHg at 20°C |
| Density (of EPON SU-8 resin) | 1200 kg/m3 |
| Refractive index | 1.668, uncross-linked; 1.67–1.8, cross-linked |
| Dielectric constant | 4–4.5 $\epsilon_0$ |
| Electrical breakdown fields | appr.$10^7$ V/m |
| Resistivity | >$10^8 \Omega \cdot cm$ |

lithography [22] and backside exposure[23] have demonstrated the large process flexibility of SU-8 which the TPV technology can benefit from [24]. Other methods to fabricate SU-8 micropillars without lithography are also explored, such as Sonication[25]. However, sonication can only produce SU-8 pillars in a solution. In this research, we focus on a low cost and scalable standard UV lithography method.

Since the SU-8 thickness used in the TPV process is larger than 100 µm, the lithographical process will be explained based on the process of thick film SU-8 in this section. To introduce the process steps in a more general sense, a silicon wafer, the most common substrate used in semiconductor manufacture, will be used as the substrate. Although automatic equipment can be used for the process, the manual process steps are explained here to reveal the details and concerns.

The main lithographic process of SU-8 negative photoresist consists of the following steps: Substrate cleaning and drying, SU-8 coating, soft bake (SB), exposure, post-exposure bake (PEB), development and hard bake (HB). Regarding the coating, there are two main approaches to coat a thick film of SU-8 onto a substrate, spin coating, and dry

film lamination. The main process flow is shown in Figure 2.3.

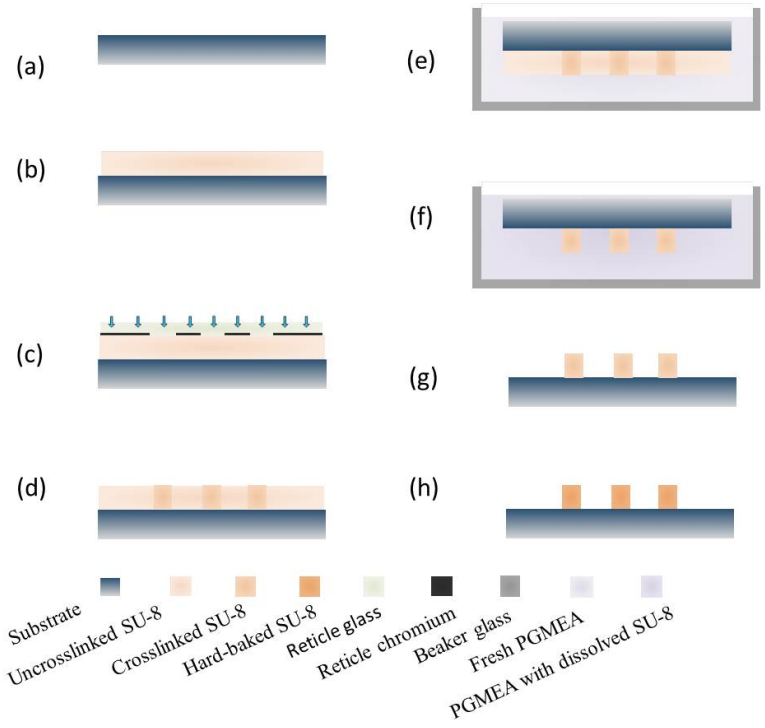


Figure 2.3: The illustration of the lithographical process flow of SU-8. (a) A clean substrate such as a silicon wafer, (b) the coating of a thick layer of SU-8, (c) the exposure of SU-8, (d) the post-exposure-baking, (e) immersing the substrate facing down into fresh PGMEA, (f) developed SU-8, (g) cleaning and drying the substrate, (h) hard baking of SU-8.

### 2.3.1. SPIN COATING OF LIQUID SU-8

Normally, a spin coating process consists of 4 steps, placing the substrate, resist dispensing, spreading, and thinning down to target thickness. If the spin coating process generates an excessive edge bead, then an edge bead removal (EBR) step can be added. Due to the high viscosity and low spin speed, thick SU-8 coating is very sensitive to non-uniform centrifugal force. When placing the wafer to the spin chuck, the operator should pay more attention to the centering of the wafer to the vacuum chuck. A poorly centered wafer can cause non-uniformity in the film thickness and even partial coverage of the wafer. Centering the dispensing of SU-8 to the Si wafer is also critical to the film coverage and uniformity. The dispensed SU-8 puddle should be in a uniform circular shape and centered on the wafer. Spreading is a low speed spinning step to spread the dispensed SU-8 puddle to cover the entire Si wafer. And to reach the desired uniform thickness, a higher speed spinning is performed after spreading. For a good spin coating result, the wettability of the SU-8 liquid is important, and the introduction of cyclopentanone to

replace GBL has significantly improved the spin coating quality [26].

The edge bead built up after the spinning of thick SU-8 film can cause an excessive non-uniformity of film thickness. During the soft bake step, the edge bead reflows and expands halfway to the center of the wafer. A significant variation of film thickness can also influence the exposure results by introducing air gaps between the mask and SU-8 film. Hence, the EBR of thick SU-8 film is highly preferred. However, unlike a thin film spin coating, a thick film of SU-8 at the end of the spinning process is still wet and flowable which complicates the EBR step. A conventional EBR step at the end of the spinning using a short-time fast acceleration spin applied for thin-film resist is not desired here for thick SU-8. For thick films, such as 100 to 300 µm, the end acceleration can change significantly the film thickness and uniformity. EBR with a chemical solvent, such as acetone, is also not suitable when SU-8 is still wet.

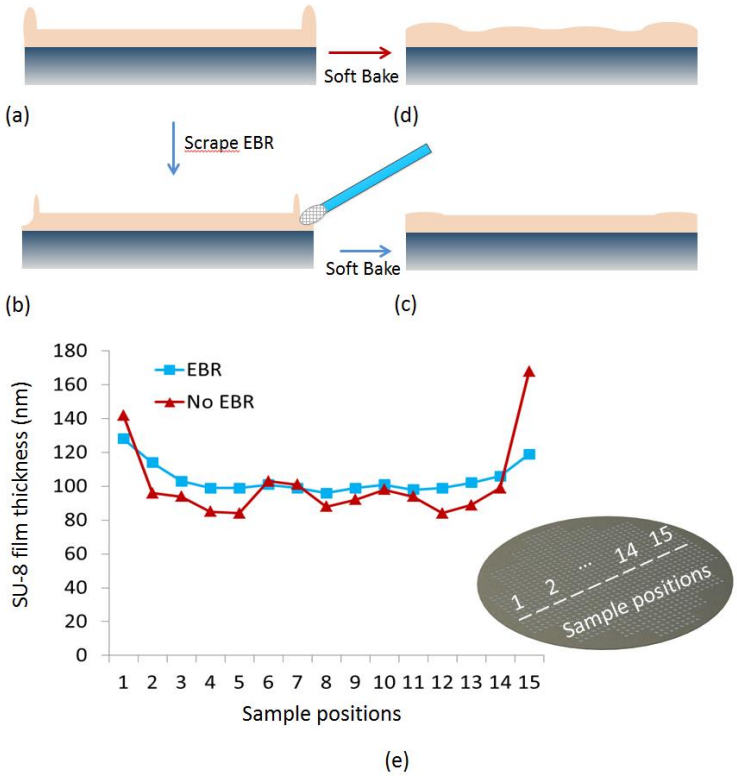


Figure 2.4: The comparison of film thickness uniformity with and without scrape EBR of the 100 µm thick spin coating recipe on silicon wafers. (a) The edge bead builds up after the spin coating, (b) the process of scrape EBR, (c) soft-baking after scrape EBR, (d) soft-baking without EBR. (e) The measured film thickness with and without scrape EBR. The pitch between the sample positions is 6 mm and the diameter of the wafer is 100 mm.

Performing the EBR after soft baking with a stream of acetone applied to the edge of the wafer is one of the options. However, because of the non-uniformity of thickness introduced by reflow during the soft baking, the improvement of such EBR is limited.

Also, the rapid cooling of the wafer caused by the evaporation of acetone can increase the internal stress of the SU-8 film. Therefore, in this work, a physical scrape EBR process is developed to provide a solution for improving the film thickness uniformity of spin-coated thick SU-8. The schematic illustration of the scrape EBR method is shown in Figure 2.4. As the word "scrape" suggested, the EBR process is carried out by bringing a cleanroom cotton stick with a tiny tip to contact with the edge bead with the wafer spinning at a very low speed, such as 10 rpm. The cotton stick takes away an amount of SU-8 from the edge bead and creates a buffering space for the remaining edge bead to reflow and expand. In such a way, the influence of edge bead to the uniformity of film thickness during soft baking can be largely reduced.

The SU-8 film thickness was measured across a 100mm silicon wafer using Dektak 8 stylus profiler. The standard deviation of the thickness in the area from sampling point number 3 to number 13, excluding the very edge areas, is reduced from 7 µm to 2 µm after applying the scrape EBR method. A thickness uniformity improvement of nearly 3.5 times is achieved. This method can be further improved by developing an engineered scrape tip shape for minimizing the formation of the secondary edge bead in combination with an automated system to perform the scraping which provides more accurate positioning of the scraping tip. Typical spin coating recipes for thick SU-8 (SU-8 2075 from KAM) including the scrape EBR process parameters are summarized in table 2.2.

Table 2.2: Typical SU-8 spin coating receipes for SU-8 2075 series

| | Spreading | | | Thin down | | | Scrape EBR | | |
|---|---|---|---|---|---|---|---|---|---|
| Film thickness | Accel. (rpm/s) | Tgt. (rpm) | t(s) | Accel. (rpm/s) | Tgt. (rpm) | t(s) | Accel. (rpm/s) | Tgt. (rpm) | t(s) |
| 100 µm | 100 | 300 | 60 | 300 | 1600 | 60 | 300 | 10 | 300 |
| 200 µm | 100 | 300 | 30 | 300 | 1000 | 30 | 300 | 10 | 300 |
| 300 µm | 100 | 300 | 30 | 300 | 700 | 45 | 300 | 10 | 300 |

After the spin coating, a soft baking step is performed to evaporate the remaining solvent and further solidify the SU-8 film. For the soft baking of thick SU-8, it is recommended to use a leveled hotplate instead of a convection oven. By using a hotplate, the heat flux is applied from the bottom surface of the film. In such a way, the solvent escapes the film easily from the top surface. In a convection oven, the heat is applied also to the top side of the film which creates a skin layer on the surface and traps the solvent inside. Leveling of the hotplate is of great importance for the soft baking of the thick SU-8 film. The tilt of the hotplate surface will induce significant non-uniformity of film thickness due to the gravity of the reflowing SU-8.

### 2.3.2. LAMINATION OF DRY FILM SU-8

Dry film lamination is another approach to coat a thick layer of SU-8 [5, 9, 15, 16, 27]. SUEX, the dry film version of SU-8 is commercially available at DJ Microlaminates. The SUEX dry film is a brittle material at 20 °C and is easy to crack. It becomes soft and bendable at a temperature of around 40 °C. The lamination can be performed with common hot roll laminators with control of roller speed and the laminate temperature. It

is recommended to use 1 ft/min speed and 50-75 °C. However, the hot roll lamination is suitable for thickness below 250 µm. For thicker layers, the SUEX film suffers from the movement on the substrate and special mold is required. Furthermore, when small patches of SUEX are used in a hot roll laminator, the movement of the roller will displace the patch with respect to the substrate.

Therefore, in this work, a vacuum hot press laminator, the MT-101 laminator from M-Triangel, is used instead of a hot roll laminator. The operating principles of both the hot roll laminator and the vacuum hot press laminator are briefly shown in Figure 2.5 (a) and (b) respectively.

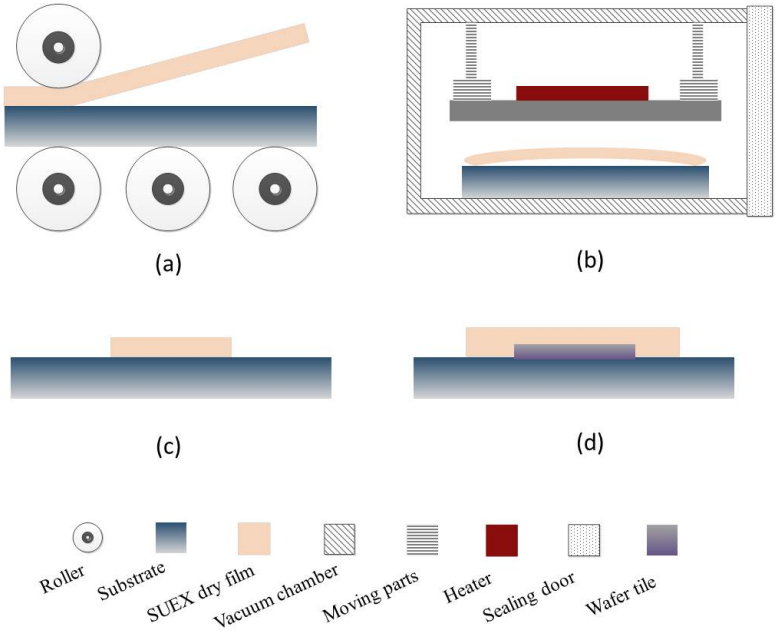


Figure 2.5: Comparison of hot roll lamination and vacuum press lamination. (a) The hot roll lamination mechanism, (b) the vacuum hot press lamination mechanism, (c) small patch lamination of SUEX dry film, (d) small patch lamination of SUEX dry film over the wafer tile and onto the substrate.

The application of smaller patches of SUEX on top of the target wafer tile avoids spin coating and enables more economical use of SU-8 material. In a high volume manufacturing environment, SUEX patches could be handled using pick&place tools. In Figure 2.5 (c) and (d), the situations of lamination of small patch SUEX dry film on a wafer and over a wafer tile onto a carrier wafer are shown, which are not suitable for a hot roll laminator. The vacuum hot press laminator is composed of a vacuum chamber, a top press plate, an embedded heater on top of the press plate, and mechanical moving parts. The combination of the SUEX dry film and the substrate is placed underneath the press plate. The lamination process consists of 4 steps, loading of materials, pumping down, press down, and holding. It is recommended to bend the SUEX dry film slightly on the corners so that it will be free-standing and not trapping air before the vacuum is applied. The

lamination is performed at 60 °C with a press holding time of 120 s. A post lamination bake at 85 °C for 3 min on a hotplate is carried out to improve the surface smoothness and adhesion.



### 2.3.3. EXPOSURE

For either the spin-coated SU-8 or the laminated SUEX, after the soft bake or the post lamination bake, the film is then ready to be patterned by UV exposure. There is a broad range of wavelengths of the light source that can be used to expose SU-8, from X-ray, extreme UV, deep UV to near UV. In this work, an i-line (350 to 500nm) mask aligner, EVG 420, is used for the exposure of SU-8.

A photo-mask with the designed images is brought in contact with the SU-8 film. The UV photons trigger the photoinitiator, triarylsulfonium hexafluoroantimonate salt, to generate a low concentration strong acid below the transparent area of the mask. And the acid works as a catalyst for the cross-linking chemical reaction and amplifies the cross-linking of the epoxy groups on the SU-8 monomer during the PEB step. The cross-linked SU-8 becomes insoluble in the developer PGMEA.

### 2.3.4. POST EXPOSURE BAKING

The cross-linking of SU-8 happens at the post-exposure bake (PEB) when the acid-induced cross-linking reaction is amplified by thermal energy. PEB has been proven to be a critical process step which has a significant influence on the results of the SU-8 aspect ratio and adhesion [28]. Both hotplate or convection oven can be used for the PEB process. According to the data-sheet of the SU-8 2000 series, the SU-8 film is suggested to be baked at 65 °C and 95 °C subsequently, and afterward with a slow cooling procedure to room temperature to reduce the internal stress. Since the uncross-linked SU-8 becomes soft and has larger thermal expansion at the baking temperatures compared to the cross-linked SU-8, the transferred image from the photo-mask will appear on the surface of the film in a few seconds after the substrate is heated.

### 2.3.5. DEVELOPMENT

For the development of SU-8, PGMEA is used as the developer. PGMEA works as the solvent of unexposed SU-8. The SU-8 solution is heavier than PGMEA and sinks to the bottom. Hence, when the substrate is developed with SU-8 film facing up, the dissolved SU-8 will remain at the surface of the substrate and reduce further dissolving of the unexposed SU-8. Thus, it is recommended to develop the substrate with the SU-8 film facing down to enable fresh solvent to reach the solvent-resist interface. Mild agitation, such as a magnetic rotor with a spin speed of 150 rpm, can be used to accelerate the development process. In the case of 100 µm thick SU-8 on a 4-inch wafer, the 1-liter fresh PGMEA developer shows a severe degradation after the 3rd wafer is developed. The development time used is 20 min.

Isopropyl alcohol ( IPA) can be used to rinse and clean the substrate after development. Water rinsing should be avoided because the residue of PGMEA on the substrate still contains the dissolved uncross-linked SU-8 which will produce a large amount of white residue when contacting with water. The white residue is difficult to remove and can contaminate the substrate. Quick immersion in acetone (e.g.10s) and then imme-

diately back to IPA can help further remove the residue. For drying the substrate, a low-temperature baking at 50 °C is recommended. In case that some residues can not be cleaned completely with solvents, an oxygen plasma flash at room temperature, with 250 cc $O_2$ flow, at 600 W, and for 1 min, can be applied to further clean the substrate.



### 2.3.6. HARD BAKING

Hard bake is performed after the development to further evaporate the absorbed solvent inside the SU-8 patterns and further cross-link the epoxy groups. Compared with the temperature of soft bake and post-exposure bake, the hard bake temperature is in the range from 120 °C to 300 °C. With higher hard bake temperature and longer bake time, the degree of crosslinking of SU-8 epoxies keeps increasing which results in an increasing Tg. A fully cross-linked SU-8 is reported to have Tg > 200 °C.

A vacuum oven is recommended for the hard bake, as the vacuum can enhance further degassing of the material. Especially in the application when there is a metalization step afterward, a thorough degas step is important to ensure the optimal quality of the deposited metal film and to avoid contamination of the equipment.

During the development and cleaning process, micro-cracks can be formed on the SU-8 structures due to internal stress. The internal stress was caused by the significant temperature drop due to the evaporation of the solvent, such as IPA or acetone. A relatively fast ramping during hard bake can soften the SU-8 structures to a certain degree and heal the cracks. Overnight slow cooling inside the vacuum is recommended to minimize the internal stress built up in the hard-baked SU-8. To ensure the thermal and mechanical stability, the SU-8 structures are recommended to be hard-baked at a temperature which is 10 to 20°C higher than the highest temperature they may encounter during further processing or as a final product.

## 2.4. METALLIZATION

In applications where the TPVs need to conduct electrical currents, a thin metal film can be coated uniformly over the SU-8 pillars by sputtering. The sputtering metalization process consists of 3 main steps.

The first step is to perform the SU-8 outgassing test. The outgassing test is performed with the process wafer loaded inside the deposition chamber, with the chamber temperature set at the process temperature and pumped down to the required vacuum level. The chamber vacuum level is measured after closing all valves and pumps for a given period of time. The rising of the chamber vacuum level indicates the outgassing of the wafer. If the vacuum level is below a certain value after a given delay time, the outgassing of the wafer is considered not critical and it is allowed to continue the process. The outgassing test is performed to ensure a good quality of metal deposition and avoid the contamination of the sputtering chamber.

The second step is to perform an in situ RF etching step to remove the native oxide on the contact pads. This process ensures a low contact resistance between the contact pad and the metalized TPVs.

The third step is the metal deposition. During the deposition, heat can be transferred to the wafer by the sputtered metal atoms. And without cooling, the SU-8 polymer can

be thermally damaged. Thus the metalization of SU-8 is carried out at 25 °C with integrated active cooling in the wafer holder. In addition, extra cooling steps in-between the depositions are implemented.



## 2.5. FILM ASSISTED MOLDING

After the TPV fabrication process, the substrate will be encapsulated by EMC using film assisted molding (FAM) technology. The conventional transfer molding process has disadvantages including EMC bleed and resin flash, time-consuming mold cleaning, mold wearing, package deformation during the ejection process, and lead frame deformation or substrate cracking due to clamping. To overcome these disadvantages, thin-film assisted molding was developed. The FAM technology started more than 15 years ago and has become a widely used advanced encapsulation technology in the semiconductor industry [7, 29–31]. Compared to conventional transfer molding, FAM has advantages such as mold protection, clean release, reduced clamping force, and high efficiency.

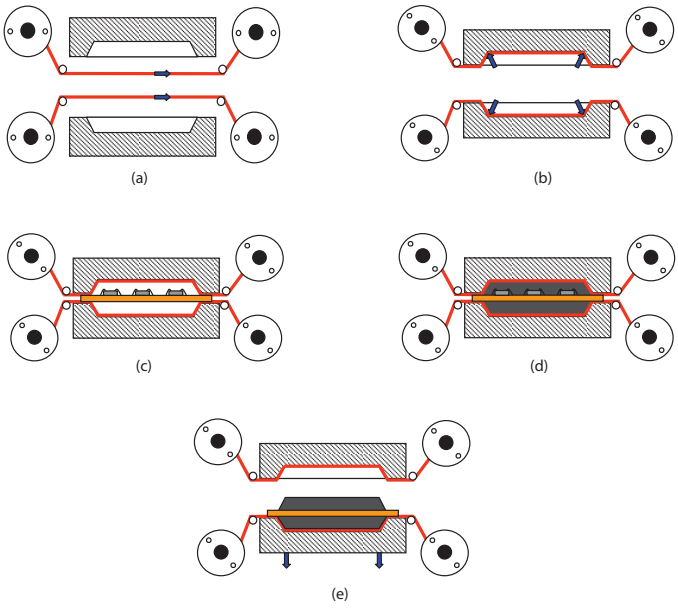


Figure 2.6: The main steps of FAM process. (a) Intake the fresh film, (b) move the mold to the film position and suck film to the mold inner surfaces by vacuum, (c) load substrates and close mold, (d) fill mold cavity by transferring epoxy molding compound, (e) open mold and unload the molded substrate. Figure adapted from [7].

The FAM process uses thin Teflon films to cover the mold parts. These Teflon films can withstand high temperatures up to 200 °C and not only protects the mold parts from wearing but also contributes to the process of releasing the substrate after molding. The main steps of FAM process are shown in Figure 2.6. Firstly, the films are refreshed in the working area and followed by applying the vacuum to fix the films to the inner surface of the mold. The substrate is then loaded and the molds are closed. The next step is to fill in

the epoxy molding compound (EMC) by transfer molding and finally, the EMC is cured and the substrate is released. The film can be refreshed again and the next molding cycle can start.

Furthermore, in the TPV process, the combination with FAM process is beneficial. By contacting and compressing the TPVs with the film, the top surfaces of TPVs are protected and kept clean. No extra step, such as grinding back, is needed for exposing the top of the TPVs.



## 2.6. CONCLUSIONS

The adaption of the TPV process to a cleanroom level manufacturing is essential to evaluate its scalability. Thick SU-8 material is considered as non-standard in the cleanroom and needs to be carefully handled to avoid contamination of equipment. A general cleanroom level guideline of the thick-SU-8 process is developed in the Else Kooi Lab (EKL) for TPV technology, which includes spin coating, lamination, soft baking, exposure, post-exposure baking, development, hard baking, and metallization.

To obtain a uniform thick SU-8 (> 100 µm) coating, the scrape EBR process is developed. The uniformity of a 100 µm thick SU-8 coating is improved from a variation of 7µm to 2 µm. Scrape EBR is suitable for improving the uniformity of spin-coated thick and wet polymer layer. Furthermore, to avoid delamination of SU-8 due to thermally induced stress, the post-development cleaning and drying process is modified. Due to CTE mismatch, the stress builds up in the SU-8 structure can eventually cause delamination and cracking. In the TPV process, hotplate drying is advantageous over spin-drying and natural convection drying.

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# 3

# VERSATILITY OF THROUGH-POLYMER VIA (TPV)

*In this chapter, multiple applications and process varieties of Through-Polymer Via (TPV) technology are discussed. TPV technology provides the possibility of creating a vertical via through an encapsulated package that conducts not only electrical signals but also optical and mass signals. The nature of TPV which uses the photo-sensitive optically transparent polymer as the building block and the combination of a functional coating layer has made this technology very flexible in packaging design and suitable for a broad range of electronic packaging applications.*

## 3.1. INTRODUCTION

Through-polymer Via technology (TPV) provides a fundamental bottom-up approach of making vertical structures through microelectronic packages. TPV structures are lithographically patterned and can take arbitrary shape and multi-scale dimension from millimeters to micrometers. The polymer structures not only provide mechanical support but also can be used as optical window thanks to the transparency of the polymer. And with a metal coating, these structures then function as electrical interconnections. Therefore, TPV has potentially a broad application range. In this chapter, the development of four different microelectronic packages using TPVs and their applications is explained in details.



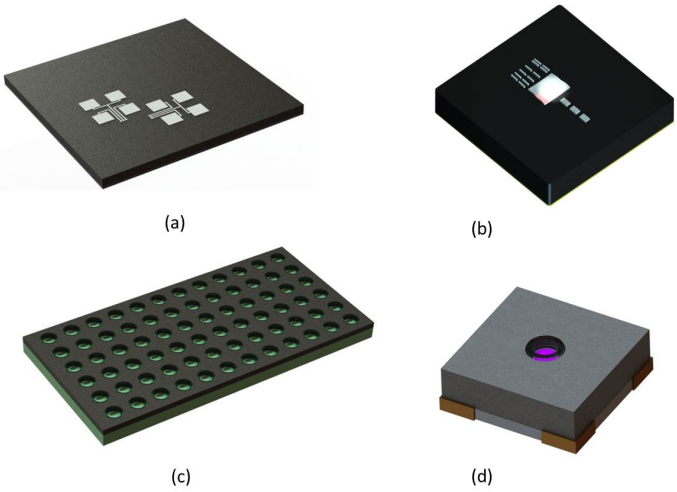



Figure 3.1: 3D models of the 4 different packages using TPVs. (a) Radar system-in-package using metalized TPVs, (b) optical encoder system-in-package using optical TPVs as micro-windows, (c) molded PCB display panel with TPV through holes for LED integration, (d) miniaturized 1x1mm QFN package with a micro TPV through-hole. The schematic shown is not to scale.

The first package developed is a radar antenna-in-package (AiP) working at 122 GHz with its antenna array integrated on top of the package, shown in Figure 3.1 (a). Here, metalized TPVs are functioning as the interconnection between the radar IC and its antennas. The second package shown in figure 3.1 (b) is an optical encoder system-in-package with segregated micro-windows for each optical sensing area. These SiPs are widely used for motion control and angle detection. The micro-windows are made by TPVs which function as a vertical optical waveguide passing the external light signal to the embedded chip. The third package shown in figure 3.1 (c) is a molded PCB display panel with through holes for LED integration. These TPVs are in the shape of rings keeping the PCB surface inside the ring clean from the epoxy molding compound (EMC). The fourth package as shown in figure 3.1 (d) is a miniaturized 1x1mm QFN package with a micro through-hole. The TPVs are also in the shape of rings and keep the area inside the rings clean from EMC. Each package has its specific TPV process conditions including the substrate type, the adhesion of the TPV structures, the surface topology of the

substrate, and whether spin coating or dry film lamination is required.

## 3.2. APPLICATION CARRIERS AND SPECIFIC PROCESS CASES

Four process codes, TPVM-C-QFN, TPVO-C-QFN, TPVH-N-PCB, TPVH-W-QFN are used as the reference of the fabrication process of the four different packages. Each process code is constructed by 3 parts segmented by two underscore symbols. The first part of the process code gives information on the type of TPVs fabricated in the process. To be more specific, TPVM represent metalized TPVs, TPVO represents optical TPVs and TPVH represents ring-like hollow TPVs. The second part of the process code gives information on which substrate the TPVs are fabricated. Here in the four codes, C represents chips or wafer tile, N represents none which means the TPV structures are fabricated directly on the substrate of the package, and W represents wafer. The third part of the process code gives information of the end package carrier. An overview of the features of the 4 different TPV process cases is shown in Table 3.1.



Table 3.1: Features of developed Through-Polymer Via process cases

| Process code | TPV carrier | Polymer material | Substrate material | Thickness of polymer (µm) | Dicing before molding | Metal coating | Number of TPVs per functional unit | In Figure 3.1 |
|---|---|---|---|---|---|---|---|---|
| TPVM-C-QFN | Wafer tile | SU-8 | Al | 150 | Yes | Yes | <10 | (a) |
| TPVO-C-QFN | Wafer tile | SUEX | $SiO_2$ | 350 | Yes | No | <10 | (b) |
| TPVH-N-PCB | PCB panel | SUEX | Au | 300 | No | No | >5000 | (c) |
| TPVH-W-QFN | Silicon wafer | SU-8/SUEX | Al | 100 | Yes | No | <5 | (d) |

## 3.3. TPVM-C-QFN PROCESS

The TPVM-C-QFN process is developed for the packaging of a 122 GHz radar TRX system-on-chip [1, 2]. In this application, a vertical electrical interconnection between the IC and the top surface of a QFN package is realized with metalized TPVs. In mm-wave applications, the IC-to-antenna interconnection becomes a critical part of the RF design. Due to the smaller size of the antennas at higher frequencies, the integration of the antennas within the IC package becomes much more practical. Considering the performance of the mm-wave antennas, such as higher radiation efficiency and wider bandwidth, the design of an mm-wave package with integrated antennas sees a trade-off in material properties and dimensions. To integrate antennas on the package of RF IC, TPV provides a novel approach with tremendous design freedom. The 3D schematic of the TPVM-C-QFN fabrication process is shown in Figure 3.2. The process details and

obtained know-how will be discussed in the following subsections.



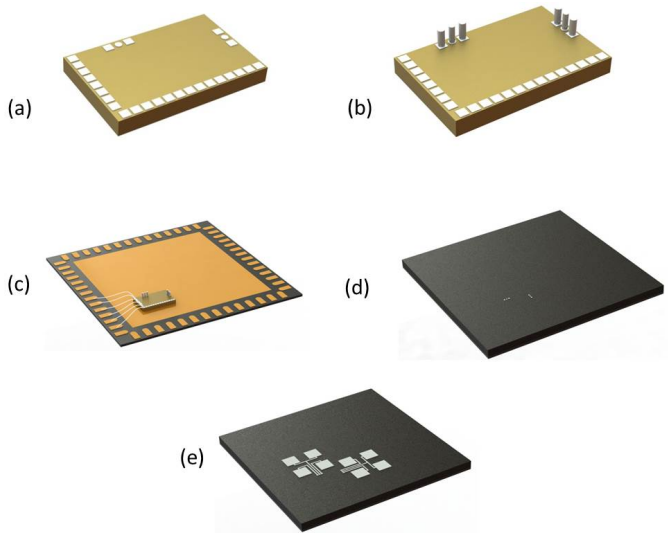



Figure 3.2: 3D schematic of the TPVM-C-QFN fabrication process. (a) 3D model of a single radar chip, (b) the radar chip with TPVs fabricated, (c) the assembly of radar chip on the QFN substrate, (d) molded QFN package, (e) QFN package with antenna array fabricated on the top. The schematic shown is not to scale.

### 3.3.1. TEMPORARY BONDING

In the TPVM-C-QFN process, wafer tiles in the dimension of 24x19mm which contains 270 radar ICs are the substrate on which the TPVs are fabricated. To make the process compatible with wafer-level handling in the lab facilities, the wafer tile was assembled onto a Si carrier wafer by using a poly(propylene carbonate) (PPC) temporary bonding layer. PPC is an amorphous, aliphatic polymer synthesized by the copolymerization of propylene oxide and carbon dioxide which has a low onset decomposition temperature between 180 °C to 240 °C [1]. The decomposition of PPC by chain scission creates a product of carbon dioxide and acetone which evaporates and leaves the substrate clean.

The carrier wafer is firstly coated with a 5 µm thick PPC layer. Before baking the PPC, the wafer tile containing radar ICs is handled by a vacuum tweezer and placed to the center of the carrier wafer manually. The assembly is then baked on a hotplate at 95 °C for 15 min to solidify the PPC layer, followed by a hard baking step in vacuum at 120 °C for 1h to further evaporation of the solvent underneath the tile which ensures good adhesion of the wafer tile to the carrier.

After the fabrication of TPVs, the wafer tile can be removed easily from the carrier wafer by heated up to 150°C and sliding off. The carrier wafer can be heated up to 200°C to clean the PPC residuals. For the processed wafer tile, acetone can be used to clean the PPC residuals.

### 3.3.2. FILM MASK DESIGN

In TPV fabrication, the feature sizes of the polymer structures are usually larger than 10 µm. Therefore, printed film masks are used. These masks are low cost compared to chromium masks and are widely used in the PCB fabrication. To attach a foil mask to a glass support plate, the four corners on the film masks are punched with through holes and are assembled by Kapton tape.

The mask for pillar fabrication is in the dark field, Figure 3.3 (a). Thus the alignment markers are designed to have a sufficient transparent window so that the alignment chips underneath the mask can be identified. The masks are aligned to the wafer tile by using the contact pad patterns of 2 chips at the corners of the wafer tile as the alignment markers. The alignment is achieved by fitting the designed black boxes to the contact pads on the two alignment chips which are shown in the zoomed-in images. The two alignment chips are located on the left-top corner and the left-bottom corner of the wafer tile. Although the dimensions are relatively larger here, the use of two alignment markers instead of one is necessary to reduce the misalignment caused by rotation and ensures the accuracy of the overall alignment. The alignment accuracy can be achieved here with the film mask is around 5 µm. The alignment mismatch can be induced because of the manual operation and the deformation of the film mask introduced by the taping method for fixing it on the glass plate. It is recommended to use an overlapping dimension of more than 5 µm to ensure that the alignment of the printed features with the underlying chip structures is within the tolerance margin.

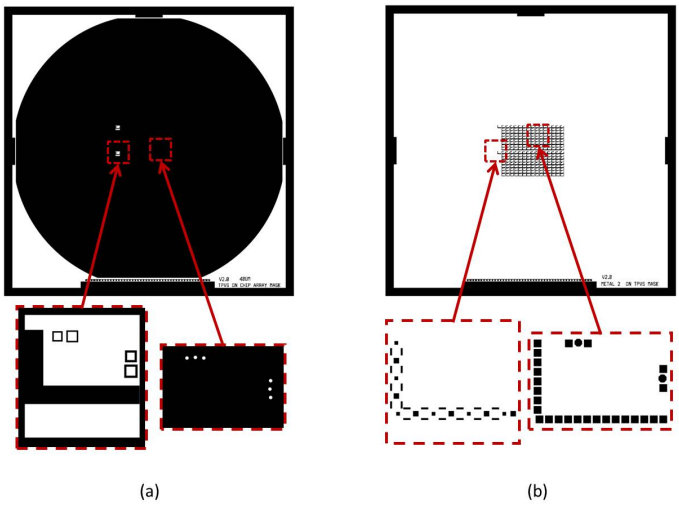



Figure 3.3: Film mask designs used in the TPVM-C-QFN process. (a) The film mask and alignment marker design for SU-8 pillar fabrication. The zoom-in image on the left shows the alignment marker design, and the zoom-in image on the right shows the pattern which defines the polymer pillars. (b) The film mask and alignment marker design used in patterning the metal coating. The zoom-in image on the left shows the alignment marker design, and the zoom-in image on the right shows the pattern on the mask which defines the contact pads.

After polymer pillar formation and metalization of TPVs, see section 3.3.3, the overall

deposited Al layer needs to be patterned. The mask used to pattern the Al layer is shown in Figure 3.3 (b). The zoomed-in images show the alignment markers and the designed Al contact pad patterns. In the mask design for pillar patterning, the alignment markers use only the RF contact pads for alignment and leave the DC contact pads on the left and bottom side of the chip covered by dark-field so that the SU-8 on that area can be cleaned after development making these DC contact pads possible to be used in the Al patterning mask as alignment markers. Patterns of lines and squares are used to fit on the borders and in the center of the contact pads.



### 3.3.3. SPIN COATING VERSUS LAMINATION

There two methods to apply a thick SU-8 film over a substrate, spin coating, and lamination. The spin coating has advantages such as better wettability and better adhesion compared to lamination. On the other hand, lamination has advantages such as better uniformity of thickness for thicker layers above 300 µm, no soft baking required, easy and time-efficient. Despite these advantages, the choice of which method to use is also depending on the substrate condition, such as material and surface roughness.

In the TPVM-C-QFN process, both methods were tested and the spin coating is chosen due to its better wettability to the substrate. The wafer tile has micro-structures on its surface, and while laminating the SUEX dry film, the air can be trapped due to the surface micro-structures and the limited wettability. The trapped air forms bubbles and affects the adhesion of the SUEX dry film. As shown in Figure 3.5, air bubbles tend to stay at the contact pads area where the TPVs needs to be made. Hence, spin coating of liquid SU-8 is recommended instead of the lamination of SUEX dry film when the substrate surface has micro roughness. A clean and bubble-free coating can be achieved by spin coating of liquid SU-8, as shown in Figure 3.5 (b).

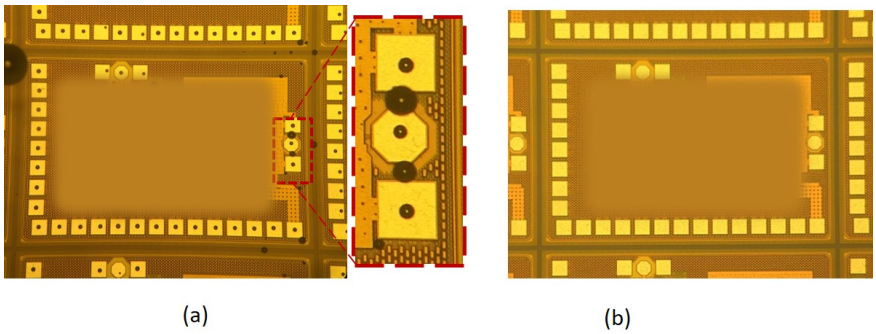



Figure 3.4: A comparison of the film quality of laminated SUEX dry film and spin coated SU-8 2075 on the radar ICs. (a) Trapped air generate micro bubbles which stay at the center of the contact pads area after SUEX lamination. (b) Air bubble free SU-8 layer applied by spin coating.

### 3.3.4. TPV FABRICATION

In Fig 3.4 (a-d), the process steps concerning TPV fabrication are concluded. The main process steps include the temporary bonding of the wafer tile, the spin coating of thick SU-8 film, the SU-8 lithography, the metallization, and patterning.

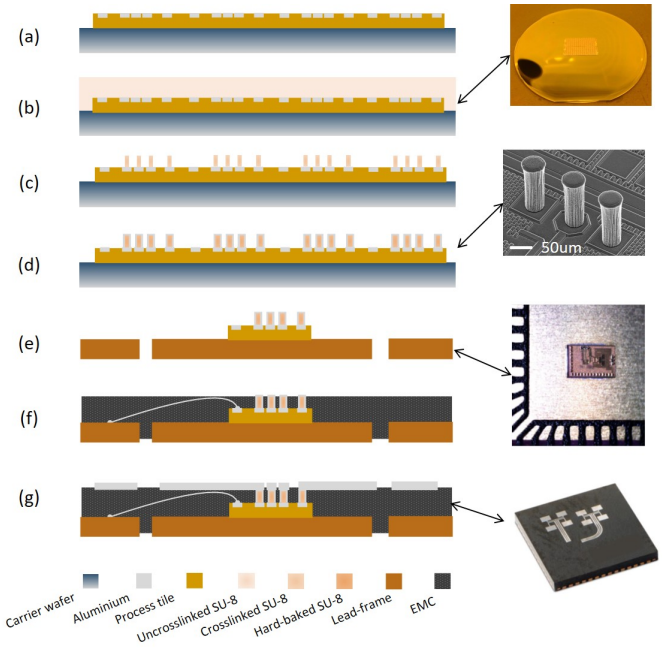



Figure 3.5: A detailed process flow of TPVM-C-QFN. (a) Temporary bonding of the wafer tile containing radar ICs onto a silicon carrier wafer, (b) spin coating of SU-8 resist, (c) lithographical steps of SU-8 to obtain high-aspect-ratio polymer pillars, (d) metallization of polymer pillars and patterning of the metal layer, (e) assembly of the singulated radar ICs onto a QFN substrate, including pick & place and wire-bonding steps, (f) film assisted molding of the QFN substrate, (g) metallization on top of the molded QFN and patterning of antenna structures. The schematic shown is not to scale. Following (g), the dicing of the QFN panel is performed to obtain individual radar SiPs.

After the temporary bonding of the wafer tile, a thick layer of SU-8 is applied by spin coating. A soft baking step is carried out to completely dry the thick SU-8 film before exposure. Next, a mask aligner system is used for broadband UV exposure. Afterward, the wafer is placed on a hotplate for the post-exposure bake (PEB). This starts cross-linking and after PEB the exposed patterns are visible in the SU-8 film. The wafer and wafer tile assembly is then immersed in a PGMEA bath with the front side facing down for development and agitation is applied by using a magnetic rotor with speed set at 150 rpm. After development, and the wet cleaning, a dry cleaning process is performed in a $O_2$ plasma cleaner to remove the remaining SU-8 residue. Afterward, the assembly is hard-baked in a vacuum oven to further crosslink and degas the SU-8 structures. After the hard bake, the wafer and wafer tile assembly can then be metalized in a sputtering equipment. A layer of Al(1%Si) is sputtered at room temperature. Other metal materials such as Cu and Ti could also be used depending on applications. Finally, the Al(1%Si) layer is patterned by lithography with spray coating resist and wet etching in a bath of phosphoric/acetic/nitric acid mixture (PES), followed by resist stripping and cleaning.

Since SU-8 is a polymer, once the deposition temperature of the metal layer is too high, it can be overly crosslinked or even pyrolysis causing size shrinkage and cracks in

the material. Thus active cooling is applied in the process to avoid overheating. The wafer stage is continuously cooled down by an embedded nitrogen flow and maintained at 20 °C. The metal layer is deposited in a multi-step sequence of deposition, 250 nm Al(1%Si) each step followed by a cooling down for 3 min. The required metal film thickness is build up in steps of deposition/cooling. Another modification to the standard metal sputter process is an increased background pressure to improve the step coverage of the metal film over the high-aspect-ratio pillars.



After the deposition of Al(1%Si) film, lithographic patterning and etching are required for the formation of contact pads. For the resist coating, spray coating is selected because it enables a conformal coating of resist over the surface with high-aspect-ratio structures. A 6 µm thick positive resist AZ9260 is spray-coated onto the wafer tile. By spray coating, the sidewall of the metalized pillars can be uniformly coated with resist. On the other hand, the pitch size of the pillars is limited by the spray coating technique. When the spacing between the pillars becomes smaller, the resist can form a bridge between the pillars, such as for the pillars with a diameter of 80 µm, a height of 150 µm and a pitch size of 100 µm. To avoid this resist bridging, the aspect-ratio of the spacing between the pillars should be smaller than 3:1.

### 3.3.5. ASSEMBLY AND MOLDING

In Figure 3.5 (e-g), the post-process steps after TPV fabrication, (post-TPV process), are illustrated. The post-TPV process starts with the dicing of the wafer tile. During the dicing step, the TPVs are exposed to water jet which can cause the delamination of the TPVs, as shown in Figure 3.6. TPV adhesion is critical for the yield after the dicing. Higher aspect ratio pillars require stronger adhesion when exposed to the water jet. Thus the adhesion, the aspect ratio, and the mechanical properties of the pillar need to be considered at the design phase.

The adhesion of a pillar is influenced by both the adhesive strength of the materials and the pillar profile at the substrate interface. Poor adhesion pillars usually have a lift off at the bottom edge, results in a smaller contact area at the interface, as shown in Figure 3.6 (b). The lifting off of the bottom edges is caused by the internal stress of the SU-8 and the mismatch of the coefficient of thermal expansion. By increasing the PEB temperature, the lifting of pillar bottom can be avoided while the diameter of the pillars will expand slightly due to the higher baking temperature. Robust TPVs are obtained with a PEB temperature of 110°C instead of 95°C, see Figure 3.7. These optimized TPVs survived the dicing process and no delamination is observed.

After the dicing process, singulated ICs are picked and placed and attached to the QFN lead frame. The pick and place accuracy has an impact on the alignment of the antennas structures in the antenna fabrication phase (see section 3.3.6). Following the die-attach process, wire bonds are made to connect the DC signals from the contact pads on the radar IC to the QFN pads. The loop height of the wire bonds needs to stay below the height of the TPVs. After the wire-bonding process, the assembly procedure is finished and the QFN lead frame is ready to be molded. At this point, 2 types of chip-to-QFN interconnects are fabricated, namely wire bonds for DC interconnects, and TPVs for the high-frequency interconnects.

Film assisted molding is used to encapsulate the assembled QFN lead frame. The

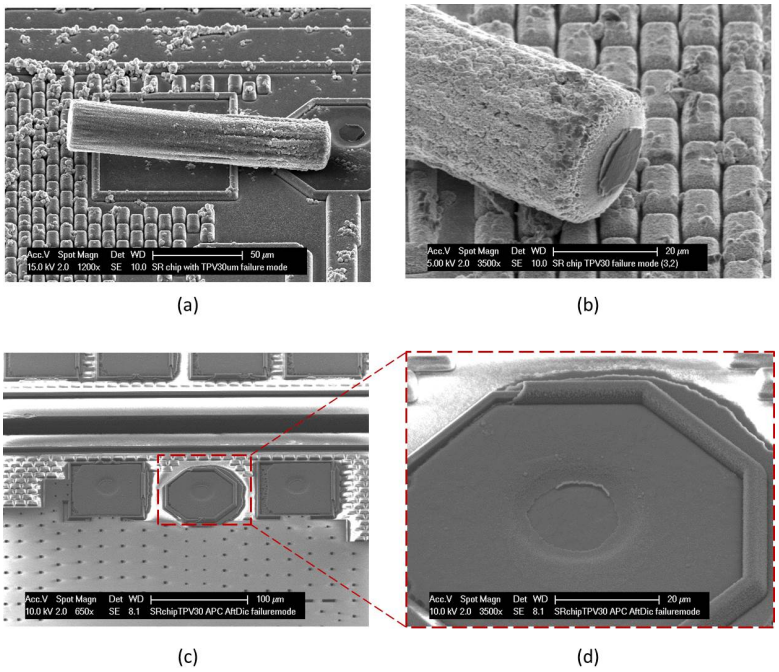



Figure 3.6: SEM images of delaminated TPVs and the delamination site on the contact pads. (a) A delaminated metalized TPV on the substrate. (b) The view of the delaminated pillar bottom. (c) The delamination site on the substrate. (d) Zoom-in view on the delamination site.

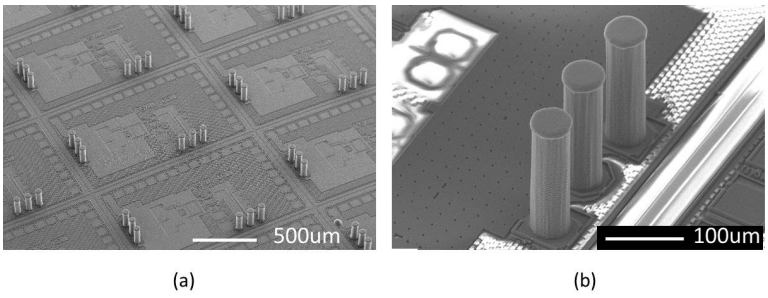



Figure 3.7: TPVs fabrication results from the optimized process setting. (a) TPVs on chip array, each chip has 2 GSG ports which requires 6 TPVs in total. (b) Close-up view of the optimized TPVs.

QFN lead frame is molded at 165 °C and with an EMC insert pressure of starting at 20 bar and controlled dynamically. The clamping pressure of the mold is around 150 bar. Furthermore, the mold height can be adjusted by inserting dedicated spacers. Optimizing the mold height reduces the damage of the TPVs, keeps the bond wires fully encapsulated, and ensures that the top of the TPVs are well clamped and kept clean during molding and hence exposed after mold release. The SEM images of TPV heads after

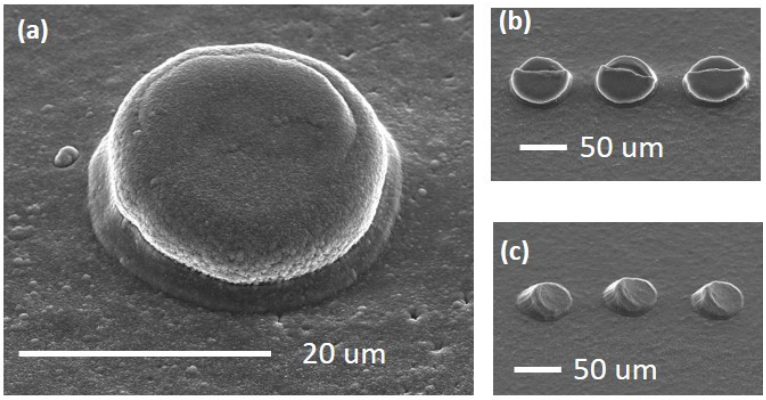



Figure 3.8: Protruding TPV heads metalized with 4 µm Al(1%Si). (a) A desired well-protected TPV head after film-asisted molding. (b) TPV heads with partially delaminated top metal layer. (c) Bended TPV heads.

molding are shown in Figure 3.8.

The mold releasing process can potentially damage the top of the TPVs as shown in Figure 3.8 (b,c). The top metallization of the TPVs can be stuck to the protecting film and peeled off. Therefore, the yield in the mold releasing step can be optimized by improving the adhesion of the metal layer to the polymer pillar, or optimizing the thin film peeling angle and peeling speed.

Further improvement can be found in a reduction of the height variation of the fabricated TPVs. The differences in the pillar heights introduce a difference in the clamping conditions where some of the TPVs are over clamped and others are not clamped. This results in tilted TPVs, damaged TPV heads, or over-molded TPV heads.

### 3.3.6. ANTENNA FABRICATION

Antenna fabrication on top of the molded QFN lead frame is the next step after molding in the TPVM-C-QFN process. Before the metalization, a cleaning process is applied to the EMC surface to remove any organic contamination and improve metal adhesion. Both oxygen plasma and solvents, like acetone, can be applied. In the case of plasma flash, it is recommended to use low power, low temperature, and short time recipe to avoid damage to the exposed TPV heads.

To form the metal coating on EMC, sputtering at room temperature and with intermediate cooling steps is performed. For the etching of the metal layer, the spin-coated resist can result in poor coverage of the TPV heads, hence it is recommended to use spray-coated resist instead. In this work, AZ9260 photoresist spray-coated with a thickness of 6 µm was applied. The printed film mask used for antenna patterning is shown in Figure 3.9. In the mask design, 36 antenna arrays can be fabricated on each QFN lead frame.

The contact pads pattern on the antenna layer is aligned to the TPV heads by visual alignment through a microscope on the mask aligner. The yield of the antenna fabrication process is closely related to both the alignment accuracy and the pick and place

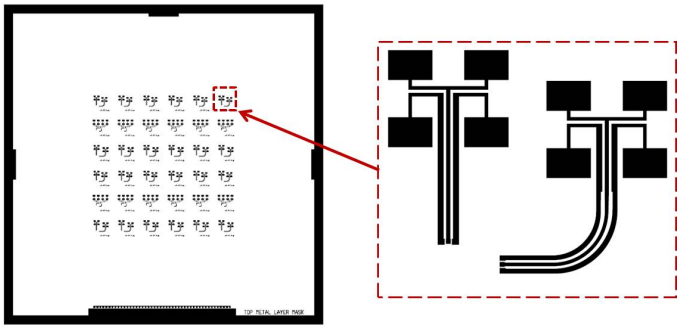


Figure 3.9: Film mask design for patterning the antenna layer. The zoomed-in image on the right shows the GCPW-fed patch antenna array design with the GSG contact pads which connect to the encapsulated IC via TPVs underneath.

accuracy during the assembly process. The alignment accuracy can be further improved by using alignment markers or field alignment with maskless lithography. Since the mask design of the antenna layer is a fixed design with multiple antennas based on the nominal position of the pick and placed radar ICs, the inaccuracy caused by the pick and place process induces the misalignment of the antenna pattern with the TPV heads which can cause no contact or bad contact. Furthermore, the pitch size between the TPVs and the required lithography of the TPV metalization layer limit the design of the overlap between the antenna contact pad and the TPV heads to compensate for the misalignment caused by the pick and place process. In this work, a TPV-to-antenna overlap of 15 µm was available. However, for production, a chip-package co-design is required to optimize the misalignment tolerance and antenna performance. The antenna fabrication results and the final AiP packages are shown in Figure 3.10.

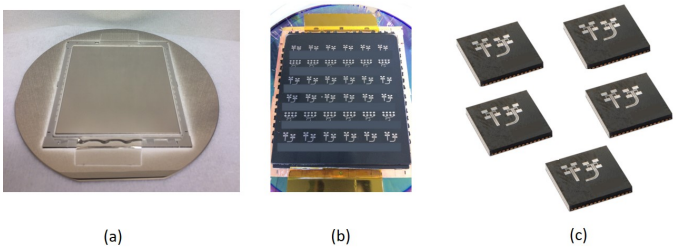



Figure 3.10: Antenna fabrication and the end results. (a) The molded QFN substrate with metal coating. (b) The fabricated antenna structures on the QFN substrate. (c) The singulated radar AiP packages.

### 3.3.7. SUMMARY

To summarize, the TPVM-C-QFN process has been developed. The proof of principle of the antenna-in-package (AiP) concept is validated. The initial challenge of the process is the inadequate adhesion of the metalized TPVs that caused delamination during the dicing procedure. Sufficient adhesion was obtained with an optimized PEB step. These

optimized metalized TPVs have an improved foot profile and a 100% survival rate after dicing. Other challenges such as the alignment of the antenna mask, the damage of the TPV heads, the over-molding caused by height difference, will require further process optimization and a chip-package co-design.

## 3.4. TPVO-C-QFN PROCESS

In the TPVO-C-QFN process, segregated micro-windows are integrated into an optical encoder system-in-package using TPV technology. The TPV polymer structures fabricated in this process function as vertical optical waveguides. The 3D schematic of the process steps of the TPVO-C-QFN case is shown in Figure 3.11.

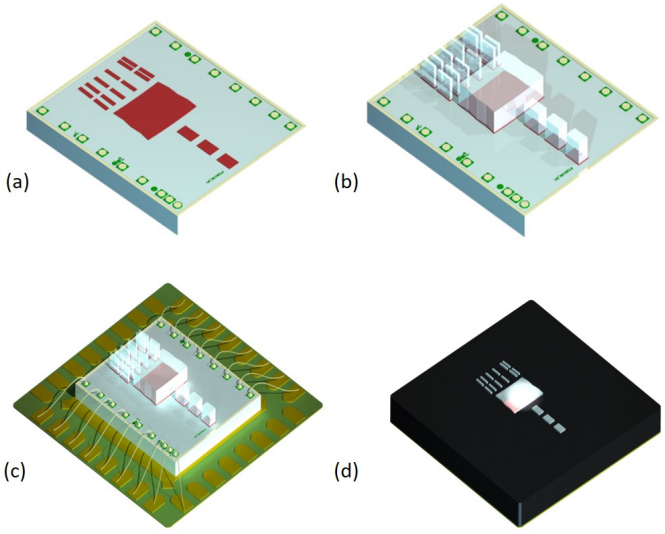



Figure 3.11: 3D schematic of the TPVO-C-QFN fabrication process. (a) The 3D model of a single optical encoder chip. The red areas in the center represent the optical sensitive photo-diodes. (b) Optical TPVs fabricated on top of the photo-diode areas. (c) The encoder chip assembled onto a QFN lead-frame and wire-bonded. (d) The 3D model of the final package after film-assisted molding.

The optical encoder chip packaged in this process is used for motion detection in electric motors [3–5]. The encoder senses the rotation angles and obtains the exact position of the rotor in real-time. Such optical encoders are usually found in the brushless DC motors (BLDC-motors) with applications in angle detection[6, 7], accurate position[8, 9] and robotic control [10]. BLDC-motors have low heat dissipation and high energy efficiency. In the BLDC-motor, the stator provides a changing magnetic field by electric current commutation which acts on the DC magnetic field of the permanent magnet on the rotor. It is suitable for applications in motion control which can adapt to the actual load demand in real-time to improve energy efficiency. Commutating the stator current at the optimal rotor position is essential for reducing electrical losses when managing variable speed and load situations. To accurately control the current commutation, the exact rotational position needs to be measured in real-time.

In the BLDC-motor driver, the three 120 degrees in-phase shifted commutation (UVW) signals are generated in real-time to trigger the electrical commutation. Various approaches are available for generating the UVW signal, such as using winding built-in Hall sensors, using software calculation based on the back-EMF data from the stator winding, attaching an optical or magnetic sensor to the motor axis, or the integration of advanced single-chip optical or magnetic encoder ICs into the motor housing.

The sensorless approach requires an effective algorithm and a fast microprocessor or DSP to reduce latency. Sensorless UVW generation is limited in situations when fast load changes, low speed, and out of sync operation is needed. Obtaining the absolute rotor position from sensors is regarded as the most reliable approach.



Mounting an optical or magnetic encoder system-in-package to the BLDC motor is advantageous in reliability and positioning accuracy. Magnetic encoders are less sensitive to dirt and moisture which has excellent reliability in harsh environment applications [11, 12]. The optical encoders, on the other hand, have the best sensing accuracy which is highly demanded in high precision control.

However, the packaging of the optical encoders requires the assembly of optical windows which increases the cost. The traditional approach to fabricate the optical window in the encoder package is to pick and place a glass plate onto the photodiode area and use film assisted molding to encapsulate the rest of the chip while exposing the glass window. As the need for encoder packages with multiple optical window increases, the cost in the glass plate assembly increases largely. Thus, low-cost advanced optical packaging solutions enabling multi-windows for the optical encoders are highly demanded.

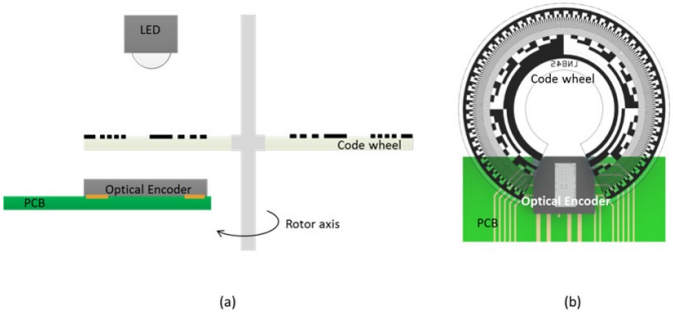



Figure 3.12: The working mechanism of an optical encoder in a motion detection system. (a) Cross-section view. (b) Top view, LED is not shown, adapted from [5].

Compared to the traditional optical encoder packaging, the optical encoder system-in-package developed in this work using TPV technology has the advantage of a better scalability using lithographically defined optical window structures without glass window pick and place. Furthermore, other advantages include high resolution and high placement accuracy of window structures, arbitrary window shape, smaller feature size, high aspect ratio, and the capability of mass production. Benefit from multiple optical windows and smaller dimensions of the windows, the encoder package can reach a higher resolution of motion sensing. The encoder chip used in the TPVO-C-QFN process works with an 850 nm wavelength LED light source and a code wheel. See Figure 3.12.

The optical encoder package which is mounted on a PCB substrate is placed on one side of the code wheel while the LED light source is placed on the other side. The code wheel is fixed on the rotor axis and rotates together with the rotor. Thus, patterns on the code wheel define the absolute position of the rotor.

### 3.4.1. FILM MASK DESIGN

For this work, the chips are supplied as a large multi-chip tile. The printed film mask used in the process is shown in Figure 3.13. The two encoder chips on the left top and bottom corners of the tile are sacrificed for the alignment. According to the contact pads position and chip layout, the alignment marker is designed and shown in Figure 3.13 (Left zoomed-in view). The patterns of the TPV structures fabricated on the encoder chip is shown in Figure 3.13 (Right zoomed-in view). The transparent areas on the mask are aligned to each photodiode area on the chip where SU-8 polymer structures are projected. To compensate for alignment errors and to ensure that the photodiode areas are fully covered with SU-8 structures, a 10 µm overlap of the TPV patterns compared to the diode areas is implemented. The largest TPV structure in the center of the encoder chip is around 1000 µm x 800 µm in dimension. The structures on the top column are around 300 µm x 200 µm and the smallest structures at the bottom rows are nearly 300 µm x 70 µm.

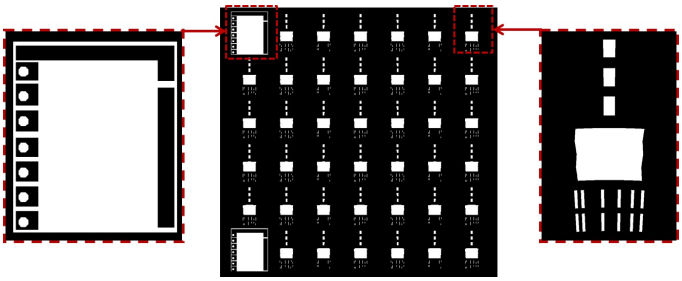


Figure 3.13: Mask design used in the TPVO-C-QFN process for TPV fabrication on encoder wafer tile. The left zoomed-in image shows the design of alignment markers. The right zoomed-in image shows the optical window patterns.

### 3.4.2. TPV FABRICATION

In the TPVO-C-QFN process, the wafer which contains the optical encoder ICs are diced into tiles in the size of 20.16 mm × 20.22 mm. Each tile contains 42 encoders and each encoder chip contains 16 photodiodes, thus each tile contains in total 672 photodiodes. Each encoder chip is in the size of 2.8 mm x 3.4 mm. For the SU-8 film, a lamination process was chosen using 350 µm thick SUEX dry film laminates. The size of each SUEX patches is 48 mm × 48 mm which is larger than the tile with chips. A 100 mm silicon carrier wafer is used for handling the tile in the cleanroom equipment. A detailed process flow of TPVO-C-QFN is described in the next paragraph and summarized in Figure 3.14.

Firstly, the encoder wafer tile is placed in the center of the carrier wafer followed by the placement of the SUEX patch. The corners of the SUEX patch are bent slightly

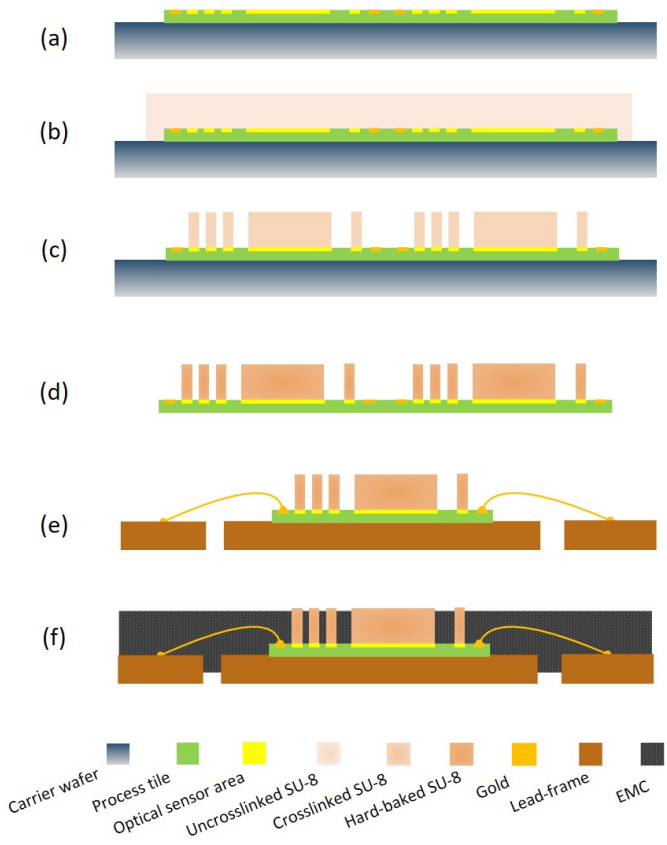



Figure 3.14: A detailed process flow of the TPVO-C-QFN process. (a) Placing the encoder wafer tile on Si carrier wafer. (b) Lamination of SUEX film over the encoder wafer tile and the Si carrier wafer. (c) Formation of the TPV structures. (d) Removing the wafer tile from the carrier wafer and hard baking. (e) Assembly of the singulated chip on the QFN lead frame. (f) Film assisted molding.

downward so that when placed over the wafer tile, there is a gap in between and no contact is made which is beneficial to avoid trapping air. The lamination is carried out on a Triangel vacuum laminator. The stack of carrier wafer, encoder wafer tile, and the SUEX dry film resist patch are placed inside the laminator between the bottom stage and the heated top press pad. The system firstly applies the vacuum and then presses down to apply both heat and pressure on the laminated stack. The SUEX dry film is laminated at 60 °C and under a pressure of 0.2 MPa. The hold time is set to 120 s to ensure good adhesion and coverage of the SUEX dry film resist. Afterward, a post-lamination bake is carried out at 85 °C on a hotplate to improve further the adhesion. To enable a slow cooling down process, the hotplate is powered off and the wafer is left on the hotplate to naturally cool down to room temperature. The cooldown process takes around 30 mins. Because the SUEX patch is overlapping the encoder tile, the tile is fixed to the carrier wafer.

The exposure is carried out using SUSS MA6 Mask Aligner in hard contact mode for 400 s with an intensity of 10 mWatt/cm. The MA6 Mask aligner uses a broadband UV source with wavelengths from 350 nm to 450 nm. With this exposure dose, an over-exposure is applied to ensure a sufficient dose at the bottom of the film to avoid the delamination of structures during development. However, the heavy over-exposure can influence the mechanical property of the SU-8 polymer and make it brittle.

A post-exposure bake is applied to start the cross-linking process at 65°C for 5 mins and 95°C for 10 mins consecutively. Slow cooling after the PEB is considered the most critical process for avoiding overly stressed SU-8 layers which causes cracking and delamination. The same cooling approach as the one after the post-lamination bake is practiced here.

After post-exposure baking, we developed the SUEX film in PGMEA for 15 mins and rinsed in IPA for 5 mins. When residual is found still on the wafer tile, acetone dip or plasma flash can be used to further clean residual photoresist. The cleaning time using acetone dip needs to be kept short, in the range of 5 to 10 seconds, because the bottom of the microstructures which has received less exposure dose, and consequently less cross-linking, can be attacked by acetone and results in delamination. After acetone dipping, the wafer should be immersed in IPA right away to avoid the abrupt decrease of temperature caused by the evaporation of acetone. Water rinsing should be avoided because it can produce a thin white redeposition and contaminate the entire sample area. Spin drying or blowing the sample with $N_2$ jet to dry should be avoided because the force applied to the high-aspect-ratio structures can cause cracking and delamination. Alternatively, drying on a hot plate or in an oven at 50 °C is recommended. If further processing involves wire-bonding, a low power $O_2$ plasma flash at room temperature for a short time is recommended to further clean the substrate surface of the wafer tile.

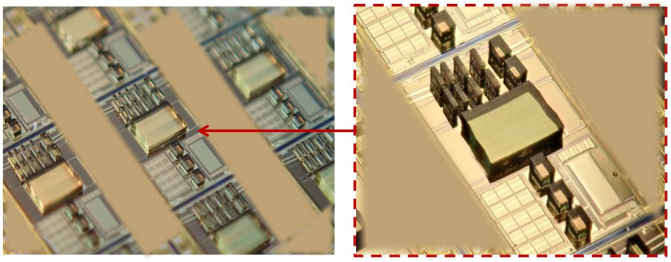
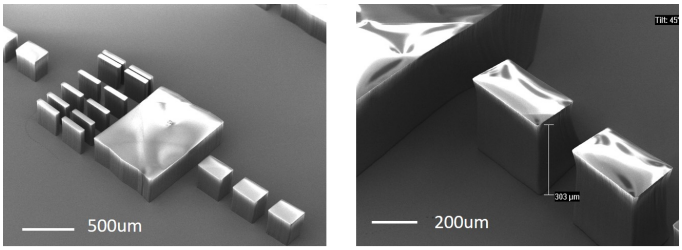



Figure 3.15: The fabricated SU-8 structures on the optical encoder ICs. (a) A picture showing the optical TPV array. (b) The zoomed-in view of optical TPVs on a single chip area.

In case some micro-cracks are observed after the development and cleaning process, these microcracks can be removed using a hard baking step to anneal the SU-8 structures. Wafer tiles are removed from carrier wafer and the backside of the tile is cleaned by IPA. Hard baking can further cross-link the epoxy groups and makes the SU-8 polymer more stable at a higher temperature. Since the molding temperature is around 165 °C, the hard baking temperature is set at 180 °C for 2 hours. The fabrication results are shown in Figure 3.15.

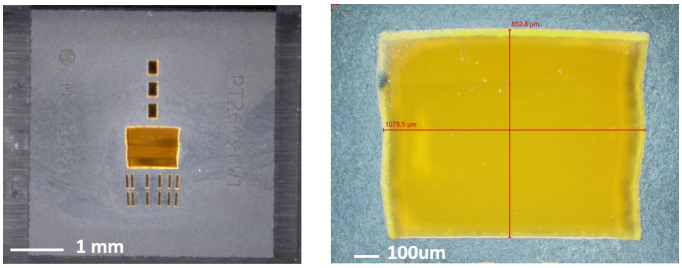



(a) (b)



Figure 3.16: The SEM images of the fabricated optical TPVs on a dummy tile. (a) Overview of the TPV array. (b) Zoomed-in view on the SU-8 structures.

This approach of making optical windows for encoder chips shows micro-meter accuracy in alignment and allows multiple windows that have feature size below 100 µm with aspect-ratio larger than 4:1 to be fabricated by a single process. The SEM images of fabricated optical TPVs on dummy silicon wafer tile are shown in Figure 3.16. Because the SU-8 collects electric charges from the SEM beam, there is a virtual distortion of the image. After the TPV fabrication process, the wafer tile is then diced and bonded to the QFN lead frame and molded. Images of the molded packages are shown in Figure 3.17.




(a) (b)

Figure 3.17: The results of the molded encoder package with 16 optical windows. (a) Top view of the 5x5 QFN package after dicing. (b) Closed-up view under microscope of the center window.

### 3.4.3. CHALLENGES

There are mainly 3 challenges in the TPVO-C-QFN process. The first challenge is the yellowing of the SU-8, as shown in Figure 3.18. The yellowing phenomenon is a thermal oxidation process of the polymer chain. The resulting oxidation products increase the absorbance of light at a shorter wavelength. The conventional approach of using glass windows has no yellowing effect. Thus, to emulate with the conventional approach, the optical TPV approach must overcome the yellowing challenge before it can be adopted. Solutions can be found in the optimization of material properties by mixing SU-8 polymer with additives such as antioxidants.

Secondly, 3 different failure modes related to the SU-8 height and height differences

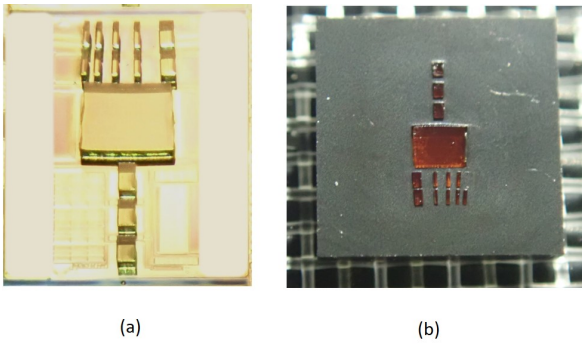



Figure 3.18: Yellowing of SU-8 due to thermal oxidation. (a) Optical image of the SU-8 structures before hard baking which shows very little yellowing. (b) Optical image of the SU-8 structures after hard baking, assembly and molding which shows a severe yellowing.

are found after the molding process, as shown in Figure 3.19 (a-c). In the FAM process, the pressure applied to the top of the SU-8 structures leads to the compression of structures. After mold releasing, the SU-8 structures tend to recover to its original height and lateral dimensions which results in excessive stress causing the cracking and delamination at the interface between EMC and SU-8. The cracked SU-8 windows leave a larger cavity inside the EMC layer and the recovered lateral dimension is the same as the non-cracked ones which are the evidence of heavy compression. Furthermore, the insufficient SU-8 thickness results in partially over-molded and completely over-molded SU-8 windows.

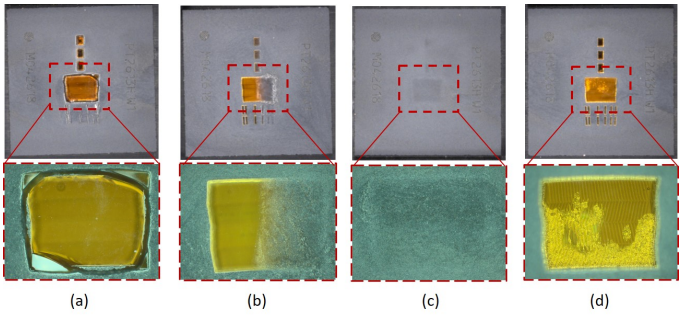



Figure 3.19: The most observed failure modes in TPVO-C-QFN process. (a) Delamination and cracking at the interface between EMC and SU-8. (b) Non-uniform thickness causing partial encapsulation. (c) Insufficient thickness of the SU-8 structures which is completely overmolded. (d) Air trapped at the interface between SU-8 and encoder chip surface.

A third challenge is the micro air bubbles trapped at the bottom interface between the SU-8 window and the chip, as shown in Figure 3.19 (b). Process related issues such as substrate wettability and vacuum levels are the main issues with the lamination of SUEX dry film over the non-flat surface.

## 3.5. TPVH-N-PCB PROCESS

Large displays on which each pixel is made of micro-LED will form the next generation of 4K LED displays. These large displays can be used in outdoor advertising, displays in sports stadiums, traffic information boards, etc. To reach a higher resolution, the size of the LED chip needs to be scaled down as well as the pitch between each LED. At the required smaller pitches, the fabrication of Through-Package holes for optical access per pixel in a 4K resolution LED panels becomes challenging with the conventional approach.

In the conventional approach, a through-hole is made by using a dedicated top mold in a film-assisted molding process [13–15]. The top mold is micro-machined with protruding pillars on locations where an optical path to the LED is needed. During the transfer molding process, these protruding parts of the mold are pressed onto the chip area where a window is required, thus keeping these areas free from the epoxy molding compound.

However, making a mold for a large array of through-holes is becoming costly for smaller dimensions and finer pitch sizes. Furthermore, with a large amount of protruding pillars on the mold surface, the vacuum applied can not hold the film tightly to surface geometry. Hence, new approaches for making high density, small dimension through-holes are needed.

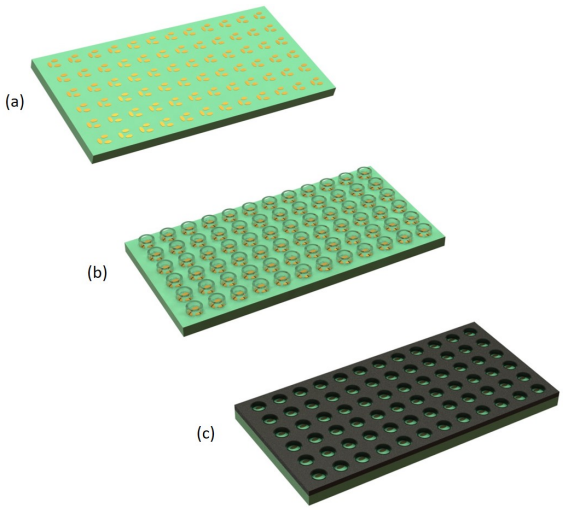



Figure 3.20: 3D schematic of the TPVH-N-PCB fabrication process. (a) 3D model of a PCB board which contains arrays of contact pads for LED integation. (b) 3D model of the PCB board with fabricated hollow TPV array. (c) Molded PCB board with through-hole array made of hollow TPVs.

In the TPVH-N-PCB process, Through-Polymer Via technology is used to create through-holes in the EMC layer of a molded PCB panel. Compared with the previously discussed cases, the manufacturing process of TPVs on a large PCB substrate is rather different. The entire PCB board is a single functional unit that requires a 100% yield of TPV structures. The adhesion of the TPV structures is extremely critical here.

Due to the substrate shape and dimensions, the spin coating of liquid SU-8 is not applicable. Thus, customized SUEX dry film is laminated onto the PCB substrate instead. The 3D illustration of the TPVH-N-PCB process is shown in Figure 3.20. On a PCB substrate, array of TPV rings are fabricated. The TPV rings act as a wall to protect the inner PCB area from EMC creating through holes after molding.

### 3.5.1. FILM MASK DESIGN

The area which requires exposure on the PCB is 8.5 × 12 cm. These dimensions exceed the exposure area of a 100 mm mask aligner used in this work. A method of two times exposure is used to cover the entire PCB. A film mask is designed to cover half of the PCB area as shown in Figure 3.21.

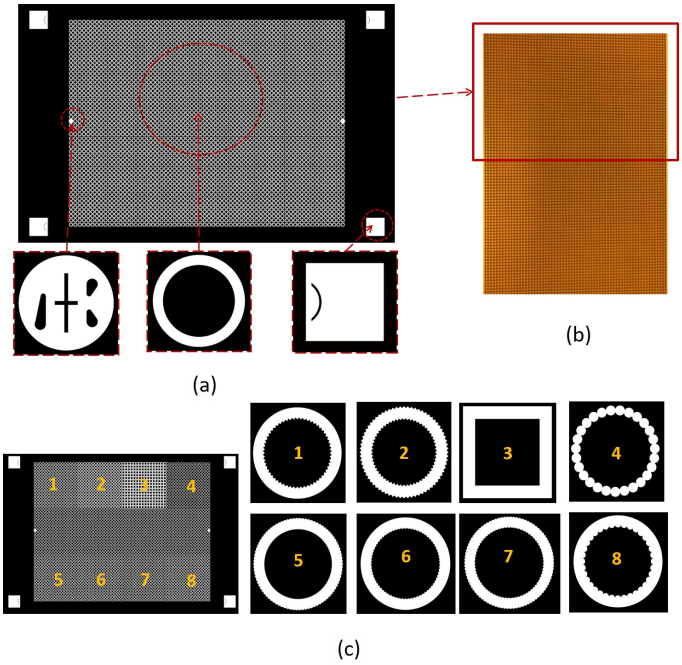



Figure 3.21: The Mask design used in the TPVH-N-PCB process. (a) Mask design of identical SU-8 rings (bottom middle), first-level alignment markers (bottom left) and second-level alignment markers (bottom right). (b) The mask covers half of the PCB substrate. (c) Special mask designs containing 7 different ring patterns with side wall features and a square pattern.

Two levels of alignment markers are designed to ensure good alignment efficiency, as shown in Figure 3.21 (a). First level alignment markers are designed to match the through holes that are outside the functional area on the edges of the PCB. Once the first level alignment markers are in position, a second level alignment marker can be used to improve the alignment accuracy. The second level alignment markers are designed according to the LED contact pads on the PCB substrate sacrificing two LED pixels on the left and right edges. For loading the PCB on a 100 mm wafer mask aligner, a dummy

100 mm wafer is taped on the backside of the PCB, so that the vacuum check of the chuck is triggered. The PCB is shifted upward or downward so that half of the PCB substrate is exposed at a time, as shown in Figure 3.21 (b).

Special ring structure designs are included in a second mask design. There are 7 different ring patterns with sidewall features and a square pattern distributed over 8 square areas on the mask, as shown in Figure 3.21 (c). These special ring designs show that TPV technology can enable the fabrication of through-holes with micro features and arbitrary shapes which goes beyond the conventional method.



### 3.5.2. TPV FABRICATION

The main steps of the TPVH-N-PCB process are shown in Figure 3.22. Firstly, the PCB substrate is cleaned by rinsing with acetone or isopropanol. The PCB substrate is then placed on a hotplate at 50 °C for quick drying after cleaning. A gentle oxygen plasma cleaning with a low RF power of 300 W and a short time of 30 seconds is applied to further clean the substrate.

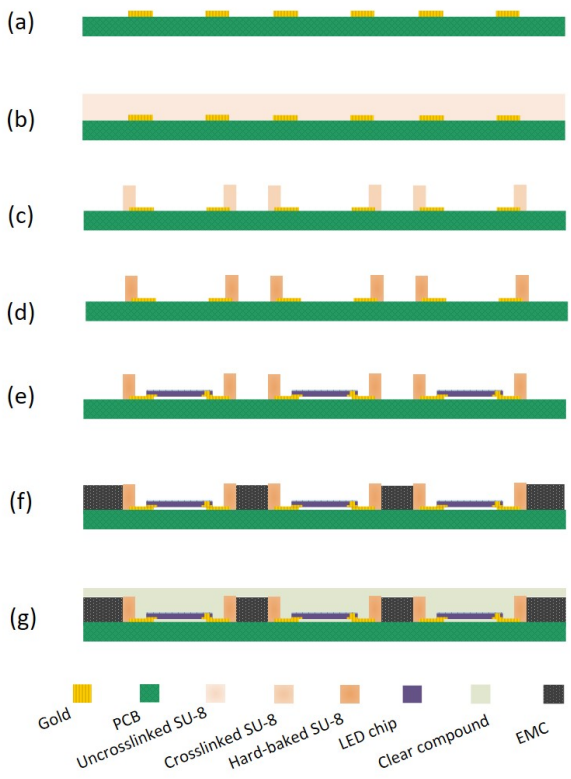



Figure 3.22: A detailed process flow of TPVH-N-PCB process. (a) The PCB substrate, (b) SUEX dry film lamination on PCB, (c) the formation of SU-8 ring structures, (d) hard baking, (e) assembly of LEDs, (f) film assisted molding, (g) clear compound molding.

After the cleaning process, the SUEX dry film resists with dimensions of 8.5 cm in width, 12 cm in length, and 300 µm in thickness is laminated on the PCB substrate using vacuum lamination. A post lamination bake process is carried out subsequently on a hotplate at 95 °C for 3 minutes and 105 °C for 1 minute to improve the adhesion of SUEX dry film to the PCB substrate.

Exposure is carried out on a mask aligner using soft contact mode, with an exposure time of 340 s at a power density of 10 mW/cm$^2$, which gives a total dose of 3400 mJ/cm$^2$. According to the SUEX dry film data sheet provided by the manufacturer, a dose of 800 mJ/cm$^2$ is recommended for 300 µm thick SUEX dry film at 365nm wavelength without a filter. However, for improving the adhesion of the SU-8 structures, a heavy over-exposure is applied here to ensure the bottom of the structures is thoroughly cross-linked.

The post-exposure bake is carried out at 130 °C for 30 min inside an oven, and the PCB substrate is cooled down slowly to room temperature inside the oven which takes about 1 hour.

The development is done by immersing the PCB substrate into PGMEA developer with the SUEX laminated surface facing down. To avoid any delamination of the TPV ring structures, no agitation is applied in the developer in this process. The PCB substrate is then rinsed in isopropanol (IPA). Acetone rinsing is avoided here because the fast cooling induced by the evaporation of acetone can potentially weaken the adhesion of the developed SU-8 structures.

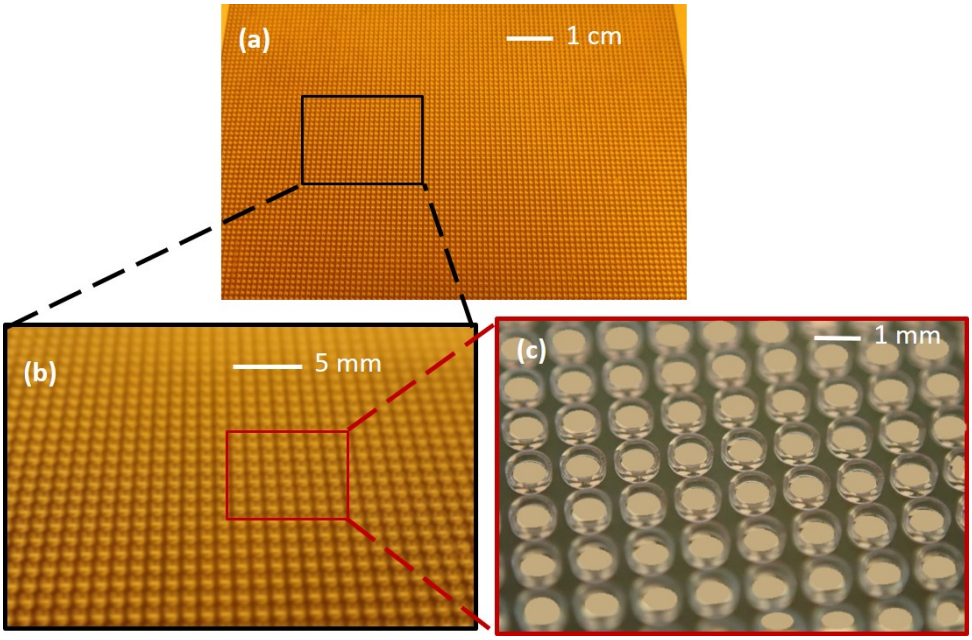



Figure 3.23: Fabrication result of TPV ring structures on PCB. (a) Overview of the entire PCB after TPV fabircation. (b) A good adhesion of SU-8 rings are achieved, no delamination is observed. (c) Close-up view of the SU-8 ring structures.

After the development, the substrate can be dried on a hotplate at 50 °C. The SU-8 structures are then hard-baked in an oven at 180 °C to further evaporate any absorbed solvent and further crosslink the material.

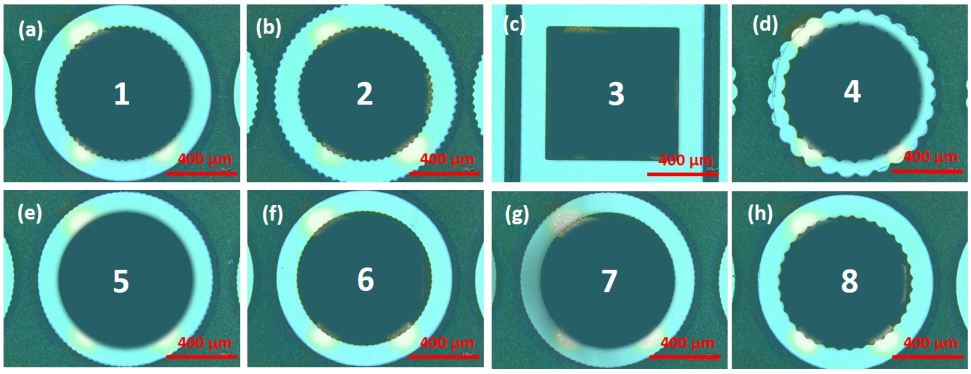



Figure 3.24: Fabrication results of the special TPV ring designs with micro-scale surface topology on the vertical sidewalls. (a) Design 1 with a zigzag edge on the inner sidewall, (b) design 2 with zigzag edges on both the inner and outer sidewalls, (c) design 3 in a square shape, (d) design 4 with large wave edges on both the inner and outer sidewalls, (e) design 5 with small wave edges on the outer sidewalls, (f) design 6 with small wave edges on the inner sidewall, (g) design 7 with small wave edges on both the inner and outer sidewalls, (h) design 8 with medium wave edges on the inner sidewall.

The fabrication result of the TPV rings on the PCB substrate is shown in Figure 3.23. There are more than 5000 SU-8 rings fabricated on a single PCB substrate. Each TPV ring has a designed inner diameter of 800 µm and a wall thickness of 110 µm. A 100% adhesion of the TPV ring structures is achieved. The zoomed-in view of the TPV rings and the contact pads are shown in Figure 3.23 (c). Each TPV ring is standing on both the contact pads surface and the PCB surface where a 15 µm step height exists between the two. The fabrication results of the 7 special ring structures and one square structure under an optical microscope are shown in Figure 3.24. This demonstrates that with the TPV method, micro-scale surface features on the inner or outer wall of the through-hole can be easily manufactured, which is a big advantage over the conventional FAM method.

### 3.5.3. ADHESION OPTIMIZATION

The adhesion of the TPV ring structures is critical for the yield of this process. Every single PCB panel is an individual functional unit which requires 100% of good adhesion of thousands of the TPV rings. Thus the focus of the optimization of the TPVH-N-PCB process is to reach a 100% yield of the TPV structures. No delamination should be found after development.

To improve the adhesion of the TPV structures, the PEB process step is optimized. By performing the PEB process according to the SUEX data sheet which is at a temperature of 95 °C, more than 70% of the structures are delaminated after development, as shown in Figure 3.25 (a). By applying a PEB temperature of 120 °C, the adhesion is largely improved as shown in (b), nearly 10% of the structures are delaminated. And finally with a PEB temperature of 130 °C for 30 min, the adhesion of the TPV structures reached 100%,

as shown in Figure 3.25 (c). At higher PEB temperature such as 140 °C, the development process in PGMEA becomes less efficient in removing all the unexposed SU-8, and the bridging between the ring structures by strings of SU-8 can be observed.

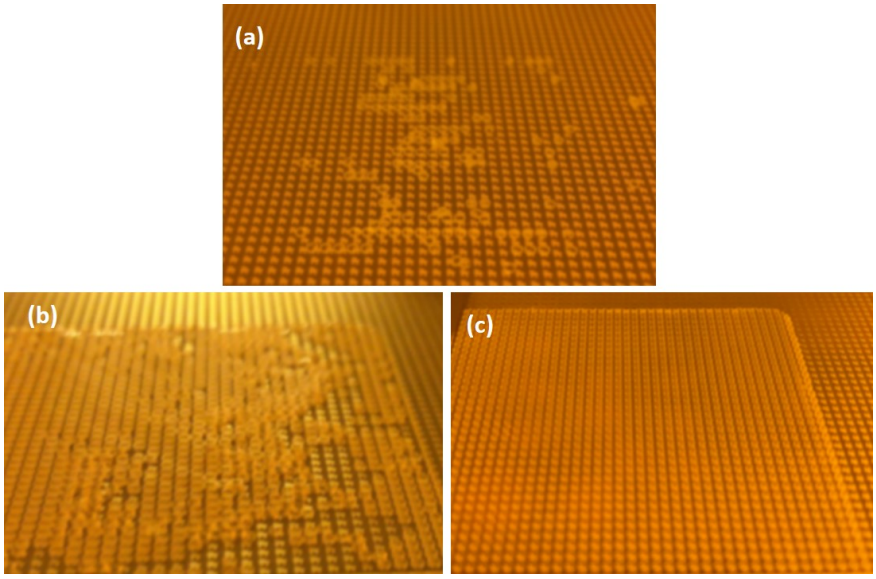



Figure 3.25: Adhesion improvement of the TPV ring structures. (a) Poor adhesion observed with strong over-exposure (340s at 10 mW/cm2) of SUEX dry film and PEB at 95 °C. (b) Improved adhesion of the ring structures by PEB at 120 °C. (c) 100% adhesion of the ring structures achieved by PEB at 130 °C.

Other than increasing the PEB temperature, methods such as using an adhesion-promoting layer between the PCB and the SUEX dry film, designing the ring structure with non-uniform wall thickness with increased thickness at the diagonal direction, or implementing interlocking microstructures at the bottom of the ring can potentially improve the adhesion further. However, these methods will increase the process complexity or the occupation of more surface area.

## 3.6. TPVH-W-QFN PROCESS

In applications like MEMS or chemical gas/liquid sensing, an exposed chip area is required after the encapsulation of the epoxy molding compound. Making open through-mold areas while keeping other chip areas encapsulated makes it possible for the embedded chip to access the environment with its circuit well protected.

The scaling down of QFN package size is approaching sub-millimeters. This brings challenges to make a smaller through-hole aligned to the encapsulated chip in a miniaturized QFN package. This pushes the conventional through mold window fabrication approach to or beyond its limits.

Conventionally, electrical discharge machining is used to make protruding structures on the inner surface of the mold to form the through-holes in the EMC. This approach is becoming costly and insufficient in quality for the Film-Assisted Molding (FAM)

process when the through-hole size and pitch keep scaling down. TPV technology provides a novel solution to make an ultra-small exposed chip area which is into micrometer dimensions.

In the TPVH-W-QFN process, the miniaturized SU-8 ring structures are manufactured on a silicon wafer on a 0.5 mm × 0.5 mm die area with Al coating, as shown in Figure 3.26. On the test silicon wafer, the Al layer is patterned into squared pads, and each pad represents a die. After the fabrication of the TPV structures, the wafer is diced and single chips with TPV structures are assembled to a QFN lead frame and finally is molded by the epoxy molding compound. In the TPVH-W-QFN process, micro-size high-aspect-ratio TPV through-holes are fabricated. Unlike the TPVH-N-PCB process which uses structures with an inner diameter around 800 µm, the through-holes need to be achieved here are much smaller, down to 50 µm.



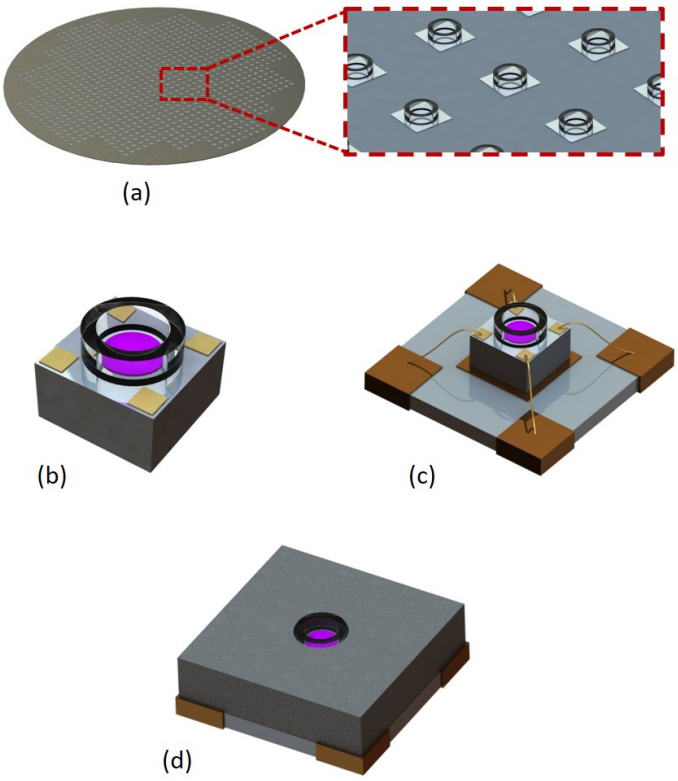



Figure 3.26: 3D schematic of the TPVH-W-QFN fabrication process. (a) Hollow SU-8 structures fabricated on a silicon wafer, (b) a single die with micro hollow SU-8 structure, (c) the assembly of the QFN substrate, the die and wire bonds, (d) the molded package with a micro through-hole.

### 3.6.1. FILM MASK DESIGN

On the film mask designed for the TPVH-W-QFN process, arrays of various TPV hollow designs are included. Some enlarged images of typical TPV structures on the mask are shown in Figure 3.27. These TPV hollow structures vary from designs of different diameters from 50 µm to 300 µm and wall thicknesses from 20 µm to 40 µm, examples are shown in Figure 3.27 (a) and (b). Designs with multiple TPV hollow structures on the same die, with other shapes such as triangle and rectangle, are also included. Special designs with an array of pillars inside the TPV ring are implemented and such structures can be potentially used as micro-probes, micro-socket, heat sinks, or antenna feeding through the air.

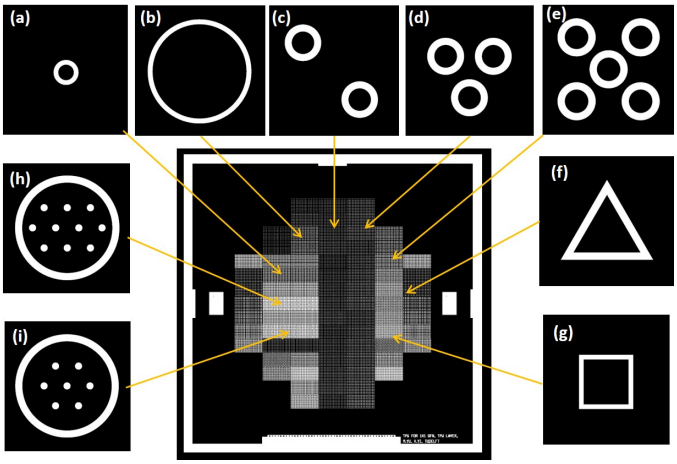



Figure 3.27: The mask design used in the TPVH-W-QFN process. (a-i) examples of the hollow TPV designs. (a) and (b) represents ring structures with a different inner diameter and wall thickness. (c-d) shows the design of making multiple structures on a single die area. (f) and (g) shows triangular and rectangular designs. (h) and (i) shows the design of structures which contains micro-pillars inside the through-hole.

### 3.6.2. TPV FABRICATION

The TPVH-W-QFN process starts on a bare silicon wafer. Firstly, alignment marks are fabricated on the wafer followed by the deposition of a 1 µm thick Al(1%Si) (further referred to as Al) layer. The Al layer is then patterned into 500 µm by 500 µm patches with a 20 µm wide dicing line in-between every two patches. Each Al patch represents a dummy chip which will be later diced and assembled to the QFN leadframe.

The silicon wafer with the Al patches is laminated with a 100 mm wafer size SUEX dry film resist. The SUEX dry film applied in this process is 100 µm thick. Vacuum lamination is performed with a vacuum time of 100 seconds, lamination time of 200 seconds at 60 °C. After the lamination, a post lamination bake is carried out on a hotplate at 85 °C for 3 min to improve the adhesion of the film.

An exposure dose of 2500 mJ/cm$^2$ is used to make sure the material is over-exposed. Post-exposure bake is then performed firstly on a hotplate at 65 °C for 5 min followed by a second step in an oven at 130 °C for 30 min. Slow cooling down to the room temperature

is critical after the PEB. The wafer is left inside the oven to cool down, and this cooling process takes about 1 hour.

The wafer is then developed in PGMEA. The wafer is first immersed into a reusable bath of PGMEA for 20 min without agitation and then removed and immersed in a second fresh bath of PGMEA for another 5 min to remove residual. Drying of the wafer in-between the two baths should be avoided, otherwise, the wet-ability of the inner area of the ring structures can be reduced. The wafer is then rinsed by IPA and dried out on a hotplate at 50 °C. In the case of residuals being observed, an oxygen plasma clean at 400 Watt for 60 seconds is applied at low power and with a short time to avoid the thermal damage of the cross-linked SU-8 structures.



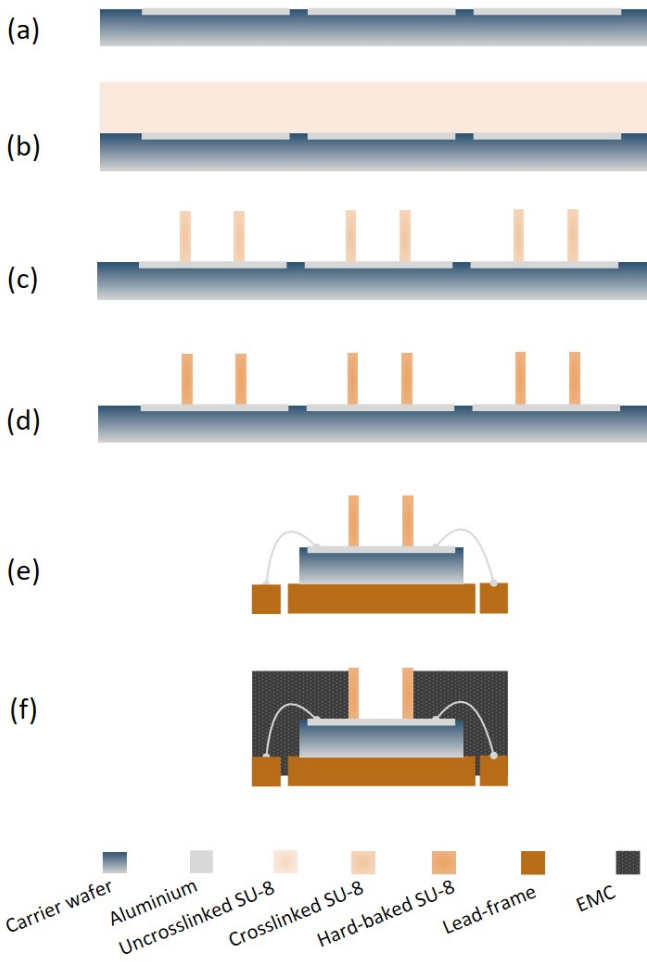



Figure 3.28: A detailed process flow of the TPVH-W-QFN process. (a) Al coating on bare silicon wafer. (b) Coating of thick SU-8 film. (c) The formation of hollow TPV structures. (d) Hard baking. (e) Assembly of the diced die to the QFN lead frame. (f) Film assisted molding.

The wafer is then hard-baked in an oven at 180 °C for 2 hours. After the hard baking, the wafer is ready to be diced and assemble to the QFN lead frames and then followed by wire bonding and molding. The process flow of the TPVH-W-QFN process is shown in Figure 3.28.

The SEM images in Figure 3.29 have shown the TPV fabrication results of a ring structure with a designed 150 µm inner diameter and 30 µm wall thickness. A 100% clearance of the inner area and 100 % adhesion is achieved. To avoid the charging effect of the SEM, the wafer is coated with a 250 nm thick Al layer.The 26° tilted view, see Figure 3.29 (b,d), shows a well-developed inner bottom surface and a vertical inner wall. The actual measured inner diameter is 133 µm and the wall thickness is measured as 40 µm. The expansion of wall thickness is caused by the heavy exposure and high PEB temperature which is applied to improve the adhesion. The wall thickness has a total expansion of 10 µm, and the expansion towards the inner circle is 8.5 µm leaving the expansion towards the outer circle only 1.5 µm.

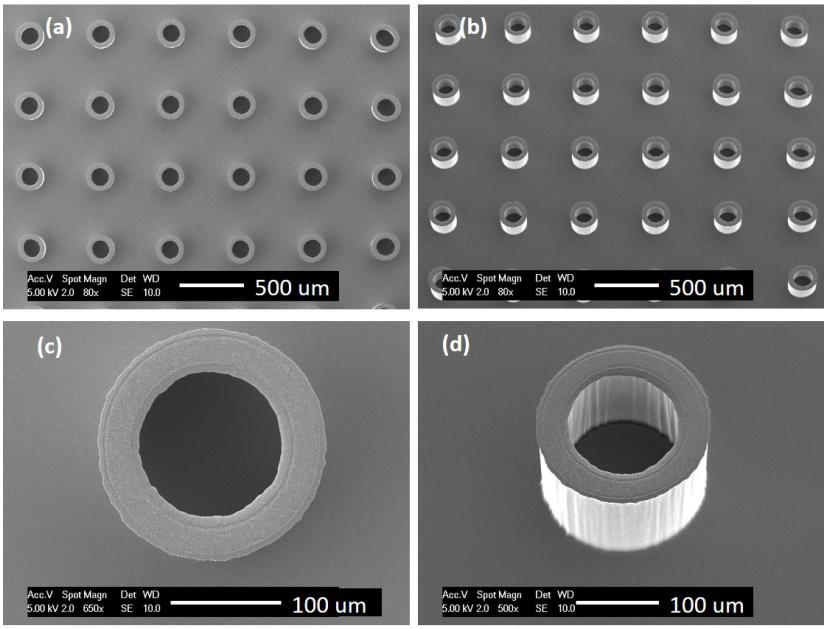



Figure 3.29: SEM images showing the fabrication results of hollow TPV structures with a inner diameter of 150 µm and a wall thickness of 30 µm. (a) Top view of TPV array. (b) Tilted (26°) view of TPV array. (c) Top view of a single TPV structure. (d) Tilted (26°) view of a single TPV structure showing clear inner wall surface and a clean inner bottom surface.

Because of the overexposure and the PEB at a higher temperature of 130 °C, the cross-linking reaction will expand towards the unexposed area. Since the inner circle is a closed area and the outer circle is an open area, the UV generated acid diffuses farther in the inner circle inducing correspondingly more cross-linking there.

The SEM images of multiple TPV ring structures, triangle shape, and square shape TPV hollow structures and the TPV ring structure with an inner pillar array are shown in

Figure 3.30. This demonstrates the flexibility of the TPV process. For example, multiple TPV ring structures on the same chip are suitable for the application where adjacent chip surfaces need to be kept free from EMC and at the same time, the cross-talk between them needs to be minimized, such as the inlet and outlet of a microfluidic package.

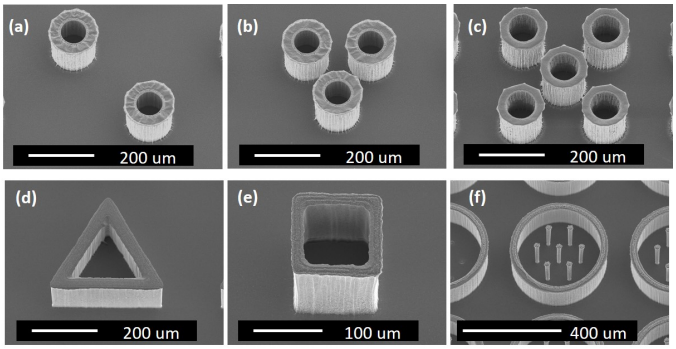



Figure 3.30: SEM images of the various designs of hollow TPV structures. (a-c) The fabication results of multiple TPV structures on a single die area. (d) The fabrication result of triangular hollow TPV. (e) The fabrication result of rectangular hollow TPV. (f) The fabrication result of hollow TPV structure with micro-pillars inside.

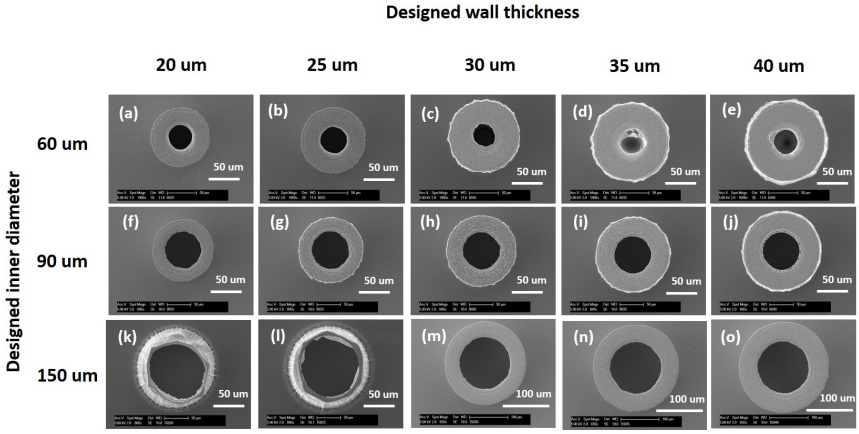



Figure 3.31: SEM images of fabricated TPV structures with different inner diameters of 60 µm, 90 µm, 150 µm, and different wall thicknesses of 20 µm, 25 µm, 30 µm, 35 µm, 40 µm. Image (d) and (e) show the poor clearance inside the ring of the TPVs with 60 µm inner diameter, and the wall thickness of 35 µm and 40 µm respectively. Image (k) and (i) show collapsed TPV structures with an inner diameter of 150 µm and a wall thickness of 20 and 25 µm respectively.

Various of combinations inner diameters and wall thicknesses are explored in the TPVH-W-QFN process. The fabrication results under SEM are shown in Figure 3.31. There are two different defects types observed. The first defect type is the poor clearance inside the inner circle of the ring structures. This occurs when the wall thickness

becomes more than 50% of the inner diameter, such as the ring structures with an inner diameter of 60 µm and wall thicknesses of 35 µm and 40 µm. Thinner wall thickness such as 20 and 25 µm shows a better clearance of the inner circle with the 60 µm diameter TPV ring structures.

The second defect type is the collapse of the ring structures. This defect is observed with ring structures which have an inner diameter of 150 µm and wall thicknesses of 20 and 25 µm which are below 20% of the diameter. However, structures with 400 µm diameter and 20 µm wall thickness have very good results where no sign of collapsing is observed. Thus the cause of the collapsing of these 150 µm inner diameter structures lies not only in the dimensions. Suspected causes are non-uniform coating thickness and non-uniformity of plasma cleaning power over the wafer.



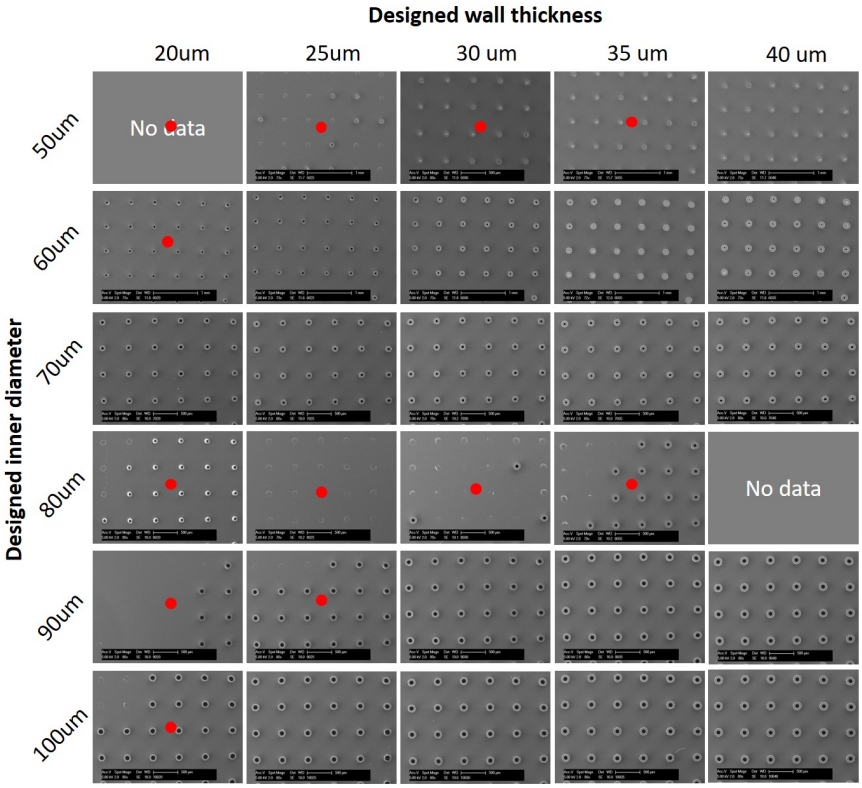



Figure 3.32: Adhesion map of the hollow TPV structures with different inner diameters and wall thicknesses. The images which are tagged by a red dot indicates the dimensions where poor adhesion of structures are observed.

Apart from collapsing and poor clearance of the inner circle, the adhesion of the ring structures is the third influencing factor to the yield. A map of adhesion of different diameter and wall thickness combinations is given in Figure 3.32. The SEM images of the TPV ring structures in the combinations of diameters from 50 µm to 100 µm with wall

thicknesses from 20 µm to 40 µm are shown in the adhesion map and the combinations that have poor adhesion are marked with a red dot. At the same diameter, the adhesion of the TPV structure increases with a thicker wall due to the increased bottom area. From the study of the adhesion map, the optimum combinations of inner diameter and wall thickness can be found.

### 3.6.3. ASSEMBLY AND MOLDING

After the TPV fabrication process, the wafer is then diced into single chips. In the TPVH-W-QFN process, chips of 500 µm by 500 µm with a thickness of 500 µm are obtained after dicing. The diced silicon chips are then picked and placed onto a QFN leadframe for 1 mm by 1 mm QFN packages. After the pick and place process, the lead frame is molded using the FAM process and the top side of the TPV ring structures are kept clean from EMC. Images of the silicon die with TPV ring structures assembled to the 1 mm × 1 mm QFN lead frame are shown in Figure 3.33 (a-c). The results after film assisted molding are shown in Figure 3.33 (d-f) and the cross-section view of the TPV through-holes, the silicon die, and the EMC are shown in Figure 3.33 (g-i).

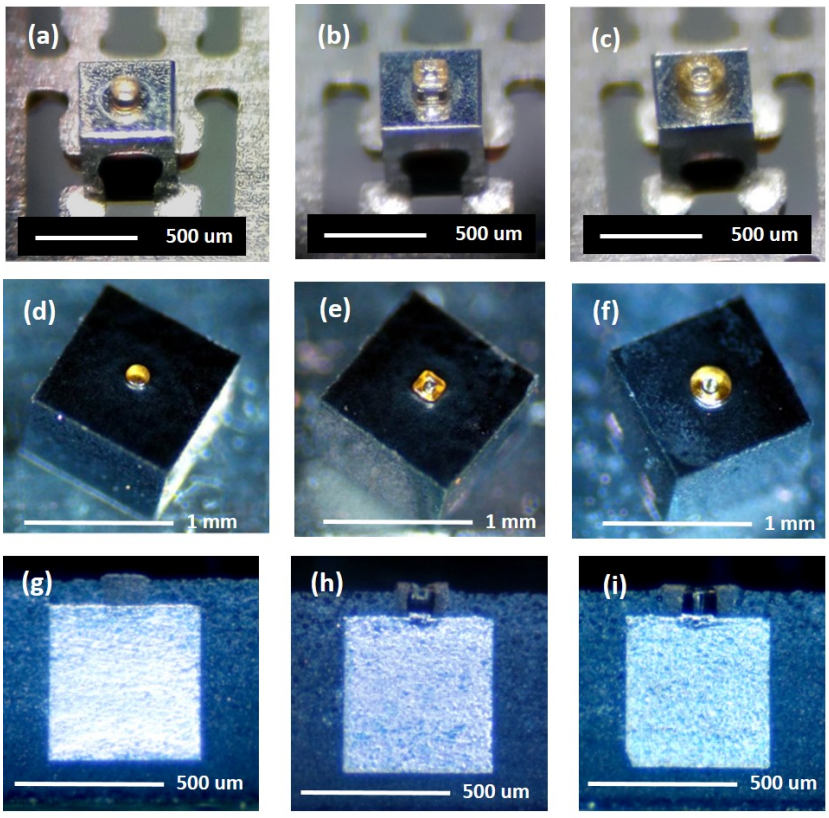



Figure 3.33: The results of assembly and molding process in TPVH-W-QFN. Images of the fabricated TPV dies (a-c), the molded 1x1 QFN packages with TPV through-hole (d-f) and the cross section of the molded package.

## 3.7. CONCLUSIONS

In this chapter, 4 different process cases of TPV technology, TPVM-C-QFN, TPVO-C-QFN, TPVH-NPCB, TPVH-W-QFN, targeting at four different application, RF, optical, LED display, and through-holes, are discussed. It has been proven that TPV technology has a broad range of application fields due to its unique features of the polymer core, metal coating, high aspect ratio, lithography defined structures with high resolution and precise positioning, excellent design freedom, and the capability of mass production. The 4 process cases have demonstrated the flexibility of TPV technology in the fabrication process on various substrates and by different coating techniques.



However, each process has its challenges which makes it a unique process compare with each other. In the TPVM-C-QFN process, since the TPVs are metalized and used as an electrical interconnection, the foot profile of the pillars where the metal coating connects to the bottom contact pad is optimized. Compare to other processes, the aspect ratio is higher and the pitch size of the TPVs is smaller in the TPVM-C-QFN process. In the TPVO-C-QFN process, the size of the structures is rather large and the concern here is to reduce the yellowing of the polymer and the stress after molding. As for the TPVH-N-PCB process, the yield of the TPVs on the PCB is the main focus since every PCB is a functional unit that contains more than 5000 TPVs and one failure of TPV means the failure of the entire PCB. In the TPVH-N-PCB process, the dimensions of the ring structures are rather large and the clearance of the inner circle is not an issue, however, in contrast, the TPVH-W-QFN process requires very small rings where the clearance of the inner circle is a challenge. In the TPVH-W-QFN process, various dimensions of structures are fabricated and both the adhesion and the clearance of the structures are the main issues to focus on.

All these process cases and applications developed in this work have shown that TPV technology is a very versatile technology for future advanced packaging. Besides the applications discussed in this chapter, there are more potential applications such as EMI shielding, microfluidic, thermal management, etc, further enabling heterogeneous integration.

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# 4

# MECHANICAL CHARACTERIZATION OF THROUGH-POLYMER VIA (TPV)

*The adhesion of polymer structures on the substrate is critical for the yield of the TPV process. The mechanical strength of TPVs under shear force is of great interest. The mechanical strength characterization of TPVs using shear tests provides insights for further optimizing the TPV structure and process.*

## 4.1. INTRODUCTION

In chapter 3, we have explored a wide application range of TPV technology. And for each type of application, a specific TPV process is developed, each with its specific challenges. The yield of TPV processes and their reliability are the key factors to promote TPV technology to be adopted by the semiconductor packaging industry. One of the major reliability issues during the TPV process is delamination. In this chapter, the mechanical strength characterization of metalized TPVs is carried out. The influence of factors, such as metal coating, pillar diameters, and shear heights, on the mechanical strength of the TPVs are discussed.

The delamination of TPVs can occur during several process steps where external forces are applied to the TPV structures, such as shear forces, which can directly cause the delamination. This can occur during development, contact mask aligner exposure, dicing, and molding. The source of forces originates from the flow of the developer generated by the solvent agitation, the capillary force during drying, the water jet applied during dicing, and the compound flow during molding. To characterize the resilience of TPV pillars against shear forces, conventional microelectronic packaging test equipment is applied. Shear testers are widely used in the microelectronic packaging field for determining the mechanical robustness of micro bonding structures such as solder balls or wirebonds [1–5].

## 4.2. FOOT PROFILE OF TPV

The adhesion of the TPV pillars on the substrate is one of the critical parameters to characterize the process quality. SU-8 polymer is known to have poor adhesion to various substrates such as silicon, gold, and glass [6–8]. A method like interlocking structures is proposed to improve the adhesion however increases the process complexity [7]. Research has been focusing on analyzing the influence of the lithographic process and baking procedures to the adhesion of the SU-8 microstructures [9–11].

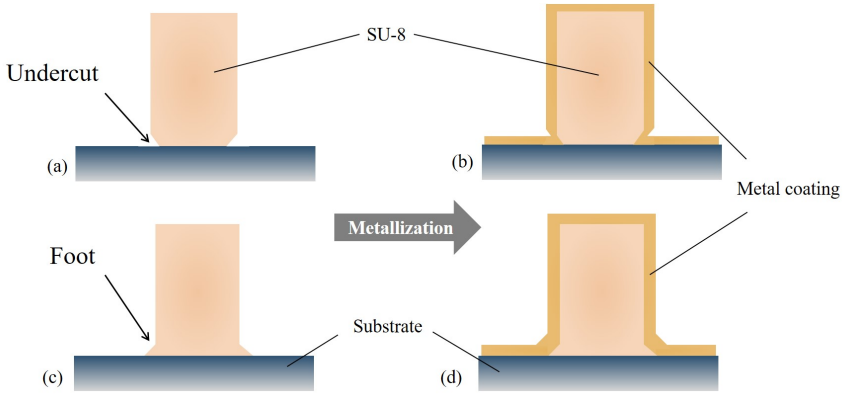


Figure 4.1: Schematic illustration of the undercut and foot profiles of SU-8 pillars and their metalization. (a) A SU-8 pillar with undercut profile at the substrate interface, (b) the metalization of a SU-8 pillar with the undercut profile, (c) a SU-8 pillar with the foot profile, (d) the metalization of a SU-8 pillar with the foot profile.

Surface treatment such as wet chemical etching of the native oxide layer on the silicon substrate can improve the adhesion [12], however not all material surfaces can be improved with the same method. Furthermore, the dimensions of the designed SU-8 structures also have an impact on the adhesion. Larger structures can suffer from more internal stress and cracks can occur that reduces adhesion and feature integrity [13, 14]. However, the stressful and poor adhesion nature can be used as a method for fabricating free-standing layer of SU-8 in combination with an ultrasonic treatment [15]. Also, the mechanical strength of fabricated SU-8 structures is influenced by environmental factors such as moisture [16].

In the TPV process, the profile of the interface between the TPVs and the substrate has a significant influence on the adhesive strength. We investigated two different interface profiles of the SU-8 resist as shown in Figure 4.1, including the undercut profile with a smaller footprint and the foot profile or "elephant foot" with a larger footprint. Photoresist footing is an unwanted feature in most of the conventional applications. The function of photoresist as a masking layer during the etching and patterning process requires it to be accurate in dimensions. Photoresist footing has a negative influence on the accuracy of the patterned line width hence research effort has been invested in the elimination of resist foot. However, in the case of TPV technology, when the SU-8 negative resist is used as the structural material for forming a metalized polymer pillar, the resist foot becomes an advantage. A SU-8 pillar with a controlled foot profile has not only improved mechanical stability but also better metal film coverage to the pillar sidewall at the bottom which is key for connection of contact pads.



For a chemical amplification resists (CAR), such as SU-8, the resist profile is determined by the cross-linking reaction during PEB. To clearly define the cross-linking reaction, the acid loss reaction and the acid diffusion need to be considered. A cross-linking reaction model of the chemically amplified negative resist was given in [17]. The model was further developed by also taking the acid evaporation during the PEB process into account. Experiment with SU-8 resist was used to validate the modeling [18, 19]. The cross-linking reaction was measured using PAGA-100 cross-linking reaction parameter measurement system (manufactured by Litho Tech Japan). The PAGA-100 system consists of an FT-IR spectrometer, exposure tool, a base plate, and a measurement chamber. The absorbance of a given wavelength by the functional group caused by the cross-linking reaction can be extracted from the spectral data to obtain the cross-linking ratio as a function of PEB time. There are two parts of the cross-linking reaction, cross-linking occurred during exposure and cross-linking occurred during PEB. Based on the Lambert-Beer Law [20], the concentration of the initiator, triarylsulfonium hexafluoroantimonate salts, is approximated and expressed in equation 4.1, as follows:

$$\frac{\partial[Triarylsulfonium]}{\partial t} = -K_{photo} I[Triarylsulfonium] \tag{4.1}$$

where $[Triarylsulfonium]$ is the normalized concentration of the triarylsulfonium initiator and $K_{photo}$ is the reactive constant of triarylsulfonium salt during exposure. $I$ is the light intensity. Based on the integral of equation 4.1, the normalized concentration of the remaining initiator can be obtained. Next, the normalized generated acid concentration, which is approximated as the same of the reacted initiator, can be expressed in

equation 4.2 below,

$$[H^+] = 1 - exp\left(-K_{photo} Dose\right) \tag{4.2}$$

*Dose* is the exposure dose. $[H^+]$ is the normalized acid concentration. The cross-linking only due to the exposure leads to a cross-linking ratio of around 9%.

The PEB process is responsible for most of the cross-linking, more than 90%, and reaches ultimately 100% given sufficiently high PEB temperature and long enough PEB time. The reaction during PEB is expressed in equation 4.3 and 4.4, as follows:

$$\frac{\partial [H^+]}{\partial t'} = -K_{loss}[H^+] + D_{acid}\nabla^2[H^+] \tag{4.3}$$

$$\frac{\partial [S_{ci}]}{\partial t'} = -K_{ci}[H^+][S_{ci}] \tag{4.4}$$

In this case, $[S_{ci}]$ is the normalized concentration of the reactive groups in the cross-linking agent, $[H^+]$ is the acid concentration, $t'$ is the PEB time, $K_{ci}$ is the cross-linking reaction constant, $K_{loss}$ is the constant corresponding to deactivation of the acid in the PEB process, and $D_{acid}$ is the acid diffusion constant. Constants $K_{ci}$, $K_{loss}$ and $D_{acid}$ are functions of temperature and the Arrhenius equation can be used to approximate these constants, as shown in equations 4.5, 4.6, 4.7 below:

$$K_{ci} = K_{0(ci)} exp\left(\frac{-E_{a(ci)}}{RT}\right) \tag{4.5}$$

$$K_{loss} = K_{0(loss)} exp\left(\frac{-E_{a(loss)}}{RT}\right) \tag{4.6}$$

$$D_{acid} = D_{0(acid)} exp\left(\frac{-E_{a(acid)}}{RT}\right) \tag{4.7}$$

Based on the above model, it was found that the profile of SU-8 structures is largely influenced by the PEB temperature. The profile changes from an undercut profile to a foot profile from PEB temperature of 65 $C^\circ$ to 125 $C^\circ$. The higher the PEB temperature is, the larger the foot is. However, at a temperature higher than 125 $C^\circ$, the bridging of the top edge of SU-8 structures is observed. In the SU-8 photoresist, the photoinitiator triarylsulfonium hexafluoroantimonate salts generate a low concentration of strong acid. The hydrogen ion provided by the acid initiates the chain reaction (Figure 2.2).

To obtain a foot profile, instead of using a PEB temperature of 95 °C as most of the SU-8 data sheets suggest, we practiced a PEB temperature at 110 °C. High-resolution SEM images of the TPVs with undercut profile and foot profile are shown in Figure 4.2. For an undercut profile, the surface below the undercut is in the shadow for the sputtered metal atoms which results in a very thin metal coating at the connecting bottom area or even an open gap. On the other hand, the foot profile has an obtuse angle at the foot where a continuous and uniform sputtered metal deposition can be achieved. To achieve a robust mechanical connection as well as a better electrical connection with lower contact resistance, the foot profile is preferred.

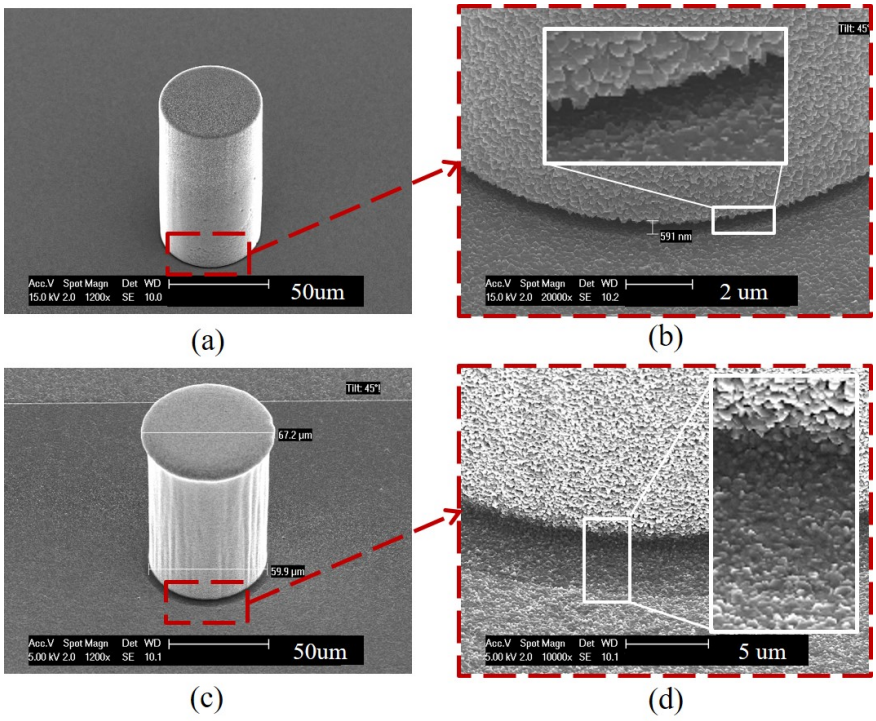


Figure 4.2: SEM images of metallized TPVs with undercut profile and foot profile.(a) The metallized pillar with a undercut profile. (b) The zoomed-in view at the bottom undercut interface which shows a discontinuity of the metallization. (c) The metallized pillar with a foot profile. (d) The zoomed-in view of the pillar foot which shows a continuous conformal coating of metal.



### 4.2.1. TEST SAMPLE PREPARATION

For the mechanical characterization of the metalized TPVs, TPVs with different diameters and multiple metal coating thickness are fabricated on a silicon wafer. The height of the TPVs is 100 um and the metal coating thickness ranges from 1.4 µm to 5.6 µm. Considering the conductivity of the TPV and the skin effect when working at mm-wave frequencies, an aluminum coating of several micrometers is chosen. It is sufficiently thick to provide good electrical connectivity and is thicker than the skin depth which is around a few hundred nanometers for Al at mm-wave frequencies.

The sample preparation follows the process flow as shown in Figure 4.3. The process parameters developed in the TPVM-C-QFN process for obtaining a foot profile is used here to maintain the same process condition. The process starts with the fabrication of alignment markers on the 4-inch test wafers. Since in the TPVM-C-QFN process, the TPVs are fabricated over Al contact pads, the test wafers used here are also sputtered with a 1 µm thick Al(1%Si) at 350 °C to make sure the same substrate condition is met. A dehydration bake is performed before the SU-8 coating to remove surface moisture and improve the adhesion. Spin coating is used to deposit a uniform layer of 100 µm thick SU-8 polymer onto the wafer. Soft baking is done on a horizontal hotplate at 95 °C for 5

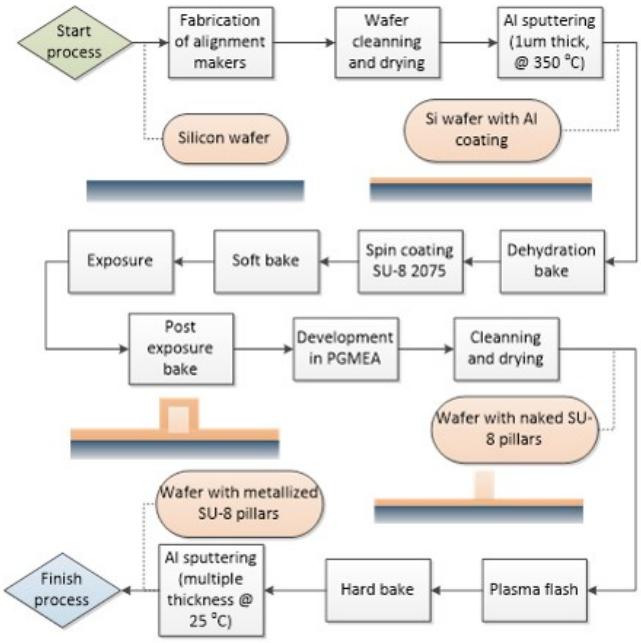


Figure 4.3: Process flow of the metalized TPVs samples used in the shear test.

min and 120 °C for 25 min. The exposure dose is set at 780 $mJ/cm^2$ on an EVG 420 mask aligner with an intensity of around 13 $mW/cm^2$ and an exposure time of 60 s. The post-exposure bake is carried out at 65 °C for 5 min, then 95 °C for 5 min and eventually 110 °C for 10 min. The wafers are cooled down to 65 °C in about 10 min. The development is performed in PGMEA solvent for 20 min. After the development, the wafers are cleaned with IPA and dried on a hotplate at 50 °C. An oxygen plasma flash is carried out afterward to remove remaining residues. A vacuum hard baking process is necessary to degas the SU-8 material and further cross-link before the metallization. The hard bake is carried out at 180 °C for 2 hours. Finally, a multi-layer Al sputtering is done at 25 °C to reach the targeted thickness.

### 4.2.2. DIAMETER EXPANSION

To obtain the foot profile of the fabricated SU-8 polymer pillars, the PEB is carried out at a higher temperature that causes the expansion of the fabricated pillar diameters, as mentioned in the previous chapter. The measured average diameters of the 20 µm, 50 µm, and 100 µm designs are 31 µm, 66 µm, and 121 µm respectively. The expansions in the radius are 5.5 µm, 8 µm, and 10.5 µm respectively. The diameter measurement results using an optical microscope are shown in Figure 4.4. The box plot in Figure 4.4 (d) shows the distribution of the measured TPV diameters and the averaged expansion of diameters. In the following discussions, the measured average value of diameter, 31 µm, 66 µm, and 121 µm, will be used to refer to the TPVs in general.

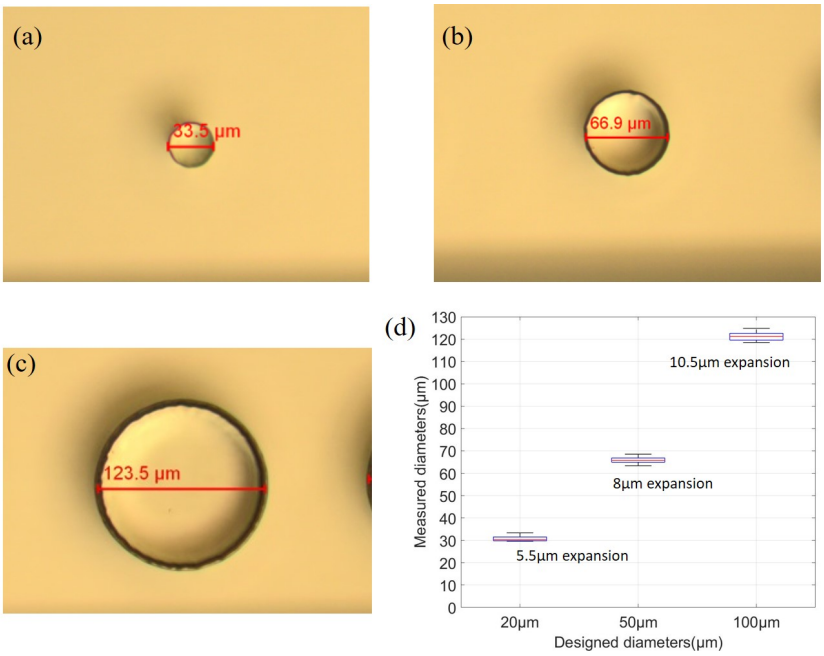


Figure 4.4: Measurement pillar diameters under optical microscope. (a-c) Examples of the measurement on TPVs with designed pillar diameters of 20 µm, 50 µm, and 100 µm, respectively. (d) The measurement results of the distribution and average value of the pillar diameters over 6 process wafers and the calculated average expansion of the diameters.

## 4.3. SHEAR CHARACTERIZATION

### 4.3.1. TEST CONDITIONS

To measure the shear force of the TPVs, a Dage 4000 bond tester system is used. The shear test mechanism, the tool head, and the metalized TPVs are shown in Figure 4.5. The speed of the tool head is set at 5 µm/s and the movement is made in approximately 0.2 µm per step every 50 ms. In about every 2 ms, a measurement of the applied force is performed. The measured shear force values are in the unit of gram*force and can be transformed to mN by multiplying 9.81. The shear tester has a detection threshold around 0.5 gram*force above which the recording starts and the displacement is set to zero. The height of the shear tool head was set to 3 different values, 10, 45, 80 µm, above the substrate surface to study the influence of the shear height to the mechanical strength of the TPVs.

### 4.3.2. SHEAR RESPONSE OF TPV

Due to the elevated PEB temperature, the pillar profile not only has a footing but also a "mushroom head". Consequently, the shear process can be divided into three stages, contacting the "mushroom head", fully contacting the pillar body, and delamination of the pillar. The schematic illustration of the process of TPV's shear response is shown in Figure 4.6 (a-c). And an example of the measured shear response of a pillar without

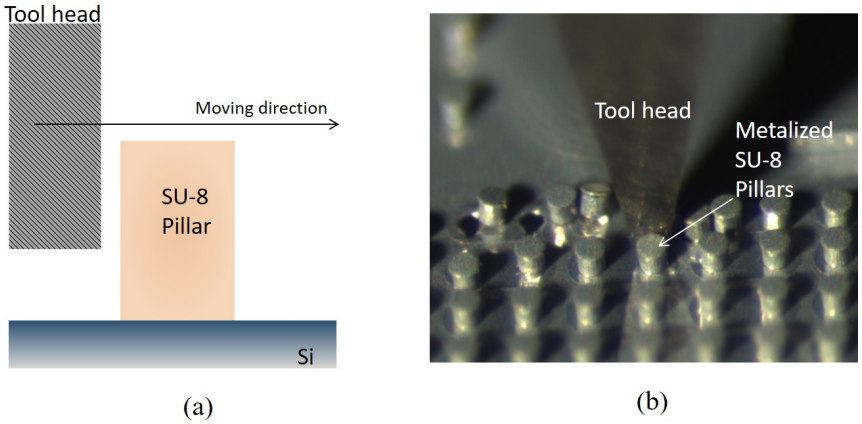


Figure 4.5: The working mechanism of a shear tester. (a) Schematic illustration of the shear tool head and the SU-8 sample under test. (b) Optical microscope view of shear tool head and metalized TPVs under test.

metal coating is shown in Figure 4.6 (d).

The measured shear force against the displacement curve has 2 linear parts, a slight slope at the beginning (region I) and a steep slope after a certain displacement value (region II). When first touching, the tool head is only in contact with the "mushroom head". Hence, upon displacement, the pillar will slightly bend until the tool head is in full contact with the pillar and then the full shear force will develop. Therefore, the "mushroom head" is responsible for the shear response in region I, and the pillar body is responsible for the shear response in region II. As the displacement increases, the shear force applied increases and reaches a peak value and then abruptly drops down to almost zero. This peak point of the shear force is the point where the TPV delamination occurs.

Furthermore, because the shear tester system has a detection threshold of around 0.5 gram*force, the displacement is recorded as zero when 0.5 gram*force is first measured. Hence, the displacement before reaching the detection threshold is not recorded. Therefore, there is an offset in the absolute displacement values. A shear tester with a lower detection threshold is required for obtaining more accurate absolute displacement values. In this work, we focus on the change of shear forces and the maximum shear force values.

### 4.3.3. SHEAR FAILURE SITES

SEM images of the fabricated metalized TPVs with different Al coating thickness and their failure site after sheared at a height of 10 µm are shown in Figure 4.7. The different thicknesses on the SU-8 pillars measured after the depositions are 1.4, 1.9, 3.8, 4.5, and 5.6 µm. The measurement of the coating thickness of the pillars is based on the change of the diameter measured under optical microscopes.

With a thin Al coating thickness of 1.4 µm, the TPVs with all three diameters break off at the bottom interface with little SU-8 residual. However, with an increasing Al coating thickness, SU-8 polymer residuals are found on the failure sites. This is because the SU-8

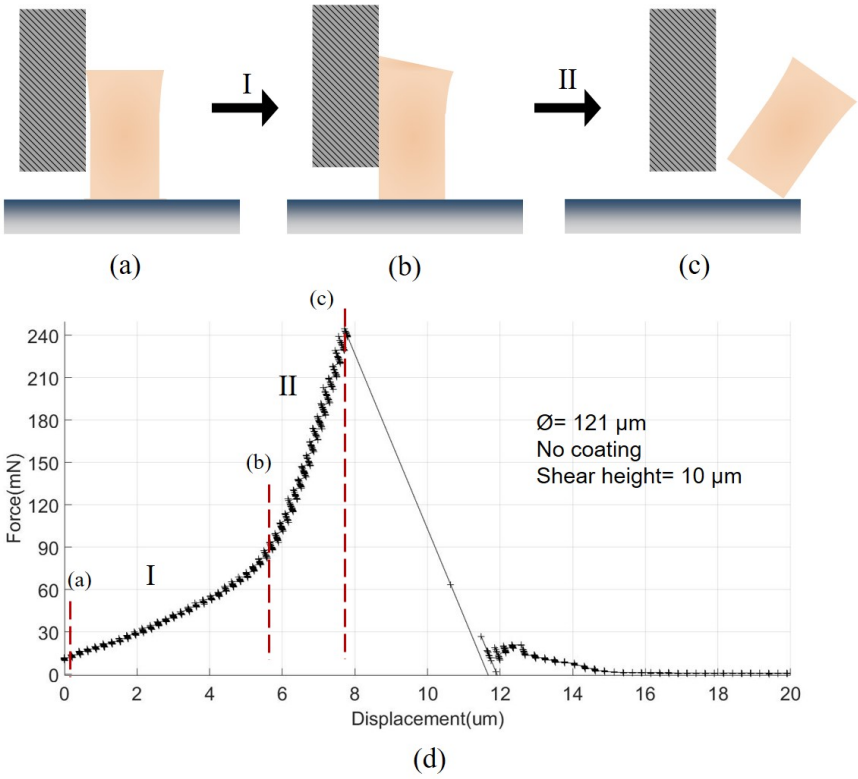


Figure 4.6: The schematic illustration of the shear process of TPV. (a) The shear tool head is touching the pillar's "mushroom head". (b) The shear tool head is in full contact with the pillar. (c) The shear tool head delaminates the pillar. (d) An example of the shear response curve of an individual pillar which demonstrates two different shear response regions, region I and II, that are corresponding to the transition from (a) to (b) and (b) to (c).

polymer foot substrate interface is lower compared with the metal layer deposited after pillar formation and hence the constraint applied by the metal layer moves the highest stress point upward and away from the bottom interface. The pillar suffers more stress at a region above the bottom interface which causes the cracking and breaking off of the polymer core. Thus the failure mechanism shifted from interface delamination towards SU-8 cracking and breaking with an increasing Al coating thickness. This phenomenon is more pronounced with small diameter TPVs.

### 4.3.4. INFLUENCE OF METAL COATING TO THE SHEAR STRENGTH OF TPVS

In this section, the influence of the Al coating to the shear response of the SU-8 pillars is discussed. The measurement results of the shear response of TPVs without coating and with 4.5 µm Al coating are compared in Figure 4.8. Examples of the shear response of individual TPVs are plotted in Figure 4.8 (a-c).

As shown in the shear response curves, the first linear slope (region I) is the shear

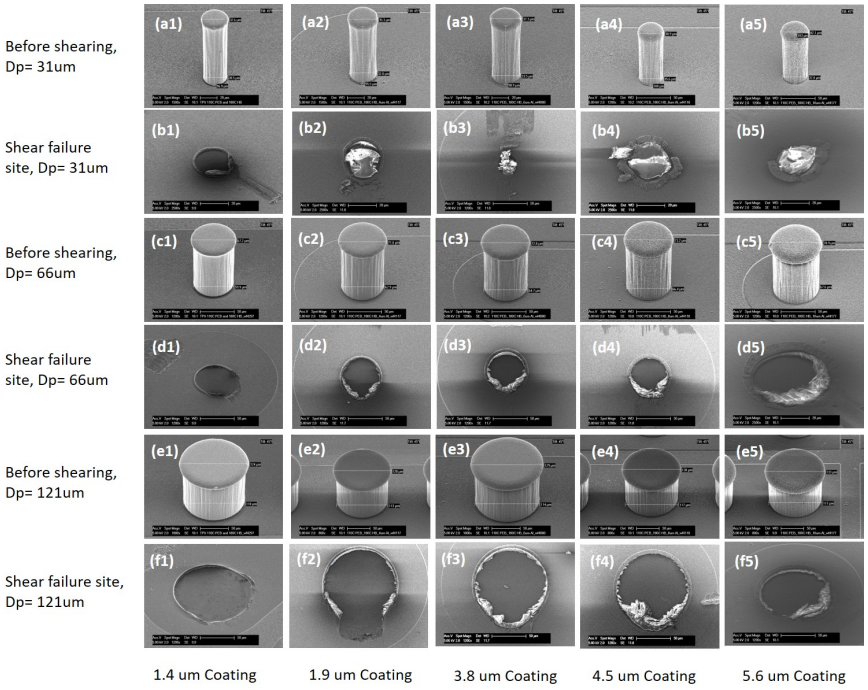


Figure 4.7: SEM images of metalized TPVs and their shear sites (the shear height is 10 µm). The fabricated metalized TPVs with different Al coating thicknesses with a diameter of 31 µm (a1-a5), 66 µm (c1-c5), and 121 µm (e1-e5), and the shear sites of the metalized TPVs with different Al coating thicknesses with a diameter of 31 µm (b1-b5), 66 µm (d1-d5), and 121 µm (f1-f5).

response of contacting the "mushroom head", and the second linear slope (region II) is the shear response of the full contacting. For the pillar with a diameter of 31 µm, the "mushroom head" is very small and results in a shear response curve with only the second linear region.

As a result, the maximum shear forces of the pillars are largely increased by the metal coating. The shear response in the linear region I is dominated by the metal coating on the "mushroom head" which shows an increased mechanical resistance. The influence of the metal coating to the gradient of region II is less significant because the bending of the polymer core still dominant the mechanical response when the pillar is fully contacted. Furthermore, the maximum shear forces for all pillars were measured in region II. Hence, the delamination of all pillars occurred when the shear tool head was in full contact with the pillar body.

Other than the uncoated TPVs, the shear forces measured after the delamination of the metalized TPVs have none-zero values. The breaking off of the uncoated TPVs from the wafer surface is abrupt and because of the elastic energy stored in bending of the pillar, once delaminated, the pillar "jumps" away from the failure site and the shear force drops suddenly to zero. However, in the situation of a metalized TPVs, the process of the failure includes both the delamination of the polymer to the bottom surface and

the breaking off of the Al layer. The process of breaking off of the metal layer ranges over a larger distance thus dragging the TPVs away instead of "jumping" away. This also caused the delamination of the 31 µm diameter pillars with a metal coating not visible in the shear response curve because there is no sudden drop of the shear force. For these cases, the highest data point which follows the linear region II gradient is chosen as the delamination point of the pillar.



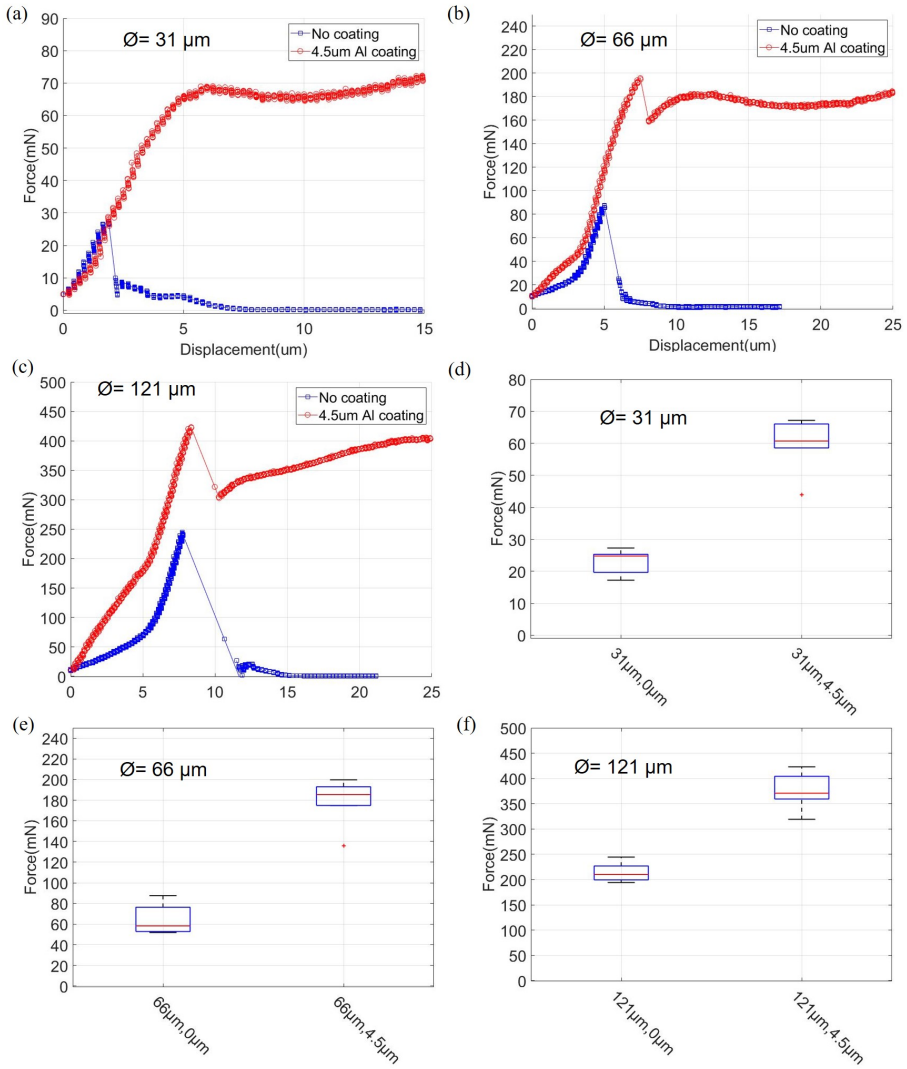


Figure 4.8: The comparison of the shear response of TPVs without coating and with 4.5 µm thick Al(1%Si) coating. The pillar diameters are 31 µm, 66 µm, and 121 µm. The shear height is 10 µm. (a-c) The shear force response measured against displacement, (d-f) box plots showing the max shear force distribution over multiple measurements.

The average values and the distribution of the max shear forces which indicates process variations are shown in Figure 4.8 (d-f). As the results show, the maximum shear force has increased from an average value of 25 mN to 61 mN for the diameter of 31 µm, 59 mN to 185 mN for the diameter of 66 µm and 210 mN to 370 mN for the diameter of 121 µm which are 144%, 213%, and 76% increase respectively.

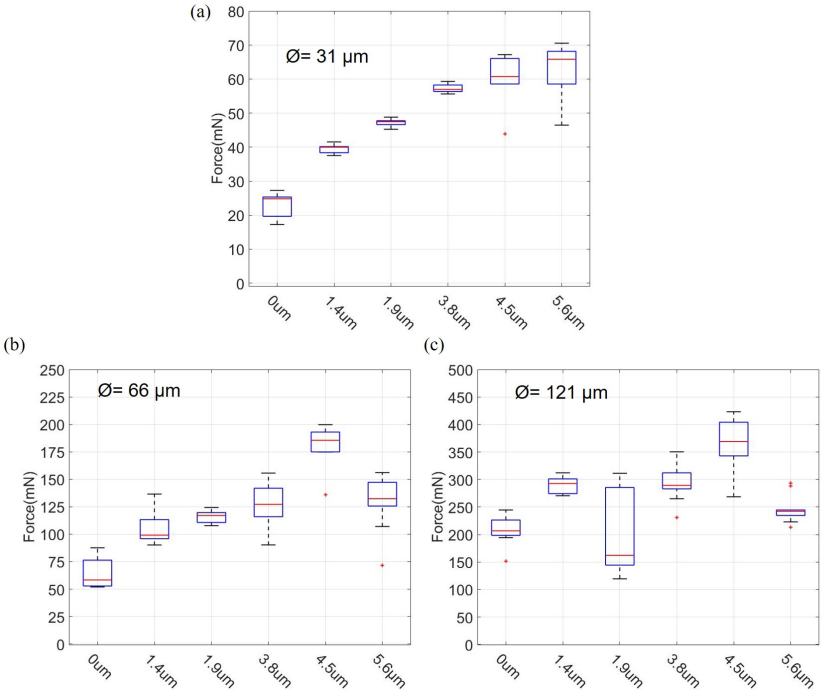


Figure 4.9: Boxplots of the distribution and average of the maximum shear forces of TPVs with different metal coating thicknesses. (a) TPVs with diameter of 31µm, (b) TPVs with diameter of 66 µm, (c) TPVs with diameter of 121 µm. The values of x axis ticks are the metal coating thickness

Boxplots of the distribution and average of the maximum force for 31 µm, 66 µm, and 121 µm diameter TPVs with different metal coating thicknesses are shown in Figure 4.9. For all 3 diameters, the maximum shear force increases with a thicker metal coating up to 4.5 µm but decreases with 5.6 µm thick coating, especially for the TPVs with diameters of 66 µm and 121 µm. Obviously, a thicker metal coating provides stronger support for the polymer core and requires more force to break off the pillar. However, the Al deposition process is also a temperature cycling process. The TPVs which are coated with thicker layers of Al is under more temperature cycles. Interfacial stress induced by thermal expansion can cause cracking or delamination at the polymer-metal interface which can potentially reduce the adhesion strength. Consequently, the TPVs with 5.6 µm thick Al(1%Si) coating showed a lower maximum shear force compared to TPVs with 4.5 µm thick coating. Furthermore, the mechanical enhancement by metal coating has a more significant effect on pillars with smaller diameters.

### 4.3.5. INFLUENCE OF PILLAR DIAMETERS TO THE SHEAR STRENGTH OF TPVS

In this section, the influence of the pillar diameter on the shear strength of the TPVs is discussed. The measured shear force against displacement and the calculated shear stress against the strain of the uncoated TPVs of 3 different diameters, 31 µm, 66 µm, and 121 µm, are plotted in Figure 4.10 (a, b). The shown response curve are examples based on individual TPV measurement.

The maximum shear force of the TPVs with 31 µm diameter is around 27 mN reached at a displacement of 1.9 µm. As mentioned before in section 4.3.2, the absolute displacement value has an unknown offset due to equipment limitation. As the diameter of the pillar increases, both the maximum shear force and the maximum displacement increases. For the TPVs with a diameter of 66 µm, the failure point measured is (87 mN, 5 µm) and for the TPVs with a diameter of 121 µm, the failure point measured is (245 mN, 8 µm). Furthermore, due to the larger "mushroom head" of the larger diameter pillars, the transition from the linear region I to linear region II also occurs at a larger displacement.



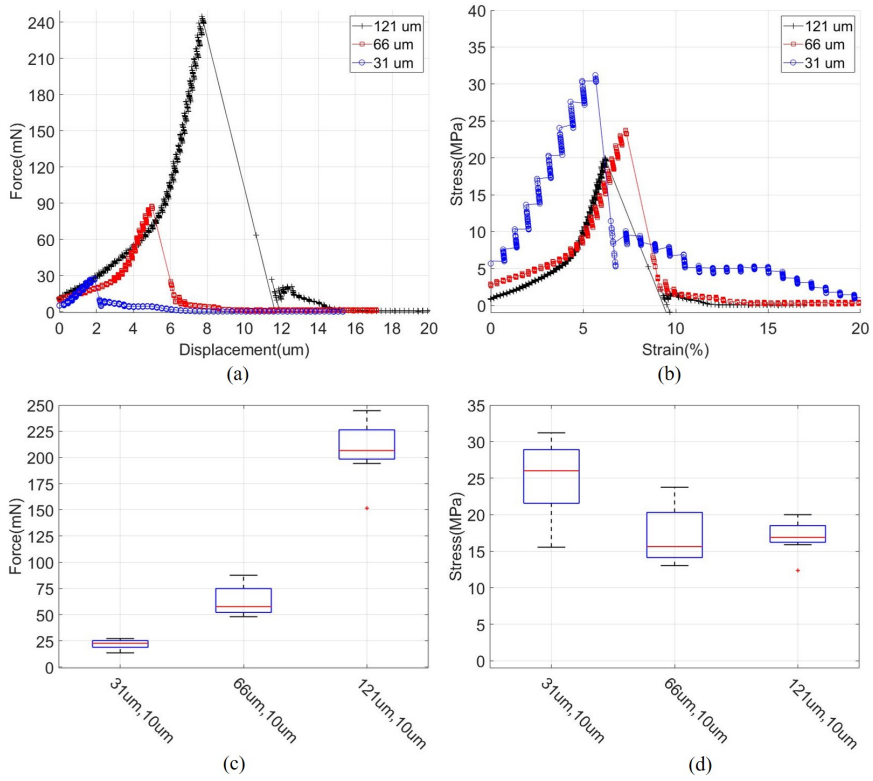


Figure 4.10: The influence of the pillar diameter to the shear strength of the uncoated TPVs. The shear height is 10 µm. (a) The shear force against displacement, (b) the shear stress against strain, (c) the distribution and average of max. shear forces, (d) the distribution and average of max. shear stress. For the box plots, on the x-axis, the first dimension is the TPV diameter and the second dimension is the shear height

The shear stress is obtained by dividing the shear force with the bottom area of the TPVs and the strain is obtained by dividing the displacement values with the diameter of the TPVs. The distribution and average of the maximum shear force and stress of uncoated TPVs with different diameters at a shear height of 10 µm are plotted in Figure 4.10 (c,d). As the results show, the maximum stress decreases with an increasing pillar diameter. This is because of the larger internal stress at the pillar substrate interface with a larger pillar diameter.

### FEM SIMULATION

Finite element matrix (FEM) simulations are performed with COMSOL Multiphyisics to model the shear process of the uncoated TPVs. The geometry of the 3D model is shown in Figure 4.11. To obtain and control the 3D geometry of the SU-8 pillar, a Bezier polygon is defined on a 2D plane first. And by revolving the 2D sketch, the 3D geometry of the pillars is obtained. Since SU-8 is a negative photoresist, the pillars fabricated are tapered which have a smaller diameter at the bottom and a larger diameter at the top. This tapered feature is also included in the geometry of the 3D model. Another modification of the geometry of the 3D model is the curvature of the sidewall. By adding curvature to the sidewall, the geometry of the TPV obtains a shape of "mushroom head", as shown in Figure 4.12.

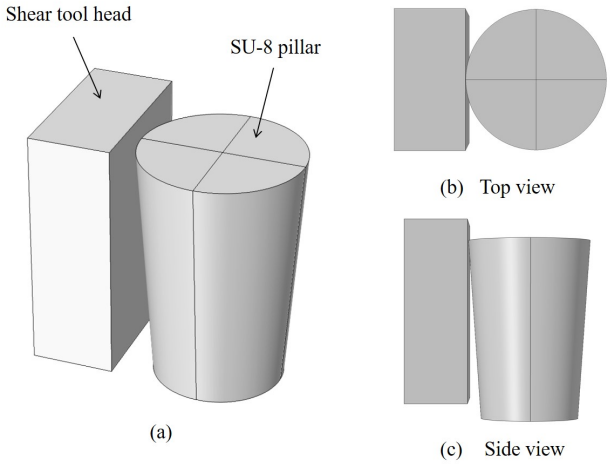


Figure 4.11: 3D models used in the FEM simulation in COMSOL. (a) The SU-8 pillar and the shear tool head. The shear tool head is in contact with the SU-8 pillar. (b) Top view showing the tool head and the top side of the SU-8 pillar. (c) Side view showing the tool head and the side profile of the SU-8 pillar.

The curvature of the sidewall is defined by a quadratic segment of the Bezier polygon. The quadratic segment is controlled by 3 points and by adjusting the height of the middle point, the curvature is tuned. Figure 4.12 (a) shows the tapered 3D geometry when the sidewall is a straight line. Figure 4.13 (b) shows the 3D geometry with a middle point of the quadratic segment set to a height of 50 µm and Figure 4.13 (c) is with the middle point set to a height of 85 µm. 3D geometry of the modeled 3 different diameters of

pillars is shown in Figure 4.13 (d-f). In Table 4.1, the parameters which control the profile of the 3D geometry are given for the pillars with 3 different diameters. $Diameter\_top$ defines the top diameter size of the pillars which are measured values from the same process wafer with uncoated TPVs, while $pillar\_bs$ controls the reduction of the bottom radius which determines the "mushroom head" size and sets the displacement value of the region I and region II transition. Here, "bs" stands for bottom shrinkage. Another parameter is the $Bezier\_h$ which controls the sidewall curvature of the pillars.

Table 4.1: The parameters used in the COMSOL model to define the pillar geometries

| Diameter_top (µm) | pillar_bs (µm) | Bezier_h (µm) |
|---|---|---|
| 33.4 | 2 | 0 |
| 68.5 | 5.5 | 50 |
| 124.8 | 7.5 | 85 |



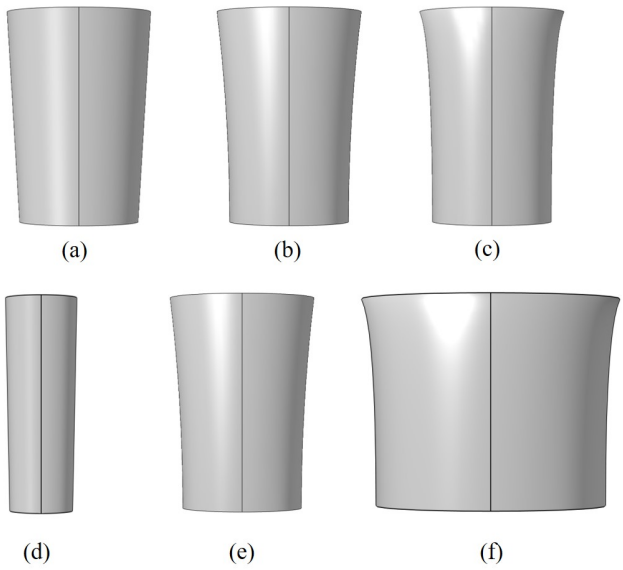


Figure 4.12: 3D models of SU-8 pillars with different sidewall curvature controlled by setting the middle point height of a quadratic segment. (a) Geometry of 68.5 µm diameter pillar with a Bezier_h value of 0 µm, (b) Geometry of 68.5 µm diameter pillar with a Bezier_h value of 50 µm, (c) Geometry of 68.5 µm diameter pillar with a Bezier_h value of 85 µm. (d-f) The corresponding pillar geometries of the 3 different diameters used in the simulation.

As for the material properties used in the simulation, the tool head is made of steel which has Young's modulus of 200 GPa and a Poisson's ratio of 0.3. The Young's modulus of the SU-8 is defined as 3.2 GPa and the Poisson's ratio is 0.33, which are from the COMSOL material library. As for the boundary conditions, the bottom surface of the SU-8 pillar is defined with a fixed constraint condition where the velocity equals zero. And

the two touching surfaces on the tool head and the SU-8 pillar are defined as a contact pair. During the FEM simulation, the displacement of the tool head is pre-defined and swept. And at each step of the displacement sweep, the force applied at the interface of the SU-8 pillar and the tool head is calculated. The displacement step size used in the simulation is 0.2 µm which is the same as the step size of the shear measurement setup.

The simulation results of the shear force response of the pillars with 3 different diameters are plotted in Figure 4.13 together with measurement results. Due to the offset in the measured displacement values, the displacement from the simulation results is shifted to match with the measurement. The simulated displacement value is shifted to zero when the simulated shear force reaches a value that is close to the measurement threshold. The delamination of the pillar is not simulated here. Larger diameter pillars possess larger "mushroom head", however, the shear response result from the "mushroom head" is not responsible for the failure point of the shear test. For all pillar diameters, the failure point is observed as the tool head of the shear tester is in full contact with the pillars, hence the shape of the pillar head is of less influence of the delamination of the pillar.



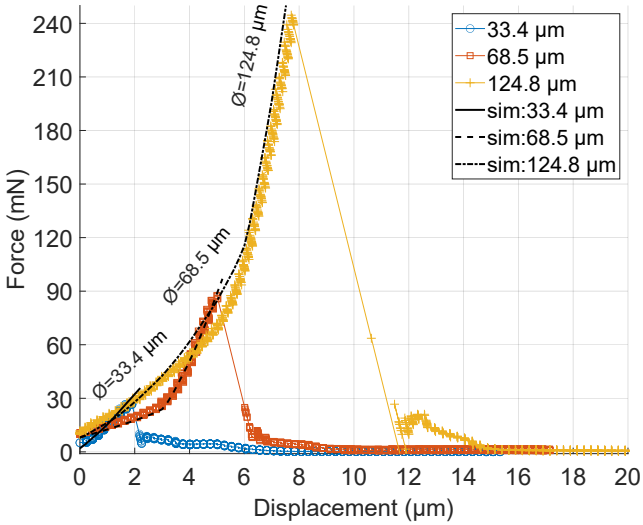


Figure 4.13: The comparison of the measurement and simulation results of the shear response of the uncoated pillars with diameters of 33.4, 68.5, 124.8 µm at a shear height of 10 µm.

The stress distributions developed at the pillars' bottom when the delamination occurs for uncoated TPVs with diameters of 33.4, 68.5, and 124.8 µm are shown in Figure 4.14. These simulation results are selected by using the measured displacement value at which the maximum shear force is reached. The stress developed on the bottom surface of the SU-8 pillar shows a similar distribution for all diameters where the edge on the side of the tool head reaches the maximum stress level of 326 MPa, 360 MPa, and 516 MPa for diameters of 33.4, 68.5, and 124.8 µm, respectively.

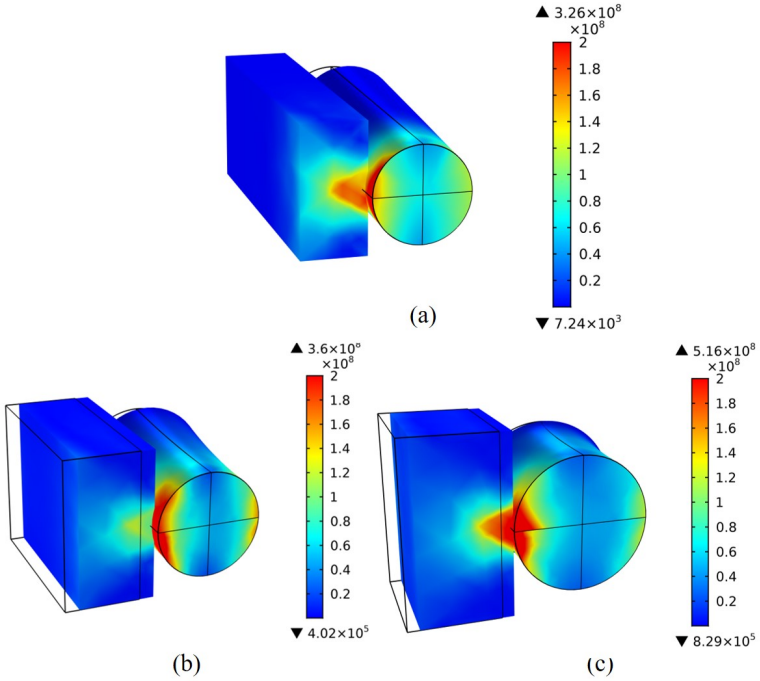


Figure 4.14: 3D simulation results of the stress distribution at the bottom of the SU-8 pillars at the failure points. The shear height is 10 µm. (a) The bottom stress distribution of the SU-8 pillar with a diameter of 33.4 µm, (b) the bottom stress distribution of the SU-8 pillar with a diameter of 68.5 µm, (c) the bottom stress distribution of the SU-8 pillar with a diameter of 124.8 µm.

### 4.3.6. INFLUENCE OF SHEAR HEIGHTS TO THE SHEAR STRENGTH OF TPVS

Until now, only the results of measurements and simulations with a shear tool height of 10 µm are discussed. However, the study of the influence of shear height can help to better understand the weakest point of the TPV pillars. Therefore, shear forces are measured at three different shear heights 10 µm, 45 µm, and 80 µm. Since the shear force value of the TPVs with 31 µm diameter at shear height of 45 µm and 80 µm is below the sensitivity of the tool, no useful data can be measured and thus we focus on the measurement of diameter 66 µm and 121 µm.

Measurement results of force against displacement and stress against strain at different shear height are shown in Figure 4.15. For both diameters, as the shear height increases, the gradient of the linear region II of the curve decreases. However, the increase of the shear height value does not influence the linear region I. As already described, this is mainly caused by the "mushroom head" of the TPV structures. Independent of the die shear tool's height, the tool head always contacts the mushroom head first. Thus, for the same pillar diameter, the linear region I is the same for all shear height cases.

The maximum shear force of the TPVs with 121 µm diameter drops from 241 mN to 230 mN at a shear height of 45 µm and 210 mN at the shear height of 80 µm. A nearly 12% of the original maximum shear force is reduced at a shear height of 80 µm. On the other

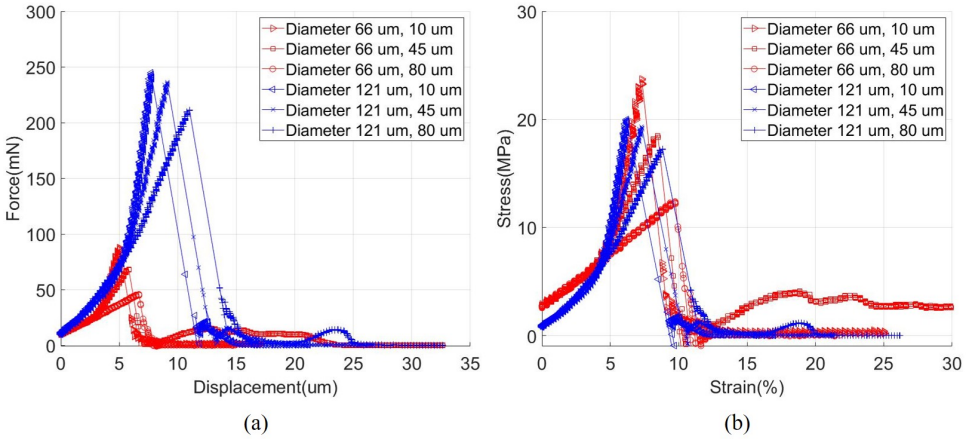


Figure 4.15: The influence of shear height to the shear response of the uncoated TPVs with diameter of 66 µm and 121 µm. (a) The shear response curve of force measured against displacement, (b) the calculated shear stress against strain.

hand, the maximum shear force of the TPVs with 66 µm diameter drops from the original value of 88 mN to 70 mN and 45 mN at a shear height of 45 µm and 80 µm respectively. And in the case of TPVs with a diameter of 66 µm, a drop of 49% of the original maximum shear force is observed.

Obviously, the aspect ratio of the TPV structures has an impact on the reduced percentage of the maximum shear force value. The influence of the shear height to the maximum shear force is stronger for the TPV structures which has a larger aspect ratio. The maximum shear strength of a TPV structure measured at a shear height of 80 µm which is the weakest point of a TPV, can be linked to the maximum force that a TPV can experience during all process steps to avoid any delamination and ensure a good yield.

## 4.4. CONCLUSIONS

The adhesion of SU-8 pillars to the substrate is optimized by fine-tuning the lithographical process steps. An increased PEB temperature is found as the optimized solution for a robust polymer pillar profile. Meanwhile, the 4.5 µm thick Al(1%Si) coating can significantly improve the mechanical strength of SU-8 pillars. The metal coating shows a greater influence on the samples with smaller pillar diameters. Furthermore, a thicker metal coating provides more mechanical enhancement in the lower thickness range from 1.4 µm to 4.5 µm. The pillar adhesion decreases with 5.6 µm thick metal coating which can be caused by the thermal stress induced by the sputtering process. The delaminations of all pillars are observed in the linear region II as the pillars are fully contacted. Hence, the "mushroom head" profile is of less influence to the delamination of the pillars.

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# 5

# Performance of a 122GHz radar Antenna-in-Package (AiP) using Through-Polymer Via (TPV)

*Low-loss IC-to-antenna connection is one of the key enablers for high-end mmW radar systems above 100GHz. In this chapter, a radar system with an on-package antenna array working at 122 GHz is developed and measured. The antenna is fabricated on top of the molded package and the IC-to-antenna interconnection is realized by Through-Polymer Via (TPV) technology. The chip layout and the antenna design is introduced. The results from the functional tests of the radar antenna-in-package (AiP) are presented and compared to a commercial quad-flat no-leads (QFN) AiP package which uses wire bonds as the IC-to-antenna interconnection. The detection margin achieved between the echo signal and the CFAR threshold is approximately 10 dB higher for the TPV radar AiP compared with the commercial QFN package.*

## 5.1. INTRODUCTION

The development of SiGe BiCMOS technology has enabled the monolithic integration of state-of-the-art system-on-chip transceiver in the G-band frequency range(110 to 300 GHz). All RF signals have been kept inside the chip except the signals from the chip to its antennas. For increasing frequencies, the IC-to-antenna interconnections are becoming more critical for the performance of the transceiver system [1, 2]. Moreover, the influence of undesired parasitic electromagnetic interference, introduced by the manufacturing stochastics of the interconnects is becoming more pronounced due to the increasing application frequencies.

A radar system using off-chip antennas has several advantages over the on-chip antennas including lower cost, design flexibility of the antenna, and broad substrate material options. Among the off-chip antenna solutions, antennas can be integrated either on a separate substrate or together with the IC package. The latter is also known as antenna-in-package (AiP). In radar applications at mm-wave frequencies, such as 122 GHz, the AiP approach is preferred due to the potentially shorter RF interconnections between the antenna and the IC which results in better performance. Furthermore, at mm-wave frequencies, the characteristic length of an antenna becomes very compatible with package dimensions which enables the miniaturization of the total RF system.

Wire bonding and embedded wafer level ball grid array (eWLB) technologies are used for connecting off-chip antennas. However, wire bonding and eWLB both have their limitations. Since the mm wavelength is comparable to the length of the wire bonds, the wire bond becomes a part of the antenna system with its corresponding manufacturing tolerances [3–5]. For reducing the influence of parasitic inductance, shorter wire bonds are desirable. However, to further reduce the length of wire bonds for mm-wave frequencies, the bond wire reliability, and fabrication yield decreases. For optimized RF performance with longer wire bonds, a compensation circuit can be integrated into the RF IC. However, for the compensation to work properly, the loop shapes of the wires need to be accurately controlled. Hence, the wire bonding process becomes time consuming, costly, and yields limited performance for mm-wave applications.

eWLB technology allows antennas to be connected to the IC by thin-film metal lines the same as on-chip antennas without consuming expensive semiconductor area [6–11]. However, in this case, the antenna layer is fabricated in the redistribution layers (RDL) at the same package side where the solder balls are also placed. The subsequent flip-chip process and assembly onto a PCB places the antenna layer between the molded substrate and the PCB which reduces the power efficiency and influences the directivity [8, 11]. Furthermore, in the case of an eWLB package, the silicon chip is flipped and processed. The backside of the chip is not in contact with any thermally conductive plane which is a disadvantage for high power MMIC application.

New package solutions for mm-wave frequency radar systems are needed. One promising package solution is to create a radar package with its antennas placed on top of the molded package and connected vertically to the radar IC. In this case, additional fabrication, assembly, and wire-bonding of an external antenna substrate are avoided. Moreover, the length of electrical interconnection can be reduced to the thickness of the epoxy molding compound (EMC) layer. The antennas are patterned on top of the EMC package, hence the package can be further miniaturized when compared to other

antenna-off-chip packaging solutions. Additionally, the IC can be bonded directly to a metal substrate, such as a QFN substrate, for improved heat dissipation. Therefore, the advantages of such radar AiPs are shorter electrical interconnection, simpler fabrication process, finer antenna features, smaller footprints, and suitable for high power MMICs.

In this chapter, we demonstrate a package solution for a 122GHz radar system with an on-package antennas array using TPV technology for the IC-to-antenna interconnection which achieves a shorter IC-to-antenna interconnection and a smaller footprint. The functional test of the radar AiP is carried out using the frequency modulated continuous wave (FMCW) method. The object detection is based on the constant false alarm rate (CFAR) threshold. A commercially available radar AiP using the same IC and same geometrical antenna design but with wire-bonding as the IC-to-antenna interconnection is used as a benchmark for the performance.

### 5.1.1. RADAR IC

The radar IC is manufactured in SiGe technology with a 0.13-µm BiCMOS process [7, 12–14]. The radar IC operates at 122 GHz ISM band and is designed for highly accurate short distance measurement. It consists of a push-push type voltage controlled oscillator (VCO), a power amplifier, an in-phase-quadrature receiver chain, a 1/32 frequency divider, external phase-locked loop (PLL), several temperature sensors and power detectors. The VCO can tune the signal frequency from 120.6 GHz to 124.3 GHz [15].



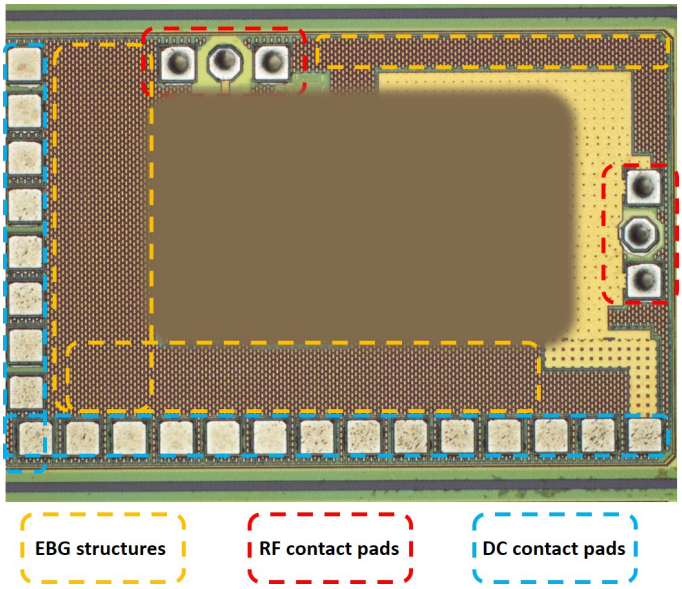



Figure 5.1: Optical microscopy image of the radar IC (top-view).

Before reaching the antenna array, the signal is boosted by a power amplifier and around 0 dBm of output power could be achieved. The radar IC occupies a total chip area of 940 µm × 1450 µm with 22 contact pads for interconnection with the quad-flat no-leads (QFN) package and 6 RF contact pads for the interconnection with its anten-

nas. A top view of the radar IC is shown in Figure 5.1. The 3 contact pads on the top side of the IC are connected to the transmitter antennas and the other 3 contact pads on the right side of the IC are connected to the receiver antennas as indicated by the annotations in Figure 5.2. The contact pads array on the left and bottom side of the IC is responsible for DC signals and the microstructures covering most of the surface areas are the electromagnetic band-gap (EBG) structures to suppress the electromagnetic interference. The total power consumption of the radar IC is around 450 mW which is supplied with a single 3.3 V [12].

### 5.1.2. ANTENNA DESIGN

Patch array antenna structures are designed for the first fabricated radar packages. For future work, these designs could be further advanced. The design uses grounded coplanar waveguide (GCPW) as the feeding network is shown in Figure 5.2 (a). The GCPW-fed antenna uses three Vias for the ground-signal-ground interconnection. The Vias and the feeding lines of the antenna are designed for an optimized impedance matching. The antenna gain could be further improved later with an additional lens structure on top of the antenna depending on the radar application. The die-attach pad of the QFN which is about 300 µm away from the antenna with EMC substrate in between is used as the antenna reflector. The 2 x 2 patches could reach around 13 dBi of directivity.



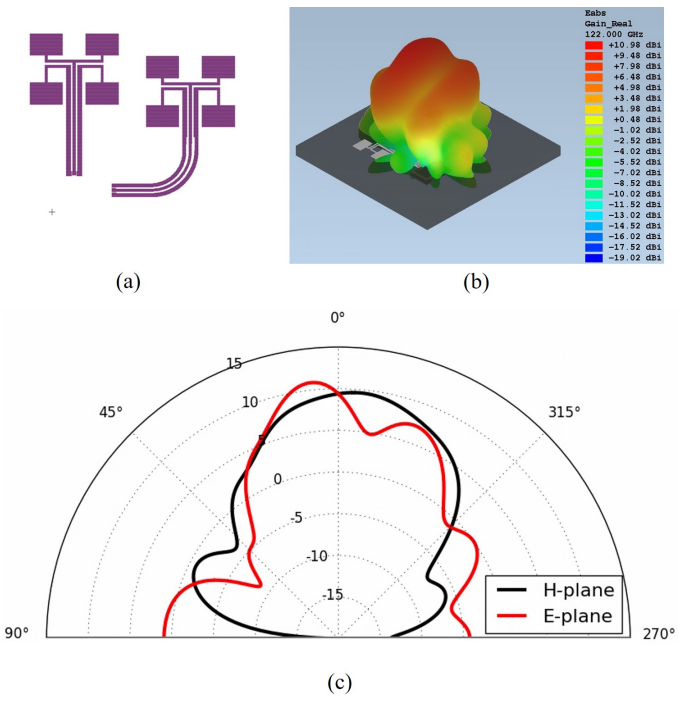


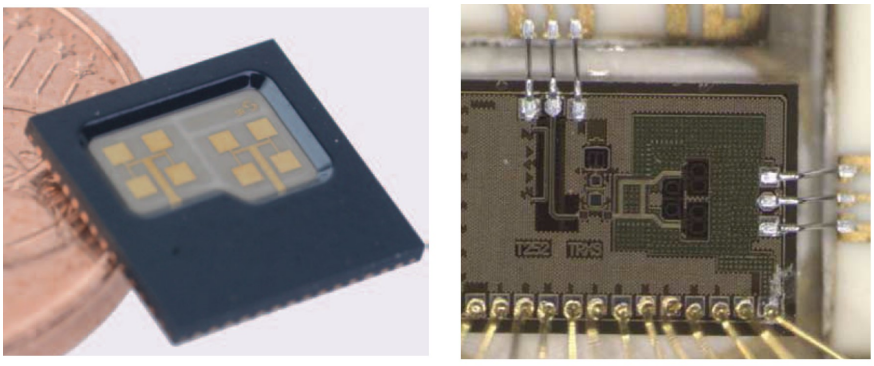

Figure 5.2: Antenna design and simulation results: (a) the antenna design utilizing GPCW matching network, (b) simulation result showing 3D radiation pattern, (c) the realized antenna gain in E-/H-plane at 122-GHz of operation frequency.

The simulations are completed using a full 3D EM model of the package with EMPIRE 3D software and the 3D radiation pattern of the GPCW antenna is shown in Figure 5.3. The impedance matching design in the simulation is simpler using TPVs compared to wire bonds which is an advantage of the packaging solution using TPVs. According to the results, the antenna could provide more than 10 dBi of realized gain through the whole IC operation band. Furthermore, the beam tilt could be eliminated by correcting antenna positioning on the package. The antenna simulation has shown similar results compared to the design used in the commercial package with wire bonds [7].

### 5.1.3. Conventional AiP using wire bonding and open cavity

The conventional radar AiP uses wire bonding with a length of 350 µm to connect the IC with its antenna array. The antenna array in the conventional AiP is fabricated on a separate substrate and placed next to the radar IC. An open cavity is formed during the film assisted molding process to expose the antennas. The conventional AiP is shown in Figure 5.3. The RF wire bonds used here are aluminum wedge to wedge bonding with a length of 350 µm. Although the wire bond loop is carefully controlled, the package can still suffer from performance variation induced by wire swings.





(a) (b)

Figure 5.3: The conventional AiP concept using wire bonds and open cavity. (a) The open cavity inside the QFN package which exposes the antenna substrate. (b) Image of the wire bonds connecting the IC and the antenna substrate. Figure adapted from [16]

## 5.2. AiP solution using TPVs

The 3D schematic of the radar AiP using TPVs for chip-to-antenna interconnection is shown in Figure 5.4. The EMC is shown transparent in Figure 5.4 (b) and (c) to view the embedded IC, DC wire bonds, and TPVs. Wire bonds are still in use for interconnecting the non-RF I/Os on the Radar IC to the QFN package leads. The minimum thickness of the molded EMC layer is in this particular design limited by the loop height of the wire bonds. The thickness of EMC above the radar IC requires a minimum of 150 µm to keep the wire bonds sufficiently shielded. Hence the TPVs are designed to be 150 um

in height. According to the position and dimension of the contact pads, the diameter and the pitch size of the SU-8 pillars are determined to be 40 µm and 100 µm. The SU-8 pillars are conformally coated with Al(1%Si) alloy by sputtering to match the metallization of the contact pads of the die. A thickness of 2.5 µm is chosen for sufficient electrical conductance and step coverage. The skin effect depth of Al at a working frequency of 122 GHz is 0.23 µm. Thus the electrical conductance of the TPVs, in this case, is limited by the skin effect rather than the metal coating thickness. The metalized SU-8 pillars have a diameter of around 50 µm and an aspect ratio around 3:1. For packaging, an 8x8 mm QFN package is used similar to the conventional AiP [17].



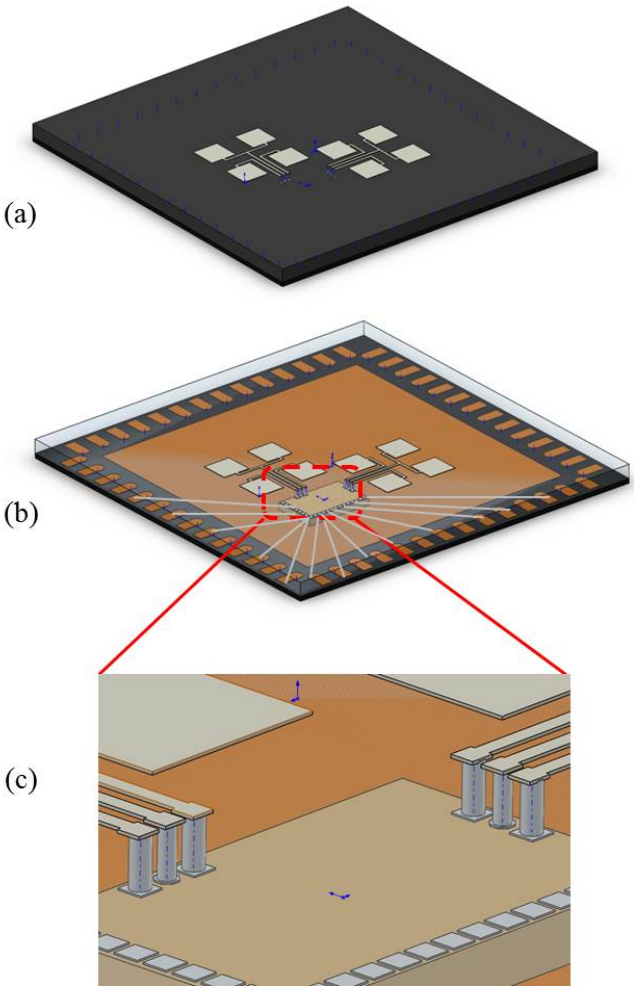



Figure 5.4: A 3D schematic of the proposed package design. (a) The overview of the package using TPVs and with antennas fabricated on the epoxy molding compound, (b) the black epoxy molding compound shown transparent to view the TPVs, the DC wire bonds and the radar IC, (c) the zoomed-in view of TPVs connecting IC and the antenna feeding lines. The schematic shown is not to scale.

The TPV process is a wafer or panel level process. 200 mm Silicon Radar wafers are diced in tiles of 24x19mm. Each tile contains 270 radar ICs. The tile is mounted on a 4-inch silicon carrier wafer using a temporary bonding layer. This allows the samples to be handled in the TUD-EKL cleanroom facilities. After the fabrication of TPVs, the wafer tile is removed from the carrier wafer by a thermal releasing process. In this design, TPVs are shorter in length and more robust, insensitive for wire sweep in the molding process compared to wire-bonds. Compared to the conventional package, the length of the RF interconnection is reduced from 350 µm of the wirebonds to 150 µm of the TPVs. The shorter electrical length will also reduce the inductive parasitic effect which is critical in mm-wave radar systems.

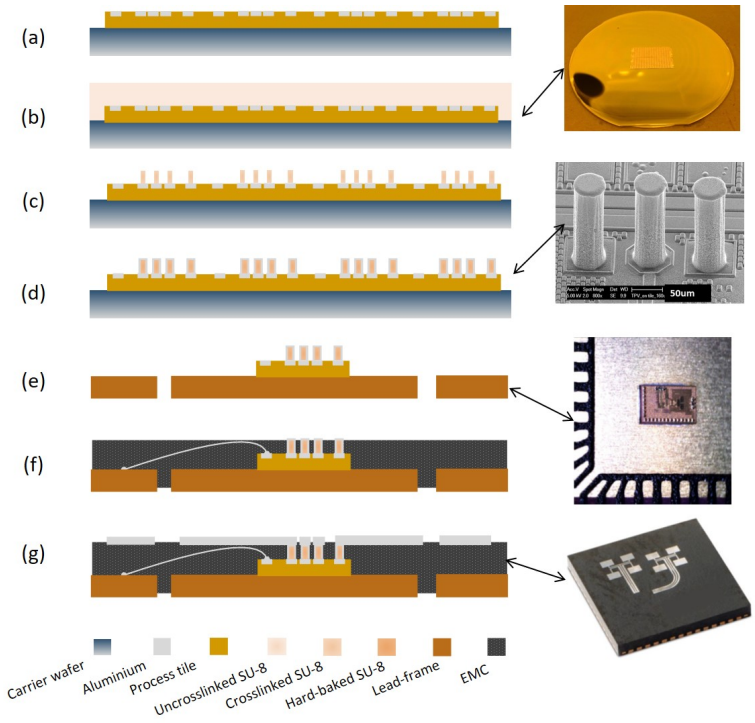



Figure 5.5: A detailed process flow of TPVM-C-QFN. (a) Temporary bonding of the wafer tile containing radar ICs onto a silicon carrier wafer. (b) Spin coating of SU-8 resist. (c) Lithographical steps of SU-8 to obtain high-aspect-ratio polymer pillars. (d) Metallization of polymer pillars and patterning of the metal layer. (e) Assembly of the singulated radar ICs onto a QFN substrate, including pick & place and wire-bonding steps. Each QFN panel was assembled with 36 radar ICs. (f) Film assisted molding of the QFN substrate. (g) Metallization on top of the molded QFN and patterning of antenna structures. The schematic shown is not to scale. Following (g), the dicing of the QFN panel is performed to obtain individual radar AiPs.

A detailed process flow is presented in Figure 5.5. First, the wafer tile is bonded onto a silicon carrier wafer. The temporary bonding material used is poly(propylene carbonate). Since the wafer tile is 150 µm thick, a 300 µm thick SU-8 layer is spin-coated at a spin speed of 500 rpm for 60 seconds so that the thickness of the SU-8 above the radar

IC is around 150 µm. After the spin coating, a soft baking step is applied to evaporate the solvent and solidify the SU-8 film. The exposure of SU-8 is carried out on an EVG 420 mask aligner with an exposure dose of 885 mJ/cm2 and exposure time of followed by a post-exposure bake (PEB) step. The PEB process was carried out on a hotplate and consists of two stages. The first stage baking is a low-temperature bake at 65 °C for 5 minutes and followed by the second stage baking with a higher temperature at 110 °C for 10 minutes. The SU-8 layer is developed in propylene glycol methyl ether acetate (PGMEA). During development, the wafer is placed in a wafer carrier facing down in the PGMEA. Gentle agitation is provided by a magnetic rotor. A low power plasma flash is applied to remove the remaining residue of SU-8 after the development process. A hard baking step in a vacuum oven is carried out before metalization which helps the SU-8 to further cross-link and degas thoroughly. A hard baking temperature of 180 °C which is higher than the molding temperature is used to ensure the thermal stability of the polymer core during the molding process.

After hard baking, sputtering of 2.5 µm thick Al with 1% Si layer is performed. During the sputtering process, the wafer holder is kept at 25 °C, however, the temperature at the surface of the wafer can rise above the glass transition temperature with continuous deposition. Hence, a cooling step is inserted after every 156 nm thick deposition. In this way, the sputtering process induces no damage to the SU-8 pillars.



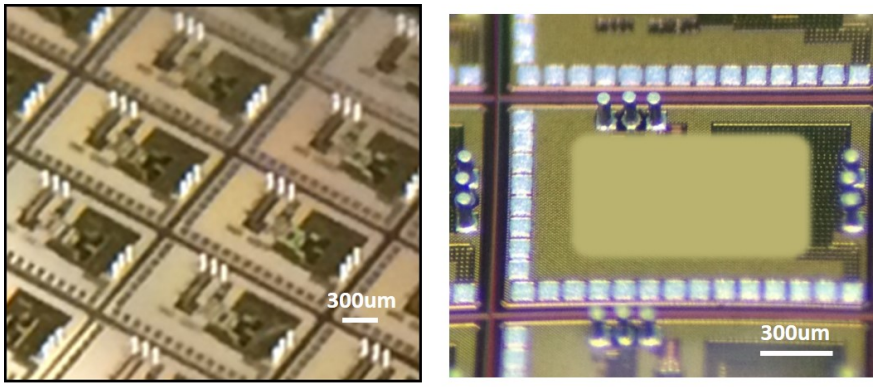



Figure 5.6: Intermediate fabrication results. (a) SU-8 pillar array on top of the radar ICs before Al coating, (b) metalized SU-8 pillars on the radar IC.

The fabrication results of SU-8 pillars and the metalized SU-8 pillars on the radar IC are shown in Figure 5.6 (a) and (b). The wafer tile containing the radar ICs is removed from the carrier wafer and diced into single chips. The singulated radar chips with metalized pillars are then picked up and placed onto a QFN panel in a 6 x 6 array. An automated wire bonder connects the remaining radar IC contact pads to the QFN panel using Al wirebonds. The entire panel is then molded using film assisted molding which keeps the top surface of the metalized pillars clean of EMC which subsequentially results in the realization of TPVs. The last step is to fabricate the antenna arrays and the feeding

networks on top of the encapsulated QFN panel. In such a way, the connections between the radar IC, the TPVs and the antenna structures are made.

The die pick & place accuracy affects the position of the TPVs on the QFN pattern. For each QFN panel, the pick & place position of every single chip should be within a certain absolute position tolerance to prevent misalignment of the antenna mask to the substrate during exposure. The maximum tolerance of the misalignment depends on the minimum overlap design between the TPVs and the contact pads of the feeding network of the antenna array. In our case, the minimum overlap design is 17 µm and thus the maximum tolerance of misalignment during die pick & place here is ±17 µm. Other than more accurate pick & place step, field alignment techniques can also be used to lower the sensitivity of misalignment from pick & place process.

Compared to the conventional AiP solution using an open cavity that requires 9 steps in the backend process, radar AiP using TPV technology needs 6 steps instead. Furthermore, the use of a specific top mold in the molding process for making the cavity to expose the antennas is avoided. With our proposed packaging solution using TPV technology, the total fabrication cost and time of radar AiPs can potentially be reduced due to fewer fabrication steps and less usage of equipment and materials.



## 5.3. RADAR FUNCTIONAL TEST

To characterize the functional performance, the fabricated radar AiPs using TPV technology were assembled on a test kit at Silicon Radar GmbH, Germany, as shown in Figure 5.7. A conventional radar AiP with an open cavity and GCPW-fed antenna design was also measured to provide a reference for the performance, see Figure 5.7 (a). In this conventional package, antennas were fabricated on a substrate called Rogers ultralam 3850 which has low permittivity and low losses up to the millimeter-wave range. In the commercial package, the antennas are connected to the radar IC by 3 aluminum bond wires with a wedge-to-wedge technique.

### 5.3.1. TEST ENVIRONMENT

The test kit consists of three main parts, the radar package frontend under test, a baseband PCB assembly, and an additional plastic lens with lateral shielding. The additional lens and lateral shielding are used to enhance the signal and reduce side lobes. The test kit was fixed with glue on the table to make sure the position of the tested packages and RF lens would not change between measurements. The two AiP shares the same baseband PCB and the same antenna lens to minimize the experiment introduced variations.

The radar test kit operates with a frequency modulated continuous wave (FMCW) principle using the constant false alarm rate (CFAR) mechanism for determining the detection threshold. The frequency of the signal is centered at 122 GHz. A bandwidth of 4500 MHz and 1024 FFT data acquisition was used to obtain an optimized detection accuracy of 19.4 mm with a maximum measurement range of 10 meters. The radar signal was beamed towards the ceiling. A schematic illustration of the measurement environment is shown in Figure 5.8.

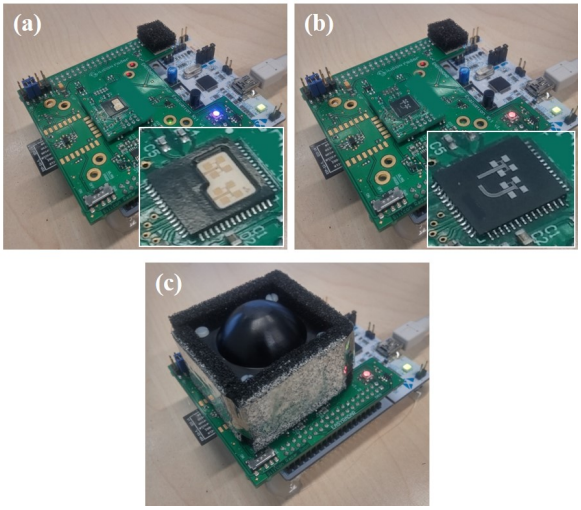



Figure 5.7: The assembly of the radar performance test kit. (a) The test kit loaded with the conventional AiP with GCPW-fed patch array antenna. (b) The test kit loaded with the AiP using TPVs. (c) The test kit assembled with an RF lens and side shielding.

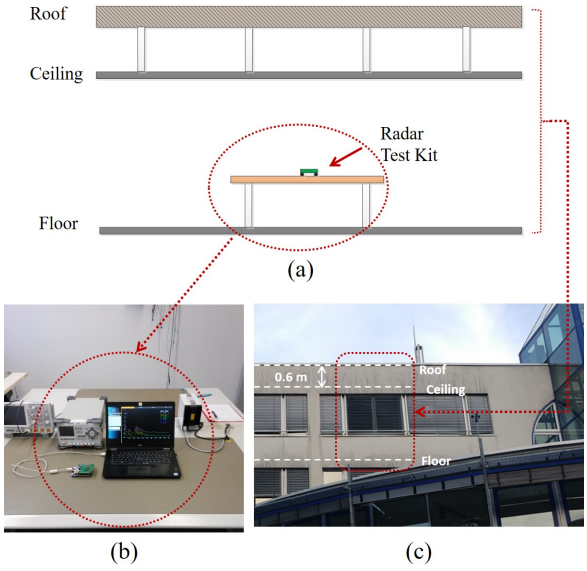



Figure 5.8: A schematic of the test environment. Both the ceiling and the roof of the building were used as targets. (a) Schematic illustration of the test environment, (b) the measurement setup including a laptop and the test kit, (c) photograph of the detected building features from outside.

### 5.3.2. PERFORMANCE COMPARISON OF THE CONVENTIONAL AIP AND THE AIP USING TPVS

The echo signal strength and the CFAR threshold curve are plotted over the measurement range for the conventional AiP and the AiP using TPVs, as shown in Figure 5.9 (a) and (b) respectively. The measurements were carried out with a refresh rate of around 10 Hz, which generated 10 sets of echo signal strength and CFAR threshold values in one second. The plotted curves of the echo signal and the CFAR threshold are the average of the 10 measured data sets. An object is considered detected when a peak is observed in the echo signal strength above the CFAR threshold curve. The target signal margin is the subtraction of the CFAR from the echo signal strength.

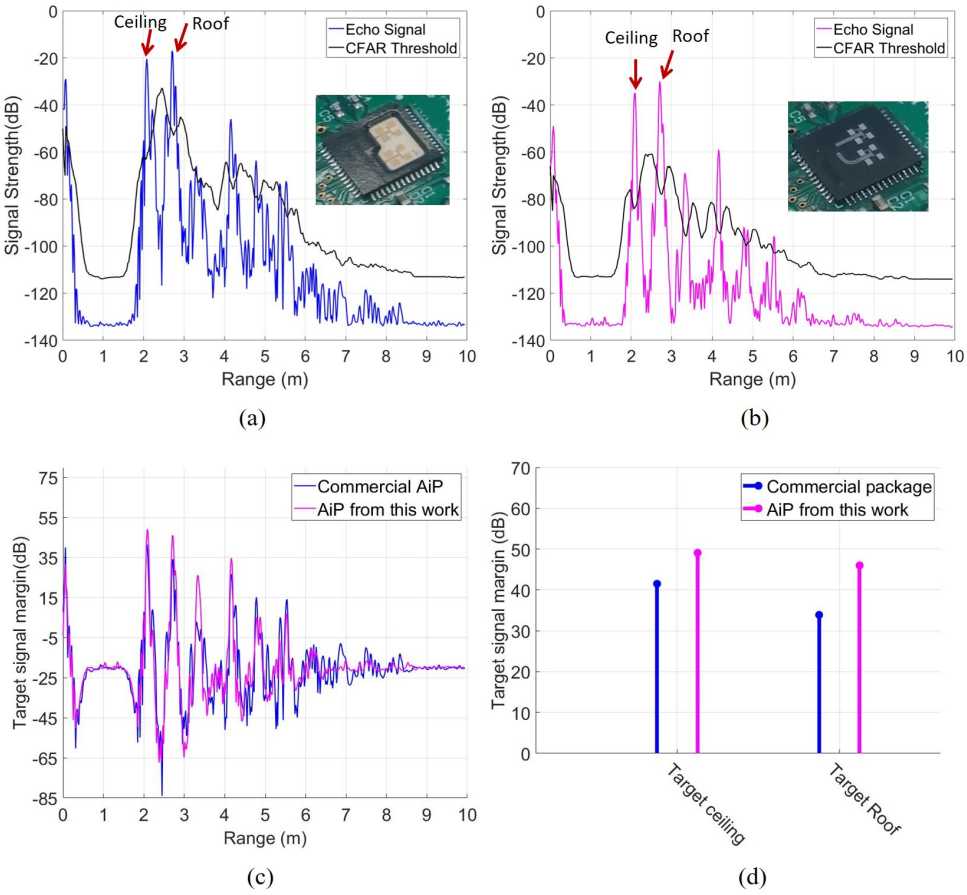



Figure 5.9: The radar performance measurement results. (a) The echo signal strength measured and the corresponding CFAR curve from the conventional AiP, (b) the echo signal strength measured and the corresponding CFAR curve from the AiP using TPVs, (c) comparison of the target signal margin of both AiPs over measurement range, (d) comparison of the detected target signal margin of the first two targets, the ceiling and the roof, measured by both AiPs.

According to the measurement results, objects at distances of 2.1 m and 2.7 m are detected. The object detected at 2.1 m away corresponds to the ceiling, while at 2.7 m away it corresponds to the roof of the building. All radar AiPs under test captured the objects with a clear echo signal. The conventional AiP using wire-bonding and open cavity receives echo signal with strengths of -21 dB and -17dB at 2.1 m and 2.7 m respectively. The AiP using TPVs with GCPW-fed antenna receives an echo signal with a strength of -35 dB and -30 dB. However comparing the measured echo signal strength with the CFAR threshold, the target signal margin obtained by the conventional AiP is around 41.51 and 33.89 dB at the two targets. The target signal margin obtained by the AiP using TPVs is around 49.09 and 46 dB which are 7.5 dB and 12.1 dB higher than the conventional AiP. This means the AiP using TPVs distinguishes the echo signals better from the background noise. The TPV interconnection which is shorter in length and lowers in parasitic effect compared to the wire bonds contributes to the low noise performance. The functional RF performance of the radar systems using the TPV packaging solution is superior to the conventional package. The prototype packages detect targets with similar accuracy compared to the commercial package with an even lower noise level. The relatively higher loss observed in echo signals can be improved by optimizing both the impedance matching and the substrate material properties.



## 5.4. CONCLUSIONS

The performance of a 122 GHz radar system with an on-package antenna array using Through-Polymer Via is characterized. The length of the electrical connection of the IC-to-antenna interconnection is reduced to an average of 150 µm. The antenna array is placed on top of the IC which enables the miniaturization of the footprint of mm-wave radar AiPs. The fabrication process of the radar AiP using TPV is simpler compared to the radar AiP using wire bonds as the IC-to-antenna interconnection. The antenna layer is fabricated directly on the epoxy molding compound as the substrate which saves the cost of extra antenna substrates. The die-attach pad of the QFN which is about 300 µm away from the antenna with EMC substrate in between is used as the antenna reflector. By tuning process temperatures, the robustness of the TPVs in the following dicing and molding process was optimized. The final packages are tested with FMCW measurements. The performance of the radar AiP using TPVs is benchmarked with the radar AiP using wire bonds. The TPV interconnection shows a better noise performance compared to the wire bonds. The margin between the echo signal and the CFAR threshold curve at the detection peak of an object is 10 dB higher on average measured by the radar AiP using TPVs.

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# 6

# CONCLUSION AND RECOMMENDATIONS

## 6.1. CONCLUSIONS

As the need for 3D integration in microelectronic packaging keeps increasing, a low-cost, reliable, high density, high-aspect-ratio multi-functional advanced through package via technology is highly demanded. Through-Polymer Via (TPV) has the potential to meet the above needs. This study aims at bringing the TPV technology into industrial applications. Firstly, a general TPV process guideline is developed to adapt the fabrication process into cleanroom level manufacturing (chapter 2). Specific fabrication processes according to four different industrial applications are then developed (chapter 3). However, due to the high failure rate of the metalized TPVs during dicing, the original TPV process is optimized through adjusting the processing parameters, such as the post-exposure baking temperature, and a 100% yield is eventually achieved. Next, the mechanical characterization with a shear test is carried out to investigate the robustness of the proposed metalized TPVs (chapter 4). Finally, a 122 GHz radar Antenna-in-Package (AiP) with the proposed metalized TPVs as the IC-to-antenna interconnection is demonstrated and the radar performances are characterized and compared to a conventional AiP (Chapter 5).

The adaption of the TPV process to a cleanroom level manufacturing is essential to evaluate its scalability. Thick SU-8 material is considered as non-standard in the cleanroom and needs to be carefully handled to avoid contamination of equipment. A general cleanroom level guideline of the thick-SU-8 process is developed in the Else Kooi Lab (EKL) for TPV technology, which includes spin coating, lamination, soft baking, exposure, post-exposure baking, development, hard baking, and metallization. Some conclusions regarding the TPV process are summarized as follows:

- To obtain a uniform thick SU-8 (> 100 μm) coating, an edge bead removal (EBR) process is proposed. Conventional cleanroom processing EBR uses a stream of liquid solvents, such as acetone, to clean the edge bead of a resist film. This is

under the pre-condition that the resist film is dry at the end of the spin. Thick SU-8 is still in liquid form after the spin and the conventional solvent EBR process does not work. To solve this problem, a scrape EBR technique is developed, in which the uniformity of a 100 µm thick SU-8 coating is improved from a variation of 7µm to 2 µm. Scrape EBR is suitable for improving the uniformity of spin-coated thick and wet polymer layer.

- To avoid delamination of SU-8 due to thermally induced stress, the post-development cleaning and drying process is modified. Due to CTE mismatch, the stress builds up in the SU-8 structure can eventually cause delamination and cracking. A more desired approach is to bake the sample on a hotplate at 50 °C. It is also time-efficient. In the TPV process, hotplate drying is advantageous over spin-drying and natural convection drying.

In this thesis work, 4 specific fabrication processes are developed based on 4 different industrial application carriers. The first process, the TPVM-C-QFN process, is developed for a radar antenna-in-package (AiP) working at 122 GHz. The TPVM-C-QFN process is aiming at achieving high-aspect-ratio, small pitch, metalized TPVs. The second process, the TPVO-C-QFN process, is developed for an optical encoder system-in-package. The TPVO-C-QFN process is aiming at achieving optical transparent TPVs with a height of 300 µm. The third process, the TPVH-N-PCB process, is developed for a molded PCB display panel with through holes for LED integration. It is focusing on the realization of large arrays (>5000) of TPV hollow structures on a PCB panel with a 100% yield. The fourth process, the TPVH-W-QFN process, is developed for a miniaturized 1x1 mm QFN package with a micro through-hole in the dimension of several tens of micrometers. Each process is unique and some findings are concluded as follow,

- To ease the handling of wafer tiles in the cleanroom, the temporary bonding technique is applied to assemble the wafer tile to a carrier wafer. Poly(propylene carbonate) (PPC) is used as the temporary bonding material. PPC is proven to be a suitable temporary bonding material that survives all the TPV process steps and can be easily released by applying heat and sliding off.
- To metalize the TPV structures, sputtering deposition of the metal layer is applied. The sputtering recipe with integrated cooling steps has proven to be suitable for TPV metallization without causing any degradation of SU-8 polymer and contamination of the sputtering chamber.
- Lamination of SUEX dry film over microstructure arrays on the IC chip, such as high-density contact pads and the electromagnetic band-gap (EBG) structures on a radar IC, can result in trapped air bubbles. The spin coating of SU-8 is more suitable for such cases.
- Yellowing effect is the most critical bottleneck for the application of TPVs in the optical field.
- Large area structures in thick SU-8 film can suffer from high stress and introduce cracks after being molded. Thus the application of large dimensional solid SU-8 structures will be a challenge and new polymer material needs to be explored.

To investigate the adhesion of TPVs to the substrate, the mechanical characterization of TPVs is carried out using the shear test. TPVs with different diameters and different metal coating thickness are fabricated. The shear tests are performed at different shear heights and SEM inspections are performed to study the TPV profile and shear failure sites. Several conclusions are listed below,

- The elevated post-exposure bake (PEB) temperature is a key parameter to obtain the "elephant foot" TPV profile. The foot profile is not desired in the normal resist process however is desired in the TPV process for an optimized pillar adhesion and better metal coating quality at the bottom interface.
- Apart from the foot profile, thick metal coating can enhance the pillar adhesion further. The 4.5 µm thick Al(1%Si) coating can significantly improve the mechanical strength of SU-8 pillars. The metal coating shows a greater influence on the samples with smaller pillar diameters.
- The shear failure happens at the interface between SU-8 and substrate with a clean break-off when a thinner metal coating is applied. With an increasing coating thickness, the failure mechanism also involves the cracking of the polymer leaving polymer residue at the failure site.

To demonstrate the benefit of TPVs in a 122 GHz radar antenna-in-package (AiP), the radar functional test of the fabricated AiP using TPV technology is performed and compared to a conventional radar AiP using the same radar IC and antenna design. Frequency modulated continuous wave (FMCW) radar measurement is carried out and the abilities of the AiPs to detect targets are compared. Several conclusions are listed below,

- By applying TPVs in the AiP, the interconnection length can be significantly reduced. The length of the electrical connection is reduced from 350 µm to an average of 150 µm.
- The TPV antenna-to-chip interconnect is very reproducible which enables a more efficient compensation of the parasitics compared with wire bonding.
- The noise background in the echo signal measured from the AiP using TPVs is lower compared to the measurement from the conventional AiP. The TPVs serve as a low noise interconnection compared to the wire bonds.
- The AiP using TPVs shows a better performance than the conventional AiP by capturing the first two targets with target signal margins 7.5 and 12.1 dB higher.

## 6.2. RECOMMENDATIONS FOR FUTURE WORK

The real commercialization of TPV technology still needs extra steps forward. With each application carrier, promising fabrication results are obtained. However, there are still challenges to overcome. From this thesis work, we have obtained the first-hand know-how and have learned from the results what to further investigate for each application carrier.

- For the radar system-in-package and the TPVM-C-QFN process, the prototype package has shown successful functional test results. The key is to further improve the fabrication yield at the assembly and molding processes.
- For the optical encoder system-in-package and TPVO-C-QFN process, the remaining challenges are the yellowing of SU-8 polymer and the stress induced by CTE mismatch which causes polymer cracking. To take this carrier application to a higher technology readiness level, a redesign of the packaging solution would be helpful.
- For the PCB display panel and TPVH-N-PCB process, the adhesion of the TPV ring structures needs to be further improved. Although high PEB temperature can result in the desired adhesion, the unwanted residual of SU-8 can appear and is hard to remove.
- For the 1x1 mm QFN through-hole and TPVH-N-QFN process, the clearance inside the ring for high-aspect-ratio or small inner diameter structures is still challenging. The ideal case in this application is thinner walls but with robust mechanical strength to minimize bending and deforming during the molding process. Extra coating layer which can significantly strengthen the polymer material, such as $SiO_2$, SiC, SiN, Ti, or TiN can potentially further develop this case.

# List of abbreviations

| | |
|---|---|
| TPV | Through-Polymer Via |
| TSV | Through-Silicon Via |
| TMV | Through-Mold Via |
| TCP | Tall Copper Pillar |
| VWB | Vertical Wire-Bonding |
| EMC | Epoxy Molding Compound |
| PR | Photo Resist |
| PoP | Package on Package |
| I/O | Input or output |
| SEM | Scan Electron Microscopy |
| HAR | High Aspect Ratio |
| MEMS | Microelectromechanical Systems |
| WLCSP | Wafer Level Chip Scale Packaging |
| ASIC | Application-Specific Integrated Circuit |
| SiP | System-in-Package |
| AiP | Antenna-in-Package |
| QFN | Quard Flat No-leads package |
| SoC | System on Chip |
| PGMEA | Propylene Glycol Methyl Ether Acetate |
| GBL | Gamma-Butyrolactone |
| CTE | Coeffecient of Thermal Expansion |
| SB | Soft Bake |
| PEB | Post Exposure Bake |
| HB | Hard Bake |
| EBR | Edge Bead Removal |
| PCB | Printed Circuit Board |
| LED | Light Emitting Diode |
| BLDC | Brushless DC (motor) |
| IPA | Isopropyl alcohol |
| CAR | Chemically Amplified Resist |
| DRIE | Deep Reactive Ion Etching |
| CMP | Chemical Mechanical Polishing |
| CMOS | Complementary Metal Oxide Semiconductor |

# SUMMARY

The rapid development of semiconductor industry in the past decades has reshaped the world tremendously and greatly changed people's lives. Two-dimensional (2D) downsizing of semiconductor devices following the "Moore's law" for many years is now reaching its boundary conditions of further exponential growth and three-dimensional (3D) fabrication approaches are getting more attention. Next to the IC manufacturing, 3D chip packaging has been playing a more important role nowadays. Much more cost-effective and scalable technologies are being developed. Vertical interconnect via technology such as through-silicon via (TSV), through mold via (TMV), tall Cu pillar (TCP), and vertical wire bonds (VWB) are the key processes in 3D chip packaging. However, they have limitations in cost, reliability, via density, scalability, and aspect ratio. In addition, as the function integration density keeps increasing, not only electrical interconnection but also optical, mechanical, fluidic, and thermal interconnections are needed in the near future. Thus, a low-cost, reliable, high density, scalable, high-aspect-ratio multi-functional advanced through package via technology is highly demanded in the future semiconductor industry.

Through-Polymer Via (TPV) is a novel bottom-up vertical through package via technology potentially low-cost process, suitable for high density and high-aspect-ratio via formation, compatible with the various packaging process and suitable for multi-functional applications. The main process of TPV technology consists of the formation of a high-aspect-ratio polymer structure through lithography in combination with subsequent film assisted molding. TPV process works with both spin coating and dry film lamination for applying the polymer material, which is suitable for low-cost wafer-level and panel-level mass production. The process uses thick photosensitive polymer materials, such as SU-8 and SUEX, and the structures are patterned via lithography, which enables a broad range of high density, and high-aspect-ratio features. Depending on the applications, non-coated polymer structures can serve for optical and mechanical functions while an optional functional coating is applied to the polymer structures to target specific applications, such as metal coating for electrical function.

In this study, cleanroom-compatible thick-SU-8 process guidelines are developed for the TPV technology, in which both spin coating and lamination are applied. Spin coating of liquid SU-8 is optimized for thickness up to 300 um with a single spin, with its corresponding poor thickness uniformity. To improve the uniformity, an edge bead removal (EBR) technique, called scrape edge bead removal, is developed. The thickness uniformity can be improved from a standard deviation of 7 μm to 2 μm after applying the scrape EBR. Moreover, vacuum hot press lamination is developed for improving the process flexibility with different dimensions of SUEX dry film in combination with various substrate dimensions. Lithographic processes are tuned by controlling overexposure and elevated post-exposure bake (PEB) temperature to achieve better polymer-substrate adhesion. The optimized process parameters vary with different applications and spe-

cific process steps. For liquid SU-8 material, the optimized PEB temperature at around 110 °C can improve the foot profile and substrate adhesion. For the SUEX process on the PCB substrate, the optimized process parameters are heavy overexposure, and PEB at around 135 °C can achieve the highest adhesion.

Next, four specific process cases are developed based on 4 different application carriers. 4 process codes are used as the reference to the fabrication process, namely TPVM-C-QFN, TPVO-C-QFN, TPVH-N-PCB, and TPVH-W-QFN. TPVM represents metalized TPVs, TPVO represents optical TPVs and TPVH represents ring-like hollow TPVs. The second part of the process code gives information about the substrate on which the TPVs are fabricated. Here in the four codes, C represents chips or wafer tile, N represents none which means the TPV structures are fabricated directly on the substrate of the package, and W represents wafer. The third part of the process code gives information on the package type.

- Based on the application of a radar system-in-package, the TPVM-C-QFN process is developed using metalized TPVs with a height of 150 µm, a diameter of 40 µm and a pitch size of 100 µm. The TPVM-C-QFN process is optimized to improve the mechanical strength by adjusting the polymer pillar foot profile and its metal coating thickness, and a 100% yield after dicing is achieved.

- Based on the application of an optical encoder system-in-package, the TPVO-C-QFN process is developed using optical TPVs as vertical micro windows. Optical TPV structures with a height of 300 µm and lateral dimension ranging from 70 µm up to 1000 µm are fabricated using SUEX dry film. Several challenges are identified including the yellowing of SUEX material due to polymer degradation, cracking of the polymer material due to stress, trapped microbubbles at the TPV-to-chip interface due to the lamination technique and over-molding of TPV structures due to non-uniformity of TPV height.

- Based on the application of a molded PCB display panel with through holes, the TPVH-N-PCB process is developed using high-density large arrays of TPV hollow structures. The TPV hollow structure keeps the inner area clean from the epoxy-molding compound (EMC). An array of more than 5000 circular TPV hollow structures are fabricated with an inner diameter of 800 µm, a wall thickness of 110 µm, a height of 300 µm and a pitch of 1.2 mm. Ring structures with designs of micro features on the inner sidewall of the TPV ring are also fabricated to demonstrate the advantage of TPV in making fine feature sidewall modification.

- Based on the application of a miniaturized 1x1 mm QFN package with micro through-holes, the TPVH-W-QFN process is developed using miniaturized TPV hollow structures with an inner diameter ranging from 50 µm to 300 µm, and wall thicknesses ranging from 20 µm to 40 µm. The process is developed with both spin-coated SU-8 and laminated SUEX. The PEB step is optimized and set to a temperature of 130 °C for improved adhesion of the TPV structures. Ultra-small TPV hollow structures with inner diameter down to 60 um and a wall thickness of 20 µm are demonstrated. Other than the circular hollow structures, other hollow structures with a square shape, a triangular shape, and groups of hollow structures with close pitch

and hollow structures with micropillars inside are also fabricated and demonstrated.

Furthermore, an in-depth investigation of the effects of foot profile control and metal coating thickness is carried out to improve the mechanical strength of metalized TPVs. The TPV profile is improved from an undercut profile to an "elephant foot" profile and the diameters of 31, 66, 121 µm and metal coating thickness ranging from 1.4 to 5.6 µm are considered in processing. Shear tests are carried out at three different shear height of 10, 45, 80 µm to characterize the mechanical strength of the TPVs. Comparing the shear response of TPVs without coating and with 4.5 µm thick Al(1%Si) coating, the maximum shear force has increased for the diameter of 31 µm, 66 µm, 121 µm by 132%, 122%, and 76% respectively. The metal coating has shown a stronger influence on the smaller diameter TPVs. As the coating thickness gets thicker, the increase of the mechanical strength is less. With diameters of 66 µm and 121 µm, the max shear forces decrease at 5.6 µm thick coating. Shear height has more influence on the max shear force of higher-aspect-ratio pillars. In the case of 66 µm diameter pillar, with a pillar aspect ratio around 2:1, the max shear force shows a 49% decrease from lowest (10 µm) to highest (80 µm) shear height. Finally, the performance of a 122 GHz radar Antenna-in-Package (AiP) with an on-package antenna array using Through-Polymer Via as the IC-to-antenna interconnection is characterized and compared to a conventional radar AiP. The conventional radar AiP uses wire bonding with a length of 350 µm to connect the IC with its antenna array. The antenna array in the conventional AiP is fabricated on a separate substrate and placed next to a radar IC. An open cavity is formed during the film assisted molding process to expose the antennas. Compared to the conventional AiP, the AiP developed in this thesis using TPV technology, which reduces the IC-to-Chip electrical length to 150 µm and avoids the negative impact of wire swing. In addition, the 3D interconnection realized by TPV enables miniaturization of the package compared to the conventional AiP. Furthermore, the antenna layer is fabricated directly on the epoxy-molding compound, which saves the cost of extra antenna substrates. In addition to the above-mentioned advantages, the die-attach pad is used as the antenna reflector. The fabricated antenna-in-package (AiP) with TPVs is soldered onto a PCB test board and the frequency modulated continuous wave (FMCW) radar measurement is performed. The FMCW radar measurement measures the echo signal strength over the detection range of 10 m and generates a constant false alarm rate (CFAR) by signal processing using customized software. A target is confirmed when the echo signal shows a peak above the CFAR signal. The AiP fabricated in this thesis has demonstrated a higher target signal margin than the conventional AiP. In the measurements performed, the AiP from this work has detected the first and second targets with target signal margins of 49.09 dB and 46 dB, which is 7.5 dB and 12.1 dB higher than the conventional AiP.

# SAMENVATTING

De snelle ontwikkeling van de halfgeleiderindustrie in de afgelopen decennia heeft de wereld enorm hervormd en het leven van mensen enorm veranderd. Tweedimensionale (2D) verkleining van halfgeleiderapparaten volgens de "wet van Moore" bereikt nu sinds jaren de randvoorwaarden voor verdere exponentiële groei en driedimensionale (3D) fabricagetechnieken krijgen meer aandacht. Naast de ic-productie speelt 3D-chip packaging tegenwoordig een belangrijkere rol. Er worden veel meer kosteneffectieve en schaalbare technologieën ontwikkeld. Verticale interconnectie via technologie zoals through-silicon via (TSV), through mold via (TMV), “Tall” Cu-pilaar (TCP) en verticale draadverbindingen (VWB) zijn de belangrijkste processen in 3D-chipverpakkingen. Ze hebben echter beperkingen in kosten, betrouwbaarheid, via dichtheid, schaalbaarheid en aspect verhouding. Bovendien, aangezien de dichtheid van de functie-integratie blijft toenemen, zijn in de nabije toekomst niet alleen elektrische verbindingen, maar ook optische, mechanische, vloeistof en thermische verbindingen nodig. Daarom is er in de toekomstige halfgeleiderindustrie een sterke vraag naar een betaalbare, betrouwbare, hoge dichtheid, schaalbare multifunctionele high-aspect ratio via “through package” technologie.

Through-Polymeer Via (TPV) is een nieuwe bottom-up “through package” via technologie wat in potentie een goedkoop proces is. Het proces is geschikt voor hoge dichtheid en hoge aspect via vorming, compatibel met het verschillende “packaging” processen en geschikt voor multifunctionele toepassingen. Het belangrijkste proces van TPV-technologie bestaat uit de vorming van een polymeerstructuur met een hoge aspectverhouding door middel van lithografie in combinatie met daaropvolgend dunne film ondersteund ingieten. Voor het aanbrengen van het polymeermateriaal in het TPV-proces kan zowel spincoating als droge film lamineren worden toegepast, processen die geschikt zijn voor goedkope massaproductie op wafer- en paneelniveau. Het proces maakt gebruik van dikke, lichtgevoelige polymeermaterialen, zoals SU-8 en SUEX, en de structuren worden gevormd via lithografie, wat een breed scala aan structuren met hoge dichtheid en hoge aspectverhouding mogelijk maakt. Afhankelijk van de toepassingen kunnen niet-gecoate polymeerstructuren worden aangewend voor optische en mechanische functies, terwijl een optionele functionele coating op de polymeerstructuren wordt aangebracht voor specifieke toepassingen, zoals metaalcoating voor elektrische functies.

In deze studie zijn cleanroom-compatibele dikke SU-8-procesrichtlijnen ontwikkeld voor de TPV-technologie, waarbij zowel spincoating als lamineren worden toegepast. Spincoating van vloeibare SU-8 is geoptimaliseerd voor dikte tot 300 um in een enkel spin proces, met overeenkomstige slechte dikte-uniformiteit. Om de uniformiteit te verbeteren, is een randverhoging verwijderings (EBR) -techniek ontwikkeld, genaamd “scrape edge bead Removal”. De dikte-uniformiteit kan worden verbeterd van een standaarddeviatie van 7 µm tot 2 µm met het toepassen van de scrape EBR. Bovendien is vacuüm-warmte pers lamineren proces ontwikkeld voor het verbeteren van de proces-

flexibiliteit met verschillende afmetingen van SUEX droge film in combinatie met verschillende substraatafmetingen. Lithografische processen worden geoptimaliseerd door middel van overbelichting en verhoogde baktemperatuur na belichting (PEB) om een betere polymeer-substraat hechting te bereiken. De geoptimaliseerde procesparameters variëren per toepassingen en specifieke processtappen. Voor vloeibare SU-8-materiaal kan de geoptimaliseerde PEB-temperatuur bij ongeveer 110 °C het voet-profiel en de hechting van het substraat verbeteren. Voor het SUEX-proces op het pcb-substraat zijn de geoptimaliseerde procesparameters zeer hoge overbelichting, en PEB bij ongeveer 135 °C waarmee de hoogste hechting kan worden bereikt.

Vervolgens worden vier specifieke procesgevallen ontwikkeld op basis van 4 verschillende applicatie toepassingen. 4 procescodes worden gebruikt als referentie naar het fabricageproces, namelijk TPVM-C-QFN, TPVO-C-QFN, TPVH-N-PCB en TPVH-W-QFN. TPVM staat voor gemetalliseerde TPV's, TPVO staat voor optische TPV's en TPVH staat voor ringachtige holle TPV's. Het tweede deel van de procescode geeft informatie over het substraat waarop de TPV's zijn vervaardigd. Hier in de vier codes stelt C chips of wafer-plaat voor, N staat voor niet, wat betekent dat de TPV-structuren direct op het substraat van de "package" worden vervaardigd, en W staat voor wafer. Het derde deel van de procescode geeft informatie over de het type "package".

- Gebaseerd op een toepassing van een radarsysteem-in-"package", is het TPVM-C-QFN-proces ontwikkeld met gemetalliseerde TPV's van 150 µm hoog, een diameter van 40 µm en een steekmaat van 100 µm. Het TPVM-C-QFN-proces is geoptimaliseerd om de mechanische sterkte te verbeteren door het aanpassen van het polymeer voet-profiel, de dikte van de metalen coating, waarmee na "dicing" een opbrengst van 100% is bereikt.

- Gebaseerd op de toepassing van een optisch encodersysteem-in-"package", is het TPVO-C-QFN-proces ontwikkeld met optische TPV's als verticale microvensters. Optische TPV-structuren met een hoogte van 300 µm en laterale afmetingen variërend van 70 µm tot 1000 µm worden vervaardigd met gebruikmaking van SUEX droge film. Er worden verschillende uitdagingen geïdentificeerd, waaronder het geel worden van SUEX-materiaal als gevolg van polymeerdegradatie, barsten van het polymeermateriaal als gevolg van mechanische spanning, ingesloten microbellen aan de TPV-naar-chip-interface als gevolg van de lamineer techniek en ingieten van TPV-structuren als gevolg van niet- uniformiteit van TPV-hoogte.

- Gebaseerd op de toepassing van een ingegoten pcb-display met doorlopende gaten, is het TPVH-N-PCB-proces ontwikkeld waarin een hoge dichtheid grote arrays van TPV-holle structuren is aangebracht. De TPV holle structuur houdt de binnenkant vrij van het epoxy ingietmateriaal (EMC). Een reeks van meer dan 5000 ronde holle TPV-structuren wordt vervaardigd met een binnendiameter van 800 µm, een wanddikte van 110 µm, een hoogte van 300 µm en een steek van 1,2 mm. Ringvormen met microstructuren op de binnenzijwand van de TPV-ring zijn vervaardigd om het voordeel van TPV-technologie aan te tonen voor het maken deze fijne zijwandstructuren.

- Gebaseerd op de toepassing van een geminiaturiseerd 1x1 mm QFN-pakket met

micro-doorlopende gaten, is het TPVH-W-QFN-proces ontwikkeld met behulp van geminiaturiseerde TPV-holle structuren met een binnendiameter van 50 µm tot 300 µm en wanddiktes van 20 µm tot 40 µm. Het proces is ontwikkeld met zowel "spin-coated" SU-8 als gelamineerde SUEX. Voorheen verbeterde hechting van de TPV-structuren is de PEB-stap geoptimaliseerd en ingesteld op een temperatuur van 130 °C. Er worden ultra kleine TPV-holle structuren met een binnendiameter tot 60 µm en een wanddikte van 20 µm gedemonstreerd. Daarnaast, worden er ook andere holle structuren met een vierkante vorm, een driehoekige vorm en groepen holle structuren met kleine steekmaat en holle structuren met micropilaren erin gefabriceerd en gedemonstreerd.

Verder wordt er een grondig onderzoek gedaan naar de effecten van het voetprofiel en de dikte van de metalen coating om de mechanische sterkte van gemetalliseerde TPV's te verbeteren. Het TPV-profiel is verbeterd van een onder-sneden profiel tot een "olifantspoot" –profiel. TPV-diameters van 31, 66, 121 µm en de metaalbekledingsdikte variërend van 1,4 tot 5,6 µm worden in onderzoek genomen. Afschuifproeven worden uitgevoerd op drie verschillende afschuifhoogtes van 10, 45, 80 µm om de mechanische sterkte van de TPV's te karakteriseren. Een vergelijking van de afschuifkracht e van TPV's zonder coating en met 4,5 µm dikke Al (1 % Si) coating laat zien dat de maximale afschuifkracht voor de diameter van 31 µm, 66 µm, 121 µm toeneemt met respectievelijk 132 %, 122 %, en 76 %. De metalen coating heeft een sterkere invloed op de TPV's met een kleinere diameter. Naarmate de laagdikte van de metaal coating dikker wordt, neemt de toename van de mechanische sterkte af. Met diameters van 66 µm en 121 µm nemen de maximale schuifkrachten af bij een coating van 5,6 µm dik. De afschuifhoogte heeft meer invloed op de maximale schuifkracht van pijlers met een hogere aspectverhouding. In het geval van een pilaar met een diameter van 66 µm, met een aspectverhouding van de pilaar rond 2: 1, vertoont de maximale schuifkracht een afname van 49% van de laagste (10 µm) tot de hoogste (80 µm) schuifhoogte.

Ten slotte worden de werking van een 122 GHz radar Antenne-in-Package (AiP) met een on-package antenne-array met TPV als IC-naar-antenne-verbinding gekarakteriseerd en vergeleken met een conventionele radar AiP. De conventionele radar AiP maakt gebruik van draadbinding met een lengte van 350 µm om de IC met zijn antennearray te verbinden. De antennearray in de conventionele AiP wordt op een afzonderlijk substraat vervaardigd en naast een radar-IC geplaatst. Een open holte wordt gevormd tijdens het film-geassisteerde gietproces om de antennes bloot te leggen. Vergeleken met de conventionele AiP, is voor de AiP die in dit proefschrift met TPV-technologie is ontwikkeld de elektrische lengte van IC-naar-chip verminderd tot 150 µm en vermijdt daarmee de negatieve invloed van draadzwaai. Ook de door TPV gerealiseerde 3D-interconnectie maakt, in vergelijking met de conventionele AiP, een verdere miniaturisatie van de "package" mogelijk. Bovendien wordt de antenne laag rechtstreeks op het epoxy-ingiet materiaal vervaardigd, wat de kosten van extra antennesubstraten bespaart. Naast de bovengenoemde voordelen wordt het chip-bevestigingsvlak gebruikt als antennereflector. De gefabriceerde antenne-in-pakket (AiP) met TPV's wordt op een PCB-testbord gesoldeerd en een frequentie gemoduleerde continue golf (FMCW) -radarmeting wordt uitgevoerd. De FMCW-radarmeting meet de echosignaalsterkte over het detectiebereik van 10 m en genereert door middel van signaalverwerking met toepassing specifiek soft-

ware een constante vals-alarmfrequentie (CFAR). Een target wordt bevestigd wanneer het echosignaal een piek boven het CFAR-signaal laat zien. De AiP die in dit proefschrift is vervaardigd, heeft een hogere marge van het target signaal aangetoond in vergelijking met de conventionele AiP. In de uitgevoerde metingen heeft de AiP van dit werk de eerste en tweede targets gedetecteerd met doelsignaalmarges van 49,09 dB en 46 dB, wat 7,5 dB en 12,1 dB hoger is dan de conventionele AiP.

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# BIOGRAPHY

Hengqian Yi was born in Shawan, Leshan, Sichuan, He received a Bachelor of Science degree in solid-state electronic engineering from University of Electronic Science and Technology of China (UESTC), Chengdu, China in 2013. His research topic focused on *Nano-Structural Optimization of Li4Ti5O12 Cathode for $Li^+$ Battery Application*.

He received the Master of Science degree in Microelectronics from Delft University of Technology (TUDelft) in 2015. During his M.Sc. research, he designed, fabricated, and characterized a thermoacoustic speaker based on CNT nanofoam material. His work resulted in a Dutch patent,*Three-dimensional thermoacoustic device composed of nano-porous material and the method to fabricate such a device*, OCT-16-042.

From 2015 to 2019, he worked in the ECTM group in TUDelft as a Ph.D. researcher. His Ph.D. work was carried out under the framework of the NWO TTW (used to be STW) funded project *Through Polymer Vias: Bridging the gap between 2D and 3D*. He has been focusing on developing Through-Polymer Via (TPV) to a higher technology readiness level. Within his research, he has developed multiple application fields for TPV including 1), a radar antenna-in-package using metalized TPVs as the chip-to-antenna interconnection, 2), through-package windows using optical TPV, and 3), through-package holes using hollow TPV.

Since December 2019, he works as a postdoc researcher at TUDelft working for Chip Integration Technology Center (CITC). He is working in the Antenna-in-Package solutions program line focusing on packaging design and material characterization for 5G/6G applications.

# List of Publications

## Journal Papers

1. **H.Yi**, E.Öztürk, M.Koelink, A.A.Damian, J.Krimmling, W.Debski, H.W. van Zeijl, G.Q.Zhang and R.H.Poelma, *An Integrated 122-GHz Radar System with On-package Antenna Array using Through-Polymer Vias*, Submitted to IEEE Transactions on Microwave Theory and Techniques (2020).

## Proposal Contribution

1. **H.Yi**, H.W. van Zeijl, R.H.Poelma and G.Q.Zhang, *Heterogeneous VIAs for wide-bandgap-semiconductor applications in e-mobility*, NWO Toegepaste Technische Wetenschappen, HTSM (2018).

## Conference Papers and Posters

1. R.H.Poelma, **H.Yi**, X.J.Fan, H.W. van Zeijl, E.Boschman and G.Q.Zhang, *Characterization and Multi-scale Modelling of Nanofoam Materials for Microfabrication*, ICT.OPEN (2016).

2. **H.Yi**, R.H.Poelma, H.W. van Zeijl, E.Boschman and G.Q.Zhang, *Through Polymer Via Technology and Its Application in Antenna On Package (AOP)*, Nijmegen workshop (2018).

3. A.M.Gheytaghi, U.Hangen, **H.Yi**, S.Lemeshko and G.Q.Zhang *Coupled Electro-mechanical Characterization of Microstructures using Advanced Nanoindentation Test*, NanoBrucken2020 conference (2020).

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1. **H.Yi**, *Sino-Dutch International IC Technology Exchange and High Talent Summer School*, Tsinghua University, Beijing, China (2017).