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A Chip Integrity Monitor for Evaluating Moisture/Ion Ingress in mm-Sized Single-Chip Implants

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***Abstract*—For mm-sized implants incorporating silicon integrated circuits, ensuring lifetime operation of the chip within the corrosive environment of the body still remains a critical challenge. For the chip's packaging, various polymeric and thin ceramic coatings have been reported, demonstrating high biocompatibility and barrier properties. Yet, for the evaluation of the packaging and lifetime prediction, the conventional helium leak test method can no longer be applied due to the mm-size of such implants. Alternatively, accelerated soak studies are typically used instead. For such studies, early detection of moisture/ion ingress using an in-situ platform may result in a better prediction of lifetime functionality. In this work, we have developed such a platform on a CMOS chip. Ingress of moisture/ions would result in changes in the resistance of the interlayer dielectrics (ILD) used within the chip and can be tracked using the proposed system, which consists of a sensing array and an on-chip measurement engine. The measurement system uses a novel charge/discharge based time-mode resistance sensor that can be implemented using simple yet highly robust circuitry. The sensor array is implemented together with the measurement engine in a standard 0.18 μm 6-metal CMOS process. The platform was validated through a series of dry and wet measurements. The system can measure the ILD resistance with values of up to 0.504 peta-ohms, with controllable measurement steps that can be as low as 0.8 MΩ. The system works with a supply voltage of 1.8 V, and consumes 4.78 mA. Wet measurements in saline demonstrated the sensitivity of the platform in detecting moisture/ion ingress. Such a platform could be used both in accelerated soak studies and during the implant's life–time for monitoring the integrity of the chip's packaging.**

***Index Terms*—Chip integrity, flexible implants, encapsulation, interlayer dielectric (ILD), silicon dioxide, resistance, time-mode, monitoring, reliability.**

I. Introduction

Striving towards less invasive therapies and inspired by scaling within the semiconductor industry, in the past years, tremendous efforts have been made in miniaturizing active implantable medical devices (AIMDs) [1], [2]. Further scaling of AIMDs, however, has always been limited by the physical constraints of the battery [3], [4]. In this regard, wireless energy transfer techniques using electromagnetic [5], [6], [7], [8], [9] and acoustic energy [10], [11], [12] have been recently proposed as alternative energy delivery solutions that can circumvent the size restriction of the battery and enable the realization of free-floating mm-sized single-chip implants. These

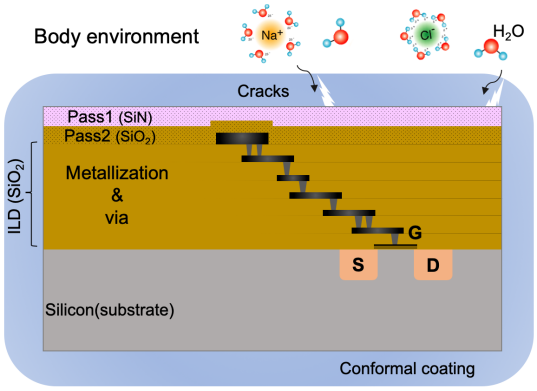

Figure 1. Schematic illustration of moisture/ion ingress through cracks for a conformally coated silicon die (dimensions not to scale).

mm-sized AIMDs can be instrumental in the expansion of new research fields within biology and medicine, e.g. implantable sensors [13], brain machine interfaces [14], neuroprosthetics [15], [16] and bioelectronic medicine [17], [18]. Furthermore, the low footprint of these devices, is expected to limit scarring and tissue inflammation [19], [20], making them ideal tools for pre-clinical and clinical research, and later on, for long-term therapy delivery.

Despite these great efforts, one of the remaining hurdles for introducing such tiny devices for clinical applications is ensuring their intended lifetime functionality when exposed to biofluids [21]. In wet ionic environments like the human body, failure of electronics can occur due to the ingress of moisture and ions through the packaging. For silicon integrated circuits, such ingress through the top passivation and interlayer dielectrics (ILD) would result in parameter changes in the passive (capacitive/resistive) and active (MOS transistor) components, as well as shorts and/or hard opens that would eventually lead to device failure [22], [23], [24]. Conventionally, AIMDs such as pacemakers and cochlear implants have relied on titanium (Ti) packages for protecting the inside electronics against the surrounding fluids. This packaging solution, however, no longer meets the dimensional requirements of mm-sized implants. For this reason, various biocompatible polymeric [16], [25] and/or thin ceramic [26],

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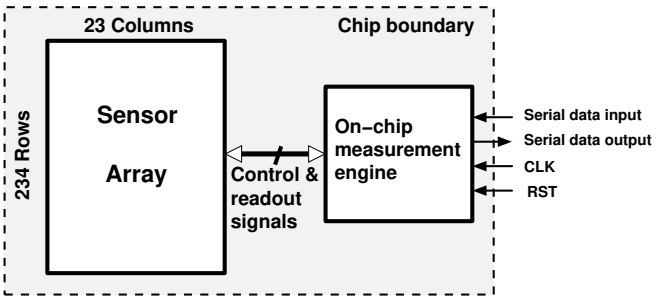
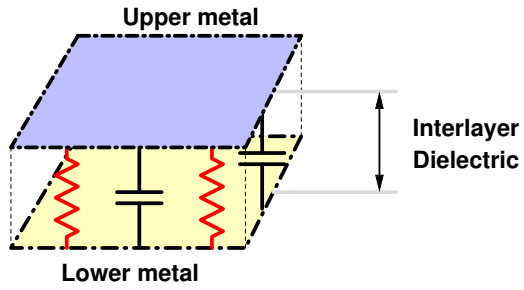
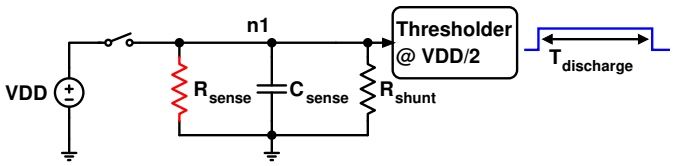


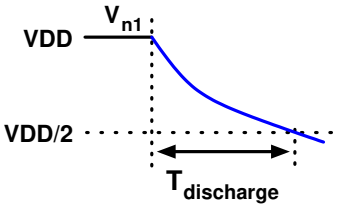
Figure 2. Block diagram of the implemented system showing the sensor array used for ion and moisture ingress experimentation and the measurement engine used for automatic control, readout, and transmission of the measurement results to off-chip for further processing.



(a) Interlayer dielectric (ILD) RC components



(b) Simple model of the proposed measurement method



(c) Discharge operation and timing

Figure 3. The proposed ultra-high resistance measurement method.

[27], [28] conformal coatings have been proposed which add minimally to the overall size and weight of the device and could make possible the realization of more flexible implants [29], [30], [31]. These protective coatings usually feature high barrier properties and aim at increasing the lifetime operation of the chip by blocking moisture and ions ingress. Despite this protection, ingress of moisture/ions could still occur either through delamination or imperfections such as cracks in the coating (Figure 1) and result in device malfunction and potential safety hazards.

To justify the use of conformally coated mm-sized implants for pre/clinical practices, their operational functionality has to be guaranteed for the intended duration of the study. So far, the lifetime functionality of AIMDs has been predicted using the standardized helium leak test method [32]. This test, however, cannot be applied to conformally coated single-chip implants, mainly due to their small size and lack of cavities [23]. In these cases, a statistical prediction is used instead, which is based on accelerated aging tests on a large group of samples. During such tests, incipient detection of moisture/ions ingress will grant a better understanding of the failure mechanisms within the chip and ultimately result in a more accurate lifetime prediction [25], [33].

In this work we propose and present the implementation of an in-situ sensor array for early detection of moisture/ion infiltration within a CMOS chip. The measurement principle employed for such a sensor array, supported by a proof of principle, was first presented in [34]. Here, in this extended manuscript, previously unpublished circuit analysis and details on the design and implementation of the proposed sensor are reported. Furthermore, additional characterization of the system in wet environments shows the more complete functional capabilities of the system. The presented and employed sensing method is based on tracking the resistance change in the interlayer dielectrics between successive metal layers in the chip, which act as ingress sensors. To verify the functionality and capability of the ingress sensors, we implemented a platform that can track the resistance change throughout the 234x23 sensor array and at different depths of the chip. The block diagram of the implemented system is shown in Figure 2. Time-mode operation as described in [35] is used, where a pulse width carries the measurement information, and quantization of pulse width measurements are used to detect the changes in the ILD with a tuneable measurement range and measurement accuracy.

The organization of this paper is as follows: the top-level overview of the proposed time-mode ILD resistance measurement concept is introduced in Section II and the design of the sensor pixel is presented in Section III. Chip implementation details and the measurement setup are shown in Section IV, followed by the measurement results in Section V. The discussion on the implemented system and the measurement concept are presented in Section VI, and, finally, conclusions are drawn in Section VII.

II. ILD Resistance Measurement

A. Measurement concept

The proposed ILD resistance measurement method is based on measuring the (RC) time constant of the ILD (Figure 3(a)) between two successive metal layers. In our method, a node with extremely high resistance in parallel to a capacitance, in this case the upper metal layer, is charged. The lower metal is hardwired to ground. Later, that same charged node is left floating to discharge through the ILD resistance. By measuring the actual time needed to discharge the capacitance and accounting for the known value of the total node capacitance, it is possible to calculate the ILD resistance.

A simple model of the method is shown in Figure 3(b). **n1** is the node that is charged and then left floating when the switch opens, R_{sense} is the resistance of the ILD oxide, representing the irregularities in the oxide structure that is intended to be monitored, C_{sense} is the oxide capacitance between the floating

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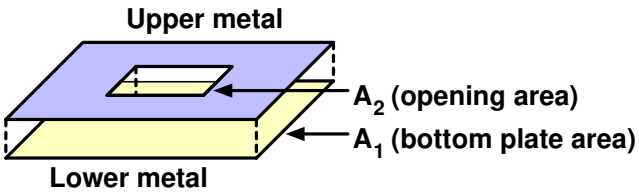

Figure 4. Optimization of openings in the top metal layer for maximum sensing capability.

node and the ground plane, and R_{shunt} represents all the other current leakage paths due to the active elements connected to **n1**. As the model in Figure 3(b) shows, a familiar parallel RC circuit is created once the switch opens. The total stored charge on the capacitor will discharge through the resistors as shown in Figure 3(c). The voltage at **n1** is VDD just before the switch opens, and after that, at time *t*, it is given by

$$V_{\mathbf{n1}}(t) = \text{VDD} \cdot e^{-t/R_{eq}C_{eq}} \tag{1}$$

where $R_{eq} = R_{sense} /\!/ R_{shunt}$ and C_{eq} is the combination of all the capacitances to ground at node **n1**. By measuring the time it takes for node **n1** to be discharged to a specific value, in our case VDD/2, the RC time constant between **n1** and ground may be measured with a very high accuracy. For a target discharge threshold of VDD/2, the discharge time and the RC time constant at **n1** are given by

$$T_{\text{discharge}} = \ln(2) \cdot R_{eq}C_{eq} \tag{2}$$

$$R_{eq}C_{eq} = \frac{T_{\text{discharge}}}{\ln(2)} \tag{3}$$

B. Sensor Element Optimization

To maximize the sensing capability and allow the water molecules or ions to pass into the ILD for measurement, there should be openings in the upper metal layer of the sensor - see Figure 4. Assuming there is an ingress event over the pixel area covered with the sensor element (A_1), for the water molecules or ions to be successfully detected, the ingress event needs to happen over the window of the opening between the upper and lower sensor plates (A_2) and propagate towards the ILD between the upper and lower metals. Therefore, the probability of measurable ingress is given by

$$p_{ingress} = \frac{A_2}{A_1} \tag{4}$$

As the ingress is detected and quantified by measuring the change in the resistance of the ILD, the intersection area between the upper and lower metals ($A_1 - A_2$) represents the sensing capability of the sensor element. Therefore, to maximize the sensing capability of the sensor element, the ratio of the area of the opening of the upper metal and the total area of the sensor element should be optimized. The opening on the top metal layer is optimized for maximum sensing capability by solving

$$\frac{\partial}{\partial A_2} p_{ingress} \cdot (A_1 - A_2) = 0 \tag{5}$$

which results in

$$A_2 = \frac{A_1}{2} \tag{6}$$

meaning the area of the upper metal layer, $A_1 - A_2$, should be half the area of the lower metal.

C. Sensing Performance

The measurement capability of the implemented pixel depends on the sensor element design and process parameters. The ILD resistance, which is the quantity to be measured, is given by

$$R_{sense} = \rho \frac{L}{A} \tag{7}$$

where R_{sense}, ρ, L, and A are the resistance, electrical resistivity, length, and area of the ILD between the sensor plates, respectively. As reported in [36] and [37], ingress and absorption of moisture/ions in SiO2 films can reduce their electric resistivity. The reduction rate, however, may not necessarily be linear and depends on the properties of the dielectric layer, e.g. composition, density, porosity and levels of defects. As the change in electrical resistivity is monotonic with increasing ingress but not linear, the platform proposed in this work is designed to track the changes in the dielectric resistance and linear change in the electrical resistivity is not a requirement for correct operation.

For the $0.18\,\mu$m process used, the distance between the metal plates (L) is $1\,\mu$m and for the chosen sensor implementation that will be presented in Section III, the area is $58.17\,\mu\text{m}^2$. The value of ρ depends on the manufacturing process, and its value ranges between $10^{12}\,\Omega$m [37] and $10^{16}\,\Omega$m [24]. Based on these values, the ILD resistance of the sensor is expected to be in the peta-ohm to exa-ohm [10^{15} - 10^{18}] range.

The measurable time constant of the sensor pixel is given by

$$\tau = R_{meas} \cdot C = R_{meas} \cdot C_{sense} + R_{meas} \cdot C_{upper} \tag{8}$$

where τ is the time constant, R_{meas} is the effective measurable resistance between the metal layers of the sensor element, C_{sense} is the capacitance between the metal layers, and C_{upper} is the total capacitance (except that of the sensor plates) to the ground connected to the upper metal layer of the sensor. The resistance R_{meas} is the parallel equivalent of two resistive elements, the ILD resistance (R_{sense}) and a resistance value (R_{shunt}) denoting the leakage due to the active elements connected to the charged node, and is given by

$$R_{meas} = R_{sense} /\!/ R_{shunt} \tag{9}$$

$$R_{meas} = \frac{R_{sense} \cdot R_{shunt}}{R_{sense} + R_{shunt}} \tag{10}$$

As we are interested in the changes in R_{sense} due to an ingress event, the way a change in R_{sense} results in a change in the measurable resistance R_{meas} is of importance. The unit change in R_{meas} due to a unit change in R_{sense} is given by

$$\frac{\partial R_{meas}}{\partial R_{sense}} = \frac{R_{shunt}^2}{(R_{shunt} + R_{sense})^2} \tag{11}$$

$$\Delta R_{meas} = \underbrace{\frac{R_{shunt}^2}{(R_{shunt} + R_{sense})^2}}_{\text{resistance transfer coefficient}} \cdot \Delta R_{sense} \tag{12}$$

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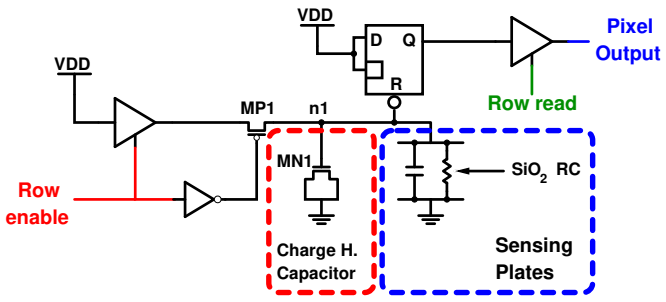

Figure 5. Schematic of the measurement pixel. The charge holding MOS capacitor and the sensing plates for measuring the oxide degradation are marked.

For our implementation and the process used, the total leakage current from the upper metal plate (node **n1**) is simulated to be 3.42 fA, resulting in an average R_{shunt} value of 526 TΩ. This value of R_{shunt} matches perfectly with our measurements presented in Section V and sets the upper limit of measurable resistance. Furthermore, any change in R_{sense} will be measured after being multiplied by the resistance transfer coefficient (RTF) in (12). In (12), as R_{shunt} gets larger, i.e., as any of the leakage currents of the active elements connected to the measurement node get smaller, RTF gets larger resulting in a larger ΔR_{meas}, i.e., a greater change in the measured resistance. Therefore, during the design of the measurement pixel, care should be taken to minimize the current leakage from the measurement node.

III. Sensor Pixel Circuit Design

A. Sensor pixel schematic

The ILD resistance measurement concept presented in the previous section has been designed and implemented in a 0.18 μm standard CMOS process with 6 metal layers. The schematic of the novel resistance sensor pixel is presented in Figure 5. The implemented pixel consists of CMOS logic gates from the standard cell library (3-state buffers, an inverter, and a D-latch with active-low reset), a MOS capacitor (MOSCAP), a high-threshold PMOS transistor, and sensor metal plates.

The MOSCAP (MN1) in each pixel is used to store charge and reduce the effect of parasitic capacitances and process mismatch capacitance variations at **n1**, reducing the pixel-to-pixel variation on the calculated resistance. In our implementation, we used an NMOS MOSCAP. During the operation of the pixel, node **n1** varies between VDD when fully charged and VDD/2 just before the pixel output switches down. As MN1 is always in strong inversion during operation, and the source, drain and bulk of MN1 are all tied together to the ground node, the change in the effective gate-bulk capacitance of MN1 is minimal [38]. In our simulations, for a very slowly changing (over 1s) gate-bulk voltage from VDD to VDD/2 the instantaneous gate-bulk capacitance of MN1 varied between 17.26 fF and 17.54 fF, and had an average capacitance value of 17.5 fF.

The high-threshold PMOS transistor (MP1) is used to further reduce the current leakage path through the 3-state buffer. By the insertion of MP1, measurement node current leakage

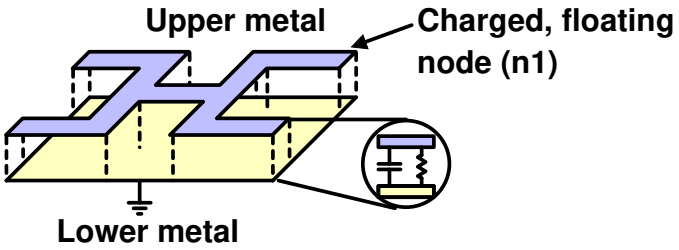

Figure 6. Capacitor structure for sensing the changes in the SiO_2 between the metal plates.

is reduced from 7.93 pA to 3.42 fA, effectively increasing the maximum measurable resistance from 227 GΩ to 526 TΩ. When transistor MP1 is turned off, this will result in charge injection, effectively charging node **n1** to a value slightly greater than VDD. However, this injected charge amount does not change from cycle to cycle, i.e., from reading to reading for a pixel, and is a fixed amount. Thus, this will result in a fixed increase in the pulse width generated by the pixel. As the targeted measurement methodology is based on comparing every reading of a pixel to a reference golden reading, i.e., when the surface of the chip is dry and there is no ingress, the results of both the dry and wet readings will be shifted by the same amount as the capacitance at **n1** doesn't change. Therefore, the effect of charge injection at **n1** is inconsequential and does not affect the expected results from the measurements.

Finally, sensing metal plates to sense the change in the ILD oxide over the pixel, as explained in the previous section, are placed over the active circuitry during the implementation. Depending on the metal layers used, ILD capacitance between the sensing plates varies between 6 and 7 fF and the implementation details of the sensor plates are presented next.

B. Sensing Plates Implementation

Based on our sensor area optimization analysis presented in Subsection II-B, we opted for a sensor structure as shown in Figure 6 to evenly distribute the possible ingress paths over the sensor within the constraints of the layout rules.

In each pixel, two successive metal layers are used as the sensing plates to monitor the changes in the properties of the oxide over the pixel (Figure 6). The top plate of the sensing structure is connected to node **n1** (the measurement node) and the bottom plate is connected to ground. In the implementation presented in this paper, there are three different versions of the sensor pixel shown previously in Figure 5, with the same active circuitry and with different metal layer pairs, namely M6-M5, M5-M4, and M4-M3.

In the layout of the sensor array to be presented in Section V, the active circuitry for each sensor cell is the same and cells with different sensor capacitors are placed alternatingly in each direction, i.e., x and y. For example, an M6-M5 cell is followed by an M5-M4 cell, which is followed by an M4-M3 cell. Such a placement is presented in Figure 7. In the extracted layout, it was seen that the total capacitance at **n1** varies between 23.5 and 24.5 fF, depending on the used metal layer pair. With such an implementation, different

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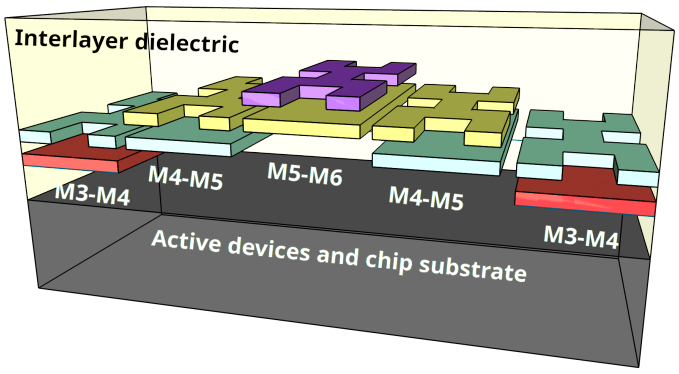

Figure 7. Placement of pixels utilizing different metal stacks as the sensing element.

metal combinations give us the ability to track the changes at different depths of the ILD over the chip surface area.

C. Operation and the Control of Sensor Pixel

The timing diagram of the pixel is shown in Figure 8. *Row enable* and *Row read* signals are controlled and supplied by digital pixel control circuitry. The operation of the pixel is as follows: When the ILD resistance of a pixel is to be measured, the *Row enable* signal for the chosen pixel row is raised for one clock cycle. During this cycle, the input 3-state buffer and the high-threshold PMOS transistor MP1 are turned on, charging node **n1** to VDD through the 3-state buffer. The node charge is stored on the MOSCAP, the SiO_2 capacitance of the sensing plates, and the parasitic capacitances at **n1**. The MOSCAP is the main charge holding element due to its capacitance, i.e., 17.5 fF. As soon as node **n1** is charged, the reset of the latch is released, and the output of the latch is automatically set to VDD, as both the D input and enable signals of the latch are connected to VDD. In the next clock cycle two things happen in parallel: i) *Row enable* is lowered, effectively stopping the charging process by turning off both MP1 and the input 3-state buffer, thus, leaving node n1 floating, and ii) *Row read* is raised to read the pixel output at the column output. It should be noted that the output 3-state buffer is used for an array implementation as explained next. If the sensor pixel is to be used in a standalone fashion, e.g., as one of the integrity monitor sensors spread over the chip area, it can be

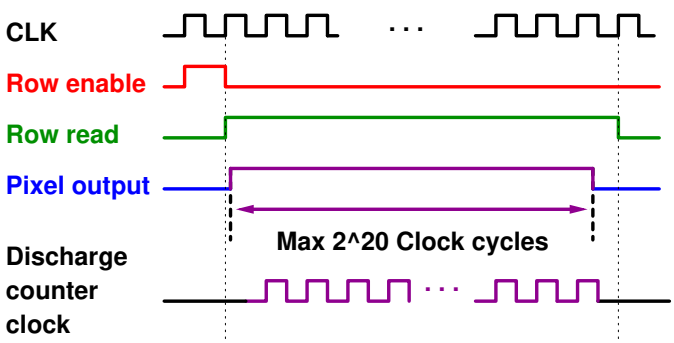

Figure 8. Timing and operation of the measurement pixel.

safely removed from the pixel to reduce the area and power consumption.

In the test chip to be presented in Section V, an array of sensor pixels and a digital measurement engine for controlling the pixels and to quantize the time measurement were implemented. During the operation, the pixel to be measured is selected through the use of *Row enable* and *Row read* signals by the measurement engine. As soon as the pixel output is enabled with the *Row read* signal and raised (the Q output of the latch is already at VDD), the 20-bit counter in the measurement engine becomes enabled and starts counting with *CLK*. The count stops when either node **n1** is discharged below the reset threshold (VDD/2) of the latch, resetting the latch (Q goes low), or a count of $2^{20}-1$ is reached. Thus, by counting the clock cycles the quantization of the time pulse generated at the output of the pixel is realized.

D. ILD Resistance Measurement Process

The measurement process of the ILD oxide change uses the self-reset feature of the latch in Figure 5, and is as follows. When node **n1** is left floating after *Row enable* goes low, the possible discharge paths are through the oxide resistance of the ILD and the current leakage paths of the active elements denoted by the shunt resistance connected to this node in the model. The active element current leakage paths are the leakage path through MP1 and the output of the 3-state buffer, the gate leakage through the latch, and the gate leakage of MN1. It is first assumed, and later proven through measurements in Subsection V-B, that, in the presence of water or ions in the ILD layer, the dominant discharge path for **n1** will be through the ILD oxide. Therefore, we use the variation in the discharge time of node **n1** to track the changes in the resistance (dominant) and capacitance (less pronounced) of the SiO_2 layer between any two metal layers that act as our sensing plates (Figure 6). Finally, we deduce the time it takes **n1** to discharge to VDD/2 by monitoring the output of the pixel (Q) and convert the pulse width at Q to a time count, and calculate the measured resistance using this time count.

In the absence of water molecules and ions in the ILD SiO_2 layer between two successive metals, the resistance of the ILD will be very high (in the order of peta-ohms, 10^{15} ohms) and in a dry state the dominating resistance at node **n1** will be mainly from the active element leakage currents. However, as the chip integrity is breached and water molecules and ions penetrate the ILD layers, there will be multiple changes but mainly: i) the conductance of the ILD SiO_2 that has been breached will increase (i.e., the resistance will reduce), and ii) due to the presence of water molecules and ions, the dielectric constant of the SiO_2 will increase, hence increasing the capacitance of the layer. In such a case, if a lower discharge time count is monitored, we can conclude that the reduction in the resistance is higher than the increase in the capacitance. Moreover, during the measurement process, we expect the discharge time of **n1** to be reduced proportionally to the reduced resistance, which in turn is inversely proportional to the amount of ions and molecules in the ILD.

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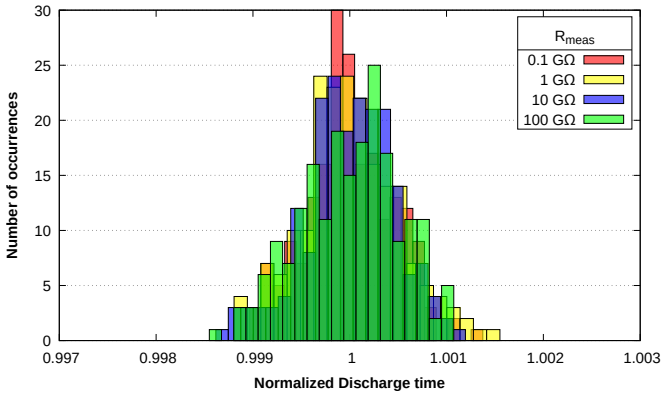

Figure 9. $T_{discharge}$ variation due to the noise in the system.

E. Noise performance

Another metric that affects the quality of the resistance measurement of the ILD is the inherent noise that is coming from the active circuitry. As the measurement is done in time-mode, i.e., the width of a pulse is measured, jitter of the generated pulse should be used as the noise metric. Therefore, the signal-to-noise ratio (SNR) of the measurement pixel can be defined as:

$$\text{SNR} = \frac{T_{discharge}}{\sigma_{\text{jitter}}} \tag{13}$$

where σ_{jitter} is the jitter that is caused by the noise sources in the measurement pixel.

RMS noise voltage σ_n of the circuit can be transferred from the voltage domain to the time-domain jitter (σ_{jitter}) by using (14). In this equation, the change in time is slow and is dominated by $T_{discharge}$. Therefore, ∂t can be approximated to be equal to $T_{discharge}$. Furthermore, assuming the discharge operation ends at VDD/2, we can approximate ∂V to be equal to VDD/2 and rewrite (14) as (15).

$$\sigma_{\text{jitter}} = \sigma_n \cdot \frac{\partial t}{\partial V} \tag{14}$$

$$\sigma_{\text{jitter}} = \frac{2\sigma_n}{\text{VDD}} \cdot T_{discharge} \tag{15}$$

$$\sigma_{\text{jitter}} = \frac{2}{\text{VDD}} \cdot \sqrt{\frac{k \cdot T}{C}} \cdot T_{discharge} \tag{16}$$

The pixel operation can be thought of being akin to a sampled system and an integrator. As the discharge happens through a passive element and off transistors (through gate leakage), the RMS noise voltage in (15) can be defined as the thermal noise on the total capacitance connected to the measurement node, i.e., $\sqrt{\frac{k \cdot T}{C}}$, where k is Boltzmann's constant, T is the temperature in kelvin, and C is the total capacitance of the node. By replacing the σ_n in (15) with the thermal noise, we reach the final equation for the σ_{jitter} of the measurement pixel in (16). By combining (13) and (16), the SNR of the pixel is given by:

$$\text{SNR} = \frac{\text{VDD} \cdot \sqrt{C}}{2 \cdot \sqrt{kT}} \tag{17}$$

In (17), it should be noted that the SNR of the measurement pixel does not depend on the discharge time and is solely set by the discharge threshold (VDD/2 in this case) and the total capacitance connected to the measurement node. For a capacitance value of 24 fF to ground, the SNR of the pixel at room temperature is calculated to be 2167, which translates to an SNR of 66.72 in dB.

To verify our calculations, transient noise simulations were performed on the extracted pixel netlist using HSPICE. As the transient noise simulations require extensive computing resources for long simulations, the value of R_{shunt} was reduced artificially by adding a much lower valued resistor in parallel, effectively reducing the equivalent measured resistance R_{meas}, and hence the discharge time as given in (2). 200-point transient noise simulations were run for R_{eq} values of 0.1, 1, 10, and 100 GΩ and the results are given in Figure 9. The figure shows the normalized transient noise simulation results. The discharge time values for each forced R_{meas} are normalized to their respective means and are plotted together to show that the variation due to the noise does not depend on the effective resistance measured. In the simulations, the SNR of the pixel varied between 65.88 dB and 67.06 dB for different R_{meas} values, confirming our derivations.

IV. Chip Implementation and Test Setup

A. System Implementation

To verify the proposed ILD resistance measurement method, an array of sensor pixels is implemented as shown in Figure 11. The array consists of 234 rows and 23 columns. To control the pixels during the measurement and to measure each pixel's value, a fully-digital measurement engine that can automatically scan all the cells for integrity and degradation within the SiO_2 ILD is implemented. In the array, *Row enable* enables a row of pixels for sensing, and *Row read* enables the output of the chosen row's pixels. All columns from the array are fed to the measurement engine (*Pixel outputs*) and the column to be measured is selected inside the measurement engine, and the pulse at the chosen pixel is quantized.

To ease the handling of the device during tests in wet environments, we minimised the number of bonding pads to 6 in total by using a serial-in, serial-out architecture. The clock (*CLK*) and reset (*RST*) signals together with the data-input port (*dataIn*) are used for controlling the on-chip measurement engine externally, and the output is sent off-chip through *dataOut*. As will be shown in Section V-A, it is possible to change both the accuracy and maximum resistance measurement capability of the system by changing the clock frequency, hence adapting the system for different measurement conditions.

A prototype system containing the sensor array and the measurement engine core is implemented in a 0.18 μm standard CMOS process. Figure 10(a) shows the implemented chip together with the polydimethylsiloxane (PDMS) covering the pads and wire bonds. For proof of concept, in this paper, all the dry and wet measurements are done with bare dies where the top passivation is the only insulating layer. For this aim, PDMS is only applied over the pads and wire bonds leaving the

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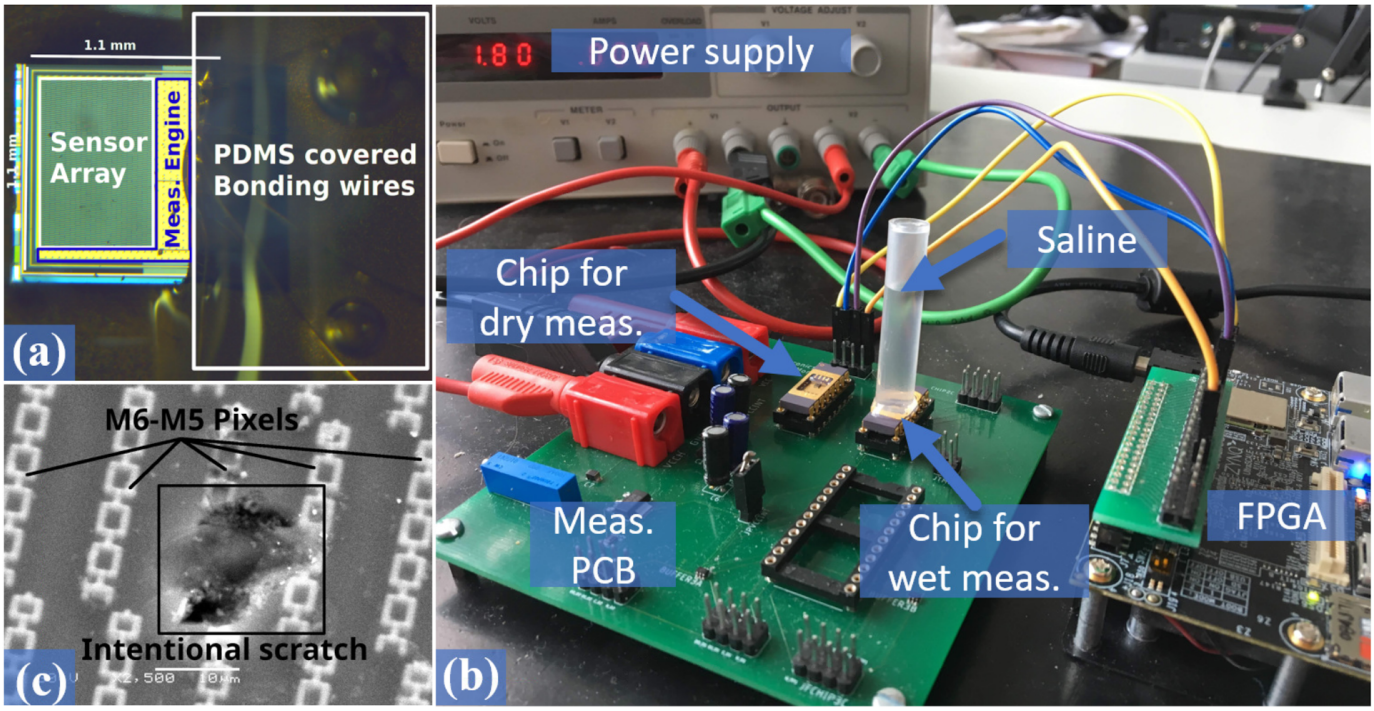

Figure 10. (a) Chip photo showing the sensor array, measurement engine, and polydimethylsiloxane (PDMS) covered bonding wires. (b) Measurement set-up showing the custom designed PCB used for both dry and wet measurements. (c) SEM image illustrating the intentionally scratched passivation surface of the chip. Pixels with M6-M5 sensor plates are marked.

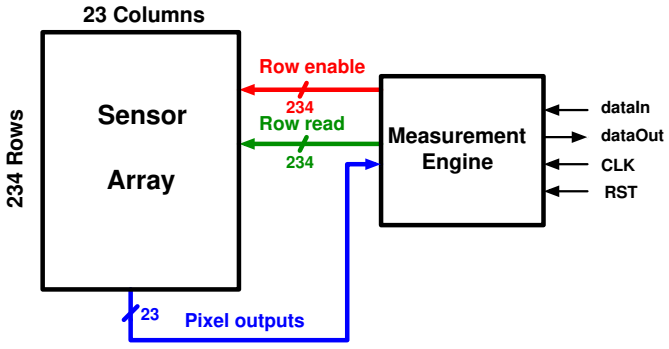

Figure 11. Implemented sensor array with on-chip measurement engine showing top-level signals.

sensor array fully exposed. The total chip area including the bonding pads is 1.1 mm x 1.1 mm. The sensor array consists of 5382 sensor pixels, with varying metal sensor plate structures, as explained previously. The size of each pixel is 3.92 μm by 29.68 μm, hence giving the same resolutions in the y and x directions, respectively.

B. Test Setup

The custom test setup consists of a PCB, a power supply and an FPGA board (Ultra96) to control the on-chip measurement engine, and to save and process the data from the chip in realtime (Figure 10(b)). The custom-designed PCB and the measurement and processing code running on the FPGA accommodate measuring three packaged chips at the same time. A setup for both dry and wet measurements is shown in Figure 10(b). To facilitate wet measurements, a tube was placed and glued to the lid opening of the chip package to the hold the test liquid. The tube joints were further supported by the PDMS to minimize the risk of liquid leakage to the electronic measurement setup.

V. Measurement Results

All the measurements presented in this section were done while the chip was supplied by a 1.8 V voltage source and the average current consumption during the measurements was 4.78 mA, which also includes the consumption of the ESD protection circuitry. The measurement engine consumes 2.72 mA while being operated with a 75 MHz clock and per pixel current consumption during the pixel measurement is 18.34 μA.

A. Dry measurements

The first measurements are done in dry conditions to verify the correct operation of the system and determine the measurement capabilities. For each chip, the dry measurement results also serve as the golden reference for comparing to the wet measurements and for calculating the possible amount of ingress. The external clock for the measurement engine is generated and supplied by the FPGA board and is adjustable from 75 MHz down to 125 kHz.

The tuning of the clock frequency allows for measurement of the discharge time with varying accuracy and maximum resistance limits. For example, for a clock frequency of 50 MHz, the minimum discharge time-step that can be measured is 20 ns. Using (3), and an average value of 24 fF for C_{eq}, it

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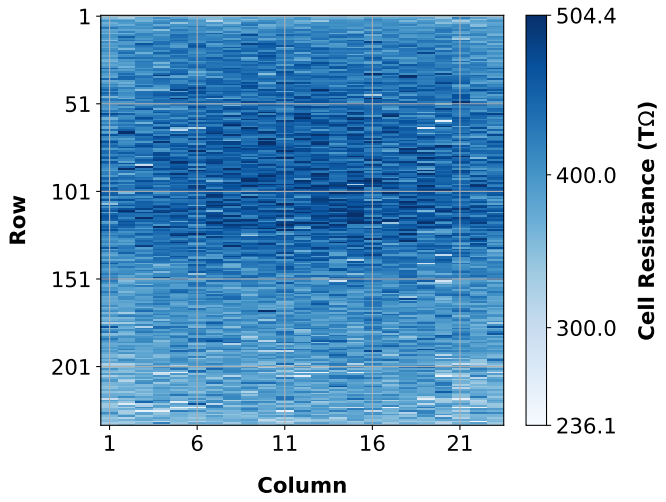

Figure 12. Dry measurement results for the whole sensor array. Calculated resistance varies between 0.236 PΩ and 0.504 PΩ due to intra-die process variation and the environment temperature changes during the measurements.

can be calculated that the minimum measurable resistance change for a 50 MHz clock is 1.2 MΩ. Any changes greater than 1.2 MΩ will be captured by the system as a change in the discharge counter, with a maximum measurable value of 1.26TΩ. To increase the measurement range, the external clock can be reduced to a lower frequency, e.g., 125 kHz, where the maximum measurable resistance becomes 0.504 peta-ohm $[0.504 \cdot 10^{15}\Omega]$.

The upper limit of applicable clock frequency is due to the critical path of the on-chip measurement engine and any input clock frequency higher than 75 MHz will result in functional errors. The lower limit of the clock frequency is set by the maximum measurable resistance due to the active element leakage currents, i.e., due to R_{shunt}. Any clock frequency lower than 125 kHz will not improve the maximum measurable resistance and will only increase measurement time. To measure all the pixels with a 125 kHz clock, approximately 12.5 hours are needed. Results of such a measurement, which also serve as a reference for the wet measurements for this particular chip, are presented in Figure 12, showing the measurement capabilities of the implemented platform. The implementation details and the capabilities of the system are summarized in Table I.

Table I
SPECIFICATIONS AND PERFORMANCE SUMMARY

Operating voltage	1.8 V
Total current consumption (including ESD)	4.78 mA
Total chip area	1.21 mm^2
Pixel area	116.35μm^2
Number of pixels	5382
Sensor array area	0.643mm^2
Max. measurable ILD resistance	0.504 PΩ
Min. detectable ILD resistance change	0.8 MΩ
Per pixel current consumption	18.34 μA
Measurement engine (ME) area	0.14 mm^2
ME max. operation frequency	75 MHz
ME current consumption @75 MHz	2.72 mA

B. Wet measurements

In the next verification step, we performed wet measurements to verify the ILD resistance change concept and the capabilities of the implemented platform in tracking water/ion ingress through the ILD stacks. Our earlier wet experiments after two weeks of continuous soaking of the test chips in saline showed no changes in the array resistances when compared to dry measurements. This suggests the good insulating properties of the chip passivation provided by the foundry. Therefore, to test the ingress monitoring functionality of the proposed circuit in a controlled environment, modifications were made on the chip passivation surface.

In the first test sample, we intentionally introduced three scratches on the chip passivation layer using an ultrasonic cutter. This allowed faster propagation of water/ions into the chip ILD layer. A SEM image of one such scratch is shown in Figure 10(c). After scratching the surface of the chip, measurements under different conditions, i.e., dry and wet, were made using a 50 MHz measurement clock. This clock value was chosen to increase the accuracy of the measurements as explained previously. Figure 13 shows the results of these measurements. In the first step, a dry measurement of the chip was done to serve as the reference. The scratched areas on the chip are seen as lighter colour pixels compared to the rest of the array in the figure. The lighter colours in the dry measurement (*Dry @0min*) indicate a faster discharge time and could either be due to an introduced damage in the sensor metals when scratching the passivation surface or due to foreign particles that got stuck in the ILD, reducing the measured resistance.

In the second step, we tested the chip in a phosphate-buffered saline (PBS) solution with a pH of 7.4. The solution was continuously kept on the sensor array using the tube (Figure 10(b)). Results of the measurement after soaking the chip in the solution for 90 minutes (*Wet @90min*), and the difference between the dry reference and wet measurements are shown in the middle and right panes of the top row of Figure 13, respectively. When the test sample was soaked, ingress occurred reducing the measured ILD resistance of the pixel. At 120 minutes after soaking the chip, another measurement was taken to verify both the effects of continuous exposure to the liquids and the resulting change in the oxide properties. The results for this measurement are shown in the second row of Figure 13. From the difference plot in this row, it is seen that ingress continues through the pixels and is reflected by further reduction of the cell ILD resistance.

Finally, another experiment was performed to verify the ILD resistance change when the liquid is removed. The liquid was removed from the tube, and after waiting for 60 minutes (180 minutes after the beginning of the measurements), another set of measurements was taken. The results are shown in the middle pane of the bottom row of Figure 13 (*Dry @180min*). During this final set of measurements, it was observed that as the liquid was removed from the chip surface, the ingress stopped, and actually, reversed, reflected by the higher resistance values, i.e., darker pixels in the figure, when compared to the *Wet @120min* measurement. The results presented in

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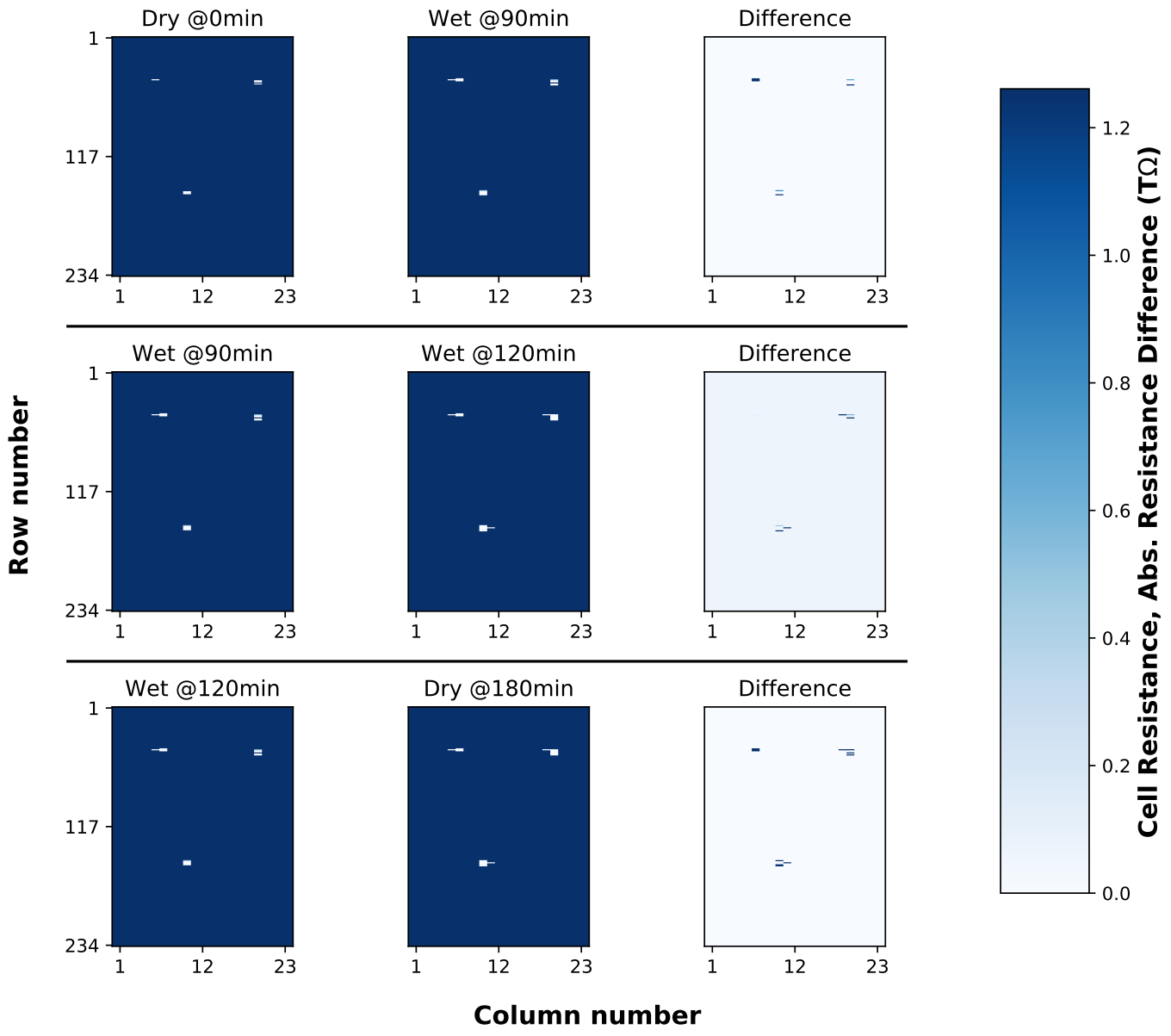

Figure 13. Dry, wet, and re-dried measurement results for a chip with scratched passivation showing how water/ion ingress through the scratched area can change the resistance in neighboring pixels.

Figure 13 show the monitoring capabilities of the chip in detecting changes in the ILD resistance as water/ions propagate in the chip structure over time, both through the damaged and undamaged neighboring cells.

Further measurements (Figure 14) were performed on another test chip to verify the real–time measurement capabilities. In this second test chip, the top passivation layers of a single pixel were removed using a focused ion beam (FIB) as shown in Figure 15. A different measurement protocol was followed for these measurements. An array of 3x3 pixels, where the FIBbed pixel is in the center, was measured continuously while the chip was soaked in a PBS solution. The measurement plots are shown in Figure 14. In the figure, only the FIBbed pixel is affected by the ingress due to removed passivation layers. The measurement steps taken were as follows. i) Put the PBS solution on the chip at t=0, ii) at t=127 minutes remove the PBS solution from the tube and continue the measurements. Just after putting the PBS solution on the chip at t=0, the measured sensor resistance decreased rapidly due to ingress, saturating around t=127 minutes at a resistance value of 3 GΩ. After the removal of the PBS, at t=127 minutes, the resistance began to increase slowly due to the lack of liquid, hence the stopped ingress and slow evaporation, on the chip surface and the ILD. Then, after t=364 minutes, the rate of increase of resistance increased due to evaporation of the water molecules from the ILD. After t=480 minutes the rate of evaporation decreases, finally saturating the resistance of the pixel in the >300 TΩ range. It should be noted that, during the measurements, the first cell to be read from is the top-left cell, therefore the beginning process of ingress, which

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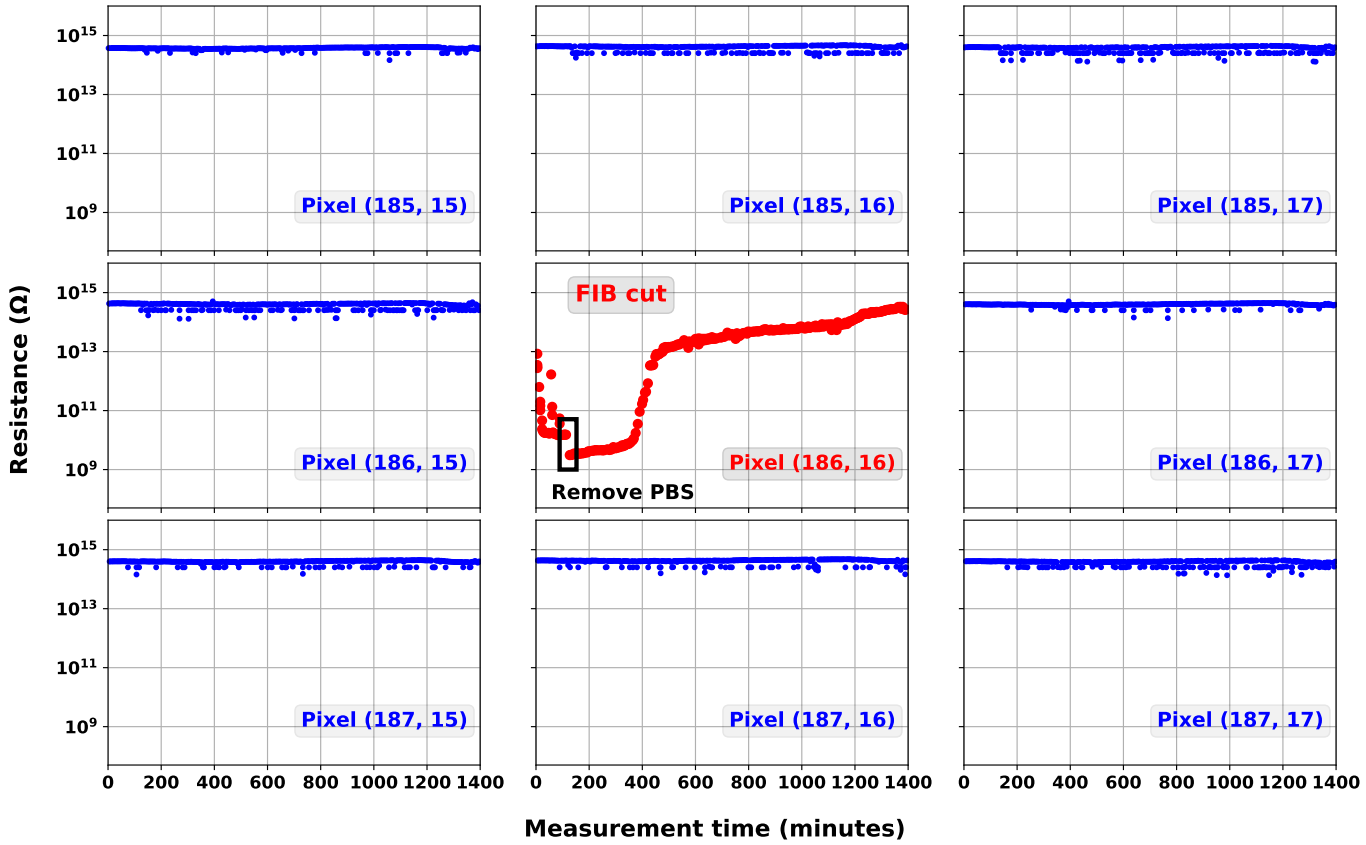

Figure 14. Results of the measurements of a scanned array of 3x3 with the Fibbed sensor pixel in the center. The array was scanned pixel-by-pixel continuously and both the ingress and evaporation after the removal of the PBS were observed.

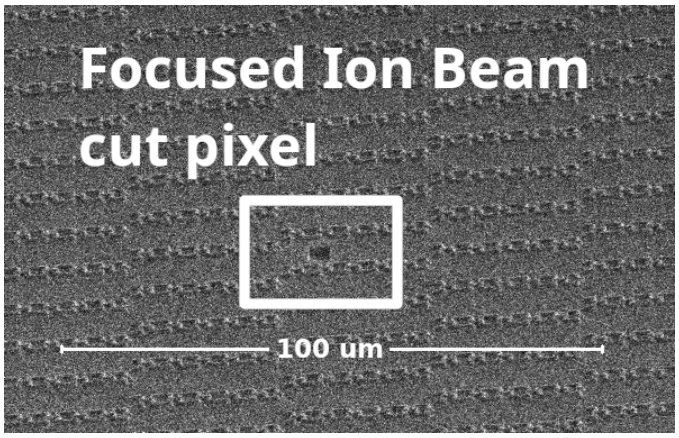

Figure 15. Close–up scanning electron microscope (SEM) image of the sensor pixel with a cut-out top passivation layer.

is very fast in the beginning, is not captured. This is reflected in our measurement as the first measurement value from the fibbed pixel is around 10 TΩ.

VI. Discussion

With the goal of higher miniaturization, great efforts have been put in realizing free-floating single-chip implants. For such devices, the first step to miniaturization has been by replacing the bulky battery power source by wireless energy transfer techniques, e.g. electromagnetic and ultrasound. The second step has been by incorporating most of the discrete components, capacitors and coils, inside the chip. The works reported in [6], [7] and [27] are three examples of such single-chip implants. For such systems, the chip integrity will determine the overall lifetime of the device. Therefore, we developed this platform with two main goals in mind: i) to be used as an investigational tool for evaluating the insulating properties of the added packaging layers, and ii) as an integrity monitor for free-floating single chip implants.

A. Evaluation and selection of materials

1) Thin conformal coating materials: One critical challenge in realizing single-chip implants is the right selection of coating materials that can guarantee the correct functionality of the device during and after its implantation. As previously explained, various biocompatible conformal coatings have been reported with the potential of being the suitable packaging solution for mm-sized implants. Nevertheless, the insulating properties of these layers are greatly affected by various factors, such as: adhesion of the coating to the substrate material, thermal expansion coefficient mismatch between the coating and the substrate and the coating deposition process. As an example, the protection offered by polymeric coatings, such as PDMS or parylene, greatly relies on their good adhesion to the substrate material [23], [39], as any adhesion failure

would result in water condensation on the chip due to the non-hermetic nature of polymers. Factors such as adhesion failure or moisture/ions ingress through the micro/nano cracks of the coating could only be evaluated during accelerated lifetime testing [25], [27]. During these tests, employing the platform presented in this work, would allow for an early evaluation of the coating on representative CMOS materials, thus increasing the certainty in the lifetime prediction of the active implant.

2) CMOS foundry materials: Once the top coating has been breached, the CMOS passivation and ILD layers will act as the barriers for protecting the metals and active components underneath. CMOS passivation layers are meant to block moisture and ions ingress, typically present in ambient environments, until their final packaging is done. The passivation and ILD layers are generally deposited using a plasma enhanced chemical vapor deposition (PECVD) process, making their mechanical and chemical properties considerably dependent on the deposition parameters [37]. Various studies have been investigating the underwater barrier properties of PECVD SiO2 and SiN layers [40], [41], all confirming the properties of such inorganic layers to be greatly dependent on their deposition parameters. Accordingly, the properties of the materials deposited by the CMOS foundries would also vary from the ones investigated elsewhere and should, therefore, be evaluated separately. Using the presented platform in bare silicon die (similar to the wet measurements given in the previous section) would allow for an evaluation of the barrier properties of the materials deposited by the CMOS foundries.

Another application of the sensor array could be to derive the time points for which moisture will propagate through the top passivation into the lower subsequent stacks of the ILD. Such information can potentially help in better understanding the failure mechanism of chips in ionic media and, therefore, help derive a better estimate on their lifetimes.

In general, we would like to emphasize that appropriate selection of materials, both for the conformal coating and the CMOS passivation/ILD, will greatly affect the overall lifetime of single chip implants.

B. Wireless monitoring for chronic studies

The platform reported in this work was originally meant to be used as an investigational tool for sensitive evaluation of the coating and characterizing ingress of water molecules and ions on the chip. Therefore, a sensor array was realized which occupied the majority of the chip surface. Furthermore, due to the required number of internal control signals to control the array, measurement engine internal column and row selection logic, and required high precision and resolution measurements, the measurement engine both occupies a substantial area and is power hungry. Nevertheless, the measurement concept can still be used by spreading the sensing cells on critical or sensitive areas of the chip. This way, the power consumption of the sensing platform could be radically reduced, as a single pixel is very power efficient, i.e., 0.97 nW and 33.01 μW are consumed for 0.6 V and 1.8 V operation, respectively. By coupling the presented pixel and time-mode measurement approach with an energy-efficient communication protocol such as single pulse harmonic modulation [42] as done in [43], it is both possible and feasible to create a monitoring unit for single-chip wirelessly powered or energy harvesting implants. In such a case, the distributed integrity sensing cells could be used to monitor the hermeticity of the chip in vivo. One can even imagine a scenario in which the sensor would communicate to the patient that a replacement of his implant is needed in the next six months, or in extreme cases, as a fuse, where the implant would stop its electrical functionality before any hazardous malfunction.

In the presented system, a fast clock is required for more accurate conversion of the generated pulse width to a digital value for a limited maximum measurable ILD resistance, e.g., 0.84 TΩ for a 75 MHz clock. As it can be seen in Figure 14, whenever there is an ingress event, the measured ILD resistance changes over a range of 6 orders of magnitude, from peta-ohms to giga-ohms. In a wireless implant scenario where the presented sensors are used for ingress detection, we are interested in the first detectable ingress event. Therefore, it is enough to sense a change occurring in the peta-ohms range, and when the proposed measurement method is implemented in an implant, a slow clock in the low 100 kHz range should suffice. Furthermore, this generated clock is used for operating a counter. As the counter in the present implementation is 20-bits long, it effectively averages the jitter coming from the clock source by a factor of 2^{20}, i.e., the jitter noise power in the pulse width measurement is reduced by 60 dB. Hence, we believe that the requirements for on-implant clock generation for the presented system are very relaxed and will not cause any problems in future implantable applications.

VII. Conclusions

In this paper, a fully integrated, standard-CMOS, chip integrity monitor array for investigative purposes has been presented. The sensor array chip has been implemented in a 0.18 μm standard CMOS process and utilizes novel charge/discharge based, time-mode pixels that monitor the changes in the sensing element's oxide through ultra-high resistance measurements. In addition to the sensor array, a digital measurement engine that continuously monitors the sensor readings is also implemented. The system measures the ILD resistance values up to 0.504 peta-ohm, with controllable measurement steps that can be as low as 0.8 MΩ.

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