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DOI
10.3390/electronics9121987

Publication date
2020

Document Version
Final published version

Published in
Electronics (Switzerland)

electronics

MDPI

Article

X-Type Step-Up Multi-Level Inverter with Reduced Component Count Based on Switched-Capacitor Concept

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Received: 21 October 2020; Accepted: 17 November 2020; Published: 24 November 2020

Abstract: This paper aims to present a novel switched-capacitor multi-level inverter. The presented structure generates a staircase near sinusoidal AC voltage by using a single DC source and a few capacitors to step-up the input voltage. The nearest level control (NLC) strategy is used to control the operation of the converter. These switching states are designed in a way that they always ensure the self-voltage balancing of the capacitors. Low switching frequency, simple control, and inherent bipolar output are some of the advantages of the presented inverter. Compared to other existing topologies, the structure requires fewer circuit elements. Bi-directional power flow ability of the proposed topology, facilitates the operation of the circuit under wide range of load behaviors which makes it applicable in most industries. Besides, a 13-level laboratory prototype is implemented to realize and affirm the efficacy of the MATLAB Simulink model under different load conditions. The simulation and experimental results accredit the appropriate performance of the converter. Finally, a theoretical efficiency of 92.73% is reached.

Keywords: multi-level inverter; self-balance; single source; bidirectional; switched capacitor

1. Introduction

Nowadays, due to the progress of power electronic devices, an increase in fossil fuel prices, and global tendency towards emitting fewer greenhouse gases, most industries tend to utilize renewable energy sources. Especially wind and solar energies have received a great deal of attention among them. Various types of electrical power converters are used to connect these renewable energy sources to the local grids, including inverters which perform the DC to AC power conversion. Multilevel inverters (MLIs), which can generate a high-quality voltage, have become more applicable recently [1–3]. They are capable of generating near sinusoidal staircase voltage, which leads to a remarkable decrease in voltage stresses across the switching devices (dv/dt) and total harmonic distortion (THD) of the output. Therefore, the output filter would be reduced in size or even removed [2,4–8].

MLIs play a significant role in applications such as fuel cells [9], solar panels [10], electric vehicles [11], wind turbines, and connecting them to the network grid [12]. The evolution of MLIs during time is illustrated in Figure 1. As conventional MLI topologies, neutral point clamped (NPC) [13], flying capacitor (FC) [14], and cascaded H-bridge (CHB) [15] have some weaknesses. These topologies have a few advantages over two-level inverters such as: Less switching and conduction losses, higher efficiency, and remarkably more power quality. On the other hand, they suffer from sophisticated control methods. Furthermore, NPC and FC struggle with voltage imbalance of their DC link capacitors and CHB requires several independent DC sources [16].

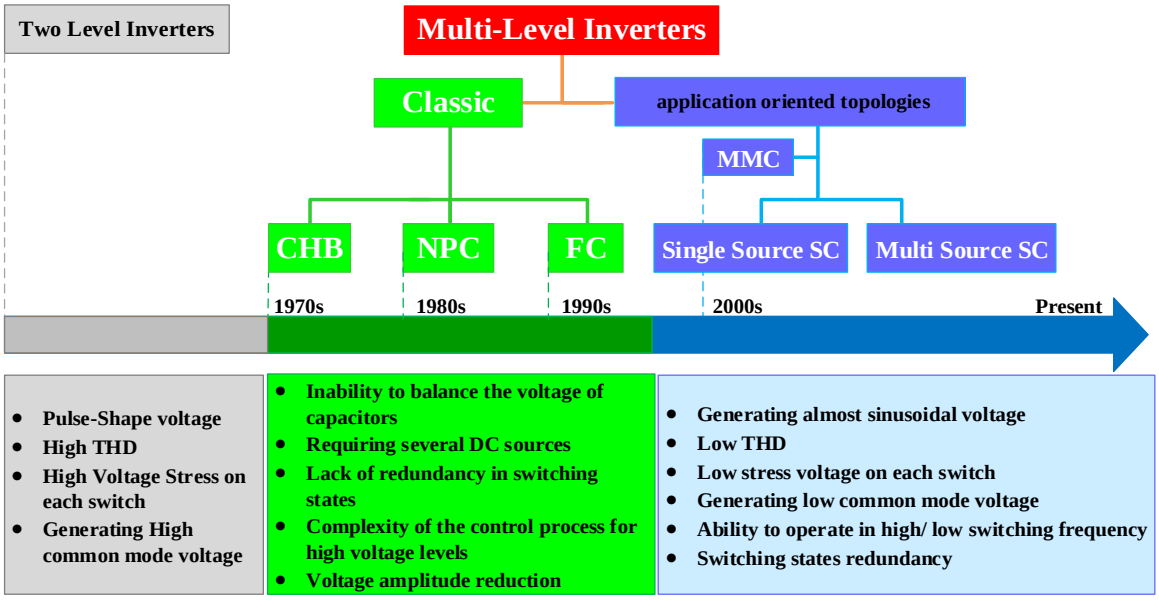


Figure 1. Gradual progress of inverters' overview.

Moreover, when an increase in output voltage levels (to lower the THD) is intended, the semiconductor devices count will considerably increase. The above-mentioned factors restrict the application of these converters in high voltage levels [6]. As a result, attaining maximum possible voltage levels with the least number of DC input sources and semiconductor devices has become the main objective for experts in the field of MLIs. As an alternative, switched-capacitor multi-level inverters (SCMLIs) were proposed to cover these issues. In this context, many new converters were designed to decrease the number of components such as semiconductors, DC sources, capacitors, and implementation costs [4].

The SCMLI circuits presented in [6,16], are comprised of the connection of a few DC/DC converters and an H bridge to change the polarity of the output. The DC/DC part is made up of a serial connection of switched-capacitor cells. Using a single DC source and multiplying the input voltage are the main advantages of these topologies [17]. However, they require many capacitors and switches, which increases the size, complexity, and overall cost of these structures. Furthermore, using an H bridge in these circuits oblige the four switches to withstand the maximum of the output voltage [18]. As a result, the need for high voltage switches restricts the application of such topologies in medium and high voltage. Hence, to overcome this concern, several step-up SCMLI with a single input source are presented in [19–21]. In this case, voltage stress across the circuit elements has been reduced, which leads to the reduction of the total standing voltage (TSV) of the structure. However, the appliance of series diodes with switches in [19] prevents the power flow back to the source. Bidirectional power flow ability, prevents the capacitors from over-charging and potential damages. Ergo, the excess charge is fed back to the input source. As a result, another crucial character for an SCMLI circuit is whether the inverter can be used in application with bi-directional power flow or not. This paper presents a novel switched-capacitor multilevel converter suitable for medium and high power usage.

The proposed topology requires no external circuit or complex control algorithm to maintain its capacitors' voltage balance. The voltage boosting and reducing the semiconductor devices count are the advantages of the presented structure over conventional topologies. Since the proposed circuit inherently generates a bipolar voltage without using an H-bridge, the switching losses and voltage stresses across the semiconductor devices are reduced considerably.

The rest of this paper is organized as follows: Section 2 describes the proposed structure, its operating principles, capacitors charging paths, and the modulation strategy in detail. A comparative study, along with the determination of the circuit capacitances, power loss analysis, and efficiency calculations are carried out in Section 3. Then, the simulation and experimental results of the proposed inverter are brought in Section 4. At last, conclusion of this paper is added to Section 5.

2. Proposed Topology: Structure and Operating Principals

Figure 2 depicts the proposed switched capacitor topology. This circuit structure uses 3 capacitors and a single DC source to boost the input voltage 6 times and generate 13 levels in the output. Likewise, it consists of 15 power switches (including 13 uni-directional and one bi-directional) and 14 driving circuits to form the required current paths.

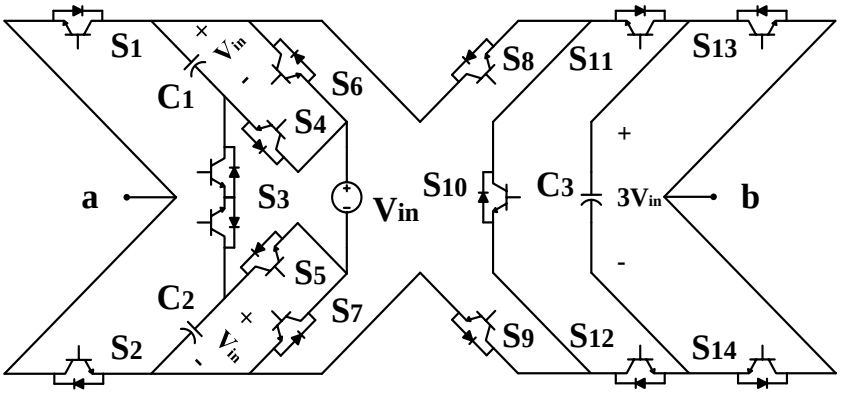
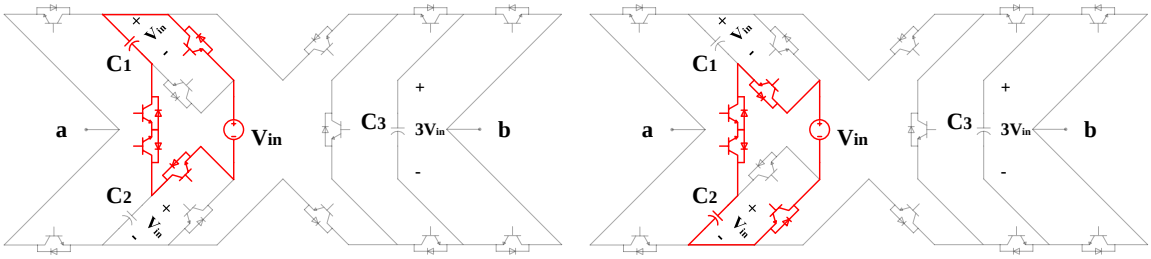


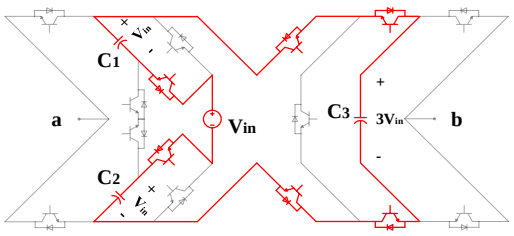
Figure 2. Schematic of the proposed X-Type (13-level prototype).

Each level of the staircase output voltage is achieved by a predetermined combination of capacitors and/or the DC source. A high-quality voltage can be obtained provided that: All capacitors are charged sufficiently, voltages of the capacitors and voltages across the switches does not exceed their rated values and the capacitors' voltage drop remains in an acceptable range [22]. As shown in Figure 3, C_1 and C_2 are charged directly by the input source up to V_{dc}. Capacitor C_3 can be charged up to $3V_{dc}$ by a series combination of C_1, C_2, and DC source (Figure 3c).



(**a**) (**b**)

Figure 3. *Cont.*



(**c**)

Figure 3. Charging path for (**a**) C_1, (**b**) C_2, and (**c**) C_3.

Table 1 brings the switching states and their relevant capacitors' state of charge. In addition, charging, discharging, and no change states of the circuit capacitors are shown by "▲", "▼", and "-", respectively.

Table 1. Corresponding switching states of the proposed circuit.

State	Active Switches	Output Voltage	C_1	C_2	C_3
1	S_1,S_4,S_5,S_9,S_{10},S_{11},S_{14}	$+6V_{dc}$	▼	▼	▼
2	S_1,S_3,S_4,S_7,S_9,S_{10},S_{11},S_{14}	$+5V_{dc}$	▼	▲	▼
3	S_1,S_3,S_5,S_6,S_9,S_{10},S_{11},S_{14}	$+5V_{dc}$	▲	▼	▼
4	S_1,S_6,S_7,S_9,S_{10},S_{11},S_{14}	$+4V_{dc}$	-	-	▼
5	S_1,S_4,S_5,S_8,S_9,S_{11},S_{12},S_{14}	$+3V_{dc}$	▼	▼	▲
6	S_1,S_3,S_4,S_7,S_9,S_{12},S_{14}	$+2V_{dc}$	▼	▲	-
7	S_1,S_3,S_5,S_6,S_9,S_{12},S_{14}	$+2V_{dc}$	▲	▼	-
8	S_1,S_6,S_7,S_9,S_{12}	$+1V_{dc}$	-	-	-
9	S_1,S_4,S_5,S_8,S_9,S_{11},S_{12},S_{13}	0	▼	▼	▲
10	S_2,S_4,S_5,S_8,S_9,S_{11},S_{12},S_{14}	0	▼	▼	▲
11	S_2,S_6,S_7,S_8,S_{11},S_{13}	$-1V_{dc}$	-	-	-
12	S_2,S_3,S_5,S_6,S_8,S_{11},S_{13}	$-2V_{dc}$	▲	▼	-
13	S_2,S_3,S_4,S_7,S_8,S_{11},S_{13}	$-2V_{dc}$	▼	▲	-
14	S_2,S_4,S_5,S_8,S_9,S_{11},S_{12},S_{13}	$-3V_{dc}$	▼	▼	▲
15	S_2,S_6,S_7,S_8,S_{10},S_{12},S_{13}	$-4V_{dc}$	-	-	▼
16	S_2,S_3,S_5,S_6,S_8,S_{10},S_{12},S_{13}	$-5V_{dc}$	▲	-	-
17	S_2,S_3,S_4,S_8,S_{10},S_{12},S_{13}	$-5V_{dc}$	▼	▲	▼
18	S_2,S_4,S_5,S_8,S_{10},S_{12},S_{13}	$-6V_{dc}$	▼	▼	▼

The procedure of generating voltage levels is as follows:

- Level $+6V_{dc}$: Figure 4a illustrates the current path for generating this level. Capacitors C_1, C_2, and C_3 are discharged across the load in series with the input source.
- Level $+5V_{dc}$: Two different switching states can be used to make this level. One is through the series connection of C_1, C_3, and DC source while charging C_2 simultaneously. The other is through series connection of C_2, C_3, and DC source while charging C_1 simultaneously.
- Level $+4V_{dc}$: C_3 and DC source make this level together.
- Level $+3V_{dc}$: This level is built with the help of C_1 and C_2 along with the DC source. Moreover, C_3 can be charged at the same time.

- Level $+2V_{dc}$: To make this level, there are two switching states. First, C_1 is discharged across the load with the DC source and at the same time C_2 is charged. Second, the capacitor C_2 and the input source supply the load and simultaneously C_1 is charged.
- Level $+1V_{dc}$: The voltage source is only used to make this voltage level (Figure 4b).
- Level zero: There are two switching states to form the level zero: First by turning the S_1, S_8, S_{11}, and S_{13} switches on. Second using the switches S_2, S_9, S_{12}, and S_{14}. Moreover, C_3 can be charged through the C_1, C_2, and DC source, as shown in Figure 4c.
- Negative voltage levels of $-1V_{dc}$, $-2V_{dc}$, ... , $-6V_{dc}$ are obtained similarly.

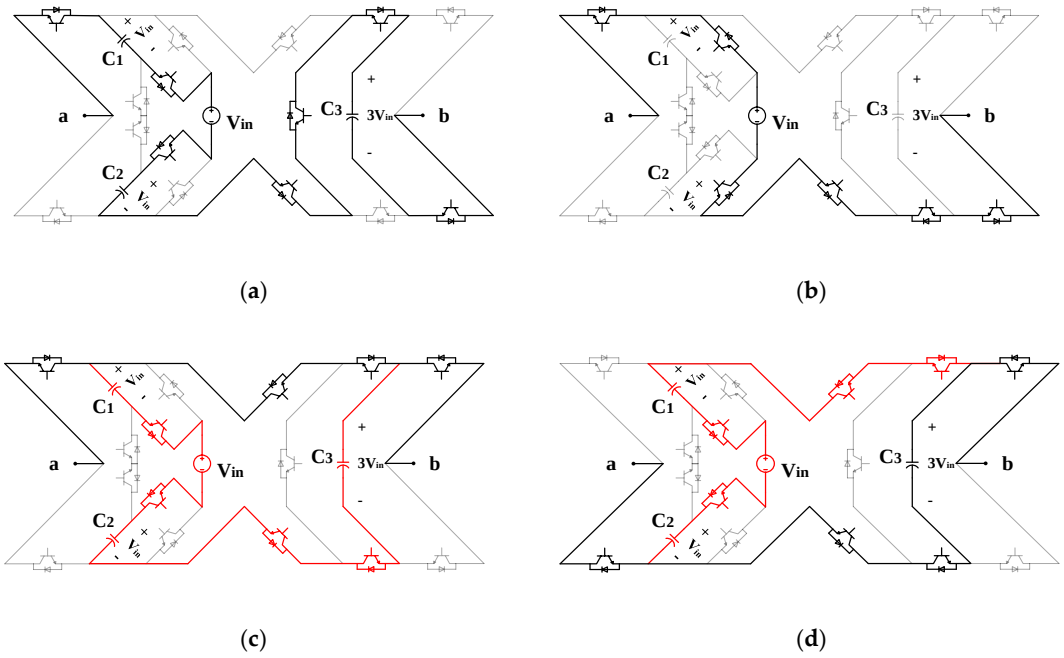


Figure 4. Current paths for generating different voltage levels (**a**) $+6V_{dc}$, (**b**) $+1V_{dc}$, (**c**) zero, (**d**) $-3V_{dc}$.

2.1. Modulation Strategy

Figure 5a shows the control procedure of producing a near sinusoidal waveform, with a 50 Hz reference frequency. The switching angles t_i (i = 0, 1, 2, ... , n) are selected based on nearest level control (NLC) method. Then, by applying these predetermined time intervals to the circuit with their corresponding switching states, the desired output waveform is shaped. This strategy tracks the closest voltage level of the sample staircase waveform to the reference [23].

By using this method, the time intervals of each voltage level to produce the desired output voltage is estimated. Then, using the switching states of Table 1 and based on the charging and discharging modes of the capacitors, the appropriate switching state for making each voltage level is selected (Figure 5b) [20].

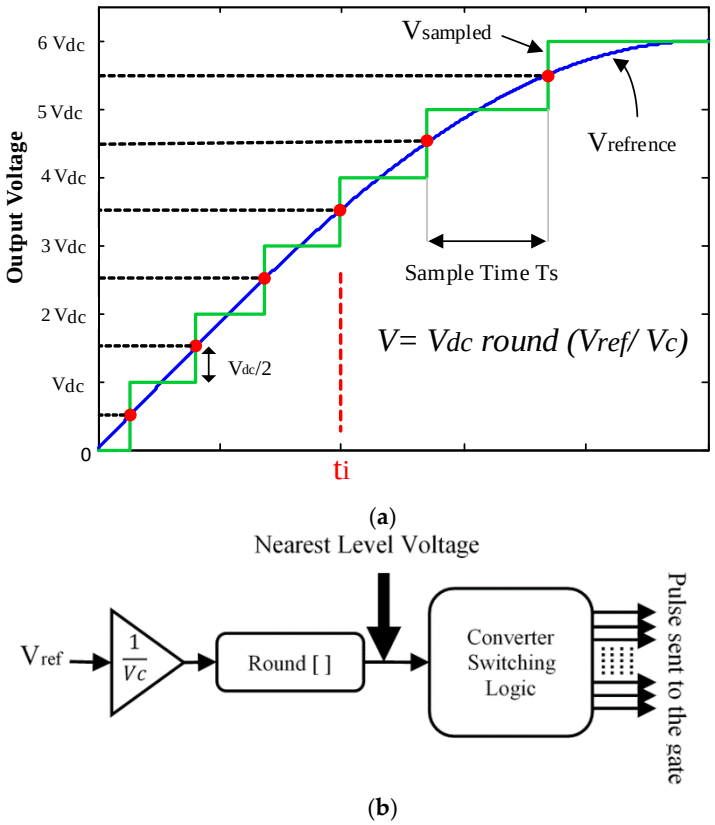


Figure 5. Nearest level control (NLC) method for the proposed 13-level switched-capacitor multi-level inverter (SCMLI) (**a**) NLC scheme waveform and (**b**) logic.

2.2. Extended Topology

The proposed X-Type topology can be extended in case a higher output is required. For high power AC application, an extension for the simple module is introduced to achieve higher voltage levels. So that, by use of a single input source and $(\frac{n}{3} + 1)$ capacitors, $(2n + 1)$ voltage levels can be generated. It depends on the type of application and the output voltage required. In some cases, the input source is capable of supplying the required load current in high voltage application. Hence, Figure 6 version is preferred. Moreover, when multiple DC sources are available such as solar panels, this can be a very good option to collect all of the low voltage panels and connect them to each other in order to reach higher AC output voltages in both stand-alone and grid connected application.

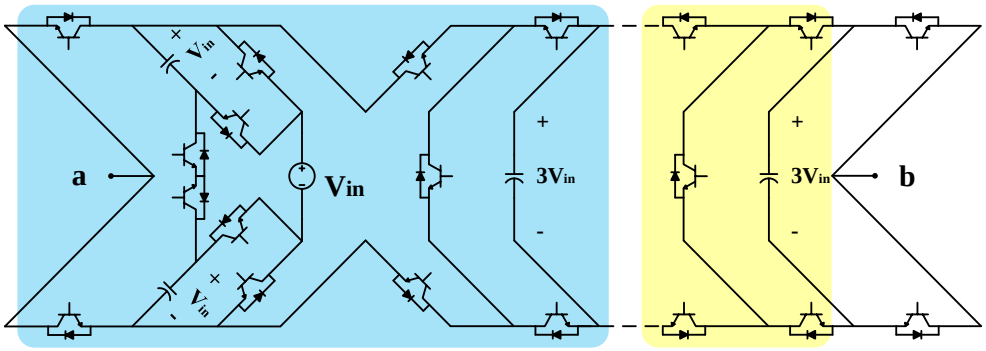


Figure 6. Schematic of the extended X-Type structure.

Moreover, as some applications normally use low voltage DC sources, high amounts of currents are drawn from the sources in the case of single DC source when a boost AC output voltage is required. This may limit the power ranges of SCMLIs due to high current ratings of some power semiconductors.

This problem can be solved by using multiple DC sources to split the amount of input current between different sources and different semiconductors. On the other hand, size of capacitors reduces as they are able to balance their voltage using paths through more DC sources. It seems that hybrid SCMLI with multiple DC sources is an intermediate solution for the drawbacks of single DC source SCMLI (high current ratings at high power application) and cascaded MLIs (high number of DC sources). Besides, by modular connection of SC cells, voltage of last cells may reduce. To achieve higher output voltages, it is needed to add some DC sources between the modules to keep the voltage in an acceptable range.

To overcome these problems, as shown in Figure 7, several basic SCMLI units of Figure 2 can be cascaded to achieve higher output voltage levels. This method would be useful where a few DC sources or DC links are accessible. The amount of different DC sources can be equal or asymmetric which depends on the number of required voltage levels and the type of application.

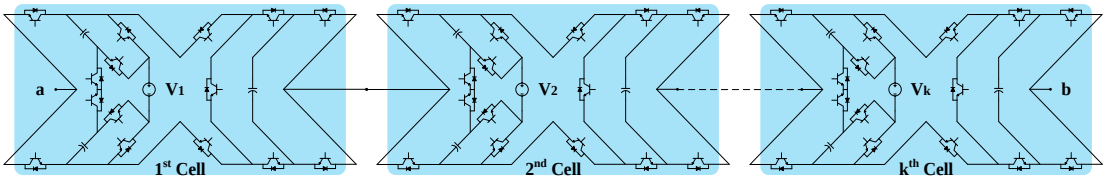


Figure 7. Circuit expansion of the proposed multilevel inverter (MLI).

In the context of step-up SCMLI in a real application, it is essential to design a topology to use maximum possible standard rating of the switches. Therefore, the input voltage should be raised until the peak inverse voltage (PIV) is less than a certain acceptable range percentage (x%) of the switches rated voltage (V_{rated}^{SW}) as PIV < x%V_{rated}^{SW}.

3. Discussion

3.1. Determination of Capacitance

The voltage drop of the circuit capacitors in a switched capacitor converter (due to repeated charging and discharging cycles) should stay in an acceptable range. The scale of this range depends on the capacitance, discharge time, and the load current. The smaller the ripple, the lower the power losses and the higher the capacitors' efficiency [21,24]. The maximum discharge rate (ΔQ) for each capacitor is obtained by:

$$\Delta Q = \int_{t_s}^{t_f} I_{out} \sin(2\pi f_{ref} t) dt \quad (1)$$

where, f_{ref} is the output frequency and I_{out} is the amplitude of the load current. Besides, [t_s, t_f] is the longest possible time interval in which each capacitor is discharged, assuming the worst case [2]. On the other hand, the maximum output current can be calculated by:

$$I_{load-\max} = \frac{V_{load-\max}}{R} = \frac{6V_{in}}{R} \quad (2)$$

Note that the capacitances C_1 and C_2 are the same. As the voltage of C_3 is three times the input, then its capacitance is one third of the other two capacitors. Then, the maximum discharge rate can be achieved by:

$$\Delta Q = \int_{t_s}^{t_f} I_{load-\max} \sin(2\pi f_{ref} t) dt = \int_{t_s}^{t_f} \frac{6V_{in}}{R} \sin(2\pi f_{ref} t) dt \quad (3)$$

Taking k as the acceptable ripple percentage (or ripple curtailment), the capacitance is obtained as follows:

$$C_{eq} \geq \frac{\Delta Q_c}{KV_{in}} \quad \Rightarrow \quad C_{eq} \geq \frac{6}{kR}\int_{t_s}^{t_f} \sin(2\pi f_{ref} t)\, dt \tag{4}$$

Since C_{eq} is formed by the series connection of the three capacitors, its capacitance is one fifth of C_1. Accordingly, the variation of the determined capacitance versus the load (R) changes with regard to the ripple curtailment is illustrated in Figure 8.

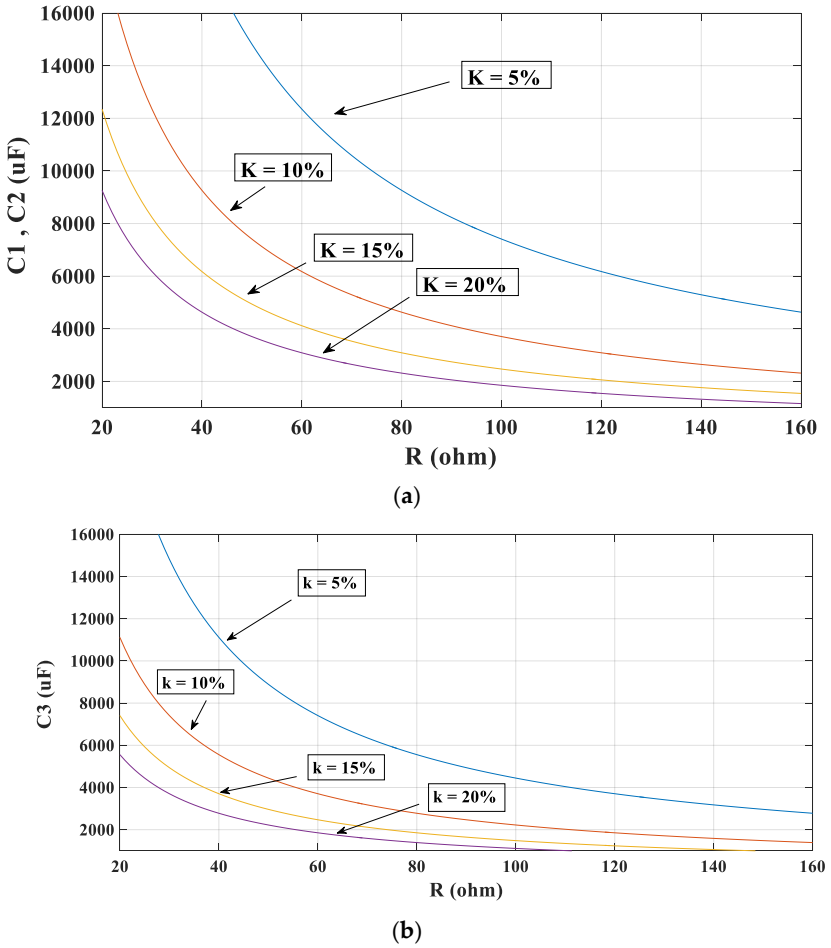


Figure 8. Capacitance curve versus load and ripple constraint for (**a**) C_1 and C_2 and (**b**) C_3.

3.2. Power Loss Analysis

Generally, power loss in switched-capacitor converters are classified into three groups: switching loss, conduction loss, and the loss caused by capacitor voltage ripple [2,20,25,26].

3.2.1. Switching Losses

Switching loss caused by a delay in switch's turn-on and turn-off time, is one of the major contributions for the power loss. Semiconductors have this kind of loss intrinsically. When the Semiconductor switch turns on, gate-emitter voltage reaches the threshold voltage and also the collector current increases and collector-emitter voltage has a downward trend until it reaches the on-state voltage of the switch that shows the turn on cycle is over. Similarly, in an opposite way in turn-off cycle and at the end of turn-off cycle, gate-emitter reaches the saturation voltage. Collector

current and emitter voltage rise and finally the turn-off process ends [27]. Turn-on and turn-off loss for active switches is calculated by Equations (5) and (6).

$$\begin{aligned} P_{s,on} &= f_s \int_0^{t_{on}} V_{off-state}(t) i_s(t) dt = f_s \int_0^{t_{on}} \left(\frac{I_{on-state}}{t_{on}} t\right)\left(\frac{-V_{off-state}}{t_{off}}(t - t_{on})\right) dt \\ &= \frac{1}{6} f_s V_{off-state} I_{on-state} t_{on} \end{aligned} \tag{5}$$

$$\begin{aligned} P_{s,off} &= f_s \int_0^{t_{off}} V_{off-state}(t) i_s(t) dt = f_s \int_0^{t_{off}} \left(\frac{V_{off-state}}{t_{off}} t\right)\left(\frac{-I_{on-state}}{t_{off}}(t - t_{off})\right) dt \\ &= \frac{1}{6} f_s V_{off-state} I_{on-state} t_{off} \end{aligned} \tag{6}$$

where, $V_{off\text{-}state}$ and $I_{on\text{-}state}$ are off-state voltage and switch current when the switch becomes fully turned on, respectively. Switching losses which is the sum of turn-on and turn-off loss is calculated by Equation (7):

$$P_{sw} = \sum_{j=1}^{N_{switch}} \left(P_{sj,on} + P_{sj,off}\right) \tag{7}$$

3.2.2. Conduction Losses

Conduction loss for power switches and power diodes is calculated by [2,23]:

$$P_{con-L} = (k_1 V_{on}^{sw} + k_2 V_{on}^{D}) i_{av-L} + (k_1 R_{on}^{sw} + k_2 R_{on}^{D}) i_{rms-L}^2 \tag{8}$$

where, V_{on}^{sw}, V_{on}^{D} are the on-state voltage of switch and the on-state voltage of diode, respectively. Additionally, R_{on}^{sw} is on-state resistance of switches and R_{on}^{D} is on-state resistance of diode [22,25]. The parasitic resistance of the circuit elements in each level ($V_j = 0, \pm 1V_{in}, \pm 2V_{in}, \pm 3V_{in}, \pm 4V_{in}, \pm 5V_{in}$, and $\pm 6V_{in}$) are listed in Table 2. I_{rms} and I_{avg} are the root mean square (RMS) and average current of semiconductors that obtain from Equation (9). It should be noted that k_1 and k_2 are the number of the switches which have been shown in this table.

$$i_{av}(nV_{dc}) = \frac{2}{\pi} \int_{t_a}^{t_b} [\mathrm{I}_m \sin t dt], \; i_{rms}(nV_{dc}) = \sqrt{\frac{2}{\pi} \int_{t_a}^{t_b} (\mathrm{I}_m \sin t)^2 dt} \tag{9}$$

Table 2. Equivalent parasitic resistance for each level.

Output Voltage Level	Equivalent Parasitic Resistance
0	$6R_{on}{}^{sw} + 1R_{on}{}^{D}$
$\pm 1Vin$	$3R_{on}{}^{sw} + 3R_{on}{}^{D}$
$\pm 2Vin$	$4R_{on}{}^{sw} + 3R_{on}{}^{D}$
$\pm 3Vin$	$6R_{on}{}^{sw} + 2R_{on}{}^{D}$
$\pm 4Vin$	$5R_{on}{}^{sw} + 2R_{on}{}^{D}$
$\pm 5Vin$	$6R_{on}{}^{sw} + 2R_{on}{}^{D}$
$\pm 6Vin$	$7R_{on}{}^{sw}$

Finally, the total conduction losses for the proposed 13-level X-Type inverter can be calculated by:

$$P_{con}^{total} = 2 \sum_{k=1}^{6} P_{con}^{(kV_{dc})} + 2 \sum_{m=-1}^{-6} P_{con}^{(mV_{dc})} \tag{10}$$

3.2.3. Losses Due to the Capacitors Voltage Ripple

The difference between the input DC voltage and the capacitor voltage is the essential of the capacitor ripple loss [19]. The ripple of the capacitor's voltage obtained from:

$$\Delta V_{ripple,C} = \frac{1}{C}\int_{t_c}^{t_d} i_C(t)dt \tag{11}$$

It is worth mentioning I_c is the capacitor current and $[t_c, t_d]$ is the discharge time of the capacitor that the period of discharge time for 13-level X-Type converter. So, the capacitor's voltage ripples losses obtain from Equation (12). Finally, sum of the losses and efficiency are calculated by Equation (13), where P_{in} and P_{out} are the converter's input and output powers, respectively.

$$P_{Rip} = \frac{f_{ref}}{2}\left(C_i \Delta V^2_{ripple,C}\right) \tag{12}$$

$$\eta = \frac{P_{out}}{P_{out} + P_{Loss}} = \frac{P_{out}}{P_{out} + P_{Sw} + P_{Con} + P_{Rip}} \tag{13}$$

3.3. Comparative Study

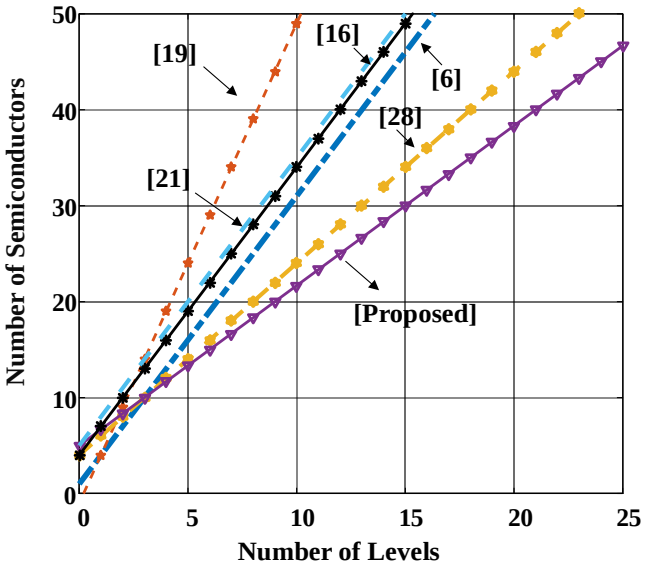
A comparative study is conducted between the proposed structure and several recently published articles on single-source structures in Table 3. This comparison is based on the number of capacitors, semiconductor devices (diodes and active switches), starter circuits, bi-directional power flow ability, PIV, and TSV per $(2n + 1)$ output levels.

Table 3. Comparison between the proposed converter and other topologies.

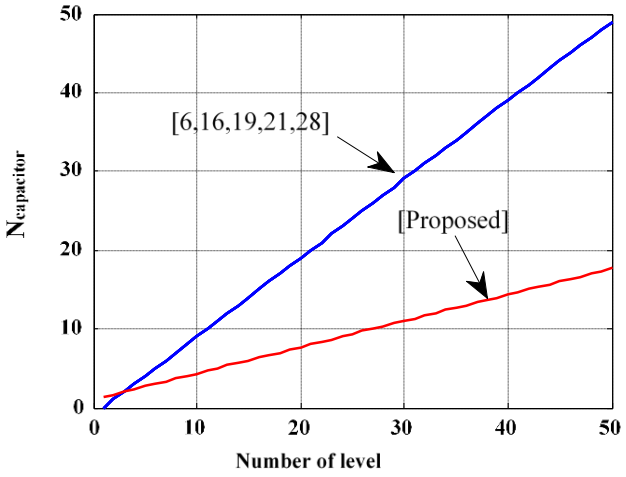
Items	[21]	[16]	[27]	[6]	[19]	X-Type
No. of Capacitors	$n-1$	$n-1$	$n-1$	$n-1$	$n-1$	$\frac{n}{3}+1$
No. of Switches	$3n+4$	$n+5$	$2n+4$	$3n+1$	$5n-1$	$\frac{5}{3}n+5$
No. of Drivers	$3n+4$	$n+5$	$2n+4$	$3n+1$	$5n-1$	$\frac{5}{3}n+4$
No. of Series Diodes	*0*	$2n-2$	$2n-2$	*0*	*0*	*0*
PIV(×V_{IN})	n	n	n	n	1	3
TSV(×V_{IN})	$7n-3$	n^2+6n+4	n^2+5n+1	$\frac{n^2}{2}+5n$	$5n-1$	$5n+2$
Polarity Generating	H-bridge	H-bridge	H-bridge	H-bridge	inherent	inherent
Bi-Directional Power Flow	NO	NO	YES	NO	NO	YES

According to the table, the proposed structure requires a smaller number of capacitors (approximately one-third) to generate the same output level. The circuits introduced in [6,16,21] consist of two parts for generating voltage levels and polarity. Therefore, they are not suitable for high-voltage applications. However, [19] and the proposed circuit can change the polarity of the load voltage without the need for an auxiliary circuit. Furthermore, the PIV and TSV in [19] are the lowest among other structures; however, it uses the most semiconductor components. It should be noted that the diodes in [16,19] limit the ability to absorb power from the load whenever it is needed.

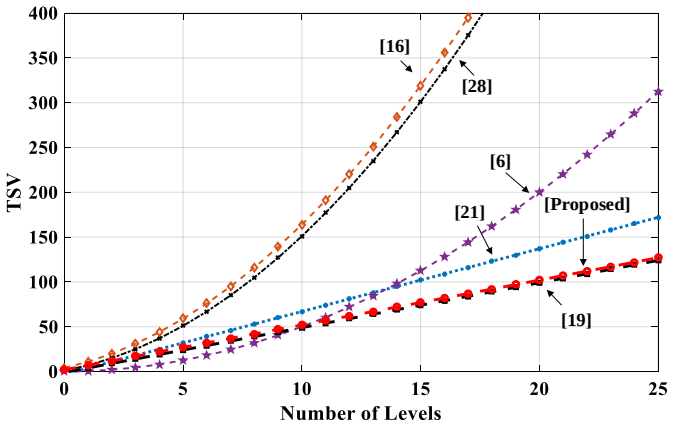
To better understand the relative superiority of the proposed structure, the graphical comparison of the number of semiconductors used, capacitors, and TSV for different number of output levels is illustrated in Figure 9.



(**a**)



(**b**)



(**c**)

Figure 9. Comparison of the parameters in terms of number of levels, (**a**) number of semiconductor, (**b**) capacitors, and (**c**) total standing voltage (TSV).

4. Performance Evaluation

This section presents a set of both simulation and experimental results in order to accredit the performance and effectiveness of the proposed model for a 13-level X-Type converter.

4.1. Simulation Results

To evaluate the function of the proposed 13-level X-Type converter, simulation studies are conducted in MATLAB Simulink environment with the characteristics listed in Table 4.

Table 4. Simulation parameters in MATLAB.

Parameters	Values
Input DC Source (V_{in})	30 V
Boost Ratio (n)	6
Output frequency (f_o)	50 Hz
Capacitances (C)	$C_1 = C_2 = 4700$ µF, $C_3 = 2200$ µF
Load (Z_L)	90 Ω, 318 mH

It should be noted that because of using low voltage capacitors, their physical dimensions are remarkably small. Figure 10a,b displays the voltage waveform and the output current under the resistive and resistive-inductive load, respectively. At inductive load, the output current is smooth. Figure 10c shows the harmonic spectrum of the output voltage. The output's THD is 6.42%. It can be seen that the amplitude of all unwanted harmonics are kept below 5% satisfying the IEEE-Std. 519-2014.

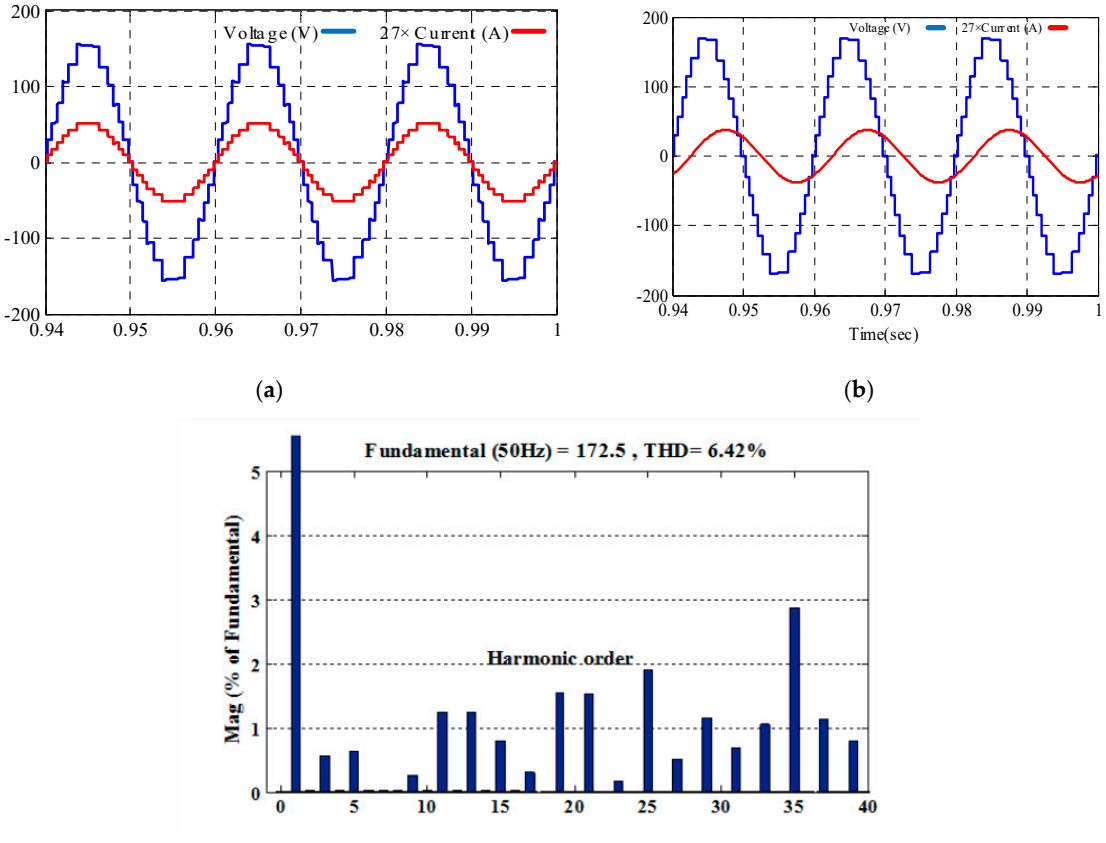


Figure 10. Simulation results, (**a**) resistive load ($Z_L = 90\ \Omega$), (**b**) resistive-inductive load ($Z_L = 90\ \Omega$ + 318 mH), and (**c**) harmonics spectrum.

In order to highlight the capability of the proposed structure in an instantaneous load change condition, the following scenario was implemented in a way that the load changes between Z_{L1} and Z_{L2}. Figure 11a shows the output current changes during instantaneous change. Likewise, during this condition, the capacitors follow the reference voltage representing the right function of the circuit which is shown in Figure 11.

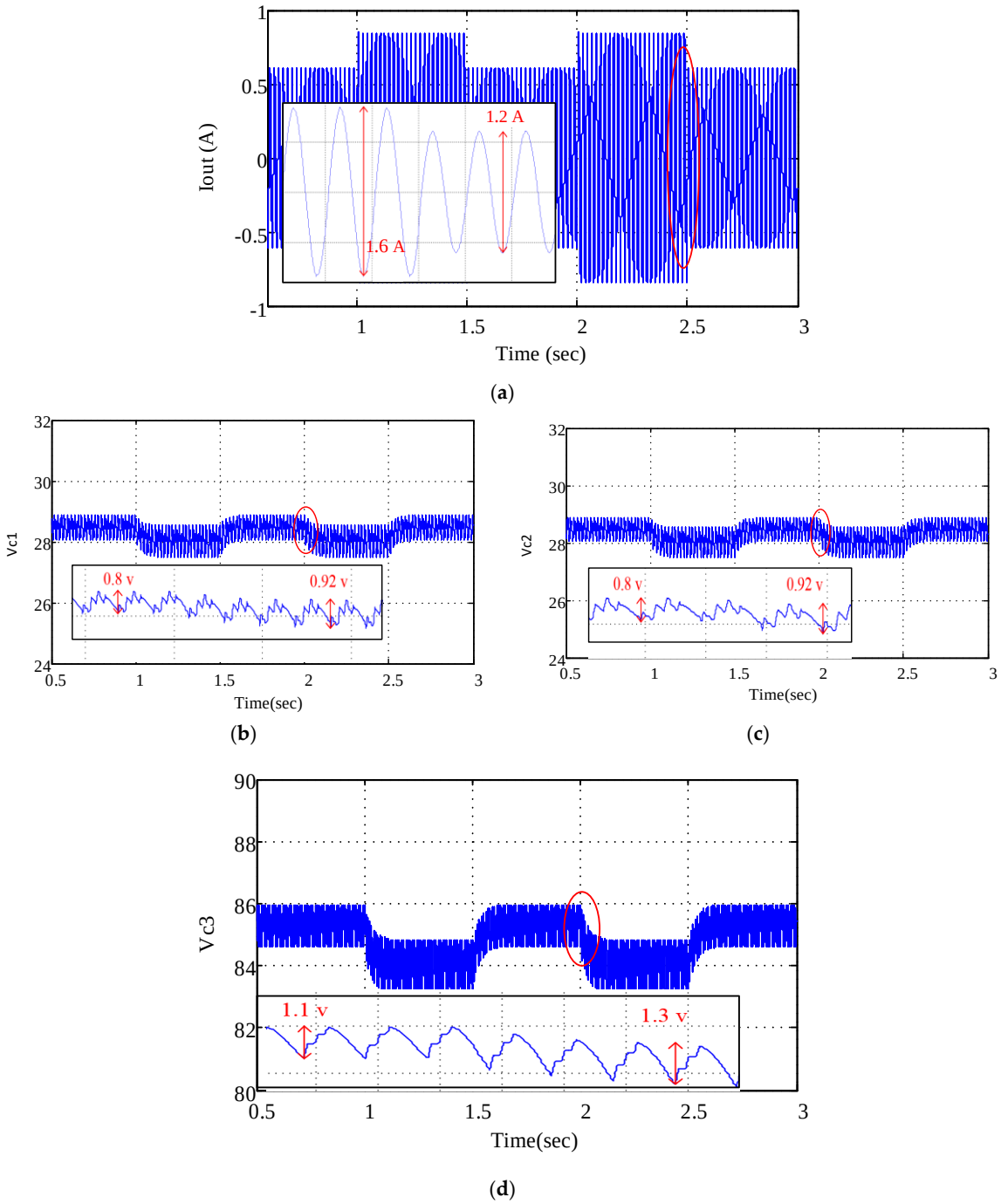
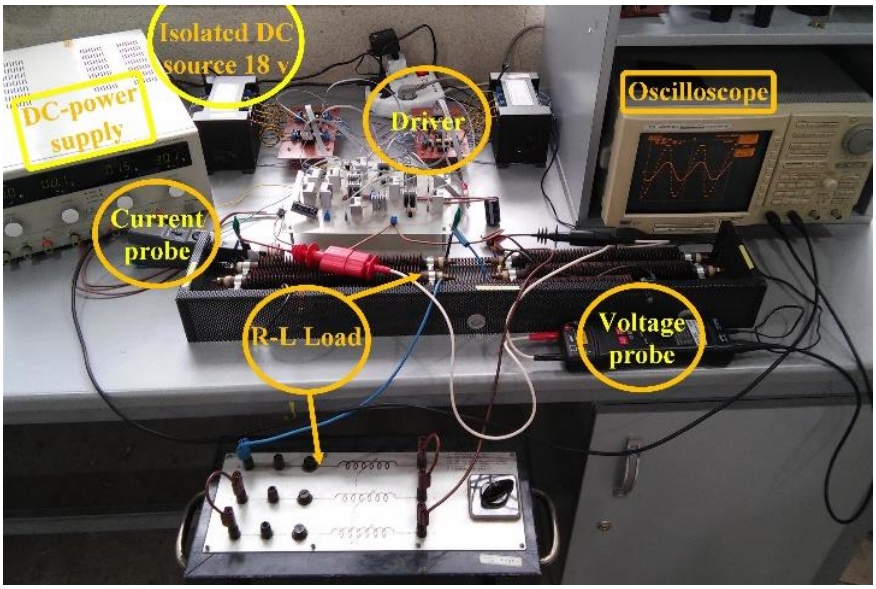


Figure 11. Simulation results under sudden load change, (**a**) output current, (**b**) V_{C1}, (**c**) V_{C2}, and (**d**) V_{C3}.

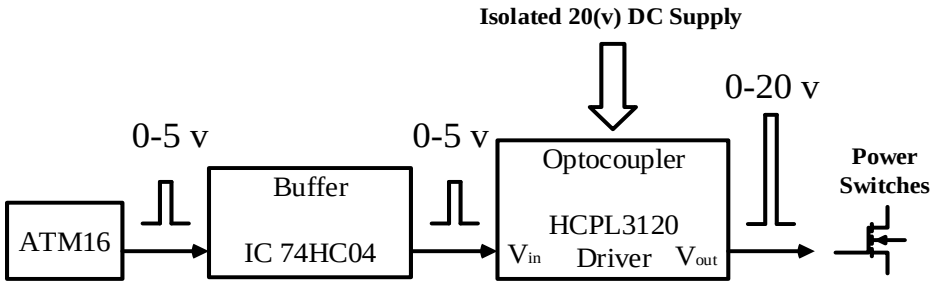
4.2. Experimental Results

Experimental model for a 13-level converter was tested to verify the function of the circuit in the power electronics laboratory (see Figure 12a). Characteristics of the experimental model are listed

in Table 5. Switching pulses were generated by AVR-ATMEGA16A microcontroller. The switching process is written in BASCOM software and loaded onto the microcontroller. Similarly, for preventing damage to the low-voltage devices, the power circuit and control circuit were isolated electrically by utilizing opto-coupler HCPL3120 in gate driver circuit which is shown in Figure 12b.



(**a**)



(**b**)

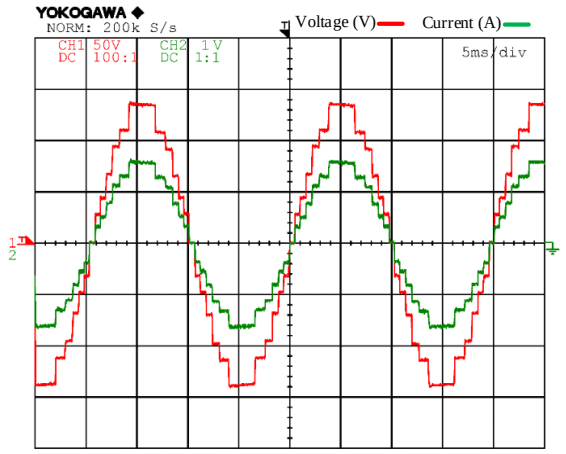
Figure 12. (**a**) Experimental setup and (**b**) switching schematic of main switches (MOSFETs).

Table 5. Specifications of the proposed 13-level X-Type inverter.

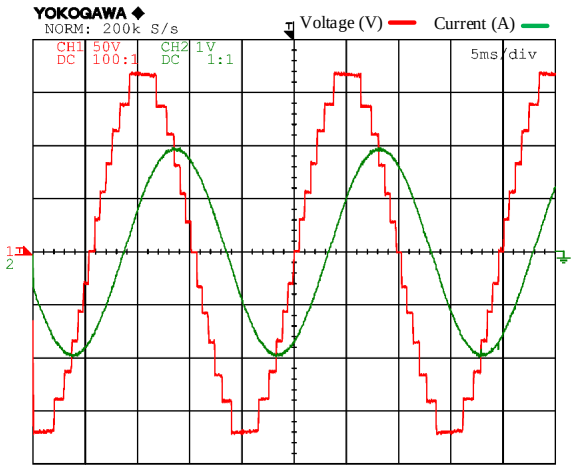
Parameters	Values
Input DC voltage (V_{in})	30 V
Boost Ratio (n)	6
Output Frequency (f_o)	50 Hz
Capacitances (C)	$C_1 = C_2 = 4700$ µF, $C_3 = 2200$ µF
Load (Z_L)	90 Ω, 318 mH
Main Switches (MOSFET)	IRFP460
Opto-coupler Driver	HCPL-3120
Main Control Chip	AVR ATMEGA16A
Voltage Probe	PINTEK DP-50
Current Probe	FLUKE 80i-110s AC/DC

Output voltage and current under resistive and resistive-inductive loads are shown in Figure 13a,b. A voltage source of 30 V is considered as input. The maximum output voltage is 180 V and also each voltage step is 30 V. An important feature of this structure is the capability of boosting the input voltage,

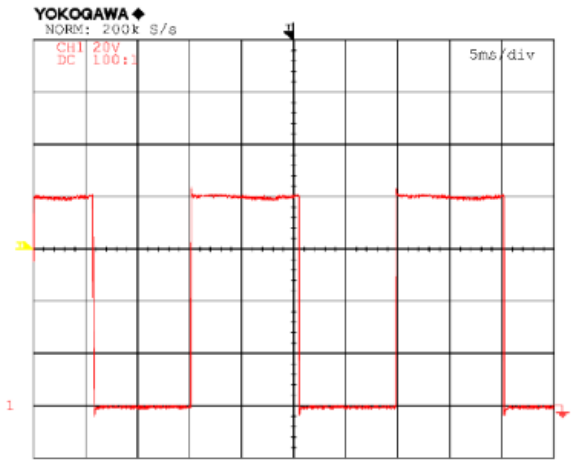
about, six times and as an example of the voltage of the switches, the voltage across the S_1 is displayed in Figure 13c.



(**a**)



(**b**)



(**c**)

Figure 13. Experimental waveforms, (**a**) resistive load ($Z_L = 90\,\Omega$), (**b**) resistive-inductive load ($Z_L = 90\,\Omega$ + 318 mH), and (**c**) voltage of S_1.

The transient performance of the proposed structure is evaluated by the load changing between Z_{L1} = 250 Ω and Z_{LP} (Z_{LP} = Z_{L1}|| Z_{L2}, Z_{L2} = 170 Ω) sequentially. In this way, the converter is operating normally under load Z_{L1} and suddenly another load (Z_{L2}) is connected in parallel. To better demonstrate the impact of such sudden load change, Z_{L2} is connected and disconnected repeatedly. Figure 14 illustrates the results of the function of the converter under sudden load changes. As revealed in this figure, the capacitors follow the reference voltage, and their voltages fluctuate within an acceptable range. So, the proposed converter has no need for any complex algorithm or external circuit for balancing the capacitor's voltage.

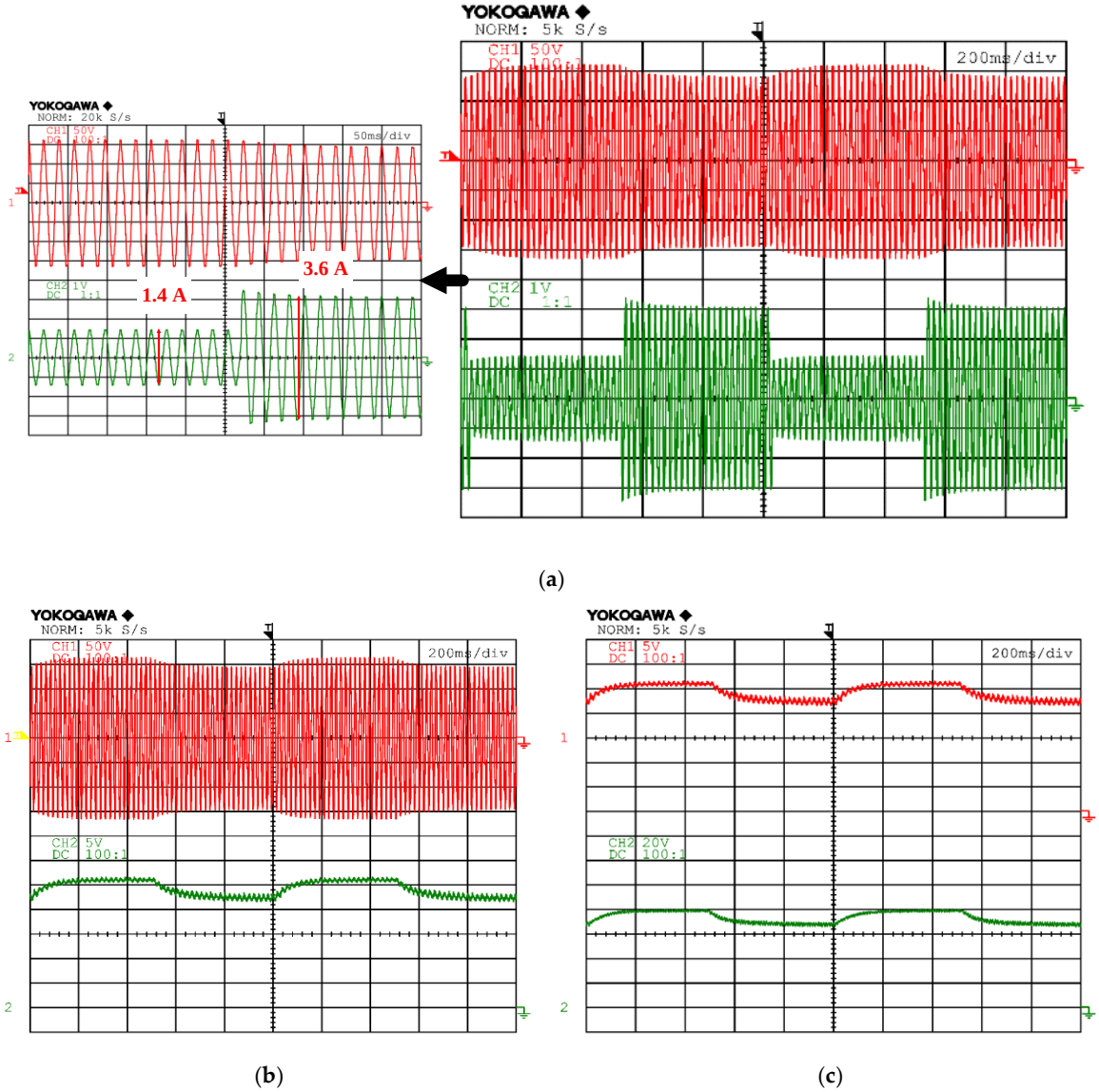


Figure 14. The experimental results under sudden change in the load (**a**) output voltage and current, capacitors' voltage (**b**) C_1, and (**c**) C_2, C_3.

5. Conclusions

In this paper, a 13-level single-source inverter with boosting capability is introduced. The ability to increase the input Voltage six times without using any inductor or transformer and also the self-balance of the capacitor's voltage without the use of an external controller are the main advantages of this converter. A comparative study with some recent topologies shows that the proposed structure reduced the number of semiconductor components compared to other structures, which would

reduce the implementing cost. This structure has less TSV and PIV than similar structures which provides conditions to reach higher levels. In particular, the modulation strategy, the calculation of the capacitance, the switching losses, and, also, conduction loss for the proposed structure have been investigated. The efficiency of the 13-level structure presented is 92.73%, and, also, the THD of output voltage for the proposed structure is 6.42%. Finally, experimental results of the proposed converter, verify its correct operation under different (resistive and resistive-inductive) loads and also instantaneous load change on the output. By analyzing the results, the proposed inverter is regarded as a suitable choice for renewable energy applications with low number of DC sources and also it is appropriate for voltage boosting at the output.

Author Contributions: Investigation, J.A.; methodology, E.M.G.R.; supervision, E.P.; writing—original draft preparation, E.A., A.K., M.J.R., M.E.A. and M.R.; writing—review and editing, E.P.; All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

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