Modular Multilevel Converter Performance with Dynamic MVDC Distribution Link Voltage Rating

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Modular Multilevel Converter Performance with Dynamic MVDC Distribution Link Voltage Rating

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***Abstract*—Back-to-back Modular multilevel converters (MMC) for medium voltage dc (MVDC) distribution link applications offer exciting opportunities due to its superior harmonic performance and high efficiency. Based on the steady state equations, it is shown that under specific active and reactive power operation, an increase in dc link voltage can be achieved without necessarily increasing the voltage seen by the MMC submodule components. Using steady state loss model, it is proved that the converter operating efficiency can be improved if this concept is applied.**

I. Introduction

A. Research Focus

Fig. 1 shows the dc link interconnecting two medium voltage distribution substations A and B. During full load conditions and/or system contingencies, the conductors of this link can be operated at a voltage higher than the nominal value. This will improve the power transfer efficiency and/or delivery capacity of the link.

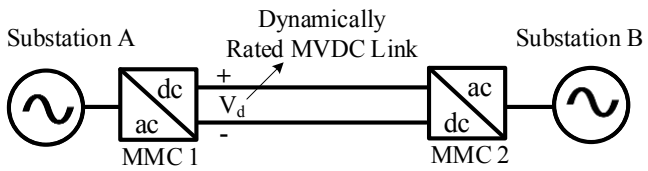

Fig. 1: Concept illustration of dynamically rated MVDC Link using MMC.

On the other hand, the capability of dynamically enhancing the link conductor voltage should avoid an increase in the voltage imposed on the substation ac-dc converter switches, as this would increase the switching losses as well as the installation cost. It is shown that this is possible with use of modular multilevel converters (MMC).

TABLE I: Different cases considered in this study.

	v_{grid}	v_{d}	P_{d}	pf	E_{av}
Case I	Fixed	Fixed	1 p.u	0.9	Fixed
Case II	Fixed	Increased, 10 %	1 p.u	0.9	Same as case I
Case III	Fixed	Fixed	1 p.u	0.9	Reduced

Table I lists the three operational cases that are compared in this study. Case I represents the normal operation with the dc link voltage v_{d} fixed at its nominal value of 1 p.u., while delivering the rated dc link power P_{d} at 1 p.u. with 0.9 ac side power factor. The average energy stored in the MMC (E_{av}) is fixed corresponding to the nominal value of the link voltage. In case II the same converter operates with 10 % higher v_{d}. It is shown that the MMC can operate with E_{av} the same as case I. In case III, the dc link voltage is fixed at its rated value and the MMC delivers the power demand with reduced E_{av} based on the concept proposed in [1]. In all three cases, the grid voltage v_{grid} is fixed to a constant value. The steady state voltages and currents imposed on the MMC components is estimated to understand whether re-sizing is necessary. The conduction and switching losses are quantified to compare the performance and to suggest the most favourable operation out of the three cases.

B. Background on the Project Objectives

The larger goal of our research is to restructure the existing medium voltage ac distribution networks using flexible dc link backbones in a reconfigurable architecture [2]. This is in line, for example, with the envisioned potential of MVDC distribution discussed in the white paper presented by companies like Siemens [3]. In [4], [5], rapidly increasing demand is identified as one of the key challenges faced by the distribution network operators (DNOs). It is discussed how refurbishing ac distribution links to operate under dc conditions could offer capacity enhancement, thus maximizing the use of existing grid infrastructure. The quantification of the expected capacity and efficiency enhancement is provided in [4], wherein, better infrastructure utilization with dc operation is combined with superior performance of modular multilevel converters (MMC) [6], [7]. The consequences of dc voltage enhancement on the cable insulation performance is empirically studied in detail [8]. Furthermore, in [9], the concept of system reconfigurability is introduced to maintain capacity enhancement during (n-1) contingencies. Various choices and trade-offs in operational reliability, cost and efficiency are highlighted in [10]. In [11], the operational efficiency boundaries of parallel ac-dc reconfigurable link system are defined.

From cable component engineering standpoint, dynamic voltage rating of the dc link is suggested as one of the potential possibilities in [4], [5]. Using this concept, dynamic capacity and efficiency gains can be obtained by increasing the operating voltage during periods of high power delivery as well as during contingencies. It was cautioned, however, that the impact of such an operational requirement on the link converter should be studied to determine whether re-sizing

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of component switches and capacitors is necessary and/or whether there is a detrimental effect on the converter efficiency. In the present work, we explore the MMC performance with dynamic voltage operation of the medium voltage dc (MVDC) link and show that some enhancement in operational efficiency of the converter is possible.

II. System Description

A 10-level, 3.3 kV IGBT switch based MMC is chosen to integrate the MVDC link in the 10 kV ac distribution network. The switch rating and number of levels are chosen based on the trade-offs between submodule (SM) capacitance, redundancy requirement, converter efficiency and effective frequency [12]. A SM capacitance of 2 mF is used. The SM switch rating and losses are governed by the steady state currents and voltage that are imposed on each arm of the converter. A good steady state analysis of MMC operation is provided in [13], [14]. The description of MMC operation using averaged-value model is presented in [15], [16]. The schematic of the medium voltage dc link MMC is shown in Fig. 2.

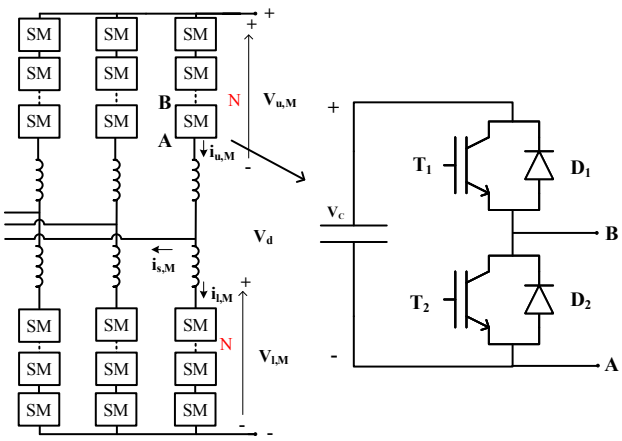

Fig. 2: Schematic of modular multilevel converter for MVDC Link.

The voltage, current and power base quantities considered in this paper correspond to the designed rated dc link parameters. The 1 p.u dc link voltage V_d is decided based on the cable dc voltage rating, which is $2\sqrt{2}$ times the rms phase voltage at the ac side of the MMC. More information on deciding the dc voltage rating of cable based on its performance under ac and dc operating conditions can be found in [8]. Case I considers rated current I_d at 1 p.u when 1 p.u active power is transferred by the dc link. The MMC is designed to support this dc link power transfer with 0.9 power factor (pf) at the ac grid side. The ac phase voltage v_s and current i_s are given by (1) and (2),

$$v_\mathrm{s} = \hat{v}_\mathrm{s} \cos(\omega t) \tag{1}$$

$$i_\mathrm{s} = \hat{i}_\mathrm{s} \cos(\omega t - \phi) \tag{2}$$

Using power balance, its peak $\hat{i}_\mathrm{s}$ can be expressed in terms of dc link current as (3),

$$\hat{i}_\mathrm{s} = \frac{2 v_\mathrm{d} i_\mathrm{d}}{3 \hat{v}_\mathrm{s} \cos\phi} = \frac{4 i_\mathrm{d}}{3m \cos\phi} \tag{3}$$

This value is 1.5 p.u with rated power at 0.9 pf if the modulation index m, which is the ratio of peak ac phase voltage ($\hat{v}_\mathrm{s}$) and the dc pole voltage to ground ($v_\mathrm{d}/2$), is taken as 1 under steady state full load condition. Consequently, under full load conditions, $\hat{v}_\mathrm{s}$ is considered 0.5 p.u. Operating range extension methods such as third harmonic injection are not considered in the analysis of the current work, however, the principles presented would be similar. The rated steady state per unit upper and lower arm voltages v_u and v_l are written as (4) and (5), respectively.

$$v_\mathrm{u} = v_\mathrm{c} - v_\mathrm{s} = 0.5 - 0.5\cos(\omega t) \tag{4}$$

$$v_\mathrm{l} = v_\mathrm{c} + v_\mathrm{s} = 0.5 + 0.5\cos(\omega t) \tag{5}$$

The circulating voltage v_c drives the dc component of the arm current and is equal to $v_\mathrm{d}/2$. The per unit upper and lower arm current i_u and i_l transferring rated dc link power at 0.9 pf on the ac side is given by (6) and (7), respectively.

$$i_\mathrm{u} = i_\mathrm{c} + \frac{i_\mathrm{s}}{2} = 0.33 + 0.75\cos(\omega t - \phi) \tag{6}$$

$$i_\mathrm{l} = i_\mathrm{c} - \frac{i_\mathrm{s}}{2} = 0.33 - 0.75\cos(\omega t - \phi) \tag{7}$$

Herein, the circulating current i_c is controlled to its dc component $i_\mathrm{d}/3$ required for active power transfer between ac and dc side, while the second harmonics can be suppressed according to the methods described in [17]–[19]. Therefore, the steady state value is 0.33 p.u for rated dc link operation.

III. Steady State Arm Parameters with Dynamic DC Link Voltage Rating

Equations (4)-(7) govern the ratings of the converter components. In this section, the variation of the steady state arm parameters with dynamic dc link voltage is described. It is assumed that the dc link voltage imposed on the cable during rated power delivery can be enhanced by 10 % to 1.1 p.u but the ac voltage magnitude is kept constant. This operation with dynamic voltage enhancement for rated power transfer is considered Case II.

A. Sum Capacitor Voltages

Upper and lower sum capacitor voltages V_cu^Σ and V_cl^Σ are the sum total of all SM capacitor voltages in the respective arms. An approximation of the analytic expressions are derived in [20], [21], given by (8) and (9),

$$V_\mathrm{cu}^\Sigma \approx v_\mathrm{d} + \frac{N}{2C v_\mathrm{d}} \left(\Delta W_\Sigma + \Delta W_\Delta\right) \tag{8}$$

$$V_\mathrm{cl}^\Sigma \approx v_\mathrm{d} + \frac{N}{2C v_\mathrm{d}} \left(\Delta W_\Sigma - \Delta W_\Delta\right) \tag{9}$$

Herein, the average component is controlled to the dc link voltage (v_d) while the ripple component is determined from the total energy ripple ΔW_Σ and imbalance energy ripple ΔW_Δ defined in (10) and (11) respectively, as per the theory presented in [20].

$$\Delta W_\Sigma = -\frac{\hat{v}_\mathrm{s}\hat{i}_\mathrm{s}}{4\omega} \sin(2\omega t - \phi) \tag{10}$$

$$\Delta W_\Delta = \frac{v_\mathrm{d}\hat{i}_\mathrm{s}}{2\omega} \sin(\omega t - \phi) - \frac{2\hat{v}_\mathrm{s} i_\mathrm{c}}{\omega} \sin(\omega t) \tag{11}$$

In [21], it was highlighted that the stored arm energy can be controlled such that the average component of V_{cu}^{Σ} is lower than the operating v_{d}. The average component is, therefore, governed by the controlled mean energy per arm ($W_{\text{arm},\Sigma 0}$), given by (12),

$$W_{\text{arm},\Sigma 0} = \frac{C k_{\text{d}}^2 v_{\text{d}}^2}{2N} \tag{12}$$

The expressions derived in (8) and (9) correspond to the condition $k_{\text{d}} = 1$. In [1], optimal selection of this constant is explored specifically for MMC based motor drives operating up to approximately a third of the base speed. It has been shown that the average SM voltage can be different from the dc link voltage, so long as the inequality described by (13) is valid for every time instant t.

$$V_{\text{cu}}^{\Sigma}(t) \geq v_{\text{u}}(t); \quad V_{\text{cl}}^{\Sigma}(t) \geq v_{\text{l}}(t) \tag{13}$$

Based on the principles explored in [1], [20], [21], Equations (8) and (9) can be modified to (14) and (15) respectively.

$$V_{\text{cu}}^{\Sigma} \approx k_{\text{d}} v_{\text{d}} + \frac{N}{2C k_{\text{d}} v_{\text{d}}} \left(\Delta W_{\Sigma} + \Delta W_{\Delta}\right) \tag{14}$$

$$V_{\text{cl}}^{\Sigma} \approx k_{\text{d}} v_{\text{d}} + \frac{N}{2C k_{\text{d}} v_{\text{d}}} \left(\Delta W_{\Sigma} - \Delta W_{\Delta}\right) \tag{15}$$

However, the energy ripple terms ΔW_{Σ} and ΔW_{Δ} remain the same as (10) and (11) respectively as they correspond to the actual power flow corresponding to the controlled dc link and ac quantities.

B. Arm Voltage Variation

Fig. 3 shows the desired voltage variation in the upper arm (blue) and lower arm (red) corresponding to the operating dc link voltage (green). The computation is shown for a dc link power at 1 p.u with an ac side power factor of 0.9. Two cases are considered, with the dc link voltage v_{d} at 1 p.u (Case I, solid line) and 1.1 p.u (Case II, dotted line). The sum capacitor voltage for upper arm (solid line, black) and lower arm (dashed line, black) are kept constant in both cases. This can be computed based on (14) and (15) with $k_{\text{d}} = 1$ for Case I and $k_{\text{d}} = 0.91$ for Case II.

It can be observed that in both cases the instantaneous arm voltages are always lower than the available sum capacitor voltages of the associated arm, thus respecting the constraint established by (13). This means that the desired operation can be achieved without increasing the voltage imposed on the SM capacitors and switches. Therefore, the enhanced dc link voltage does not require a corresponding increase in required voltage rating of the converter components in the considered conditions.

Further, it can be observed that a 10 % increase in dc link voltage results in a 5 % increment in the offset of the peak instantaneous arm voltages. This is because the absolute offset is split between the two arms, while the ac side voltage is kept constant. This implies that if dynamic dc link voltage enhancement necessitates some unavoidable increment in the SM voltages, this disproportionate change can offer some benefits.

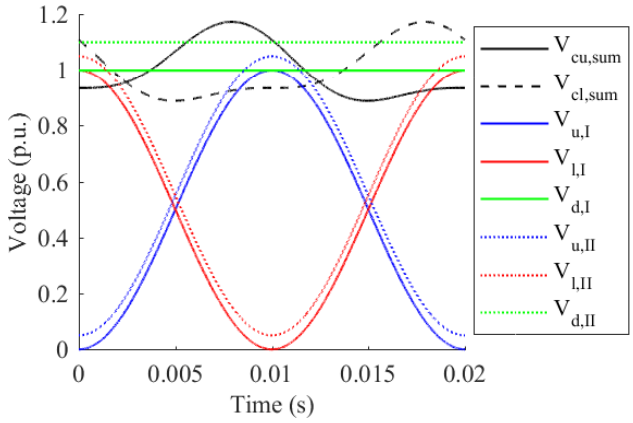

Fig. 3: Steady state voltage variation during MMC operation in one fundamental period for Case I (Solid coloured lines) and Case 2 (Dotted Coloured Lines) while maintaining the same sum capacitor voltages for 1 pu dc link power at 0.9 pf.

Another option available is to decrease the average sum capacitor voltages by 5 % while keeping the dc link voltage fixed at 1 p.u (Case III) as shown in Fig. 4.

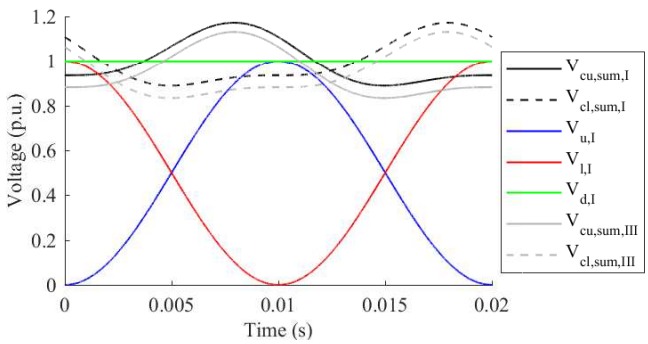

Fig. 4: Steady state voltage variation during MMC operation in one fundamental period for sum capacitor voltages in Case I (Black) and Case III (Grey) with the same dc and arm voltages at 1 p.u. dc link power and 0.9 pf at ac side.

The arm voltages in Case I and III are the same because both ac and dc side voltages of the MMC are the same while transmitting 1 p.u dc link power at 0.9 pf on the ac side. k_{d} of 0.95 is used and it can be seen that if it is lowered further, the constrain (13) may be breached, which is unacceptable. The advantage of operating in Case III is that switching losses can be lowered as compared to Case I and II, as shall be explored in Section IV-B.

C. Arm Current Variation

Fig. 5 shows the upper (blue) and lower (red) arm currents for Case I (solid line) and Case II).

With 10 % higher dc link voltage, there is an equivalent percentage reduction in the peak arm current for the same operating power. Since the ac voltage is unaltered, so is the ac component of the arm current. However, the dc component of the arm current reduces. The immediate inference is that

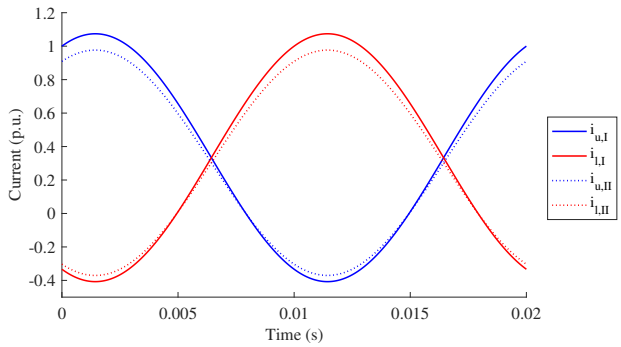

Fig. 5: Steady state upper and lower arm currents with rated dc link voltage operation ($i_{\mathrm{u,I}}, i_{\mathrm{l,I}}$) and dynamically enhanced dc link voltage ($i_{\mathrm{u,II}}, i_{\mathrm{l,II}}$) during full load operation.

the conduction losses reduce in case II as shall be quantified in Section IV-A. This is advantageous because dynamic dc link voltage enhancement is carried out at high active power transfer wherein the efficiency is most significant.

A second advantage is the possibility of reducing the component current rating. In [22] it was discussed that since switching losses are lower in the MMC IGBTs, the operating current rating is not chosen on the thermal constraints, but on the expected peak of the arm current. In case the dc link power demand is not expected to be raised beyond 1 p.u, the switch with lower current rating can be chosen using this concept. On the other hand, by keeping the current rating the same, power capacity boost can be achieved.

The steady state arm currents in case III are the same as case I, and therefore not shown. Consequently, it can be inferred that the conduction losses are higher in case III as compared to case II. Therefore, the total converter efficiency as a trade-off for conduction and switching losses governs the choice between operational mode represented by case II and III.

IV. Converter Losses

The effect of dynamic dc voltage enhancement on the converter efficiency is important to quantify. This section describes the MMC conduction and switching losses for the two cases considered in this paper. The analysis is based on the steady state loss model proposed in [23].

A. Conduction Losses

In Section III-C it was argued that the conduction losses are expected to be lower in case II as the arm currents are lower due to lower dc component of circulating currents corresponding to higher dc link operating voltage for the same power demand.

An important simplifying assumption made is that all switches are operating at maximum junction temperature of $125\,^{\circ}C$. In reality, the SM switches would be operating at lower temperature depending on the total losses corresponding to the switching frequency, the time of operation governed by insertion and bypass of relevant SM, cooling strategy employed and whether the conducting element is the IGBT or the anti-parallel diode depending on the direction of the arm current. On the other hand, these factors have similar influence on both the cases studied, while we are interested in exploring the worst scenario difference in losses. Furthermore, it can be deduced that since the arm current is lower in the second case, the actual junction temperature is lower. This implies that case II has lower conduction losses from operating temperature point of view.

It is necessary to establish which power electronic component of the SM is conducting at any given instant of operation [23]. Fig. 6 (a) and (b) show that with positive arm current, the diode D1 conducts when the SM is inserted, while IGBT T2 conducts when the SM is bypassed. Similarly, Fig. 6 (c) and (d) depict that when arm current is negative, IGBT T1 conducts in inserted while diode D2 conducts in bypass state.

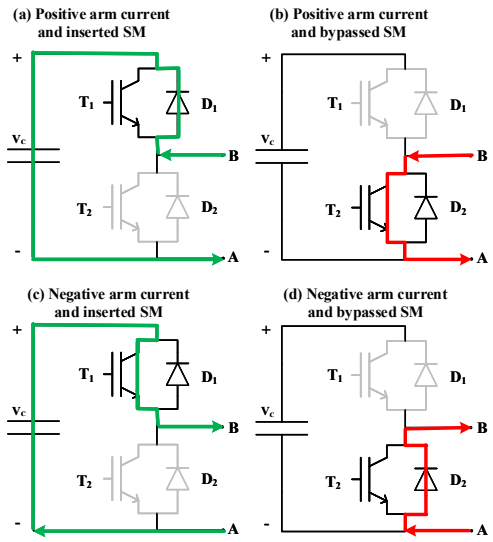

Fig. 6: Current Flow in inserted/bypassed SMs for different arm current directions.

Based on the current flow in SM devices, the instantaneous total upper arm conduction losses corresponding to the active IGBTs ($P^{\Sigma}_{\mathrm{cond,u,T}}$) and active diodes ($P^{\Sigma}_{\mathrm{cond,u,D}}$) in one fundamental time period T_{f} are given by (16) and (17) respectively. Similar equations can be written for the lower arm conduction losses.

$$P^{\Sigma}_{\mathrm{cond,u,T}} = \begin{cases} \frac{1}{T_{\mathrm{f}}}\int_0^{T_{\mathrm{f}}} (N - n_{\mathrm{u}}) \cdot V_{\mathrm{ce}} \cdot i_{\mathrm{u}} \cdot dt & ;\text{ if } i_{\mathrm{u}} \geq 0 \\ \frac{1}{T_{\mathrm{f}}}\int_0^{T_{\mathrm{f}}} n_{\mathrm{u}} \cdot V_{\mathrm{ce}} \cdot i_{\mathrm{u}} \cdot dt & ;\text{ if } i_{\mathrm{u}} < 0 \end{cases} \tag{16}$$

$$P^{\Sigma}_{\mathrm{cond,u,D}} = \begin{cases} \frac{1}{T_{\mathrm{f}}}\int_0^{T_{\mathrm{f}}} n_{\mathrm{u}} \cdot V_{\mathrm{f}} \cdot i_{\mathrm{u}} \cdot dt & ;\text{ if } i_{\mathrm{u}} \geq 0 \\ \frac{1}{T_{\mathrm{f}}}\int_0^{T_{\mathrm{f}}} (N - n_{\mathrm{u}}) \cdot V_{\mathrm{f}} \cdot i_{\mathrm{u}} \cdot dt & ;\text{ if } i_{\mathrm{u}} < 0 \end{cases} \tag{17}$$

V_{ce} is the voltage drop of the IGBT and V_{f} is the forward voltage drop across the diode while conducting current i_{u} under considered operating conditions. The instantaneous conduction current dependent voltage drops at $125\,^{\circ}C$ are found using interpolation of data-points in a look-up table obtained from the datasheets provided by the manufacturer [24]. n_{u} is the number of inserted SMs in the upper arm. In this paper, n_{u}

is determined from Equation (18), based on the nearest level control (NLC) described in [25], [26]. Instantaneous insertion indices corresponding to other modulation techniques such as carrier based pulse width modulation can also be used for computation, but this is not the focus of our present paper.

$$n_{\mathrm{u}} = round\left(N * \left(\frac{v_{\mathrm{u}}}{V_{\mathrm{cu}}^{\Sigma}}\right)\right) \tag{18}$$

The per unit steady-state diode, IGBT and total conduction losses in a single upper arm of the MMC for the two cases for one fundamental time period is shown in Fig. 7.

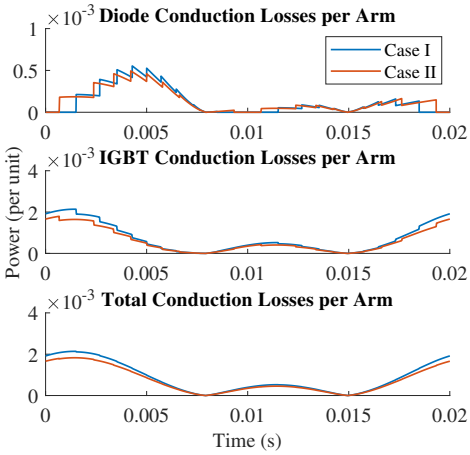

Fig. 7: Steady state conduction losses in one arm of the MMC for Case I and II.

As expected, the conduction losses are lower for Case II. Integrating over the fundamental time period and combining the conduction losses of all six arms of the MMC, the total converter conduction losses are 0.5 % for Case I and 0.44 % for Case II, expressed as a percentage of power transferred by the dc link. Since the arm current is the same, the conduction losses are the same for Case I and III.

B. Switching Losses

First, the switching losses corresponding to the upper arm are computed for NLC scheme. Each SM is therefore, operating at fundamental frequency. A discussion on estimating the switching losses for MMC with NLC is provided in [27]. Fig. 8 shows the level transition instants and the upper arm current for one fundamental period.

The level transition is +1 if a SM in upper arm inserted and -1 if a upper arm SM is bypassed. Since there are 9 SMs per arm, total number of transitions $N_{\mathrm{transitions}} = 18$ are observed. The circled group A represents positive arm current accompanied by positive transitions. From corresponding Fig. 6 (a) and (b) it can be deduced that SM commutation is accompanied by a diode D1 turn-on and transistor T2 turn-off. 'B' represents negative arm current accompanied with a positive transition, which corresponds to a diode D2 turn-off and transistor T1 turn-on as seen in Fig. 6 (c) and (d). Similarly, group C represents transitions accompanied with T1 turn-off and D2

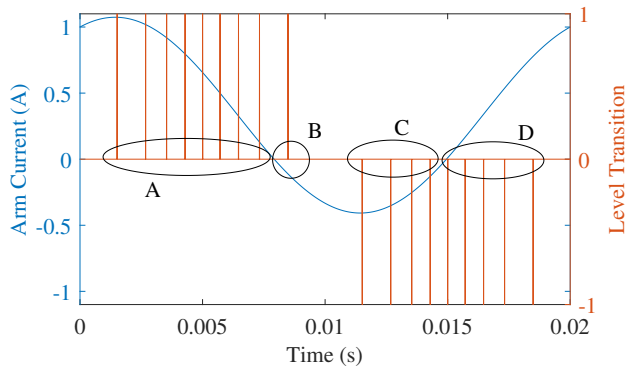

Fig. 8: Level transitions and corresponding arm current for one fundamental period for a 9 SM upper arm operating with NLC.

turn-on while transitions in group D are accompanied D1 turn-off and T2 turn-on.

For every transition, the switching losses are computed based on the knowledge of commuting devices. The turn-off losses of diode $E_{off,D}$, turn-off losses $E_{off,T}$ and turn-on losses $E_{on,T}$ of the transistor corresponding to the instantaneous current at 125 $^{\circ}C$ are determined by interpolating the look-up tables obtained from the device datasheet [24]. Integrating over one fundamental period, these are 0.03 % for case I, 0.029 % for case II and 0.028 % for case III. The losses are slightly lower in Case two because of lower arm currents. However, since the losses depend on the instantaneous currents during switch transition, this reduction is not proportional. The switching losses in case III are the lowest corresponding to the 5 % reduction in average SM voltages.

C. Converter Efficiency and Effective Frequency

The effective frequency f_{eff} at which the converter operates is given by (19) based on the number of submodules per arm N and switching frequency f_{sw}.

$$f_{\mathrm{eff}} = f_{\mathrm{sw}} * N \tag{19}$$

For a nine SM arm with fundamental switching frequency gives $f_{\mathrm{eff}} = 450$ Hz. During actual operation, the f_{eff} can be expected to be higher due to capacitor balancing and harmonic performance requirements, implying higher switching losses. Fig. 9 shows the total converter efficiency considering the conduction and switching losses in SMs of all the six arms for different operating cases with increasing f_{eff}.

The slope for efficiency with respect to frequency is slightly smaller in case II as compared to case I, implying that difference in efficiency improvement increases with f_{eff}. The slope is lowest for case III, however it is still less efficient than case II even at effective frequency of 4 kHz because the improvement in conduction losses is the decisive factor in the conditions studied.

V. Conclusion

The main conclusion is that under some operating conditions, it is possible to dynamically enhance the dc link

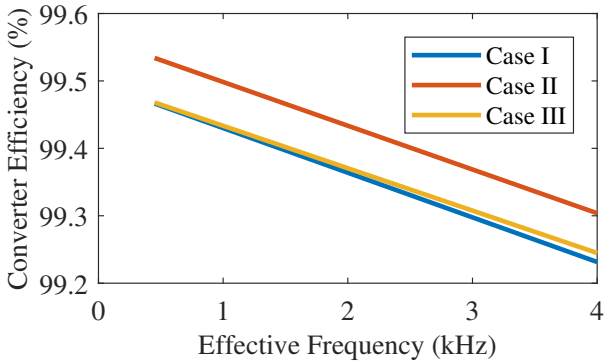

Fig. 9: Total converter efficiency with respect to the effective frequency of operation.

voltage of the MMC without imposing a higher voltage on its submodule components. This can potentially improve the power delivery capacity and at the same time, offer some system efficiency gains without increasing the designed ratings of the converter components.

On the other hand, as the operating conditions in terms of active and reactive power vary, the boundary of dc link voltage enhancement changes. If this concept is used for maximizing system efficiency, it can be applied whenever the relevant constraints allow such an operation over the lifetime. However, for improving the system capacity, it may be necessary to navigate the constraints actively to create a possibility to dynamically enhance the dc link voltage whenever required. Furthermore, for capacity gain objective, redesign of submodule capacitance may be necessary, as it is a function of the apparent power of the MMC. Therefore, depending on the control objective, the operational constraints and the corresponding potential of implementing this concept needs to be defined as a future objective.

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