

Out-of-band Interference Immunity of Negative-Feedback Amplifiers

Totev, E.D.

DOI

[10.4233/uuid:9cb2d621-5a55-404a-a278-8d562ad8f57b](https://doi.org/10.4233/uuid:9cb2d621-5a55-404a-a278-8d562ad8f57b)

Publication date

2021

Document Version

Final published version

Citation (APA)

Totev, E. D. (2021). *Out-of-band Interference Immunity of Negative-Feedback Amplifiers*. [Dissertation (TU Delft), Delft University of Technology]. <https://doi.org/10.4233/uuid:9cb2d621-5a55-404a-a278-8d562ad8f57b>

Important note

To cite this publication, please use the final published version (if applicable).
Please check the document version above.

Copyright

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

Takedown policy

Please contact us and provide details if you believe this document breaches copyrights.
We will remove access to the work immediately and investigate your claim.

Out-of-band Interference Immunity of Negative-Feedback Amplifiers

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus, Prof.dr.ir. T.H.J.J. van der Hagen,
chair of the Board of Doctorates
to be defended publicly on
Monday 4 January 2021 at 15:00 o'clock

by

Emil Dimitrov TOTEV
Master of Science in Electrical Engineering,
Delft University of Technology, The Netherlands
born in Sofia, Bulgaria.

This dissertation has been approved by the
promotor: Prof.dr.ir. W.A. Serdijn,
promotor: Prof.dr. J.R. Long,
copromotor: Dr.ir. C.J.M. Verhoeven.

Composition of the doctoral committee:

Rector Magnificus	Chairman
Prof.dr.ir. W.A. Serdijn	Delft University of Technology, promotor
Prof.dr. J.R. Long	University of Waterloo, promotor
Dr.ir. C.J.M. Verhoeven	Delft University of Technology, copromotor

Independent members:

Prof.dr.ir. F.P. Widdershoven	Delft University of Technology
Prof.dr.ir. B. Nauta	University of Twente
Prof.dr.ir. L.J. Breems	Eindhoven University of Technology
Prof.dr.ir. L.C.N. de Vreede	Delft University of Technology
Prof.dr. P.J. French	Delft University of Technology, reserve member

Published and distributed by:

Emil D. Totev
Delft
The Netherlands
e-mail: emil.totev@philips.com

ISBN 978-90-6824-066-5

Copyright © 2020 by E.D. Totev, Delft, The Netherlands.

All rights reserved.
No part of the material protected by this copyright may be reproduced or utilized in any form, electronic or mechanical, including photocopying, recording, or by any information storage and retrieval system, without written permission from the author.

Printed in the Netherlands.

Contents

1	Introduction	1
1.1	Background	1
1.2	Contributing factors	4
1.3	Example	6
1.4	Design challenge	7
1.5	Motivation	12
1.6	Problem definition	13
1.7	Thesis outline	15
2	Review of the state of the art	17
2.1	Distortion mitigation	18
2.1.1	Negative feedback	18
2.1.2	Filtering	20
2.2	Distortion cancellation	21
2.2.1	The differential stage	21
2.2.2	The symmetrically driven stage	26
2.2.3	The double differential pair	27
2.2.4	The bootstrapped differential pair	30
2.2.5	Error feed-forward	31
3	Non-linear distortion analysis	33
3.1	Non-linear small-signal transistor model	33
3.2	Analysis of the negative-feedback amplifier	38
3.2.1	Influence of C_μ	43
3.2.2	Influence of C_{out}	45
3.2.3	Node susceptibility analysis	49
3.2.4	Individual contributions of non-linearities	55
3.2.5	Out-of-band criterion	57
3.3	Conclusion	59
4	Simplified non-linear analysis	61
4.1	Amplifier stage model	62
4.1.1	Steady-state response	63
4.1.2	Intermodulation products	64

4.2	Linear analysis of negative-feedback amplifiers	64
4.2.1	Impact of spurious signals	64
4.2.2	Behaviour at high frequencies	66
4.3	Non-linear analysis approach	67
4.4	Example	68
4.4.1	Non-linear input stage	69
4.4.2	Non-linear output stage	70
4.4.3	Discussion	72
4.5	Conclusions	73
5	Design for immunity	75
5.1	Pole positions and interference	75
5.1.1	Loop versus system poles	76
5.1.2	Filtering of the first stage pole	77
5.1.3	Example	80
5.2	Local feedback	81
5.2.1	Frequency-dependent local feedback	83
5.2.2	Filtering versus local feedback	84
5.2.3	Example	85
5.3	Dummy stage placement considerations	88
5.4	The complementary differential stage	90
5.5	Non-linear local-feedback compensation	92
5.6	Predistortion	101
5.7	Conclusions and discussion	103
6	Design example	107
6.1	Signal source	107
6.2	Electrical size verification	108
6.3	Circuit implementation	110
6.4	Measurement results	116
6.5	Benchmarking and conclusions	118
7	Conclusions and recommendations	121
A	Biasing non-linear local-feedback loops	125
	Bibliography	127
	Summary	134
	Samenvatting	135
	About the author	136

Chapter 1

Introduction

“jip-en-janneketaal: eenvoudige,
voor iedereen begrijpelijke taal”

*Van Dale Groot woordenboek
van de Nederlandse taal*

1.1 Background

We live in a time when technology has become an indispensable ingredient of nearly every aspect of human life. A great variety of devices exist around us to facilitate even the most mundane everyday activity. Technology is pervasive and often indispensable in many areas of economy, culture, science, and society in general. Sometimes the devices we employ are part of a network. Their value lies in the ability to exchange information with their peers, and the rest of the infrastructure around them. Typically, a human being is the end user of this information. This is the case for numerous applications, such as electronic mail, remote patient monitoring, or voice communications. More and more often, however, the information represents interdevice communication enabling concerted action of a distributed system; machines talking to each other. A sensor network monitoring structural integrity is an example of that, a smart grid system is another. As the complexity and autonomy of such electronic systems increase, so do the volume and diversity of the exchanged information between their nodes. A sustained increase in the number of connected devices has led to a rising demand for information exchange capacity. Figure 1.1 illustrates the observed trends in user base growth for several areas of the telecommunications sector [1]. The total number of globally deployed fixed telephone lines is plotted in the figure, together with the number of mobile telephony subscribers and Internet users, over a period of two decades. The data suggests that while the amount of fixed lines is past its peak, the number of mobile subscribers is still increasing, although it appears to be saturating as nearly everyone in the world already owns, or has access to a mobile telephone. It is also apparent

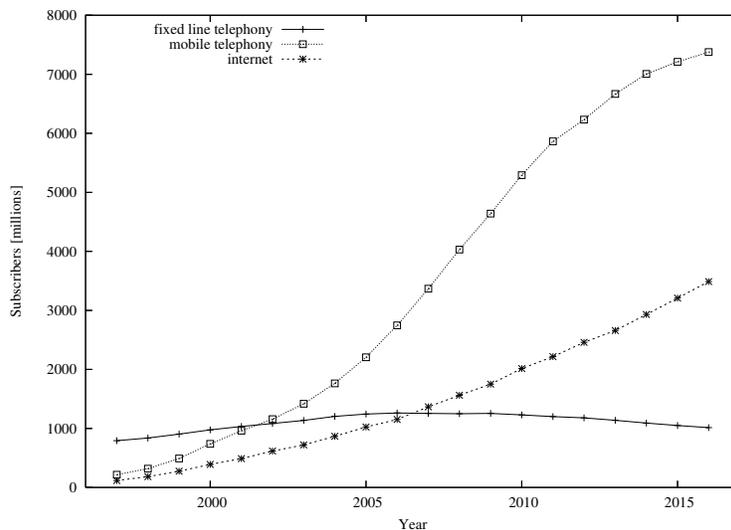


Figure 1.1: Steadily rising deployment of global communications media, and in particular wireless.

that there is an exponential growth of Internet usage, with the number of users already having exceeded that of the available fixed telephony lines. The land line network has traditionally been the infrastructure of choice for (domestic) broadband Internet access. From the curves follows that even at maximum utilisation, the fixed line infrastructure cannot be the sole provider of Internet connectivity. Of course, dedicated lines are also used, but these are typically quite expensive for domestic deployment. In addressing this issue, it has become feasible to offer various data services, including regular Internet access, wirelessly. Figure 1.2 shows this trend. It is apparent that wireless Internet has shown an exceptionally strong growth and is now the dominant access mode. In view of the intense demand and the increasingly richer content supplied to mobile subscribers, the trend is expected to continue. This shift towards wireless is observed across nearly all segments of the telecommunications sector.

Both industry and governments are working to accommodate the growth and provide for future expansion of the wireless infrastructure. While new higher-frequency bands are continuously being approved, and high-speed interchange standards emerge, much effort is put in utilising the current technology to the fullest. Consider an existing communications channel that is to be optimised. According to Shannon [2] the information carrying capacity, C , of a channel is given by

$$C = B \log_2 \left(1 + \frac{S}{N} \right), \quad (1.1)$$

where B is the channel bandwidth, and $\frac{S}{N}$ is the ratio of signal to noise power.

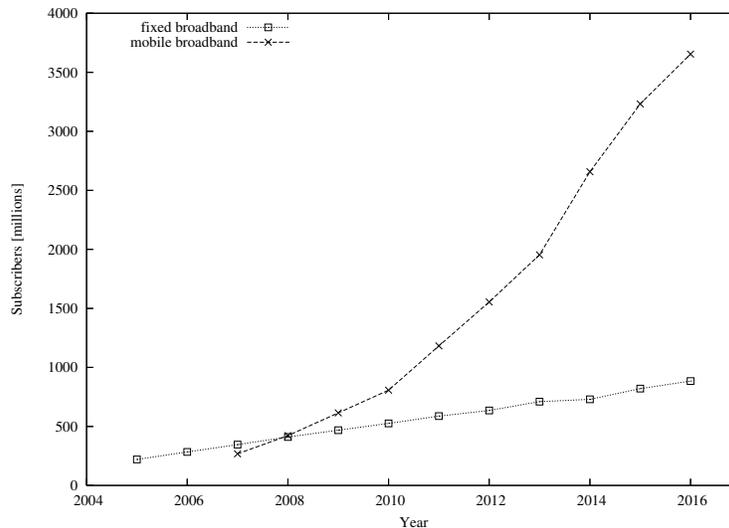


Figure 1.2: Fixed line vs. wireless broadband Internet deployment.

Assuming a Gaussian distribution of the noise spectral density, i.e., white noise, several steps can be taken in order to increase the channel capacity:

- the bandwidth, B , could be increased. For an existing channel within a regulatory framework this is almost never a viable alternative. So, either auxiliary channels are added to the system, thereby increasing its effective bandwidth, or the entire system is migrated to a new channel with a wider bandwidth,
- the noise floor, N , of the system could be decreased. Noise levels are governed by the physical properties of the equipment, and ultimately present a hard limit to optimisation efforts,
- the signal power, S , could be increased. Of course, this can not be scaled arbitrarily and is restricted not only by what is practical to implement, but also by various rules and regulations. The latter ensure that channels adjacent in the frequency domain do not interfere with each other, nor that strong channels interfere with weak ones. This is a fundamental consideration, addressing the fact that the frequency selectivity of electronic equipment is not infinite.

Generally, in response to the increasing demand for information exchange capacity, two trends may be differentiated:

- there is a continuous drive towards higher frequencies as bands of existing transmission domains become congested, and expansion is called for,

- power levels are maximised in order to fully utilise existing infrastructure.

As a result, both the frequency and energy density of communications bands are rising. This development does not pass unnoticed in equipment operating at the low end of the frequency spectrum. Often this is affected adversely in the presence of high-frequency signals, which it is neither designed to handle, nor to detect. Sometimes, as more and more functionality is built into a device, the high-frequency disturbance may even originate from within the device itself. For this reason, it is becoming increasingly important to ensure that low-frequency systems, such as baseband negative-feedback amplifiers, are immune to interference from high-frequency signals. Design methods are being developed to improve the robustness of baseband circuitry, and these are the focus of the present investigation. The following section gives an overview of the factors responsible for the interference mechanism.

1.2 Contributing factors

Baseband negative-feedback amplifiers comprise a class of electronic circuits that provide signal amplification, or buffering, prior to subsequent signal processing, in a wide range of analog and mixed-signal applications, such as audio, video, sensing, and interfacing. Negative feedback is a technique that ensures accurate gain is achieved across the operating frequency range [3]. Baseband amplifiers typically process signals from DC to a certain maximum frequency. This frequency band of operation is known as the information band. Like most electronic circuits, baseband negative-feedback amplifiers are normally implemented with semiconductor devices, such as transistors and diodes. These devices exhibit non-linear behaviour while processing electrical signals [4]. Active components, such as transistors, provide signal gain and are essential in the design of a semiconductor amplifier. As they are in the signal path, they invariably contribute some degree of non-linearity to the overall transfer function of the amplifier.

The general form of an arbitrary non-linear transfer function of a time-dependent input quantity, $x(t)$, to a time-dependent output quantity, $y(t)$, is given by the infinite power series:

$$y(t) = a_0 + a_1x(t) + a_2x^2(t) + a_3x^3(t) + \dots \quad (1.2)$$

If a single-tone signal with an amplitude A_1 and angular frequency ω_1 is present at the input, i.e., $x(t) = A_1\cos(\omega_1t)$, the output becomes:

$$y(t) = a_0 + a_1A_1\cos(\omega_1t) + a_2A_1^2\cos^2(\omega_1t) + a_3A_1^3\cos^3(\omega_1t) + \dots \quad (1.3)$$

This can be rewritten as:

$$y(t) = a_0 + \frac{a_2A_1^2}{2} + \left(a_1A_1 + \frac{3a_3A_1^3}{4}\right)\cos(\omega_1t) + \frac{a_2A_1^2}{2}\cos(2\omega_1t) + \frac{a_3A_1^3}{4}\cos(3\omega_1t) + \dots \quad (1.4)$$

So, a single frequency, ω_1 , present at the input gives rise to many frequencies at the output. This process is known as non-linear distortion. The new frequencies are called harmonics and are integer multiples of ω_1 , i.e., $0, \omega_1, 2\omega_1, 3\omega_1$, etc. Starting from the second-order, all harmonics occur at frequencies higher than ω_1 . No signals will be observed between 0 and ω_1 , for example. However, if a second tone is present at the input, with an amplitude A_2 and frequency ω_2 , the resulting output spectrum will contain all linear combinations of ω_1 and ω_2 :

$$m\omega_1 + n\omega_2 \quad m, n \in \mathbb{N}. \quad (1.5)$$

Harmonics of ω_1 and ω_2 will occur for either m or n equal to zero in (1.5). All other frequency components are referred to as intermodulation (IM) products. Certain IM products are of particular interest to the circuit designer, such as IM_2 (signals at frequencies $\omega_1 \pm \omega_2$) and IM_3 (signals at frequencies $2\omega_1 \pm \omega_2$ and $\omega_1 \pm 2\omega_2$). Should ω_1 and ω_2 be close to each other, even if each of them is large in absolute value, their difference, i.e., the IM_2 product, could be at a much lower frequency. Consider Figure 1.3, which illustrates the interaction between two adjacent high-frequency bands with centre frequencies ω_1 and ω_2 , and a (non-linear) baseband circuit, such as an amplifier. The bandwidth of

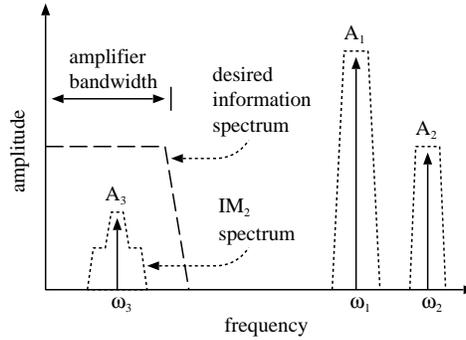


Figure 1.3: Illustration of out of band interference in a low-frequency device.

the amplifier is much lower than either ω_1 or ω_2 . As a result of non-linear distortion, the IM_2 product of the two high-frequency signals appears in the baseband. In the figure, ω_3 is the difference frequency of ω_1 and ω_2 . This corresponds to a situation, such as the one discussed in the previous section, where a high-frequency communications device interferes with a baseband circuit. The baseband application could be completely independent from the interferer, such as a self-amplified computer speaker that picks up interference from a nearby mobile telephone. Interference could also occur between two parts of the same system, for example between the (low-frequency) touch-screen driver and the (high-frequency) wireless-network radio front-end of a smart watch. Of course, the latter is normally anticipated during the system design, and the appropriate measures are taken to avoid it. In practice, problems with interference occur

when the baseband circuit is unintentionally exposed to an interferer, or its design is insufficiently robust to cope with the presence of one that is expected.

This outlines the mechanism, through which a baseband negative-feedback amplifier can be perturbed by signals of frequency (far) beyond its information band. Such signals are referred to as out-of-band interference. Interaction between an (out-of-band) interferer and an electronic device is also known as radio-frequency interference (RFI). Once the intermodulation products of out-of-band interferers enter the information band, they become indistinguishable from the information being processed, and effectively degrade its signal to noise ratio (SNR). Strong interferers could even saturate the amplifier and cause it to cease processing information altogether. The effect of RFI is difficult to predict without prior knowledge of the interferer, and much design effort could be expended to avoid it.

1.3 Example

Amateur class rocketry is increasingly becoming a platform for scientific research, education and hardware testing. An amateur rocket is equipped with a motor providing several seconds to several tens of seconds of sustained thrust in a single burn. The craft is thus able to attain an altitude of up to a few kilometres above the launch pad, before its propellant runs out. A parachute is subsequently deployed, allowing the rocket, and any useful payload it may contain, to descend safely to the surface. Parachute deployment is typically accomplished by ejecting the nose section of the rocket with a pyro charge. Ignition of the pyro charge is controlled by a board computer, based on elapsed flight time or atmospheric pressure data. Due to the considerable height attained, and an unpredictable descent trajectory, many amateur rockets are equipped with a radio beacon. This serves to guide recovery parties to the landed craft. In the Netherlands, the Dutch Amateur Association for Rocket Research (NAVRO) [5] is one of the organisations that handles launches, hardware testing and certification. At a launch event of the association the craft of Krancher and Uitendaal [6], shown in Figure 1.4, is equipped with a supplementary tracking system. This comprises a GPS (Global Positioning System) receiver coupled to a mobile telephone. Every 5 minutes an SMS (Short Message Service) message is sent, containing the current geolocation coordinates. This is necessary, as the regular 433 MHz transponder is not always effective, and vehicles are lost after leaving line of sight. The new tracking module is placed in the electronics compartment of the rocket, together with the flight electronics. This is shown in Figure 1.5. The mobile telephone can be seen stacked above a flight computer board. It is a GSM (Global System for Mobile Communications) 1.8 GHz device, capable of transmitting at power levels up to 33 dBm (2 W). The launch is conducted on an artillery testing range, far from communications infrastructure. The nearest GSM base station is, therefore, at a considerable distance, and the mobile telephone must transmit at a high power level. Shortly before takeoff, the board computers of the rocket are activated, and the countdown commences. Several



Figure 1.4: The rocket before launch.

seconds prior to ignition, the mobile telephone transmits its periodical SMS message. The GSM signal couples into the flight electronics and causes a premature activation of the pyro actuator releasing the parachute. This is captured in Figure 1.6. The nose cone is ejected, leaving the craft in a configuration that would have catastrophic consequences should the engine be fired. As a result, the flight is aborted, with some damage nevertheless sustained by the rocket. Later investigation by Uitendaal [6] positively correlates misfiring of the pyro charge with SMS transmission. This clearly identifies the incident as an example of out-of-band interference. The flight electronics is not designed to handle the high-frequency GSM signal, leading to unpredictable results. In this case, under the influence of interference, the board computer registers a sudden altitude drop. This is a condition for parachute deployment, which is duly executed. During the payload design no precautions are taken by the craft operators to improve its robustness to interference. It is assumed that the board computer is already suited for work alongside a radio transponder, so there is no objection to operate it next to a mobile telephone. However, the power level (and frequency) of the GSM signal is significantly higher than that of the transponder. It is able to couple in on the atmospheric pressure sensor front-end and be interpreted as a pressure increase.

1.4 Design challenge

The problem of RFI is not new, and its effect on electronic circuits is the topic of continuing research. It is generally approached as a type of electromagnetic

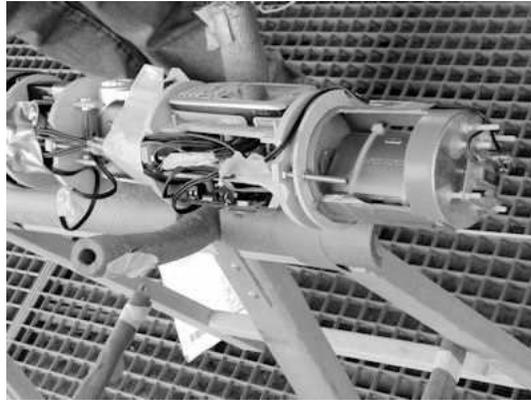


Figure 1.5: Electronics compartment, including mobile telephone to be used for localization after landing.



Figure 1.6: Premature parachute deployment prior to launch due to interference from a mobile telephone.

interference (EMI). A typical interference scenario consists of three main components:

- the source of interference: a (sub)system that produces an electromagnetic (EM) perturbation, either conducted or radiated, that ultimately causes the interference. As a rule, the signal is an unintended consequence of the

functioning (or failure thereof) of the system, but in many cases it is an intended feature, albeit for a different purpose,

- the channel: the medium through which the electromagnetic perturbation travels, after being produced by the interferer. This medium could be a conductor or an insulator and determines the mode of propagation of the interference signal,
- the interference target: the (sub)system that unintentionally receives the disturbance and experiences some loss of functionality after interacting with it. The interference source and target could be parts of the same device, or be completely independent systems, separated by a large distance. Because of the adverse effect the interferer has on the target, the latter is also referred to as the victim.

Depending on the distance between interferer and victim, and the nature of the channel, the interference problem could be treated as a form of cross-talk [7]. This could be classified as one of the following:

- capacitive (electrostatic): near-field electric field coupling. The dielectric (or free space) between the coupled bodies serves as channel. The permittivity of the channel determines the amount of coupling,
- inductive (magnetostatic): near-field magnetic field coupling. The channel is either an insulator or a galvanically isolated conductor. The permeability of the channel determines the amount of coupling,
- electromagnetic: coupling through an EM wave in the far field. In this case, the channel is typically the free space between conductors,
- common path (galvanic): coupling through an electrical current flowing through a common branch of an electrical circuit. For example, two independent subcircuits of the same system could influence each other by sharing a common (non-ideal) ground. The conductivity of the common path will determine the amount of coupling.

Figure 1.7 depicts a general interference scenario and emphasizes its distinct components. The source of interference could be unintentional, such as the electric discharge of a car ignition system, or intentional, such as the electromagnetic signal emitted by a radio broadcast antenna. The free space between the interferer and the victim acts as channel for the signal. The victim, in this example a record player, unintentionally picks up the electromagnetic radiation and suffers a degradation of the quality of its signal processing, manifesting as noise in the audio band.

A number of methods have been developed to mitigate EMI. Perhaps the most trivial of them is to eliminate the source of interference. In the absence of a disturbance, the susceptibility of the target ceases to be an issue. Unfortunately, this approach is the least practical. Often, it is either unfeasible or undesirable

to eliminate the interferer. Additionally, the target remains vulnerable and will be affected if another source of interference appears.

It is also possible to enhance the separation between the source and the victim. This is depicted in Figure 1.8 for the spatial domain - the distance between source and victim is increased. The amount of signal power picked up by the victim is inversely proportional to the square of the distance to the interferer, so increasing the distance will diminish the effective strength of the latter. Attenuation by the channel could reduce the power of the disturbance even further. The directionality of the interferer may also be made use of. Separation between interferer and target could also be obtained in a different domain, such as:

- amplitude: if the ratio between the powers of the information signal and the interference signal is large enough, effective signal processing could still take place,
- frequency: ensuring that the information signal is at another frequency than the interferer is common practice. However, this is ineffective in the case of out-of-band interference,
- time: the victim operates only while the source of interference is inactive, and is deactivated otherwise,
- signal carrier: if the interferer and victim process signals in a different signal carrier domain, i.e., electrical vs. light, or mechanical vibration, it is easier to avoid interference between the two.

Achieving domain separation normally restricts design freedom and applicability. It may be costly and is not always practical. Signal carrier domain, for instance, is generally fixed before an EMI problem manifests itself and changing it requires a complete redesign of the system. Additionally, as seen in the case of out-of-band interference, domain separation is not necessarily effective.

To reduce cross-talk, the channel between the source of interference and the target could be modified to impede or altogether eliminate the propagation of the disturbance. This is shown in Figure 1.9. Shielding and filtering are

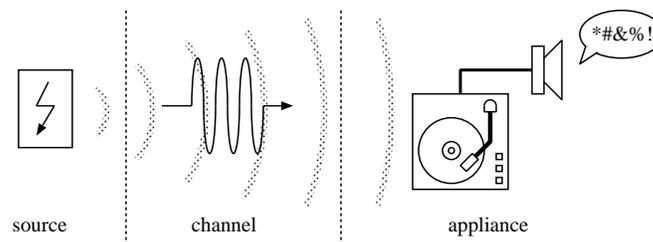


Figure 1.7: Interference scenario showing various components involved.

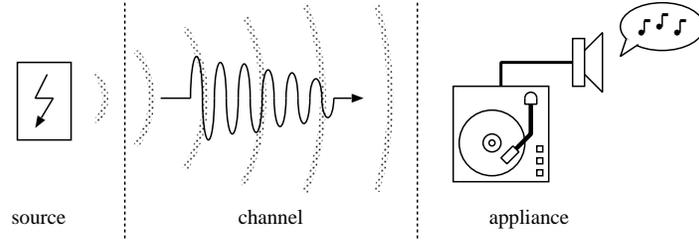


Figure 1.8: Increasing the distance between interferer and victim.

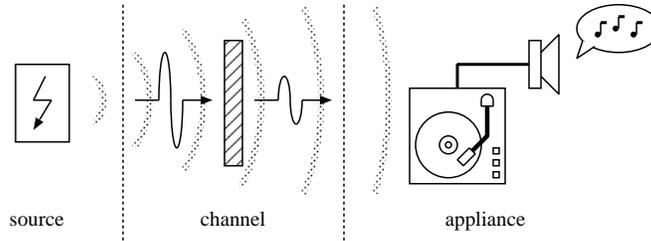


Figure 1.9: Introducing an obstruction between interferer and victim.

examples of this approach. They attenuate the interfering signal and ensure an insignificant fraction of its energy reaches the victim. Shielding is used to reduce electromagnetic coupling, either in the near or the far field. Filtering has a similar effect, but in the electrical domain. Shielding involves placing either the source of interference or the susceptible (sub)system in a suitable enclosure that prevents signals from passing through. Filtering normally uses a passive component network to suppress the frequency band of the interference in conductors carrying the interference signal to the victim.

The classical approach of EMI mitigation is to prevent the disturbance from reaching any semiconductor (i.e., non-linear) component of the victim's circuitry [8]. This is usually achieved through shielding and filtering. However, certain circuit topologies are less susceptible to interference, despite the fact that they contain non-linear components. It is, therefore, possible to design an electronic circuit in such a way that its primary function is not (significantly) influenced by EMI. This results in an application that can be placed freely in a hostile electromagnetic environment, as shown in Figure 1.10. No precautions are necessary regarding the nature of the interferer, and the transmission of its signal through the channel.

A likely subsystem of the record player depicted in Figure 1.7, that converts the (out-of-band) radio-frequency (RF) interference into an audible signal, is the audio amplifier. This is typically a baseband negative-feedback amplifier operating in the audio range (20 Hz-20 kHz) and is an example of the class

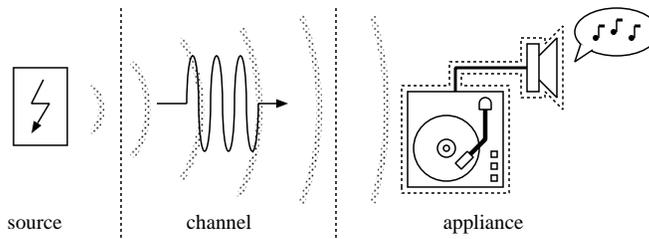


Figure 1.10: Victim immune to interference by design. No further precautions necessary.

of electronic circuits analysed in this work. An application that conforms to the situation shown in Figure 1.10 requires an amplifier that is inherently immune to out-of-band interference. A design method is, therefore, sought to produce such a circuit. This would translate into a set of measures preventing or actively opposing changes in biasing, transfer function, linearity, or other amplifier parameters, under the influence of an interference signal. Such measures are executed on circuit level, and ideally result in a topology that retains the original performance parameters, but is less susceptible to EMI.

As outlined in Section 1.2, the non-linear circuit components of a baseband negative-feedback amplifier provide the mechanism for susceptibility to out-of-band interference. Through the second-order intermodulation product, IM_2 , the difference frequency of two out-of-band signals can enter the information band. The second-order intercept point, IP_2 , is a measure for the relative linearity of an amplifier [9] and is based on the ratio of the low-frequency amplifier gain, A , and IM_2 :

$$IP_2 = \frac{A}{IM_2}. \quad (1.6)$$

A circuit with a high IP_2 figure would produce less second-order intermodulation distortion and would consequently be less susceptible to EMI. In order to obtain inherent immunity to out-of-band immunity on circuit level, a baseband negative-feedback amplifier should, therefore, be designed for a maximal IP_2 . Some methods have been proposed to achieve that, using different architectural approaches. These are predominantly based on distortion cancellation by means of symmetry [10], or isolation and subsequent subtraction of error terms [11]-[13]. It is also possible to reduce distortion by modifying the impedance of selected nodes of the amplifier circuit [14].

1.5 Motivation

Baseband amplification aims to boost the amplitude of a signal, without adding any significant noise or distortion. Over time, a tremendous amount of effort has been invested in improving the in-band noise and linearity performance of

amplifier circuits [15, 16]. Methods exist for systematic amplifier design optimisation [17] to obtain the best trade-off between the available circuit resources and the performance obtained. However, much less attention has been given to the impact of out-of-band interference signals on the operation of a baseband amplifier, and how baseband circuitry can be optimally configured to minimize it [18]. The latter is rapidly gaining importance due to the steadily growing number of wireless (RF) interferers.

Protection of the desired signal from EMI in a baseband application is typically implemented through passive filtering and shielding. While effective, this approach is considered too expensive for low-cost, highly integrated wireless systems on a chip (SoCs) intended for high volume production. The use of transformers, inductors or large capacitors, for filtering and isolation, in amplifier circuits tends to be avoided, to realize the highest level of integration on chip while minimizing chip area and cost. Shielding is not always practical to apply, such as when the source of interference is located on the same chip die as the baseband circuitry. Even when applicable, it is associated with its own set of drawbacks [19]:

- placing the device in a shield makes it less accessible,
- including a shield in the design increases its price,
- the final implementation is heavier and bulkier,
- the appliance is more difficult to build and maintain.

Addressing interference immunity early in the design process tends to reduce the overall development cost [8, 19]. Often EMI problems are only discovered during system testing and certification. This is far into the development cycle, and the necessary corrective action can be costly in terms of time to market, additional materials, and complexity. Sometimes, an EMI problem is discovered when the system is already on the market, which can be even more difficult to solve. For this reason, it appears most cost-effective to address out-of-band interference during the initial circuit design. Implementing circuit topologies that are inherently immune to interference eliminates the need for subsequent mitigation on system level using resource-intensive methods, such as filtering, decoupling, and shielding.

1.6 Problem definition

To overcome the disadvantages of current methods for EMI reduction and address the emerging need for low-cost, robust baseband amplifiers, new circuit design techniques are pursued in this work to improve the immunity of negative-feedback amplifiers to out-of-band interference. These techniques are intended to be orthogonal to standard amplifier design methods, and existing EMI mitigation strategies. Orthogonality in this context implies that the original performance of the amplifier is not influenced by the functionality added to increase

its immunity to out-of-band interference. Moreover, classical EMI mitigation methods, such as shielding and filtering, could still be made use of independently, to render the system even more robust.

The present analysis is restricted to negative-feedback amplifiers with a low-pass response that are intended for in-band operation from DC to a corner frequency, f_c , defined by the desired information bandwidth. Out-of-band signals lie at frequencies higher than the upper corner frequency of the information band. Second-order intermodulation is assumed to be the dominant source of interference at baseband. Desensitization and blocking are regarded as high-power effects [20] and are not treated in this work. These are third-order intermodulation mechanisms which are assumed to be of secondary importance to the present analysis. The amplifier under investigation is expected to be functioning well below levels where clipping appears at its output, with distortion products that are comparable to the desired signal (i.e., weak distortion generating mechanisms). Figure 1.11 illustrates the different operating regions of a negative-feedback amplifier as a function of frequency and signal level. The

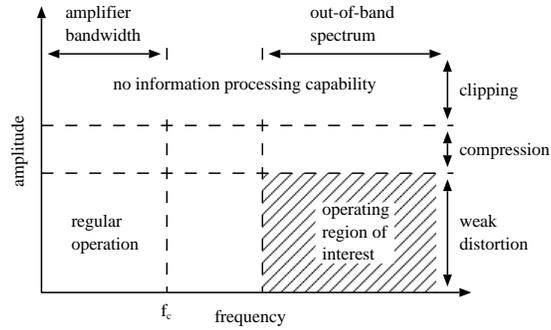


Figure 1.11: Identifying the region under investigation in the signal space.

lower-left quadrant reflects the normal operating conditions of the circuit, i.e., from DC to the corner frequency, f_c , and for signal swings that are sufficiently low to cause only weak distortion. As the signal swing increases, compression effects commence. Further increase of the signal level leads to clipping, and the loss of information processing capability of the amplifier. Along the horizontal axis, as the frequency increases, the out-of-band portion of the spectrum is reached. The shaded section of Figure 1.11 indicates this frequency range, for signal levels such that only weak distortion occurs. This defines the out-of-band signal space assumed throughout the study.

A circuit approach is chosen to improve the out-of-band interference immunity of baseband amplifiers. This is identified as the most flexible and broadly applicable method, and also the most cost-effective. A circuit solution gives an immediate advantage in all other interference mitigation scenarios. Design methods are considered that are suitable for monolithic integration, or can be

applied in an already integrated solution. Hence, no use is made of (large) capacitors or inductors. Similarly, bulky components, such as transformers, are avoided. Furthermore, no distinction is made of semiconductor component type or technology (e.g., silicon CMOS/BICMOS or III-V HBT).

Designers favor differential circuit topologies when dealing with interference caused by second-order intermodulation (IM_2), because IM_2 distortion products are rejected by a perfectly symmetric differential circuit (i.e., IP_2 approaching infinity) rendering an amplifier insusceptible to EMI. However, a purely differential source and load are required. Also, a differential signal path increases the pin count and packaging costs of the amplifier and limits the design freedom when interfacing the amplifier to other circuit blocks. Therefore, input and output signals in many applications are single-ended. For example, capacitive sensors are often buffered with a single-ended FET preamplifier to lower their source impedance [21]. To address such practical situations, the emphasis in this work is placed on single-ended input and output configurations, while differential circuits are applied internally.

In the following analysis, active components are modelled by a simple equivalent circuit in order to obtain tractable expressions for the Volterra kernels of the system. The transistors are represented by (non-linear) voltage-controlled current sources [22], where the device transconductance is the foremost source of non-linearity. In addition, only the linear capacitive component of the transistor input impedance is considered, as this is expected to dominate the frequency response for out-of-band interference [23]. These simplifications have been verified by comparing the resulting circuit response with predictions from the full device models in a circuit simulation.

1.7 Thesis outline

An overview of the most commonly used design methods for addressing out-of-band interference in negative-feedback amplifiers is given in Chapter 2. The mathematical tools for non-linear distortion analysis are presented in Chapter 3. A simplified non-linear small-signal transistor circuit model is developed and discussed. The Volterra series is subsequently used for circuit analysis. In Chapter 4, a simpler alternative to the Volterra series approach is proposed that is tailored specifically to out-of-band interference in negative-feedback amplifiers. This is easier to apply in initial calculations where general trends are investigated. Chapter 5 proposes several new methods for improving the out-of-band interference immunity. A novel technique is implemented in a practical amplifier circuit and verified experimentally. Chapter 6 details the measurement setup, procedure and results.

Chapter 2

Review of the state of the art

“Awareness of ignorance is the beginning of wisdom.”

Socrates

Several directions can be explored in pursuing the design for immunity to out-of-band interference of negative-feedback amplifiers. These can be grouped according to their underlying principle and form two general classes; one is based on distortion mitigation, and the other on distortion cancellation. The former attempts to reduce the signal swing present at the input of non-linear circuit components, while the latter employs various methods to eliminate some of the distortion in an amplifier so that the influence of an out-of-band signal is minimised. Figure 2.1 illustrates this classification, together with the further differentiation of solution approaches. Distortion cancellation addresses the root cause of the interference mechanism and, as such, is considered as the more robust method. It is based on accepting that non-linear behaviour is always present in a circuit and pursues arranging it so that the distortion products of different devices cancel each other out. This could be achieved either by suitably predistorting the signal arriving at a non-linear component or by applying the same excitation to two identical non-linearities, and then subtracting the distortion products. The latter technique is based on symmetrical compensation and could be implemented in a number of different ways. These are also shown in Figure 2.1 and will be treated in detail later in this chapter. An example of distortion mitigation is using the frequency selectivity of electronic components to prevent out-of-band signals from reaching non-linearities present in a system. Here, an obstruction is created in the path of the interference signal, between its source and the point of entry into the information band. This blocks the disturbance but can be made transparent to the regular information-carrying quantity that the amplifier handles normally. Since device non-linearities remain unaffected, however, this method is generally not as robust as distortion cancellation. The system is then still potentially susceptible to out-of-band interference, which may reach its vulnerable components along a different route.

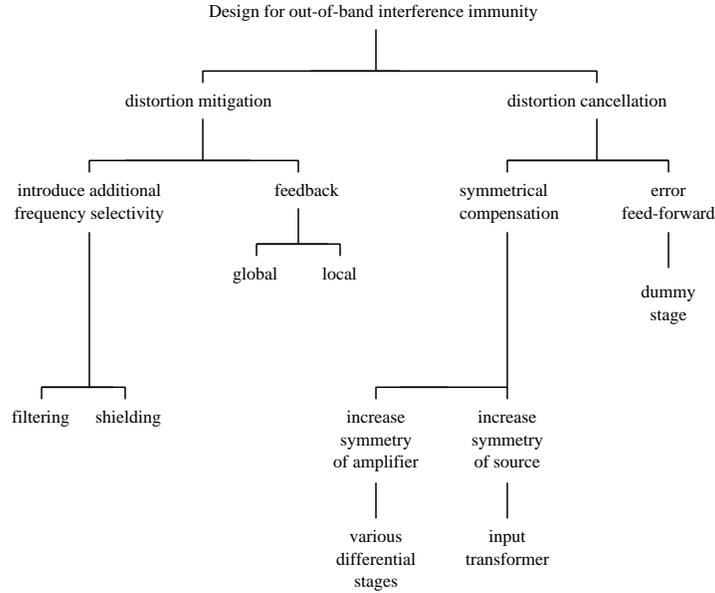


Figure 2.1: Review of methods to achieve EMI resistant design.

Shielding is included in Figure 2.1 to indicate its place in the classification but is outside the scope of the present investigation. As discussed in Chapter 1, this work focuses on circuit-based methods for immunity enhancement.

Ideally, steps taken to lower EMI susceptibility should not (adversely) influence the in-band performance of a negative-feedback amplifier. Here, it will be shown that this is generally not the case. To obtain an optimal circuit, a certain degree of orthogonality is required between in-band design and out-of-band interference immunity enhancement. Such orthogonality is fundamental to structured amplifier design and ensures the developed methodology can be applied with uniform success in every situation. Of course, often a compromise has to be made in favour of a particular performance metric, at the expense of another. The choice is then left to the designer to determine the exact trade-off. A number of such cases are considered here. This serves to give the designer a better perspective of the available options and could provide a viable solution when some in-band performance may be sacrificed to improve EMI immunity.

2.1 Distortion mitigation

2.1.1 Negative feedback

Negative feedback was originally conceived as a linearisation technique and is capable of suppressing the distortion products of a non-linear amplifier [3]. Con-

sider the general topology of an amplifier with a global negative-feedback loop shown in Figure 2.2. Linearisation is achieved by ensuring that the transfer

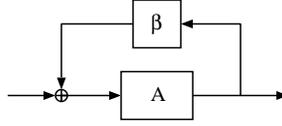


Figure 2.2: Global negative-feedback amplifier topology.

function of the feedback network, β , is linear. Provided that the (non-linear) forward gain, A , is large enough, the transfer function of the entire system is essentially dependent only on β and is, therefore, also linear [17, 20]. Effectively, negative feedback achieves a lowering of the signal level at the input of A . This results in an exponential decrease of its non-linear products represented by the high-order terms of the Taylor decomposition (1.2). Negative feedback can also be applied to individual components or whole sub-circuits of the forward-gain section. This is depicted in Figure 2.3 and is known as local feedback. In this

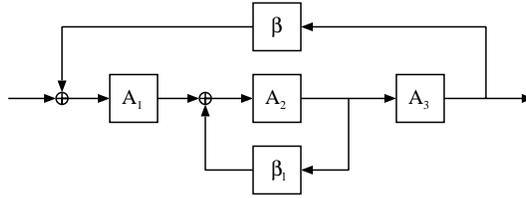


Figure 2.3: Local feedback in a negative-feedback amplifier.

example, A is partitioned into three stages, A_1 , A_2 and A_3 , where $A = A_1 A_2 A_3$, and β_i is the (linear) local-feedback coefficient. Linearisation of A_2 is achieved by trading-in some of its gain at the expense of the overall system loop gain. For this reason, applying local feedback at an arbitrary place in a negative-feedback amplifier generally degrades its overall non-linear distortion performance. This may only be avoided by placing local feedback across the amplifier stage that dominates the linearity behaviour. The loss of performance can then be insignificant [49].

In order to deal with out-of-band signals using negative feedback, sufficient forward gain must be available at the frequency of the interference [18]. This is not the case for a global feedback baseband system (as shown in Figure 2.2) where the out-of-band loop gain is normally too low for linearisation to occur. However, since the transit frequency of the devices used to implement the forward gain of a negative-feedback amplifier is typically an order of magnitude, or more, above the amplifier's bandwidth, local feedback could still be effective. Applying it without further precautions generally becomes a trade-off between

in-band linearity and susceptibility to out-of-band interference.

2.1.2 Filtering

Filtering is a well-known method for frequency discrimination based on the properties of (linear) reactive components, such as capacitors and inductors [24]. Passive filters are, therefore, suitable for attenuating high-frequency signals without producing non-linear artifacts, such as intermodulation products. They present a useful approach for dealing with out-of-band interference, as the frequency bands of the information signal and the interference are clearly distinct; the former needs to be admitted while the latter is suppressed. Filtering may be applied both at the input(s) of a negative-feedback amplifier (Figure 2.4a) and in its interior (Figure 2.4b) in order to protect components that are particularly vulnerable to disturbances. In practice, a number of factors may limit the scope of applications where filtering is feasible. Placing a filter at the

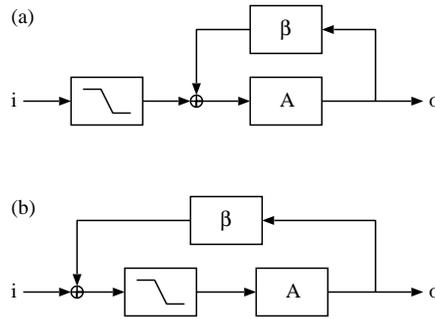


Figure 2.4: Filter placement in an amplifier; (a) at the input, (b) in the loop.

input of a circuit is effective only if no other path exists that can bypass it. If the interference signal is able to reach the input of the forward-gain section, A , or another non-linearity via an alternative route, the purpose of the filter would be defeated. The influence of the feedback network and the output must, therefore, be taken into consideration. Should the former have a relatively large physical size, as may be the case with the external feedback network of an operational amplifier, filtering the input signal would be of little use. Similarly, interference coupling into the output of a negative-feedback amplifier may propagate through the feedback network and reach the input. This can be solved by placing a filter inside the loop, for example in front of the first stage of the amplifier. If the in-band frequency response of the system is to remain unchanged, however, the additional poles, that are introduced, must be above the dominant loop poles, while they still provide sufficient attenuation at the frequency of the interference. Otherwise, the frequency compensation of the amplifier could be compromised [59], resulting in instability. This may require a prohibitively complex filter topology, that is impractical to implement. There are areas, on the

other hand, where filtering is much easier to apply. In the context of out-of-band interference immunity, one such case is the elimination of disturbance injection through the biasing circuitry. There, none of the above-mentioned objections are applicable, which implies a lot less demanding filter implementation.

2.2 Distortion cancellation

Another strategy to deal with out-of-band interference in a circuit is to reduce the non-linearities that are responsible for causing it. Due to the nature of the interference, this reduction has to be frequency independent or, at least, be functional at the frequency of the out-of-band signal. A possible approach is to subtract the outputs of two identical non-linear devices that are driven by identical anti-phase signals, thereby canceling some of their distortion components. This principle is employed in various symmetrical configurations, such as the differential stage. Of course, not all distortion components can be accounted for in this way, due to the periodic nature of the sign of a negative input quantity in the Taylor decomposition of a non-linear function. Conversely, the outputs of two identical and identically driven non-linear devices could be subtracted. This will lead to compensation of all distortion components. Unfortunately, the desired signal transfer, i.e., the linear term of the Taylor polynomial, will then also be zero, so separation of the useful signal from the interference is necessary.

2.2.1 The differential stage

A method to deal with out-of-band interference in a circuit is to subtract the outputs of two identical non-linear devices that are driven by identical anti-phase signals, thereby canceling some of their distortion components. This principle is employed in various symmetrical configurations, such as the differential stage. Not all distortion components can be eliminated in this way due to the periodic nature of the sign of a negative input quantity in the Taylor decomposition of a non-linear function (1.2). The differential pair is commonly used in amplifier design due to the fact that it can be configured as both an inverting and a non-inverting stage. It is well suited for use in designs with enhanced immunity to out-of-band interference because of its inherently odd transfer function and its suppression of various common-mode phenomena. The principal schematic of its BJT variant can be seen in Figure 2.5. In order to derive the large-signal transfer function of the differential stage in the figure, the following relationships are considered:

$$V_{in} = V_{BE1} - V_{BE2}, \quad (2.1)$$

$$\begin{aligned} I_{out} &= I_{C1} - I_{bias} \\ &= I_{bias} - I_{C2}, \end{aligned} \quad (2.2)$$

$$I_{C1} + I_{C2} = 2I_{bias}. \quad (2.3)$$

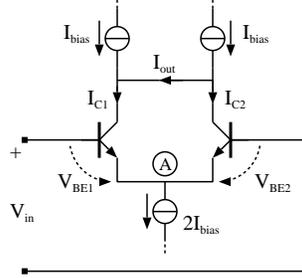


Figure 2.5: Bipolar transistor differential pair.

Substituting the general BJT transfer function (3.8) into (2.3) and (2.2) and rearranging the result yields the well-known expression for the input-output relationship of the circuit [61]:

$$I_{out} = (I_{bias} + I_S) \tanh\left(\frac{V_{in}}{2V_t}\right). \quad (2.4)$$

The large-signal transfer function (2.4) is analysed in the context of out-of-band interference. As already discussed in Chapter 1, the non-linear behaviour of circuit components is solely responsible for the problems associated with interfering signals outside the information band. The transfer function of the differential stage is non-linear and will, therefore, result in out-of-band interference. Since, however, (2.4) is an odd-symmetry function, comprising exclusively odd intermodulation products, out-of-band interference may only occur for disturbances with frequencies below the information band in case of a bandpass system. For the purpose of this study, interfering signals at frequencies (far) above the information band are considered. As no frequency folding takes place in the transfer of a differential stage, the latter, therefore, provides a principal solution to the out-of-band interference problem.

Due to variation of certain circuit parameters, the behaviour of the differential stage deviates from that described by (2.4). The equation suggests that one possible signal-dependent parameter, other than the input voltage, V_{in} , is the bias current, I_{bias} [62]-[63]. The influence of the latter on the transfer function is analysed. Consider the multivariate Taylor polynomial expansion:

$$\begin{aligned} f(x, y)|_{x_0, y_0} = & f(x_0, y_0) + x \frac{\delta}{\delta x} f(x_0, y_0) + y \frac{\delta}{\delta y} f(x_0, y_0) \\ & + \frac{1}{2!} \left[x^2 \frac{\delta^2}{\delta x^2} f(x_0, y_0) + 2xy \frac{\delta^2}{\delta x \delta y} f(x_0, y_0) + y^2 \frac{\delta^2}{\delta y^2} f(x_0, y_0) \right] \\ & + \dots \end{aligned} \quad (2.5)$$

Converting the expression of (2.4) to this form yields:

$$\begin{aligned}
I_{out}(V_{in}, I_{bias})|_{V_{IN}, I_{BIAS}} &= (I_{BIAS} + I_S) \tanh \frac{V_{IN}}{2V_t} \\
&+ \frac{V_{in}}{2V_t} (I_{BIAS} + I_S) \left(1 - \tanh^2 \frac{V_{IN}}{2V_t}\right) \\
&+ I_{bias} I_{BIAS} \tanh \frac{V_{IN}}{2V_t} \\
&+ \frac{V_{in}^2}{4V_t^2} (I_{BIAS} + I_S) \left(1 - \tanh^2 \frac{V_{IN}}{2V_t}\right) \tanh \frac{V_{IN}}{2V_t} \\
&+ \frac{V_{in} I_{bias}}{V_t} \left(1 - \tanh^2 \frac{V_{IN}}{2V_t}\right) \\
&+ I_{bias}^2 \cdot 0 + \dots
\end{aligned} \tag{2.6}$$

Around $V_{IN} = 0$ (2.6) evaluates to:

$$I_{out}(V_{in}, I_{bias})|_{0, I_{BIAS}} = \frac{V_{in}}{2V_t} (I_{BIAS} + I_S) + \frac{V_{in} I_{bias}}{V_t} + \dots \tag{2.7}$$

Figure 2.6 depicts a simplified small-signal equivalent circuit of a differential stage. The input signal is represented as the sum of its common-mode (v_{cm}) and differential-mode (v_{dm}) components. The tail current bias source, denoted as $2I_{bias}$ in Figure 2.5, has a finite source impedance, which is modelled by Z_t .

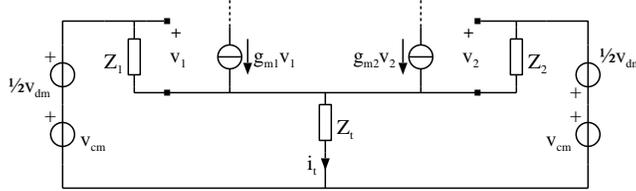


Figure 2.6: Small-signal equivalent circuit of a differential stage with non-ideal tail current source.

Due to variations of the input voltage, a leakage current will flow through the non-ideal bias source [25, 26]. This is represented by i_t in the figure and for $g_{m1} = g_{m2} = g_m$ is given by the following expression:

$$i_t = g_m \frac{\frac{2}{Z_t} v_{cm} + v_{dm} \left(\frac{1}{Z_2} - \frac{1}{Z_1}\right)}{2g_m + \frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_t}}. \tag{2.8}$$

For a symmetrical BJT differential pair, $Z_1 = Z_2 = Z_\pi$, with $Z_\pi = \frac{r_\pi}{1 + s r_\pi C_\pi}$. The bias source impedance is represented by a capacitor, C_t , since its capacitive component will most likely be dominant at the frequencies of the interference. In the frequency domain, (2.8) evaluates to:

$$i_t(j\omega) = \frac{j\omega C_t g_m r_\pi v_{cm}(j\omega)}{1 + j\omega r_\pi (C_\pi + \frac{C_t}{2}) + g_m r_\pi} \approx \frac{j\omega C_t g_m v_{cm}(j\omega)}{j\omega (C_\pi + \frac{C_t}{2}) + g_m}. \tag{2.9}$$

Taking the inverse Fourier transform of the above yields:

$$i_t(t) = \mathcal{F}^{-1}[i_t(j\omega)] = |i_t(j\omega)| \cos(\omega t + \angle i_t(j\omega)). \tag{2.10}$$

Equation (2.9) demonstrates that the effective bias current of the differential pair is dependent on the common-mode component of the input signal. Variations in the bias point will, in turn, affect the transfer function of the stage. In order to determine the effect on the output current, (2.9) is combined with the result obtained in (2.7):

$$i_{out}(t) = \frac{g_m v_{in}(t)}{2} + \frac{v_{in}(t) i_t(t)}{2V_t} + \dots \quad (2.11)$$

For small values of the input voltage, the high order terms of the polynomial become insignificant. Using (2.10):

$$i_{out}(t) \approx \frac{g_m v_{dm}(t)}{2} + \frac{v_{dm}(t) |i_t(j\omega)| \cos(\omega t + \angle i_t(j\omega))}{2V_t}, \quad (2.12)$$

with $v_{in}(t) = v_{dm}(t) = \hat{v}_{dm} \cos(\omega t)$. Further expanding (2.12) yields:

$$i_{out}(t) \approx \frac{g_m v_{dm}(t)}{2} + \frac{\hat{v}_{dm} \cos(\omega t) |i_t(j\omega)| \cos(\omega t + \angle i_t(j\omega))}{2V_t}. \quad (2.13)$$

Through decomposition of the expression above, the frequency-dependent offset of the output current is obtained. This is denoted by $I_{out,off}$ and can be found to be:

$$i_{out,off}(t) = \frac{\hat{v}_{dm} |i_t(j\omega)| \cos(\angle i_t(j\omega))}{4V_t}. \quad (2.14)$$

Combining (2.14) and (2.10), and taking $v_{cm}(t) = \hat{v}_{cm} \cos(\omega t + \varphi_{cm})$, results in:

$$i_{out,off}(t) = \frac{\hat{v}_{dm} \hat{v}_{cm} \left| \frac{j\omega C_t g_m}{j\omega(C_\pi + \frac{C_t}{2}) + g_m} \right| \cos \left\{ \varphi_{cm} + \angle \left[\frac{j\omega C_t g_m}{j\omega(C_\pi + \frac{C_t}{2}) + g_m} \right] \right\}}{4V_t}. \quad (2.15)$$

The effect can be demonstrated through a simulation of a bipolar transistor differential stage. This is set-up as shown in Figure 2.7. There, the input voltage

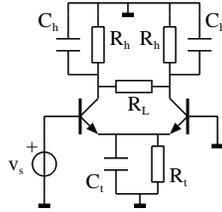


Figure 2.7: Experimental circuit of a BJT differential stage.

source, v_s , is composed of two discrete frequency components. Their frequencies are chosen such that they differ by 1%. Note that although the circuit is driven completely unilaterally, both a common-mode and differential-mode component

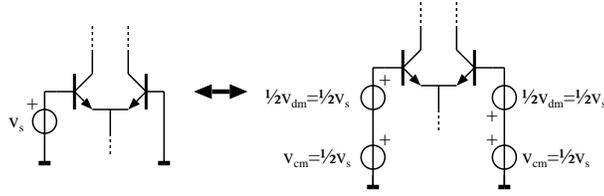


Figure 2.8: Common and differential-mode components of single-ended drive.

are present at the base of each transistor. This corresponds to the situation treated analytically and is depicted in Figure 2.8. Both transistors are biased with ideal sources, which are omitted from the figure for clarity. The values of C_h and R_h model the output impedance of the upper bias current sources. As the tail current is double the collector current of each of the differential stage transistors, $C_t = 2C_h$ and $R_t = \frac{R_h}{2}$. A complementary bipolar process is used in order to be able to investigate different types of devices. The circuit of Figure 2.7 is implemented with either PNP or NPN transistors and simulated. The current through the output resistor, R_L , is measured and the magnitude of its DC offset (or the second-order intermodulation product) is plotted against that predicted by (2.15). The results for the two complementary configurations are shown in Figure 2.9. From the data, it can be observed that there is a good

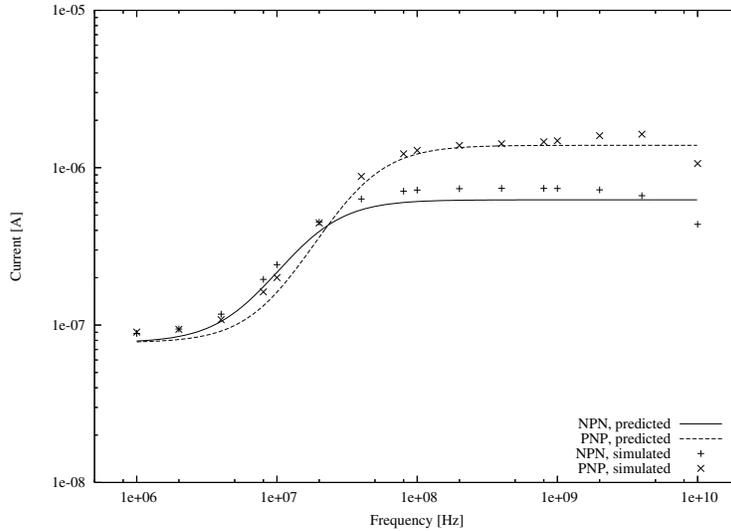


Figure 2.9: Predicted and simulated offset current for PNP and NPN differential stages.

correspondence between the theoretical estimate and the simulated circuits. It

may, therefore, be inferred that (2.15) accounts for the dominant mechanism of even order distortion in a differential stage.

The composition of (2.15) is furthermore analysed. Several conclusions may be drawn after evaluating its various constituent parameters. The contribution to the output signal of variation in the effective bias current is dependent on the size of the tail current source parasitic capacitance, C_t . Furthermore, both a common-mode *and* a differential-mode signal must be present at the input in order for the output to be affected. Therefore, for example, a fully symmetrically driven differential stage would be immune to the effect discussed here.

2.2.2 The symmetrically driven stage

As seen in the previous section, a symmetrically driven differential stage would be immune to the intermodulation phenomena brought about by out-of-band interference. While simple to describe theoretically, a purely differential-mode signal may be difficult to provide (or sustain) in practice. Many transducers yield single-ended signals and the same applies to various signal sources and signal processing circuitry. Of course, it is possible to build circuits symmetrically [64]-[66], but then the possibility always remains that a common-mode component appears due to interference. Nevertheless, methods do exist to generate a purely differential-mode signal from a single-ended source while remaining relatively unaffected by frequencies beyond the information band. One such alternative is to use a transformer at the input of the amplification chain. A possible implementation of this method is shown in Figure 2.10. Employ-

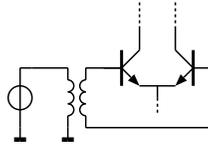


Figure 2.10: Transformer-decoupled differential stage.

ing a transformer decouples the (single-ended) source and effectively eliminates common-mode signals at the input of the differential stage. Transformers, however, are often bulky or expensive to use and, at the best of times, difficult to integrate. At the time of writing of this work, the useful frequency range of an integrated transformer is from approximately hundred megahertz to several tens of gigahertz [67, 68]. This means that a fully integrated solution is only possible if the information band falls within this range. The latter implies that the frequency of the interfering signal is at least an order of magnitude higher, which is currently encountered in a relatively few cases. Certainly, as the operating frequencies of electronic circuits increase and integration techniques advance, this method may become feasible on a larger scale.

To demonstrate the concept, the circuit shown in Figure 2.11 is simulated.

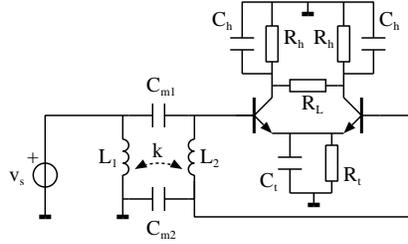


Figure 2.11: Circuit to investigate transformer decoupling.

The transformer is modelled as two coupled inductors, L_1 and L_2 , with coupling factor k . In this example $k = 1$, so that the circuit can be compared directly to an identical differential pair with single-ended drive. The mutual capacitance, C_m , of the transformer is also included. This is the distributed capacitance between the coils of L_1 and L_2 . If it is sufficiently large, it can significantly degrade the symmetry of the entire structure and is, therefore, interesting to consider in this analysis. C_m is quite prominent in integrated planar stacked inductors [69, 70]. Here, C_m is modelled somewhat pessimistically by dividing it equally between two lumped capacitances, C_{m1} and C_{m2} . Bias current source impedances are accounted for by C_h , R_h , C_t and R_t . Their values are derived from the output resistance and substrate capacitance of devices from the same process biased at the corresponding collector current. The transistors are biased with ideal sources, which are left out from Figure 2.11 for clarity. A two-tone signal is generated by v_s and the detected intermodulation signal across R_L is measured. The respective frequencies, f_α and f_β , of the two tones are related by $f_\beta = f_\alpha + f_\gamma$, where f_γ is set to 10 MHz, while f_α is swept between 100 MHz and 10 GHz. The magnitude of the current at frequency f_γ through the load resistor, R_L , is plotted in Figure 2.12 for a the transformer decoupled differential pair. The figure also includes the corresponding result from a reference circuit without decoupling, which is driven directly by a (single-ended) voltage source. To illustrate the influence of C_m , several simulations are carried out with different values of C_{m1} and C_{m2} . The loss of performance is apparent, with a value of C_m of 100 fF almost entirely nullifying the action of the decoupling transformer. In this context, it is, therefore, vital to reduce the mutual capacitance, which could be achieved by using a magnetic flux guide, as already suggested.

2.2.3 The double differential pair

As outlined in 2.2.1, the classical differential pair deviates from its expected transfer function due to the finite source impedance of the tail current bias source. It is possible to compensate for this non-ideal behaviour by cross connecting two differential stages, as shown in Figure 2.13. By ensuring that their intermodulation offset currents cancel each other, compensation is achieved.

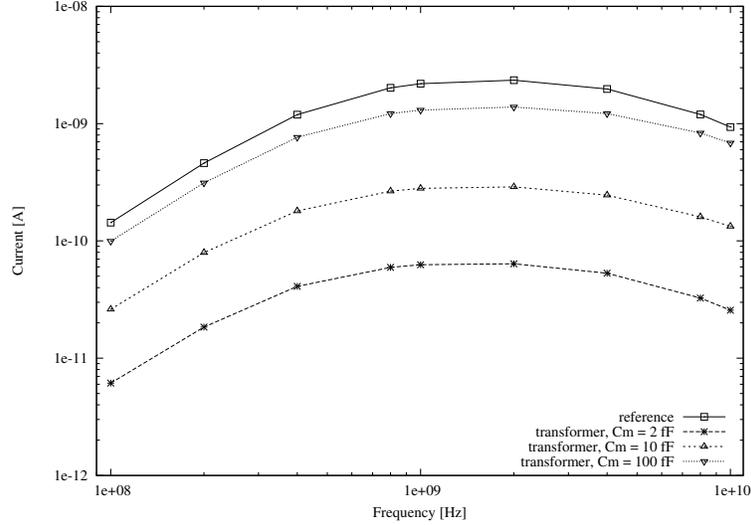


Figure 2.12: Simulated IM_2 current through the load of the transformer decoupled differential pair.

This implies that the equation

$$I_{out,off_1}(t) = I_{out,off_2}(t), \quad (2.16)$$

must be solved, where $I_{out,off_1}(t)$ represents the parasitic offset current of the first differential stage (consisting of $T_{1,1}$ and $T_{1,2}$), as given by (2.15), and $I_{out,off_2}(t)$ that of the second differential stage ($T_{2,1}$ and $T_{2,2}$). The trivial solution of (2.16) is to use two identical transistor pairs, driven at the same current and having the same bias circuits. This, of course, is not practical, because then the transfer function of the entire stage is zero for all input frequencies. A non-trivial solution is demonstrated for a MOSFET differential stage [13, 71]. There, a primary transistor pair is compensated by a smaller secondary pair. The latter is biased at a significantly lower current so as to minimise overhead. Alternatively, two cross-coupled complementary differential stages could be used [12]. The W/L ratio of the field effect transistors is used to tune their transconductance until (2.16) is solved. As the g_m of bipolar transistors is primarily dependent on the collector current, there are fewer degrees of freedom to modify it without affecting other relevant transistor parameters. It seems that in order to obtain a workable solution of the equation, the primary stage of a BJT double differential pair implementation needs to be degraded (i.e. by artificially increasing C_π or C_t). This has consequences for the regular function of the circuit and is, thus, undesirable. Since the input stage of a negative-feedback amplifier typically does not dominate the power dissipation of the entire circuit, it is possible to bias the supplementary differential pair

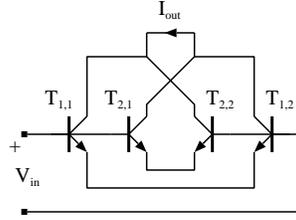


Figure 2.13: Signal circuit of double differential pair.

at a higher current than the primary without incurring a significant penalty in overall current consumption. The overall performance of the double differential stage can then be made to approximate that of the original differential pair. Of course, certain parameters, such as noise, will invariably degrade, with the latter increasing by a factor of approximately 2 (depending on noise optimisation). This could be significant in the context of structured electronic design where the first stage defines the noise behaviour of the entire amplifier.

To demonstrate the method, a BJT double differential stage is set up, as shown in Figure 2.14. There, the primary pair, $T_{1,1}$ - $T_{1,2}$, is compensated by

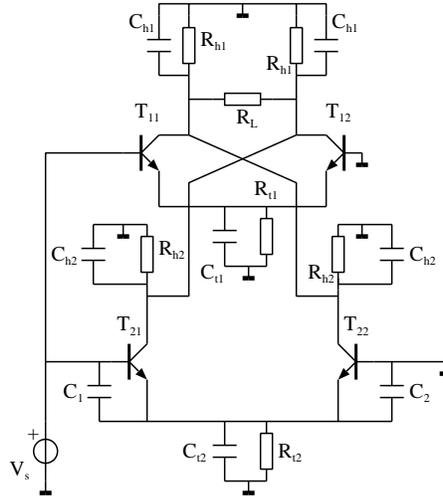


Figure 2.14: Evaluated circuit of BJT double differential pair.

the cross coupled $T_{2,1}$ - $T_{2,2}$. Note that transistors $T_{2,1}$ and $T_{2,2}$ are degraded by additional base-emitter capacitances C_1 and C_2 , in order to achieve a solution of (2.16). The supplementary differential pair is biased at twice the collector current of the primary. In this way, the transconductance of the entire circuit is approximately equal to that of the primary differential pair, but has the opposite

sign. A two-tone signal is presented at the input of the circuit and swept from 10 MHz to 10 GHz. The intermodulation product at the difference frequency is determined for the current flowing through the load resistance, R_L . The resulting data is plotted in Figure 2.15 across the frequency range evaluated.

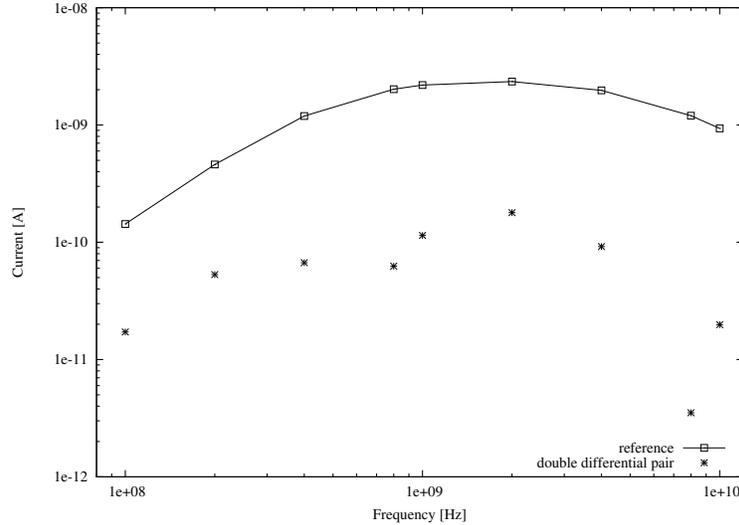


Figure 2.15: Simulated IM_2 product of the bipolar double differential pair.

The response of only the primary differential pair is also included in the figure. This is simulated separately under identical conditions and serves as reference. From the plots it can be concluded that the compensation is able to suppress the undesired intermodulation product by more than an order of magnitude.

2.2.4 The bootstrapped differential pair

This is also known as the source-buffered differential pair and is another method to improve the effective symmetry of the classical differential stage. It attempts to reduce the common-mode transfer function between the input of the differential pair and the common node of the differential pair transistors, i.e., Node A of Figure 2.5 [27]. This is equivalent to reducing \hat{v}_{cm} of (2.15) and reproduces the conditions of fully differential drive. It is achieved by driving the substrate of the differential stage transistors using a second differential stage, as shown in Figure 2.16 for a MOSFET implementation. This arrangement can significantly decrease the capacitance of Node A , which is beneficial for lowering the output offset current (2.15). Full cancellation of the common-mode transfer function can be achieved by adding extra capacitance between the inputs of the circuit and A [14, 28].

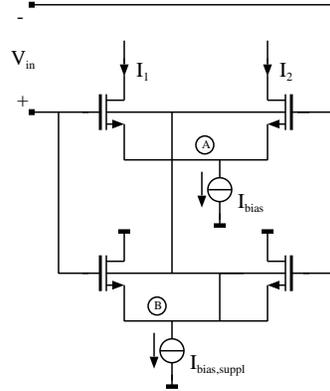


Figure 2.16: MOSFET source-buffered differential pair.

2.2.5 Error feed-forward

This distortion cancellation approach predates the discovery of negative feedback [29] and is based on subtraction of non-linear signal components from the output of the amplifier. Its principle of operation is illustrated in Figure 2.17.

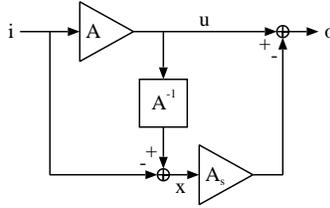


Figure 2.17: Principal implementation of error feed-forward.

An input signal, i , is processed by a main amplifier, A , resulting in a signal u . Due to the non-linear behaviour of A , u contains distortion components alongside the amplified copy of i . The output of the main amplifier is attenuated by its gain factor, and the input signal is subtracted from it. The resulting signal, x , contains only the distortion components of A . These are amplified by an auxiliary amplifier, A_s , and are subtracted from the output of the main amplifier, u . So, the output of the circuit, o , consists only of the amplified input signal and no distortion components. However, in order for perfect cancellation to occur, a number of conditions must be fulfilled. First, all signals must be in phase when they are added or subtracted. Furthermore, the addition or subtraction operations must be perfectly accurate. Finally, the auxiliary amplifier must be linear, otherwise its own distortion components will appear at o , resulting in an incomplete cancellation. Ensuring that all these conditions are met is not

easy in practice. Nevertheless, implementations have been proposed that make use of this method [30]. In the design for out-of-band interference immunity a somewhat different topology is typically used to achieve feed-forward compensation. This is based on creating symmetry by replicating a circuit and its associated non-idealities as faithfully as possible. Subsequently, both identical copies of the circuit can be exposed to out-of-band interference, but only one of them processes an in-band signal [72]. This is illustrated in Figure 2.18 and is also known as dummy circuit compensation. The regular in-band input signal,

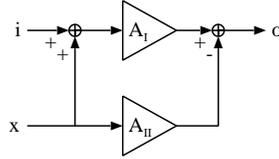


Figure 2.18: Conceptual schematic of dummy circuit compensation.

i , together with the interference signal, x , reach the input of amplifier A_I , while only x is present at the input of A_{II} . The two amplifiers are identical; A_I is the main amplifier and A_{II} is the dummy. The (in-band) distortion products due to x are present at the outputs of both amplifiers and cancel each other out in the subtraction at the output of the circuit. The in-band input signal is amplified only by A_I and appears as the sole component (together with its own distortion products) of the output signal, o . In order for this scheme to work, it must be possible to separate the information signal from the interference (normally, the two will arrive at the input of the circuit combined, i.e., $i + x$). In practice, this is achieved by suppressing the in-band portion of the combined signal using a high-pass filter at the input of the dummy amplifier [11, 73], as shown in Figure 2.19.

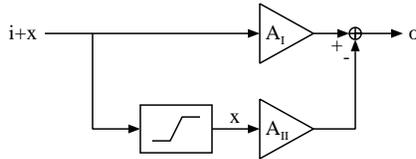


Figure 2.19: Practical implementation of dummy circuit compensation.

Chapter 3

Non-linear distortion analysis

“Anything that happens, happens.
Anything that in happening causes something
else to happen, causes something else to happen.
Anything that in happening happens again, happens again.
Though not necessarily in that order.”

Douglas Adams, *Mostly Harmless*

The non-linear behaviour of negative-feedback amplifiers is investigated in this chapter. In order to develop circuits with a low second-order intermodulation distortion, IP_2 , as defined by (1.6), the dominant sources of distortion must first be known, and the mechanisms through which they affect the information-carrying quantity identified. Steps can subsequently be taken to eliminate this mechanism or, at least, reduce its effect to an acceptable level.

Active devices, such as transistors, provide signal gain and are the fundamental building blocks of electronic amplifiers. These are non-linear by nature and are responsible for the distortion that occurs in amplifier circuits. It is, therefore, essential to account for this aspect of their behaviour in the analysis.

3.1 Non-linear small-signal transistor model

Advanced models describe the non-linearities of a transistor under a variety of operating conditions [31]-[34]. These models are sufficiently mature to deliver accurate and dependable simulation of circuits containing transistors and other semiconductor devices for the design of integrated circuits in production [35]-[37]. To achieve such accuracy and context independence, transistor models are specified using a significant number of technology-dependent parameters [38]-[40]. The complexity of current device models effectively precludes an accurate analytical treatment of even the simplest circuits. Numerical methods

are used to perform most circuit calculations. This is convenient for implementation in computer-aided design (CAD) tools, but results in a loss of insight for the designer. However, simplified transistor models that describe only the basic functionality of the devices may be used during the first stages of circuit design to approximate the circuit response. The hybrid- π , small-signal model [41], shown in Figure 3.1, is one such representation for a bipolar junction transistor (BJT). It is based on the linear approximation of a device's behaviour around its bias point, which eliminates the need to include biasing circuitry (loading due to the latter must still be considered). The transistor is modelled as a frequency-dependent controlled current source, independent from a power supply. In small-signal operation, all components of the model are linear and

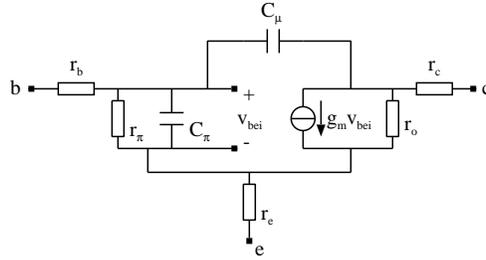
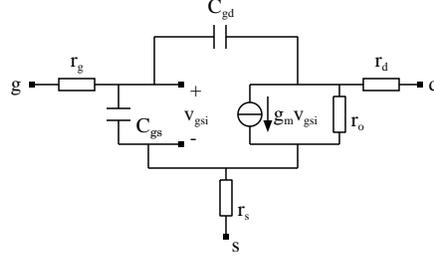


Figure 3.1: Hybrid- π model of a bipolar transistor.

time-invariant. Transconductance g_m is the main functional characteristic of the transistor. Capacitors C_π and C_μ model the charge stored in the base-emitter and base-collector junctions, respectively, and are essentially parasitics. Resistor r_π constrains the current flowing through the base-emitter junction, and r_o is the effective output resistance of the device. Resistors r_c , r_b and r_e account for the ohmic losses extrinsic to the collector, base and emitter, respectively. Often they are omitted from the equivalent circuit, as their effect is normally minor. Furthermore, they are the only elements of the small-signal model that describe a linear property of the device. All the other model parameters approximate processes that in reality are non-linear, signal-dependent, or both.

The situation is similar for the hybrid- π , small-signal model of the metal-oxide semiconductor (MOS) transistor. This is shown in Figure 3.2 and is not unlike the BJT. Again, the device transconductance is represented by g_m , with an output resistance r_o . Capacitor C_{gs} describes the storage of charge passing through the channel and C_{gd} accounts for the parasitic coupling capacitance between the gate conductor and the drain diffusion [42]. There is no (direct) current flowing through the gate, except for leakage due to tunneling through the very thin gate oxide of the latest semiconductor processes, hence r_π of the BJT equivalent is absent from the MOS model. Resistors r_d , r_g and r_s reflect the resistance of the drain, gate and source, respectively. Once more, these are usually omitted due to their secondary significance in most analyses.

Figure 3.2: Hybrid- π model of the MOS transistor.

Being linear, the hybrid- π model is unsuitable for predicting the distortion of a circuit. As outlined in the previous chapter, distortion in negative-feedback amplifiers is the focus of this study. Therefore, a model is needed that is simple enough to allow analytical investigation of non-linear effects, yet is sufficiently detailed to obtain a useful approximation. A method is proposed to address this problem, that merges the simplicity of the small-signal approach with the functionality needed for basic distortion analysis. As with the hybrid- π model, this is achieved by considering only the dominant effects and signal trends.

For both the MOS and the bipolar transistor, non-linearity of the transconductance g_m is the fundamental source of distortion. Depending on the operating point, the transconductance of a MOS transistor could be a linear or an exponential function of the gate-source voltage, V_{gs} . If V_{gs} is larger than the threshold voltage, V_{th} , the channel of the device is said to be in strong inversion. For small drain-source voltages, i.e., $V_{ds} < V_{gs} - V_{th}$, the transistor is in the conduction region, and its drain current is given by [43, 44]:

$$I_d = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} [(V_{gs} - V_{th})^2 - (V_{gd} - V_{th})^2], \quad (3.1)$$

where μ is the charge carrier mobility, C_{ox} is the capacitance per unit area of the gate oxide, and $\frac{W}{L}$ is the width to length ratio of the channel. When the drain-source voltage exceeds $V_{gs} - V_{th}$, the transistor operates in saturation, and its drain current becomes approximately:

$$I_d = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} (V_{gs} - V_{th})^2, \quad (3.2)$$

for long channel devices. The transconductance in both cases of strong inversion is:

$$g_m = \mu C_{ox} \frac{W}{L} (V_{gs} - V_{th}). \quad (3.3)$$

For gate-source voltages below the threshold voltage, V_{th} , the transistor enters the weak-inversion mode of operation. In the conduction region, its drain current is given by:

$$I_d = \frac{W}{L} I_{d0} \left(e^{\frac{V_{gs}}{nV_t}} - e^{\frac{V_{gd}}{nV_t}} \right). \quad (3.4)$$

In saturation the drain current becomes:

$$I_d = \frac{W}{L} I_{d0} e^{\frac{V_{gs}}{nV_t}}, \quad (3.5)$$

where I_{d0} and n are process-dependent constants, and V_t is the thermal voltage given by:

$$V_t = \frac{kT}{q}, \quad (3.6)$$

with k Boltzmann's constant, T the absolute temperature, and q the electron charge [45]. In the weak-inversion mode, the transconductance of the device is:

$$g_m = \frac{W}{L} \cdot \frac{I_{d0}}{nV_t} e^{\frac{V_{gs}}{nV_t}}. \quad (3.7)$$

The behaviour of a BJT is very similar to that of a MOS transistor in weak inversion saturation throughout the entire input-output signal range. In general, the collector current of a bipolar transistor is given by:

$$I_c = I_s \left(e^{\frac{V_{be}}{V_t}} - 1 \right), \quad (3.8)$$

where I_s is the saturation current. This results in the following transconductance:

$$g_m = \frac{I_s}{V_t} e^{\frac{V_{be}}{V_t}}. \quad (3.9)$$

To accommodate non-linear behaviour of g_m in a simple model, the hybrid- π small-signal equivalent circuit is taken as a foundation. Its linear transconductance is substituted by a non-linear function, \tilde{g}_m , of the form:

$$\tilde{g}_m(v) = K_0 + K_1 v + K_2 v^2 + K_3 v^3 + \dots, \quad (3.10)$$

where v is the (small-signal) controlling voltage. The coefficients $K_n \in \Re$ (where index $n \in \mathbb{N}$) are constants dependent on the transistor type and region of operation. For example, the coefficients of a MOS transistor in strong inversion saturation are:

$$\begin{aligned} K_0 &= \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \\ K_1 &= \mu C_{ox} \frac{W}{L} \\ K_2 &= K_3 = K_4 = \dots = 0, \end{aligned} \quad (3.11)$$

where V_{GS} is the gate-source bias voltage. Similarly, for a bipolar transistor, these coefficients are given by:

$$\begin{aligned} K_0 &= \frac{I_C + I_s}{V_t} \approx g_m \\ K_1 &= \frac{I_C + I_s}{11V_t^2} \approx \frac{g_m}{11V_t} \\ K_2 &= \frac{I_C + I_s}{21V_t^3} \approx \frac{g_m}{21V_t^2} \\ &\vdots \end{aligned} \quad (3.12)$$

with $g_m = \frac{I_C}{V_t}$, where I_C is the collector bias current. As far as the out-of-band frequency range is considered, i.e., frequencies above $\frac{f_t}{\beta}$, in case of a bipolar transistor, impedances in the model are expected to be dominated by the capacitive components. Therefore, resistors, such as r_π , may be neglected. For simplicity, resistive losses in series with the terminals are also left out. The resulting strongly simplified circuit model of an active device is shown in Figure 3.3. Capacitor C_1 corresponds to C_π , in case of a BJT, and C_{gs} , in case of

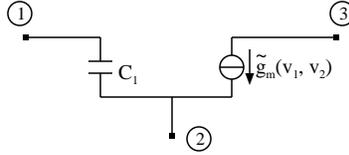


Figure 3.3: Strongly simplified non-linear transistor model for out-of-band analysis.

a MOS transistor, respectively. Note that C_1 is assumed linear, while in reality it is signal-dependent, and will exhibit some non-linearity [46]. Analysis of the relative contribution of capacitive non-linearities to the output current of a bipolar transistor [9] suggests that at high frequencies the effect of C_π is comparable to that of the (non-linear) device transconductance, \tilde{g}_m . However, due to differences in phase, the two may partially cancel each other, resulting in a lower overall non-linearity. In a MOS transistor, the gate-source capacitor, C_{gs} , exhibits a much weaker non-linearity than \tilde{g}_m throughout the frequency range. The contribution of C_{gs} to the overall non-linearity of the device is, therefore, negligible. In general, assuming C_1 linear in the proposed model appears justified, as it does not significantly underestimate the non-linear behaviour of the transistor, while the mathematical analysis is simplified considerably. Effectively, it implies that any (even order) intermodulation products due to the input non-linearities of the transistor are disregarded, as their role is expected to be insignificant compared to the non-linear transconductance.

The proposed transistor equivalent circuit is suitable for analytical investigation of distortion in simple amplifier circuits. It makes no distinction between bipolar and field-effect devices, but allows for differences in their transfer functions. To verify that the non-linear, small-signal model is sufficiently accurate, its response will be compared to simulation results based on the full device models at every step. Without loss of generality, all examples in this work are further evaluated using bipolar transistors. The respective analyses for MOS devices apply the same methods and follow the same procedures, except that the appropriate circuit coefficients must be adjusted.

3.2 Analysis of the negative-feedback amplifier

A negative-feedback amplifier consists of three main components: a forward gain section A , an inverting feedback coefficient β and a summing point at the input of the amplifier. At the summing point, the input signal is added to the output of the feedback block before appearing at the input to the gain section. This arrangement is shown in Figure 3.4. The transfer function from the input

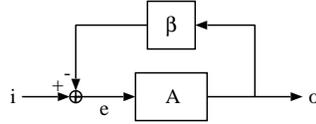


Figure 3.4: General form of a negative-feedback amplifier.

i to the output o can be derived directly from the schematic:

$$\frac{o}{i} = \frac{A}{1 - A\beta} \quad (3.13)$$

To obtain negative feedback, by convention, $\beta < 0$. However, strictly speaking, the same result could be achieved by ensuring that either A , β or the sign of the summing point (or all three) are negative. This gives the designer some freedom to choose the most convenient implementation. Normally, in electronic negative-feedback amplifier circuits, the forward gain is chosen to be negative.

The reason for applying feedback instead of specifying the amplifier gain directly with A is that the latter will typically show some implementation-specific variation. Negative feedback ensures that the influence of forward-gain variation on the overall transfer function is diminished. The only requirement for A is that it is large; the larger A is, the more accurately the transfer function is approximated by β . Taking the limit of (3.13) demonstrates this:

$$\lim_{A \rightarrow \infty} \left(\frac{o}{i} \right) = -\frac{1}{\beta}. \quad (3.14)$$

Figure 3.4 shows a generic representation of a negative-feedback configuration, where both i and o are dimensionless. The input and output signals of an amplifier are electrical quantities, such as voltage, current or charge. Complex feedback configurations also allow compound quantities, such as power or impedance [47]. An electrical implementation of a negative-feedback amplifier is shown in Figure 3.5. The input current, I_{in} , is converted into an output voltage, V_{out} , via the feedback coefficient g_{mfb} . Forward gain is provided by a nullor [17], which is a network theoretical component with infinite gain and bandwidth. The nullor also provides signal inversion. Due to the infinite forward gain, the transfer function of the amplifier is independent of the source impedance R_s and the load R_L :

$$\frac{V_{out}}{I_{in}} = -\frac{1}{g_{mfb}}. \quad (3.15)$$

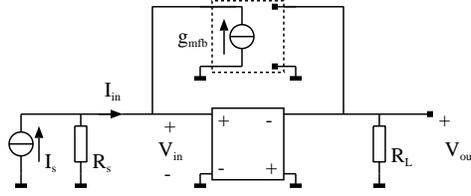


Figure 3.5: General form of a transimpedance amplifier.

The input voltage, V_{in} , is 0 V , i.e., the input is at virtual ground. There is no current flowing through R_s and $I_{in} = I_s$. The unit of the transfer function (3.15) is Ohm (Ω), hence this amplifier is known as transimpedance amplifier. Note, that the nullor may be non-linear. As long as its gain and bandwidth are infinite, the transfer function will be determined solely by g_{mfb} .

In practice, the functionality of a nullor can only be approximated by cascading a number of transistor stages to obtain the highest possible gain. This is shown in Figure 3.6 for a two-stage amplifier. The transistors are assumed

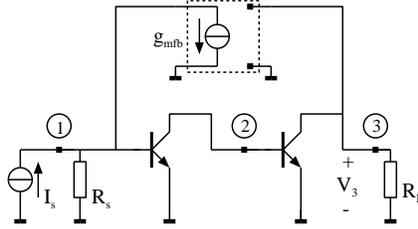


Figure 3.6: Two-stage transistor implementation of a transimpedance amplifier.

ideally biased, so that no offset currents or voltages appear at their terminals. Bias sources are not shown in the circuit. There is no net inversion in the forward gain, so the polarity of the feedback transconductor, g_{mfb} , is reversed to preserve negative feedback. The transfer function, $\frac{V_3}{I_s}$, of the circuit is ideally given by (3.15) but an error term is introduced due to the finite forward gain, as suggested by (3.13). Non-linear behaviour of the transistors will also affect the signal transfer. To ascertain the combined impact of finite gain and non-linearities on the transfer function of the amplifier, the Volterra-series approach is used. The Volterra series is a mathematical tool for analysis of non-linear systems using linear algebra [48]. It is a recursive method that obtains a better estimate of the state of the system every consecutive time it is applied. At each iteration, a Volterra kernel \mathbf{H} and a non-linear source vector \mathbf{IN} of the respective order are calculated. \mathbf{H} is a vector that, for the case of an electrical circuit, contains all of the node voltages. \mathbf{IN} reflects the non-linear currents in

the circuit. The general form of the Volterra kernel equation is given by:

$$\mathbf{Y} \left(\sum_{k=1}^n s_k \right) \times \mathbf{H}(s_1, s_2, \dots, s_n) = \mathbf{IN}_n, \quad (3.16)$$

where n is the kernel order and \mathbf{Y} is the admittance matrix of the circuit. Depending on the order, n , each Volterra kernel is a function of several discrete frequencies, s_1, s_2, \dots, s_n , and the admittance matrix is a function of the sum of these frequencies, i.e., $s_1 + s_2 + \dots + s_n$. To obtain \mathbf{H} , the inverse of \mathbf{Y} is calculated, so that (3.16) can be rewritten as:

$$\mathbf{H}(s_1, s_2, \dots, s_n) = \mathbf{Y}^{-1} \left(\sum_{k=1}^n s_k \right) \times \mathbf{IN}_n. \quad (3.17)$$

The non-linear current source vector \mathbf{IN}_n comprises the non-linear current sources of the respective order, summed per circuit node:

$$\mathbf{IN}_n = \begin{bmatrix} i_{NL1} \\ i_{NL2} \\ \vdots \\ i_{NLm} \end{bmatrix}. \quad (3.18)$$

To analyse the amplifier of Figure 3.6, the transistors present in its circuit are first substituted by their non-linear small-signal equivalent circuits. The model proposed in Section 3.1 (see Figure 3.3) is used. This results in the circuit shown in Figure 3.7. The device transconductances \tilde{g}_{m1} and \tilde{g}_{m2} are non-linear

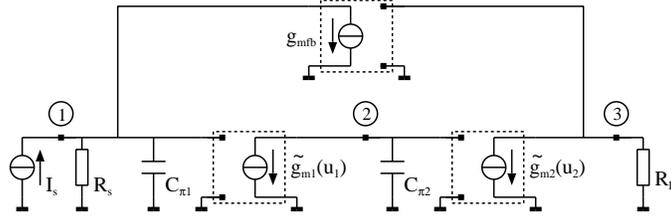


Figure 3.7: Small-signal non-linear model of the transimpedance amplifier of Figure 3.6.

functions according to (3.10):

$$\tilde{g}_{mx}(v) = g_{mx} + \frac{g_{mx}v}{V_t} + \frac{g_{mx}v^2}{2!V_t^2} + \frac{g_{mx}v^3}{3!V_t^3} \dots, \quad x \in [1, 2]. \quad (3.19)$$

The non-linear output current of each transistor can be found by integrating (3.19) with respect to the controlling voltage:

$$\begin{aligned} \tilde{I}_{gmx}(v) &= \int \tilde{g}_{mx}(v) dv \\ &= g_{mx}v + \frac{g_{mx}v^2}{2!V_t} + \frac{g_{mx}v^3}{3!V_t^2} + \dots, \quad x \in [1, 2]. \end{aligned} \quad (3.20)$$

Combining the coefficients on the right-hand side yields:

$$\tilde{I}_{gm_x}(v) = K_{1gm_x}v + K_{2gm_x}v^2 + K_{3gm_x}v^3 + \dots, \quad x \in [1, 2], \quad (3.21)$$

with:

$$\begin{aligned} K_{1gm_x} &= g_{mx} \\ K_{2gm_x} &= \frac{g_{mx}}{2V_t} \\ K_{3gm_x} &= \frac{g_{mx}}{6V_t^2}, \quad x \in [1, 2]. \end{aligned} \quad (3.22)$$

$$\vdots$$

These coefficients are used to define the non-linear current source vector \mathbf{IN}_n for the higher order terms of the Volterra series, i.e., $n \geq 2$. The admittance matrix of the circuit is subsequently compiled. The resulting matrix is given by:

$$\mathbf{Y}(s) = \begin{bmatrix} g_s + sC_{\pi 1} & 0 & g_{mfb} \\ g_{m1} & sC_{\pi 2} & 0 \\ 0 & g_{m2} & g_L \end{bmatrix}. \quad (3.23)$$

The normalised input linear current source vector \mathbf{IN}_1 is:

$$\mathbf{IN}_1 = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}. \quad (3.24)$$

The linear Volterra kernels $\mathbf{H}(s_1)$ of the amplifier can now be calculated from (3.17) with $n = 1$. The following equation is solved:

$$\mathbf{H}(s_1) = \mathbf{Y}^{-1}(s_1)\mathbf{IN}_1, \quad (3.25)$$

with

$$\mathbf{H}(s_1) = \begin{bmatrix} H_{1,1}(s_1) \\ H_{1,2}(s_1) \\ H_{1,3}(s_1) \end{bmatrix}. \quad (3.26)$$

This yields the linear transfers from the input current source I_s to the node voltages:

$$H_{1,1}(s_1) = \frac{s_1 C_{\pi 2} g_L}{s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}}, \quad (3.27)$$

$$H_{1,2}(s_1) = -\frac{g_{m1} g_L}{s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}}, \quad (3.28)$$

$$H_{1,3}(s_1) = \frac{g_{m1} g_{m2}}{s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}}. \quad (3.29)$$

Note, that (3.29) is the transfer $\frac{V_3}{I_s}$, i.e., the linear transimpedance of the amplifier from Node 1 to Node 3. This is plotted in Figure 3.8 against the result from a full-model simulation of the original transistor circuit of Figure 3.6. It can be concluded from the plots that the bandwidth of the amplifier is approximately

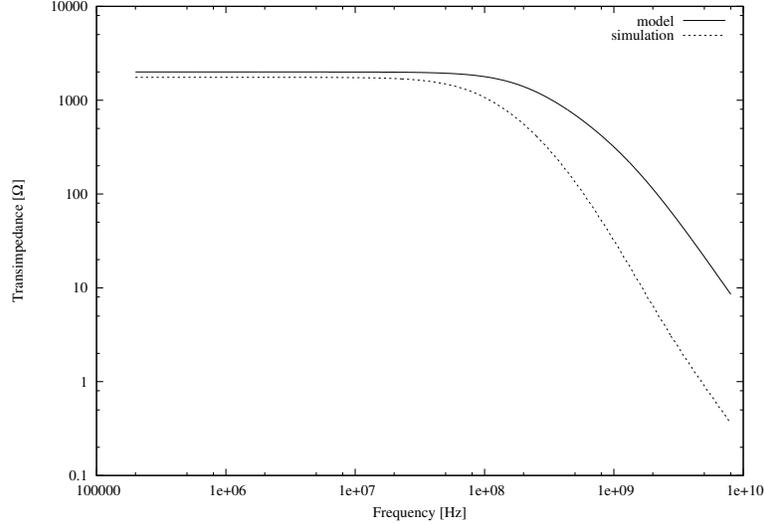


Figure 3.8: Linear transfer function of the amplifier.

100 MHz, and that there is a reasonably good match between the full transistor model and the proposed simplified, non-linear transistor model. Of course, the latter gives a more optimistic result, which is somewhat expected, considering the small number of device parasitics included in the simplified analysis.

To obtain a first estimate of the second-order intermodulation products of the amplifier, the next element of the Volterra series is calculated. The second-order admittance matrix is derived from (3.23):

$$\mathbf{Y}(s_1 + s_2) = \begin{bmatrix} g_s + (s_1 + s_2)C_{\pi 1} & 0 & g_{mfb} \\ g_{m1} & (s_1 + s_2)C_{\pi 2} & 0 \\ 0 & g_{m2} & g_L \end{bmatrix}, \quad (3.30)$$

and the non-linear current source vector is given by:

$$\mathbf{IN}_2 = \begin{bmatrix} 0 \\ -i_{NLgm1} \\ -i_{NLgm2} \end{bmatrix}. \quad (3.31)$$

The non-linear currents i_{NLgm1} and i_{NLgm2} are calculated from the coefficients obtained in (3.22), and the linear Volterra kernels (3.27)-(3.29):

$$i_{NLgm1} = K_{2gm1}H_{1,1}(s_1)H_{1,1}(s_2), \quad (3.32)$$

$$i_{NLgm2} = K_{2gm2}H_{1,2}(s_1)H_{1,2}(s_2). \quad (3.33)$$

To determine the second-order Volterra kernels $\mathbf{H}(s_1, s_2)$ of the circuit, (3.17) must be solved for $n = 2$:

$$\mathbf{H}(s_1, s_2) = \mathbf{Y}^{-1}(s_1 + s_2)\mathbf{IN}_2, \quad (3.34)$$

with

$$\mathbf{H}(s_1, s_2) = \begin{bmatrix} H_{2,1}(s_1, s_2) \\ H_{2,2}(s_1, s_2) \\ H_{2,3}(s_1, s_2) \end{bmatrix}. \quad (3.35)$$

This results in the following expressions for the second-order kernels:

$$H_{2,1}(s_1, s_2) = \frac{g_{m1}g_{m2}g_{mfb}g_L^2 C_{\pi 2} [(s_1+s_2)g_{m1}-s_1s_2C_{\pi 2}]}{2V_t (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1}g_{m2}g_{mfb})} \cdot \frac{1}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1}g_{m2}g_{mfb})} \cdot \frac{1}{[(s_1+s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1+s_2) C_{\pi 2} g_s g_L + g_{m1}g_{m2}g_{mfb}]} \quad (3.36)$$

$$H_{2,2}(s_1, s_2) = -\frac{g_{m1}g_L^2 [(s_1^2 s_2 + s_1 s_2^2) C_{\pi 1} C_{\pi 2}^2 g_L + s_1 s_2 C_{\pi 2}^2 g_s g_L + g_{m1}^2 g_{m2} g_{mfb}]}{2V_t (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1}g_{m2}g_{mfb})} \cdot \frac{1}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1}g_{m2}g_{mfb})} \cdot \frac{1}{[(s_1+s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1+s_2) C_{\pi 2} g_s g_L + g_{m1}g_{m2}g_{mfb}]} \quad (3.37)$$

$$H_{2,3}(s_1, s_2) = -\frac{g_{m1}g_{m2}g_L^2 C_{\pi 2} [(s_1+s_2)C_{\pi 2}+g_s] [(s_1+s_2)g_{m1}-s_1s_2C_{\pi 2}]}{2V_t (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1}g_{m2}g_{mfb})} \cdot \frac{1}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1}g_{m2}g_{mfb})} \cdot \frac{1}{[(s_1+s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1+s_2) C_{\pi 2} g_s g_L + g_{m1}g_{m2}g_{mfb}]} \quad (3.38)$$

From these the second-order intermodulation product IM_2 can be obtained. At the output of the circuit, the latter can be calculated from (3.38) using:

$$IM_2 = \hat{a}_1 \hat{a}_2 |H_{2,3}(s_1, s_2)|, \quad (3.39)$$

where \hat{a}_1 and \hat{a}_2 are the amplitudes of the signals of angular frequencies ω_1 and ω_2 applied at the input. Once more, the result predicted by the small-signal non-linear model is compared to a simulation of the transistor circuit of Figure 3.6. A two-tone input signal is applied in each case, of tone frequencies ω_1 and ω_2 , such that:

$$\omega_1 - \omega_2 = \Delta\omega. \quad (3.40)$$

The magnitude of the resulting intermodulation product at frequency $\Delta\omega$ is shown in Figure 3.9 for a sweep of ω_1 with $\Delta\omega = 100$ MHz. The difference frequency is chosen at the high end of the amplifier band in order to shorten the (transient) simulations of the circuit. The plots show relatively good agreement between the proposed equivalent circuit and the full transistor model for frequencies beyond the cutoff frequency of the amplifier. There is some mismatch between the results from the simulation and the proposed simplified non-linear transistor model, which is attributed to the simplicity of the latter. To determine the impact of neglecting certain device parasitics in the model, these are added to it and the circuit is re-evaluated. This is performed in the following sections.

3.2.1 Influence of C_μ

The Miller capacitance, C_μ , was excluded from the non-linear small-signal device model to simplify the mathematical analysis. An additional round of calculations is carried out to ascertain the impact of this omission and determine when

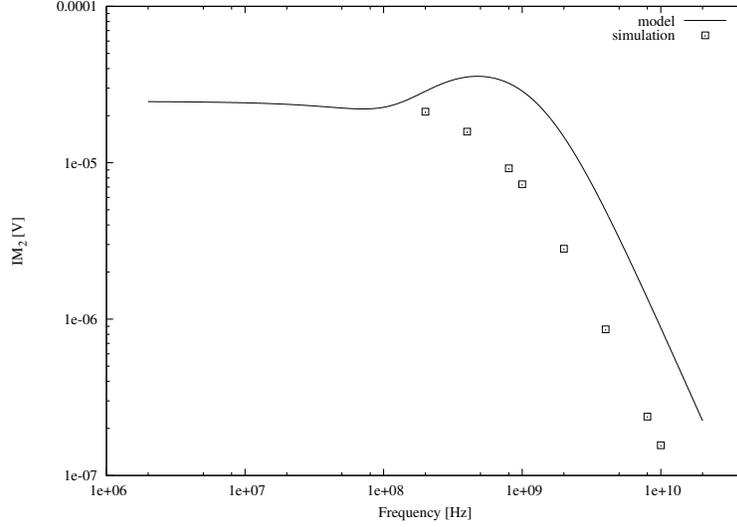


Figure 3.9: Second order intermodulation product of the amplifier.

it is acceptable. The simplified transistor model is expanded to reflect the Miller capacitance [23], as shown in Figure 3.10. The capacitor C_2 corresponds to C_μ

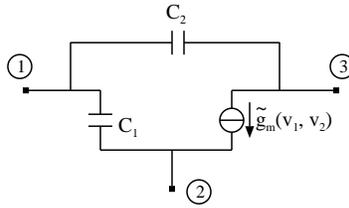


Figure 3.10: Simplified non-linear transistor model including Miller capacitance.

or C_{gd} , in case of a BJT or a MOS transistor, respectively. The equivalent circuit of the transimpedance amplifier of Figure 3.7 is likewise augmented. This is shown in Figure 3.11. Consider the admittance matrix of the circuit given by (3.23). Including the Miller capacitors in the node equations of the amplifier modifies the matrix coefficients as follows:

$$\mathbf{Y}(s) = \begin{bmatrix} g_s + sC_{\pi 1} + sC_{\mu 1} & -sC_{\mu 1} & g_{mfb} \\ g_{m1} - sC_{\mu 1} & sC_{\pi 2} + sC_{\mu 1} + sC_{\mu 2} & -sC_{\mu 2} \\ 0 & g_{m2} - sC_{\mu 2} & g_L + sC_{\mu 2} \end{bmatrix}. \quad (3.41)$$

Equation (3.25) is solved with (3.41) to determine the linear Volterra kernels, $\mathbf{H}(s_1)$. Even at this early stage, the resulting expressions are so cumbersome

that a symbolic solver [50] is needed to evaluate them. For this reason, they will not be given here. As it is difficult to gain insight into the impact of including the Miller capacitance by analysing these expressions, their graphical representation is considered instead. The linear input-output relationship, $H_{1,3}(s_1)$, is plotted in Figure 3.12. The result obtained from (3.29), as well as the full transistor simulation of the amplifier are plotted in the figure. It can be concluded from the curves that accounting for C_μ gives a somewhat better estimate of transfer function around the cut-off frequency, but the effect diminishes at higher frequencies. The second-order Volterra kernels are subsequently obtained from (3.34). The complexity of the expressions increases exponentially, so, once more, it is not practical to list them. To evaluate the influence of $C_{\mu 1}$ and $C_{\mu 2}$ on the second-order Volterra kernels, the intermodulation product is calculated. A two-tone signal is applied at the input of the circuit and the output IM_2 is evaluated at the difference frequency, $\Delta\omega$, i.e., 100 MHz. This is compared to the response of the circuit based on the simplified non-linear small-signal model, as well as the full transistor model simulation. The results can be seen in Figure 3.13 for a sweep of the tone frequencies, while $\Delta\omega$ is kept constant. From the plots it can be observed that there is a better agreement between the reference transistor simulation and the proposed small-signal model when the Miller capacitor is included. In the out-of-band region there is an approximately constant offset between the results from the two model variants, so both follow the same trend. It may be concluded that disregarding C_μ in the analysis leads to an acceptably accurate approximation. However, should all error currents need to be considered, such as when a cancellation scheme is investigated, this may no longer be the case. So, while convenient for simplicity, neglecting the Miller capacitor in the non-linear small-signal model is not always possible and should be considered with care.

3.2.2 Influence of C_{out}

Another parasitic that has so far been disregarded in the simplified non-linear transistor model is the output capacitance, C_{out} . This corresponds to the substrate capacitance of a bipolar transistor or the drain-bulk capacitor of a MOS-

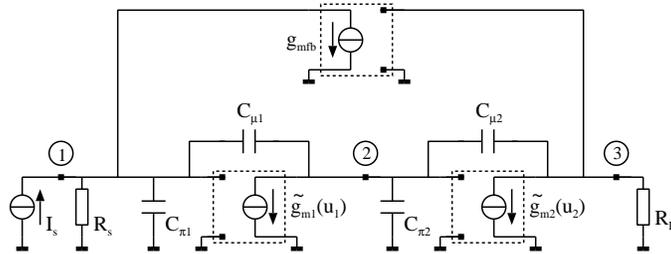
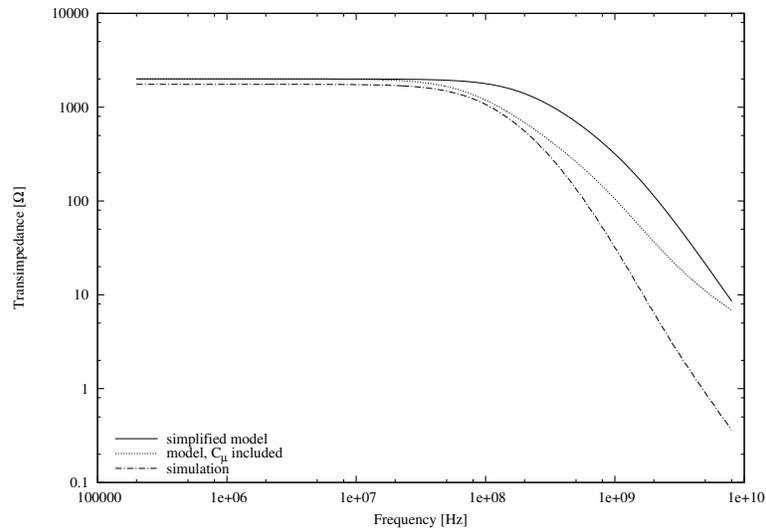
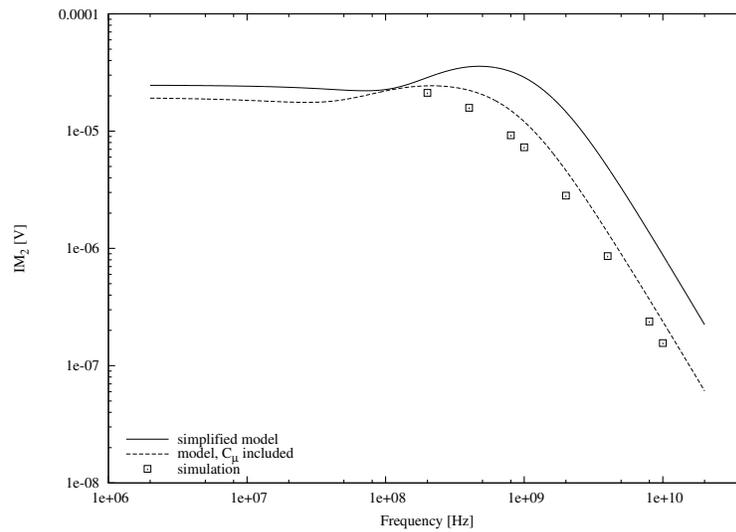


Figure 3.11: Simplified model of the transimpedance amplifier including C_μ .

Figure 3.12: Linear transfer of the amplifier when considering C_{μ} .Figure 3.13: IM_2 product of the amplifier when considering C_{μ} .

FET. To account for its influence, this is included in the circuit of Figure 3.10. The resulting transistor model is shown in Figure 3.14. This is substituted in the amplifier example of Figure 3.6 to yield the circuit shown in Figure 3.15.

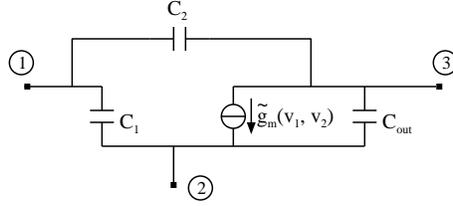


Figure 3.14: Simplified non-linear transistor model including output capacitance.

The admittance matrix of the system is now given by:

$$\mathbf{Y}(s) = \begin{bmatrix} g_s + sC_{\pi 1} + sC_{\mu 1} & -sC_{\mu 1} & g_{mfb} \\ g_{m1} - sC_{\mu 1} & s(C_{\pi 2} + C_{out1}) + sC_{\mu 1} + sC_{\mu 2} & -sC_{\mu 2} \\ 0 & g_{m2} - sC_{\mu 2} & g_L + sC_{\mu 2} + C_{out2} \end{bmatrix}. \quad (3.42)$$

This is used to calculate the linear Volterra kernels, $\mathbf{H}(s_1)$, with (3.25). The transfer function of the amplifier, $H_{1,3}(s_1)$, is plotted in Figure 3.16, together with the corresponding result obtained without additional parasitics and the full transistor model simulation. The plots reveal that after adding the output capacitance to the simplified model, its prediction becomes very close to that of the simulation throughout the frequency range. The second-order intermodulation product of a two-tone input signal is subsequently calculated from $\mathbf{H}(s_1, s_2)$ using (3.34). This is plotted in Figure 3.17 for a sweep of the tone frequencies, where $\Delta\omega = 100$ MHz. The curves suggest that considering C_{out} results in a marginal improvement of the accuracy of the prediction around the cut-off frequency of the amplifier. In this case, it may be concluded that leaving the output capacitance out of the simplified non-linear transistor model will have a minor impact on the final result. However, there are situations, in which C_{out} can play a more prominent role, as demonstrated in the following section. Disregarding the output capacitance in the simplified model should, therefore, be performed judiciously, after due consideration of its location in the circuit

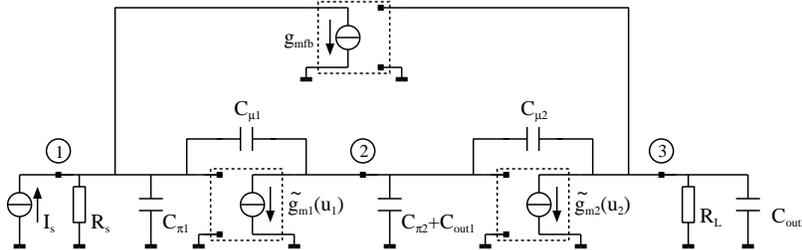


Figure 3.15: Simplified model of the transimpedance amplifier including C_{out} .

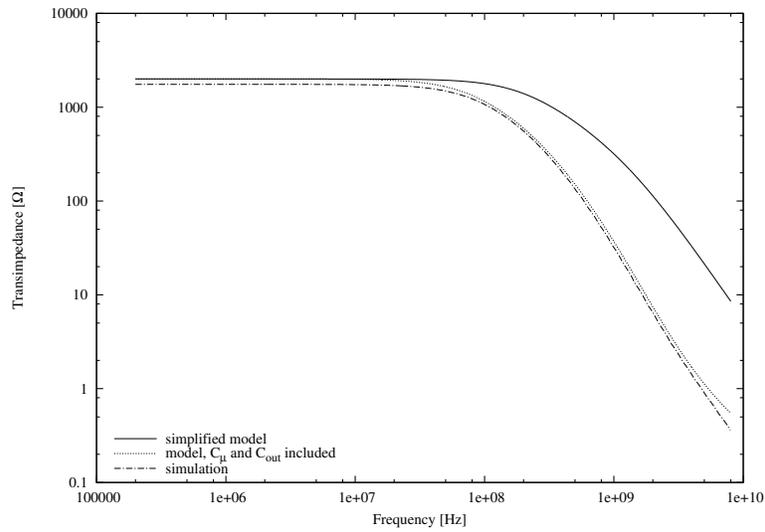


Figure 3.16: Linear transfer of the amplifier when considering C_{out} .

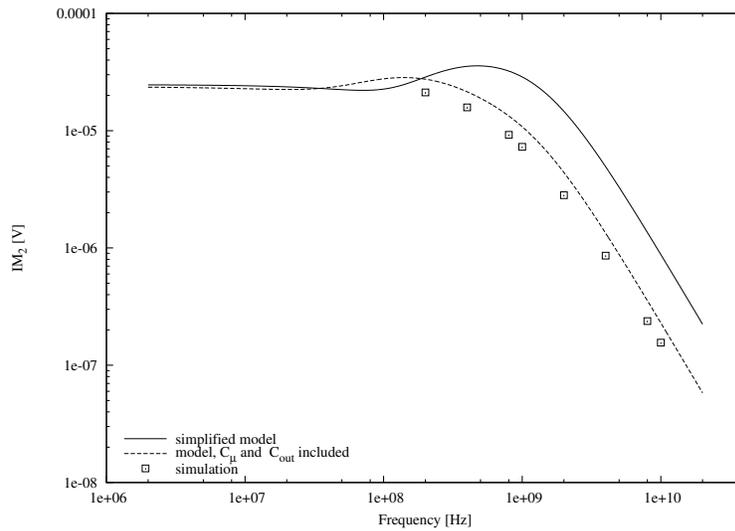


Figure 3.17: IM_2 product of the amplifier when considering C_{out} .

and the desired prediction accuracy.

3.2.3 Node susceptibility analysis

As outlined in Chapter 1 of this thesis, the second-order intermodulation product, in conjunction with the gain of the amplifier, is a measure for the susceptibility of the circuit to out-of-band interference. This measure is given by the second-order intercept point, IP_2 . For the amplifier example treated in this chapter (see Figure 3.7), the second-order intercept point can be calculated from (1.6) and (3.39):

$$IP_2 = \left| \frac{H_{1,3}(s_1)}{H_{2,3}(s_1, s_2)} \right|. \quad (3.43)$$

The relative susceptibility of the output node to (out-of-band) signals applied at the input can be inferred from (3.43). To determine the overall susceptibility of the amplifier, it is sufficient to identify the circuit node that is most sensitive to interference and calculate the IP_2 figure at the output, with respect to that node. This is achieved by consecutively applying the same stimulus to every circuit node and then calculating the second-order intermodulation product at the output. The iteration resulting in the largest IM_2 value indicates the most susceptible node.

The transfer function from the input of the amplifier, i.e., Node 1 in Figure 3.7, to the output (Node 3) is given by (3.24)-(3.38). The signal source is subsequently removed from the input and placed at Node 2, as shown in Figure 3.18. This does not affect the admittance matrix of the circuit (3.23) but yields

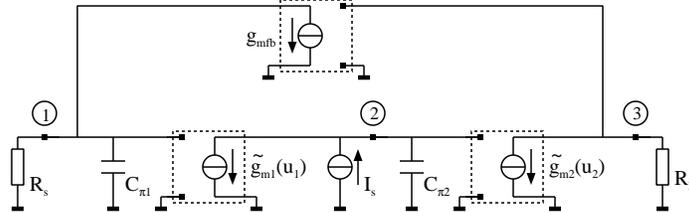


Figure 3.18: Model of the amplifier with the signal source applied to Node 2.

the following normalised linear current source vector:

$$\mathbf{IN}_{1,n2} = \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix}. \quad (3.44)$$

The linear Volterra kernels $\mathbf{H}_{1,n2}$ can be obtained by solving (3.25) with (3.44):

$$H_{1,1,n2}(s_1) = \frac{g_{m2}g_{mfb}}{s_1^2 C_{\pi1} C_{\pi2} g_L + s_1 C_{\pi2} g_s g_L + g_{m1} g_{m2} g_{mfb}}, \quad (3.45)$$

$$H_{1,2,n2}(s_1) = \frac{g_L (s_1 C_{\pi1} + g_s)}{s_1^2 C_{\pi1} C_{\pi2} g_L + s_1 C_{\pi2} g_s g_L + g_{m1} g_{m2} g_{mfb}}, \quad (3.46)$$

$$H_{1,3,n2}(s_1) = -\frac{g_{m2}(s_1 C_{\pi 1} + g_s)}{s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}}. \quad (3.47)$$

The second-order kernels $\mathbf{H}_{n2}(s_1, s_2)$ are subsequently determined from (3.34) and $\mathbf{H}_{1,n2}$, with (3.31):

$$H_{2,1,n2}(s_1, s_2) = \frac{\left[\frac{s_1 s_2 C_{\pi 1}^2 + (s_1 + s_2) C_{\pi 1} g_s + g_s^2}{2V_t} (s_1 + s_2) C_{\pi 2} g_L^2 - g_{m1} g_{m2}^2 g_{mfb}^2 \right]}{2V_t (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{g_{m2} g_{mfb}}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{[(s_1 + s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1 + s_2) C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}]}, \quad (3.48)$$

$$H_{2,2,n2}(s_1, s_2) = -\frac{\frac{s_1 s_2 C_{\pi 1}^2 g_L + [(s_1 + s_2) C_{\pi 1} + g_s](g_s g_L + g_{m2} g_{mfb})}{2V_t} (s_1 + s_2) C_{\pi 2} g_L^2 - g_{m1} g_{m2}^2 g_{mfb}^2}{2V_t (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{g_{m1} g_{m2} g_{mfb} g_L}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{[(s_1 + s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1 + s_2) C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}]}, \quad (3.49)$$

$$H_{2,3,n2}(s_1, s_2) = -\frac{\left[\frac{s_1 s_2 C_{\pi 1}^2 + (s_1 + s_2) C_{\pi 1} g_s + g_s^2}{2V_t} (s_1 + s_2) C_{\pi 2} g_L^2 - g_{m1} g_{m2}^2 g_{mfb}^2 \right]}{2V_t (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{[(s_1 + s_2) C_{\pi 1} + g_s] g_{m2}}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{[(s_1 + s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1 + s_2) C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}]}. \quad (3.50)$$

The intermodulation product, $\text{IM}_{2,n2}$, at the output of the amplifier can be obtained by evaluating (3.39) with (3.50).

In the last iteration of the analysis, the signal source is removed from Node 2 and connected to Node 3, i.e., the output of the amplifier. This is shown in Figure 3.19. The corresponding normalised linear current-source vector is then

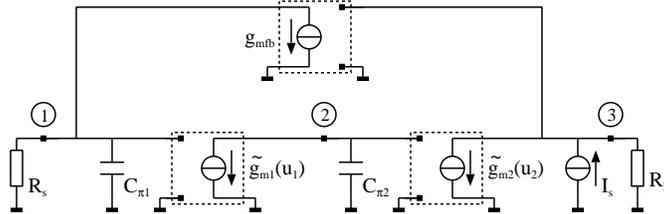


Figure 3.19: Model of the amplifier with the signal source applied to Node 3.

given by:

$$\mathbf{IN}_{1,n3} = \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix}. \quad (3.51)$$

To calculate the linear Volterra kernels $\mathbf{H}_{1,n3}$, (3.25) is solved with (3.51). This yields the following expressions:

$$H_{1,1,n3}(s_1) = -\frac{s_1 C_{\pi 2} g_{mfb}}{s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}}, \quad (3.52)$$

$$H_{1,2,n3}(s_1) = \frac{g_{m1}g_{mfb}}{s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}}, \quad (3.53)$$

$$H_{1,3,n3}(s_1) = \frac{s_1 C_{\pi 2} (s_1 C_{\pi 1} + g_s)}{s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}}. \quad (3.54)$$

The second-order Volterra kernels $\mathbf{H}_{n3}(s_1, s_2)$ are determined by solving (3.34) with $\mathbf{H}_{1,n3}$ and (3.31):

$$H_{2,1,n3}(s_1, s_2) = \frac{[s_1 s_2 C_{\pi 2} - (s_1 + s_2) g_{m1}] C_{\pi 2} g_{m1} g_{m2} g_{mfb}^3}{2V_i (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{[(s_1 + s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1 + s_2) C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}]}, \quad (3.55)$$

$$H_{2,2,n3}(s_1, s_2) = -\frac{[(s_1 + s_2) C_{\pi 1} + g_s] s_1 s_2 C_{\pi 2}^2 g_L + g_{m1}^2 g_{m2} g_{mfb}}{2V_i (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{g_{m1} g_{mfb}}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{[(s_1 + s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1 + s_2) C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}]}, \quad (3.56)$$

$$H_{2,3,n3}(s_1, s_2) = \frac{[s_1 s_2 C_{\pi 2} - (s_1 + s_2) g_{m1}] [(s_1 + s_2) C_{\pi 1} + g_s]}{2V_i (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{C_{\pi 2} g_{m1} g_{m2} g_{mfb}^2}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{[(s_1 + s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1 + s_2) C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}]}. \quad (3.57)$$

The corresponding intermodulation product $IM_{2,n3}$ can be found by substituting (3.57) in (3.39).

At this point, it is possible to compare relative values of the output intermodulation products due to stimulation of each circuit node. This is achieved by calculating the ratios of IM_2 as given by (3.39), to $IM_{2,n2}$ and $IM_{2,n3}$. As the amplitudes of the input signals are the same in each case, this is equivalent to evaluating the ratios of the corresponding output-node, second-order Volterra kernels. So, for instance:

$$\frac{IM_{2,n2}}{IM_2} = \left| \frac{H_{2,3,n2}(s_1, s_2)}{H_{2,3}(s_1, s_2)} \right|. \quad (3.58)$$

Substituting (3.38) and (3.50) to the above expression yields:

$$\frac{H_{2,3,n2}(s_1, s_2)}{H_{2,3}(s_1, s_2)} = -\frac{(s_1 + s_2)(s_1 C_{\pi 1} + g_s)(s_2 C_{\pi 1} + g_s) C_{\pi 2} g_L^2 - g_{m1} g_{m2}^2 g_{mfb}^2}{[s_1 s_2 C_{\pi 2} - (s_1 + s_2) g_{m1}] C_{\pi 2} g_{m1} g_L^2}. \quad (3.59)$$

For a two-tone signal at the input, with difference frequency $\Delta\omega$, according to (3.40):

$$\frac{H_{2,3,n2}(s_1 + \Delta s, -s_1)}{H_{2,3}(s_1 + \Delta s, -s_1)} = -\frac{(s_1^2 C_{\pi 1}^2 + s_1 \Delta s C_{\pi 1}^2 - \Delta s C_{\pi 1} - g_s^2) \Delta s C_{\pi 2} g_L^2 + g_{m1} g_{m2}^2 g_{mfb}^2}{[s_1^2 C_{\pi 2} + s_1 \Delta s C_{\pi 2} + \Delta s g_{m1}] C_{\pi 2} g_{m1} g_L^2}. \quad (3.60)$$

For out-of-band input signals with an in-band difference frequency, i.e., $\omega_1, \omega_2 \gg \Delta\omega$, (3.60) can be simplified as follows:

$$\left| \frac{H_{2,3,n2}(s_1 + \Delta s, -s_1)}{H_{2,3}(s_1 + \Delta s, -s_1)} \right| \approx \left| \frac{s_1^2 C_{\pi 1}^2 \Delta s C_{\pi 2} g_L^2}{s_1^2 C_{\pi 2}^2 g_{m1} g_L^2} \right| = \left| \frac{C_{\pi 1}^2 \Delta s}{C_{\pi 2} g_{m1}} \right|. \quad (3.61)$$

A first-order approximation of the frequency-dependent current gain of the transistors is given by:

$$\beta(s) = \frac{g_m}{sC_\pi}. \quad (3.62)$$

Using the expression for $\beta(s)$, the ratio (3.61) can be rewritten as:

$$\left| \frac{H_{2,3,n2}(s_1 + \Delta s, -s_1)}{H_{2,3}(s_1 + \Delta s, -s_1)} \right| \approx \left| \frac{C_{\pi 1}}{C_{\pi 2}\beta(\Delta s)} \right|. \quad (3.63)$$

So, assuming that the current gain (3.62) for in-band signals is (much) greater than unity, and $C_{\pi 1}$ and $C_{\pi 2}$ are of the same order of magnitude, (3.63) will be less than one. In other words, $|H_{2,3}(s_1 + \Delta s, -s_1)| > |H_{2,3,n2}(s_1 + \Delta s, -s_1)|$. Similarly, the ratio is calculated of the output node second-order Volterra kernels for signals applied at Node 1 and 3, respectively, and is given by:

$$\left| \frac{H_{2,3,n3}(s_1, s_2)}{H_{2,3}(s_1, s_2)} \right| = \frac{g_{mfb}^2}{g_L^2}. \quad (3.64)$$

This will be less than unity for $g_{mfb} < g_L$, as is normally (but not always) the case. The result (3.64) can also be interpreted by inspecting the circuit of Figure 3.19. Neglecting local feedback through $C_{\mu 2}$, a signal source at Node 3 appears directly at the input of the circuit, i.e., Node 1, through the transfer $\frac{g_{mfb}}{g_L}$. Assuming that the load impedance and the transfer of the feedback network are linear as far as the non-linear distortion mechanism of the circuit is concerned, injecting a signal at Node 3 is equivalent to doing so at the input node, albeit with a scaled amplitude. From this and (3.63) it can be concluded that the dominant path for (second-order) intermodulation distortion passes through the input of the amplifier.

To verify the validity of the model and the Volterra series analysis, $IM_{2,n1}$ through $IM_{2,n3}$ are compared to the corresponding results from simulations based on the full transistor model. The circuits of Figure 3.18 and 3.19 are implemented with transistors, as shown in Figure 3.20a and 3.20b, respectively.

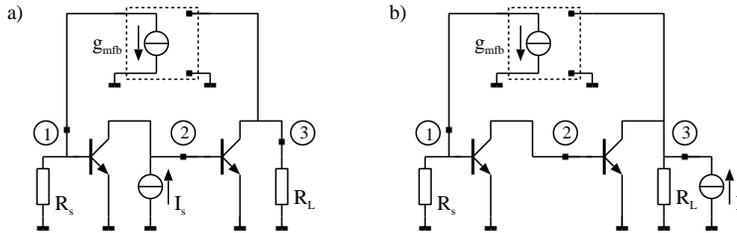


Figure 3.20: Full transistor model circuits for signal injection at Node 2 (a) and Node 3 (b).

In each case, the current source I_s is configured to generate tones at angular

frequencies ω_1 and ω_2 , as defined by (3.40). The in-band difference frequency $\Delta\omega$ is kept constant at 100 MHz, and the magnitude of the output signal at that frequency is determined. This is plotted in Figure 3.21 for a sweep of ω_1 .

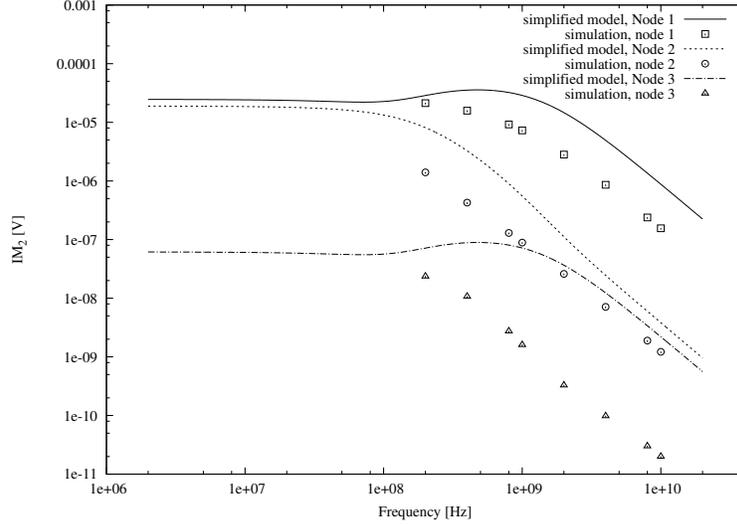


Figure 3.21: Second-order intermodulation product of the amplifier with the signal source at Node 1, 2 or 3.

The plots suggest that there is relatively good fit between the results from the mathematical analysis and the simulation for signals injected in nodes 1 and 2 of the circuit. However, there is an offset of more than an order of magnitude between the predictions of the proposed model and the full transistor model when the output of the amplifier, i.e., Node 3, is driven. This is investigated by including additional parasitics in the proposed model and re-evaluating the circuit in the manner described in sections 3.2.1 and 3.2.2. First, the Miller capacitance is added to the model, as shown in Figure 3.10. The Volterra kernels of the system are calculated by solving (3.17) with (3.41) and (3.24), (3.44) or (3.51), for a signal source present at Node 1, 2 or 3, respectively. The intermodulation products, $IM_{2,n1}$, $IM_{2,n2}$ and $IM_{2,n3}$, are subsequently obtained and plotted in Figure 3.22. It can be observed that while the prediction of $IM_{2,n1}$ and $IM_{2,n2}$ is improved, accounting for C_μ does not appear to influence the prediction of $IM_{2,n3}$ significantly. The simplified transistor model is, therefore, further expanded by including the output capacitance, as shown in Figure 3.14. The Volterra kernels of the amplifier are obtained by solving (3.17) with (3.42) and (3.24), (3.44) or (3.51), so as to be able to calculate $IM_{2,n1}$ through $IM_{2,n3}$. The resulting intermodulation products are plotted in Figure 3.23 and show very good match to the full transistor model simulations. In particular, the prediction of $IM_{2,n3}$ is much better, compared to the cases where C_{out} is neglected. This

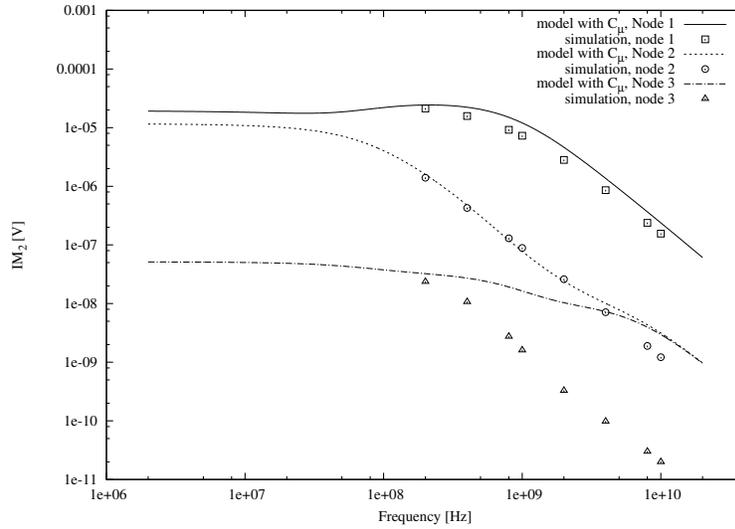


Figure 3.22: Responses of Figure 3.21 with C_{μ} included in the simplified transistor model.

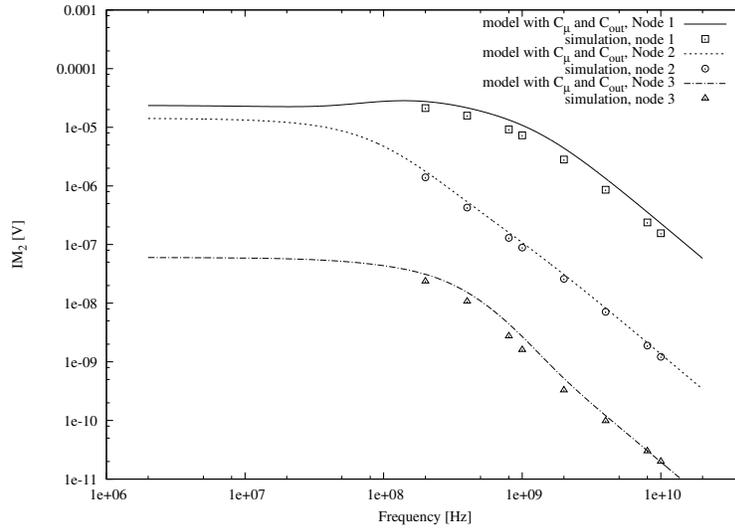


Figure 3.23: Responses of Figure 3.21 with C_{μ} and C_{out} included in the simplified transistor model.

is somewhat expected, as the output capacitance of the second stage transistor and the load resistance, R_L , define a pole in the transfer function of the signal

source at Node 3, which is otherwise disregarded.

3.2.4 Individual contributions of non-linearities

Once the most sensitive node of the amplifier is known, the most critical non-linearity in the signal path can be identified for signals injected at that node. This is achieved by calculating the individual contribution of each non-linear component in the amplifier to the overall transfer function.

Consider that the higher-order Volterra kernels of a system express the combined effect of all circuit non-linearities. For example, for the circuit of Figure 3.7, the second-order Volterra kernel (3.35) accounts for the non-linear behaviour of both \tilde{g}_{m1} and \tilde{g}_{m2} . It is possible to separate the contributions of each non-linear transconductance by decomposing the non-linear current source vector (3.31) into a linear combination of its individual components, as given by:

$$\mathbf{IN}_2 = \mathbf{IN}_{2,gm1} + \mathbf{IN}_{2,gm2}, \quad (3.65)$$

such that each element $\mathbf{IN}_{2,x}$ of the sum contains only the current(s) from a single non-linearity, i.e.,

$$\mathbf{IN}_{2,gm1} = \begin{bmatrix} 0 \\ -i_{NLgm1} \\ 0 \end{bmatrix}, \quad (3.66)$$

and

$$\mathbf{IN}_{2,gm2} = \begin{bmatrix} 0 \\ 0 \\ -i_{NLgm2} \end{bmatrix}. \quad (3.67)$$

Subsequently, (3.34) is evaluated separately for (3.66) and (3.67). This results in the following equations:

$$\mathbf{Y}(s_1 + s_2)\mathbf{H}_{gm1}(s_1, s_2) = \mathbf{IN}_{2,gm1}, \quad (3.68)$$

and

$$\mathbf{Y}(s_1 + s_2)\mathbf{H}_{gm2}(s_1, s_2) = \mathbf{IN}_{2,gm2}. \quad (3.69)$$

Solving them yields the partial second-order Volterra kernels $\mathbf{H}_{gm1}(s_1, s_2)$ and $\mathbf{H}_{gm2}(s_1, s_2)$. The former reflects solely the non-linearity of \tilde{g}_{m1} , and the latter that of \tilde{g}_{m2} . The following applies:

$$\mathbf{H}(s_1, s_2) = \mathbf{H}_{gm1}(s_1, s_2) + \mathbf{H}_{gm2}(s_1, s_2), \quad (3.70)$$

with the partial Volterra kernels given by:

$$\mathbf{H}_{gm1}(s_1, s_2) = \begin{bmatrix} H_{2,1,gm1}(s_1, s_2) \\ H_{2,2,gm1}(s_1, s_2) \\ H_{2,3,gm1}(s_1, s_2) \end{bmatrix}, \quad (3.71)$$

and

$$\mathbf{H}_{gm2}(s_1, s_2) = \begin{bmatrix} H_{2,1,gm2}(s_1, s_2) \\ H_{2,2,gm2}(s_1, s_2) \\ H_{2,3,gm2}(s_1, s_2) \end{bmatrix}. \quad (3.72)$$

Essentially, solving (3.68) and (3.69) amounts to calculating the second-order Volterra kernels of the circuits shown in Figure 3.24a and 3.24b, respectively.

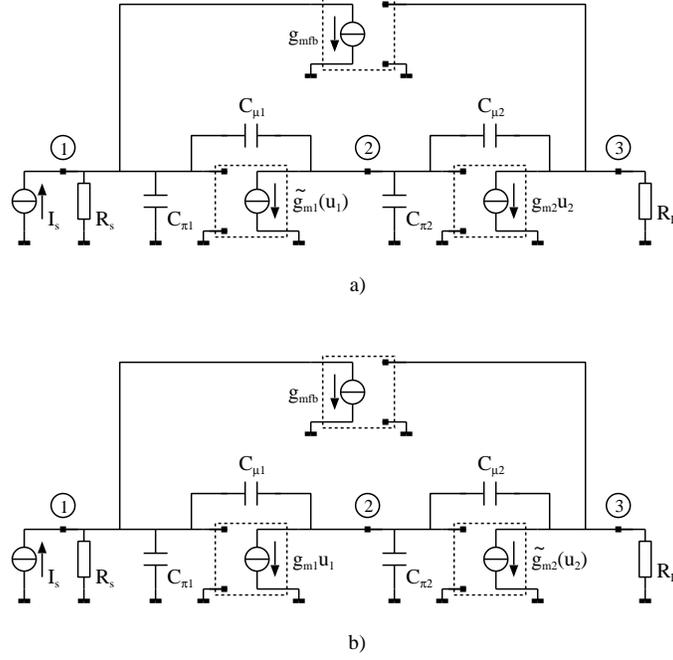


Figure 3.24: The amplifier with non-linearity either only in the input (a) or the output (b) stage.

The non-linearity of either the output stage (a) or the input stage (b) is substituted by a linear transconductance. The linear Volterra kernels for both circuits are the same and are given by (3.36)-(3.38). Solving (3.68) yields the partial second-order Volterra kernels due to \tilde{g}_{m1} :

$$H_{2,1,gm1}(s_1, s_2) = \frac{-\frac{s_1 s_2 C_{\pi 2}^2 g_{m1} g_{m2} g_{mfb} g_L^2}{2V_t (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})}}{\frac{1}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{[(s_1 + s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1 + s_2) C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}]}}}, \quad (3.73)$$

$$H_{2,2,gm1}(s_1, s_2) = \frac{-\frac{s_1 s_2 C_{\pi 2}^2 g_{m1} g_L^3 [(s_1 + s_2) C_{\pi 1} + g_s]}{2V_t (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})}}{\frac{1}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{[(s_1 + s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1 + s_2) C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}]}}}, \quad (3.74)$$

$$H_{2,3,gm1}(s_1, s_2) = \frac{s_1 s_2 C_{\pi 2}^2 g_{m1} g_{m2} g_L^2 [(s_1 + s_2) C_{\pi 1} + g_s]}{2V_t (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{[(s_1 + s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1 + s_2) C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}]} \quad (3.75)$$

Similarly, evaluating (3.69) yields the contribution of the second-order non-linearity of \tilde{g}_{m2} :

$$H_{2,1,gm2}(s_1, s_2) = \frac{(s_1 + s_2) C_{\pi 2} g_{m1}^2 g_{m2} g_{mfb} g_L^2}{2V_t (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{[(s_1 + s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1 + s_2) C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}]} \quad (3.76)$$

$$H_{2,2,gm2}(s_1, s_2) = -\frac{g_{m1}^3 g_{m2} g_{mfb} g_L^2}{2V_t (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{[(s_1 + s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1 + s_2) C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}]} \quad (3.77)$$

$$H_{2,3,gm2}(s_1, s_2) = -\frac{(s_1 + s_2) C_{\pi 2} g_{m1}^2 g_{m2} g_L^2 [(s_1 + s_2) C_{\pi 1} + g_s]}{2V_t (s_1^2 C_{\pi 1} C_{\pi 2} g_L + s_2 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{(s_2^2 C_{\pi 1} C_{\pi 2} g_L + s_1 C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb})} \cdot \frac{1}{[(s_1 + s_2)^2 C_{\pi 1} C_{\pi 2} g_L + (s_1 + s_2) C_{\pi 2} g_s g_L + g_{m1} g_{m2} g_{mfb}]} \quad (3.78)$$

To verify these results, the non-linear transconductors in the circuits of Figure 3.24a and 3.24b are substituted by full transistor models, as shown in Figure 3.25a and 3.25b, respectively. The transistor circuits are simulated with a two-tone signal at the input with tone frequencies ω_1 and ω_2 , such that (3.40) applies. The amplitude of the output (Node 3) signal at the difference frequency $\Delta\omega$ is determined, and plotted in Figure 3.26 for a sweep of ω_1 . Likewise, the IM₂ values obtained from (3.75) and (3.78) with (3.39) are plotted in the figure. A good match between the predictions of the non-linear small-signal model and the full transistor model is observed. It can furthermore be concluded that the non-linearity of the first and second stages of the amplifier manifests itself differently at different frequencies. At low frequencies the output stage contributes the dominant fraction of the total non-linearity, as suggested by negative-feedback amplifier theory [49]. However, as the frequency increases, the role of the output stage diminishes and the input stage becomes the dominant contributor. This is convenient for formulating an out-of-band criterion for the amplifier.

3.2.5 Out-of-band criterion

As seen in Figure 3.26, the relative contribution of the first and second stage non-linearity to the signal transfer function of the amplifier varies with frequency. According to classical negative-feedback amplifier theory, the output stage dominates the distortion behaviour, as it experiences the largest signal swing. However, the plots of Figure 3.26 suggest that this ceases to be the case at high frequencies. The attenuation of the devices then becomes larger than their gain, and there is a net decrease of (high-frequency) signal swing along the amplification chain. The input stage receives the strongest excitation,

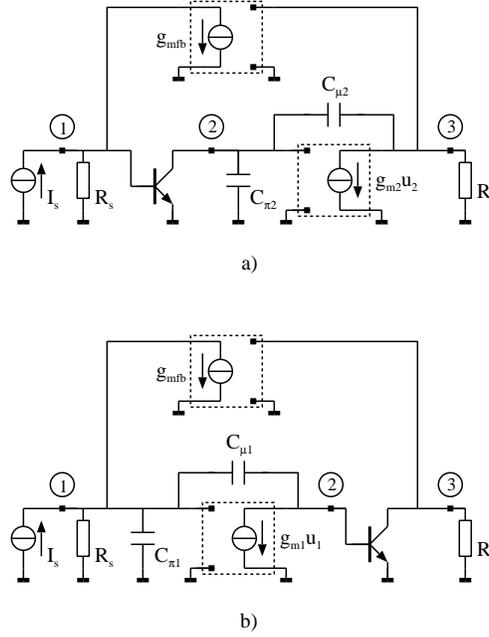


Figure 3.25: The amplifier with a transistor stage either at the input (a), or the output (b).

and hence becomes the dominant source of non-linear distortion. This shift of relative impact of the device non-linearities from output to input is used to formulate a criterion defining the onset of the out-of-band frequency range. The latter is defined as the frequency at which the input stage starts to dominate the second-order intermodulation product of the amplifier. For the circuit of Figure 3.7, this can be determined by comparing the transfers of non-linear transconductances \tilde{g}_{m1} and \tilde{g}_{m2} to the output of the system. This amounts to determining the ratio of the partial second-order Volterra kernels at the output node. Using (3.75) and (3.78), this can be shown to be:

$$\left| \frac{H_{2,3,gm1}(s_1, s_2)}{H_{2,3,gm2}(s_1, s_2)} \right| = \left| \frac{C_{\pi 2} s_1 s_2}{g_{m1}(s_1 + s_2)} \right|. \quad (3.79)$$

The input stage non-linear transconductance \tilde{g}_{m1} will begin to dominate the contribution to the IM_2 product for frequencies such that the above expression becomes greater than unity. Note that the ratio (3.79) is dependent on the difference between the two tones represented by s_1 and s_2 . The out-of-band criterion can be generalised by determining the unity value of (3.79) for the maximum in-band intermodulation frequency. In the present example, this is the corner frequency of the amplifier, i.e., 100 MHz. Solving (3.79) for $\Delta\omega$ equal to 100 MHz yields approximately 75 MHz as the onset of the out-of-band region.

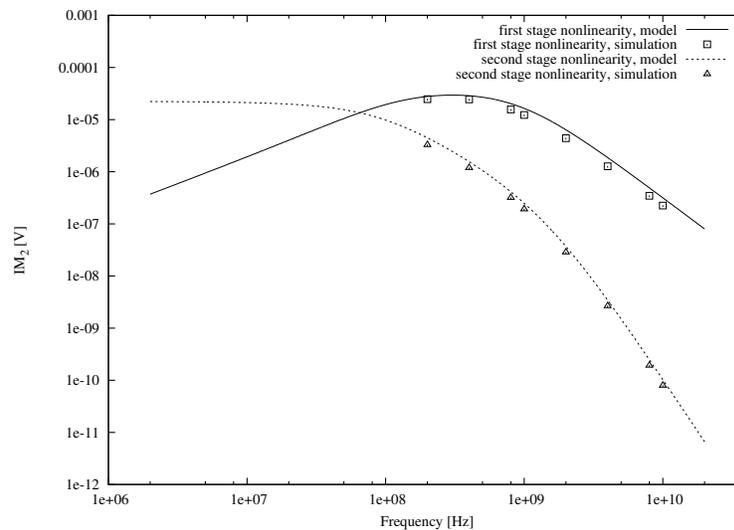


Figure 3.26: Second-order intermodulation product of the amplifier.

3.3 Conclusion

A strongly simplified transistor model is proposed in this chapter to aid the non-linear analysis of negative-feedback amplifiers. This model is independent of device type and technology and is based on the device transconductance as the dominant source of non-linear distortion. The impact of various simplifications in the proposed model is evaluated by using it to analyse a generic amplifier and comparing its predictions to a full-complexity SPICE simulation. The results suggest that both the overall non-linear response of the amplifier and the amplifying stage that dominates it can be adequately determined. Of course, there are differences between the predictions of the proposed model and the SPICE simulations due to the considerable degree of simplification of the former. These approximations are considered acceptable for the purposes of this study because the correct trends are predicted by the proposed model, which is more conservative than the full model.

Chapter 4

Simplified non-linear analysis

“Pluralitas non-est ponenda sine necessitate.”

William of Ockham

A high-frequency non-linear device model was proposed in the previous chapter and used to investigate a generic negative-feedback amplifier. The amplifier circuit was analysed using the Volterra series, which is an established method for treating non-linear frequency-dependent systems. Being a general analysis tool, the Volterra series introduce a high degree of complexity, as all non-linear terms of the signal at each circuit node are systematically accounted for. A streamlined alternative is proposed here, which focuses exclusively on the down-conversion of out-of-band interference in a (baseband) negative-feedback amplifier. This aims to provide a simplified approach to susceptibility estimation, and the evaluation of design strategies. It is intended as a first-order indication of the non-linear behaviour of the amplifier. Its estimate can subsequently be refined using the Volterra series analysis outlined in Chapter 3, or full complexity circuit simulation. The restriction of scope to down-conversion in a negative-feedback system allows a number of simplifications compared to a general circuit analysis. These simplifications concern the non-linear behaviour of the circuit at different frequencies and are outlined below.

In-band behaviour Negative feedback was originally introduced to amplifiers as a measure to improve their linearity [3]. It can be shown that increasing the loop gain of a system with (linear) negative feedback results in an increased linearity of its transfer function [51]. This is routinely made use of in amplifier designs. Typically, the in-band loop gain of a negative-feedback amplifier is sufficiently high to suppress the effect of circuit non-linearities. So, to simplify the baseband analysis, the entire system can be assumed to be linear for in-band signals.

Out-of-band behaviour The loop gain of a negative-feedback amplifier is not constant, and tends to diminish with increasing frequency. This is caused by the limited bandwidth of the active devices used in the circuit, and is reflected by the loop poles [52]. In contrast to the in-band loop gain, at high frequencies the loop gain declines progressively until its influence on the overall transfer function of the amplifier becomes insignificant. Therefore, for far out-of-band excitation signals, the negative feedback can be assumed absent. The amplifier can then be treated as an open loop system, which simplifies the non-linear analysis.

Sources of non-linearity It is assumed that the essential sources of non-linearity in an amplifier circuit are the active components that implement signal gain [9]. These can be divided into a number of stages, which form the signal chain of the amplifier. All other circuit functionality that employs active devices but does not involve signal gain, such as biasing and filtering, could, in principle, be implemented with passive components, hence its associated non-linearity is considered as avoidable. Passive components can exhibit some form of non-linear behaviour [53, 54], particularly when defects are present in their structure [55], but normally these are only weak non-linearities and may also be disregarded. There are strongly non-linear passive components, such as switches, but since switching amplifiers are outside the scope of this work, such components are not expected to affect the steady-state operation of the circuits we consider.

Based on the above assumptions, the problem of characterising a negative-feedback amplifier is reduced to modelling the non-linear behaviour along a chain of amplifying stages at high frequencies, followed by a linear analysis at low frequencies. Each amplifier stage is represented by an arbitrary frequency-dependent non-linear function, such that the open loop gain of the whole circuit is given by the product of the non-linear transfer functions of the individual stages. The frequency-dependent non-linear function is subsequently regarded as a product of a frequency-dependent linear component and a frequency-independent non-linear component. The former accounts for the frequency behaviour of the amplifying stage, while the latter models its core non-linearity, i.e., the non-linear device transconductance.

4.1 Amplifier stage model

The forward gain section of the amplifier circuit can be regarded as a cascade of amplifying stages. Each of these is modeled as a black box comprising an arbitrary non-linear transfer function, in combination with a frequency-dependent linear gain. This seems particularly suited to transistors because there the foremost source of non-linearity is the device transconductance and the transfer function of its control voltage is frequency-dependent. Partitioning of the forward gain is carried out according to the number of stages of the amplifier, so that every segment accounts for one dominant loop pole. The input and output quantities of each segment depend on the partitioning of the circuit and need

not be specified in advance. A schematic of a frequency-dependent non-linear stage is shown in Figure 4.1.

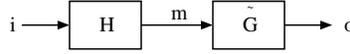


Figure 4.1: Model of a frequency-dependent non-linear stage.

The frequency-dependent transfer, H , is a first-order linear function of the form:

$$H(j\omega) = \frac{H_0}{1 + \frac{j\omega}{p}}. \quad (4.1)$$

The non-linear frequency-independent section, \tilde{G} , can be represented by a Taylor series:

$$o(t) = \tilde{G}(m(t)) = g_0 + g_1 m(t) + g_2 m^2(t) + g_3 m^3(t) + \dots \quad (4.2)$$

In a transistor-based amplifier stage, \tilde{G} reflects the transconductance of the device, and the signal at Node m of Figure 4.1 is expressed as a voltage. Typically, the output quantity, o , is a current but will ultimately depend on the topology of the amplifier. The input quantity, i , may also be a current, for example when it reflects the output signal of a preceding stage, but will likewise depend on the exact circuit topology.

4.1.1 Steady-state response

Let a sinusoidal excitation of frequency ω_α and amplitude \hat{i}_α be present at Node i of Figure 4.1. In the time domain, this input signal is then given by:

$$i(t) = \hat{i}_\alpha \cos(\omega_\alpha t). \quad (4.3)$$

The system is subsequently considered in steady-state. In the Fourier domain, the signal observed at Node m simply follows from (4.1):

$$M(j\omega) = I(j\omega)H(j\omega). \quad (4.4)$$

This can be rewritten in the time domain by taking the inverse Fourier transform of (4.4):

$$m(t) = \mathcal{F}^{-1}[M(j\omega)] = |M(j\omega)| \cos(j\omega + \angle M(j\omega)). \quad (4.5)$$

So, for the single-tone input signal (4.3), substituting (4.1) in (4.5) yields:

$$m(t) = \hat{i}_\alpha |H(j\omega_\alpha)| \cos(\omega_\alpha t + \angle H(j\omega_\alpha)). \quad (4.6)$$

By combining (4.2) and (4.6), the overall input-output relation of the stage depicted in Figure 4.1 can be derived. For a single tone of frequency ω_α and amplitude \hat{i}_α present at the input, the output signal is given by:

$$\begin{aligned} o(t) = & g_0 + g_1 \hat{i}_\alpha |H(j\omega_\alpha)| \cos(\omega_\alpha t + \angle H(j\omega_\alpha)) + \\ & \frac{g_2 \hat{i}_\alpha^2 |H(j\omega_\alpha)|^2}{2} [\cos(2\omega_\alpha t + 2\angle H(j\omega_\alpha)) + 1] + \\ & \frac{g_3 \hat{i}_\alpha^3 |H(j\omega_\alpha)|^3}{4} [\cos(3\omega_\alpha t + 3\angle H(j\omega_\alpha)) + \\ & 3\cos(\omega_\alpha t + \angle H(j\omega_\alpha))] + \dots \end{aligned} \quad (4.7)$$

So, the amplitude, \hat{o}_α , of the output signal component at frequency ω_α is found to be:

$$\hat{o}_\alpha = \frac{g_1 \hat{i}_\alpha H_0}{\left|1 + \frac{j\omega_\alpha}{p}\right|} + \frac{3g_3 \hat{i}_\alpha^3 H_0^3}{4 \left|1 + \frac{j\omega_\alpha}{p}\right|^3} + \dots \quad (4.8)$$

The constant coefficients in (4.8) may be grouped according to:

$$N_1 = g_1 H_0; \quad N_3 = \frac{3g_3 H_0^3}{4}; \quad N_5 = \dots, \quad (4.9)$$

resulting in:

$$\hat{o}_\alpha = \frac{N_1}{\left|1 + \frac{j\omega_\alpha}{p}\right|} \hat{i}_\alpha + \frac{N_3}{\left|1 + \frac{j\omega_\alpha}{p}\right|^3} \hat{i}_\alpha^3 + \dots \quad (4.10)$$

4.1.2 Intermodulation products

Let the input contain two harmonic components ω_α and ω_β with respective amplitudes \hat{i}_α and \hat{i}_β , of the form given by (4.3). Then a signal of frequency ω_γ will appear at the output, where ω_γ is the difference of ω_α and ω_β . The amplitude, \hat{o}_γ , of the output signal component at frequency ω_γ is given by:

$$\begin{aligned} \hat{o}_\gamma = & \frac{N_2}{\left|1 + \frac{j\omega_\alpha}{p}\right| \left|1 + \frac{j\omega_\beta}{p}\right|} \hat{i}_\alpha \hat{i}_\beta + \\ & \frac{N_4}{\left|1 + \frac{j\omega_\alpha}{p}\right|^3 \left|1 + \frac{j\omega_\beta}{p}\right|} \cdot \frac{3\hat{i}_\alpha^2 \hat{i}_\beta}{2} + \\ & \frac{N_4}{\left|1 + \frac{j\omega_\alpha}{p}\right| \left|1 + \frac{j\omega_\beta}{p}\right|^3} \cdot \frac{3\hat{i}_\alpha \hat{i}_\beta^2}{2} + \dots, \end{aligned} \quad (4.11)$$

with

$$\omega_\gamma = |\omega_\alpha - \omega_\beta|. \quad (4.12)$$

4.2 Linear analysis of negative-feedback amplifiers

Consider the general form of a negative-feedback amplifier shown in Figure 3.4. This consists of a forward gain A and a feedback transfer β . Both A and β are assumed to be linear, time-invariant parameters. An input quantity, i , is transformed into an output quantity, o , such that the transfer function of the system is given by (3.13), i.e., $\frac{A}{1-A\beta}$. For large values of A , as is normally the case for a negative-feedback amplifier, the transfer function approximates $-\frac{1}{\beta}$, i.e., it is solely determined by the feedback coefficient [3].

4.2.1 Impact of spurious signals

To obtain net amplification, the negative-feedback network of an amplifier is attenuating, which is the reason it can be, and typically is, implemented with

passive components. This explains its inherent linearity, and the beneficial effect it has on the overall linearity of the system. On the other hand, the forward gain of the amplifier is designed to be as large as possible, which is achieved by using active devices, such as transistors. These exhibit various forms of non-linear behaviour and impart that on the overall transfer function. To achieve a high gain, the amplification chain often consists of a number of cascaded gain stages. Consider an arbitrary partitioning of the forward gain, A , in two sections, A_I and A_{II} , such that:

$$A = A_I A_{II}. \quad (4.13)$$

Due to non-linear behaviour of the components used to implement the first section, its transfer function may differ from A_I . In a linear system this can be modelled by adding a (signal-dependent) error term, ϵ , to its output. For example, ϵ could be the spurious in-band signal appearing as a result of out-of-band interference at the input of the amplifier. This parasitic signal is superimposed on the regular information that is currently being processed and will be propagated to the output of the amplifier together with it. Such superposition is illustrated in Figure 4.2. Negative feedback is able to suppress ϵ to a certain

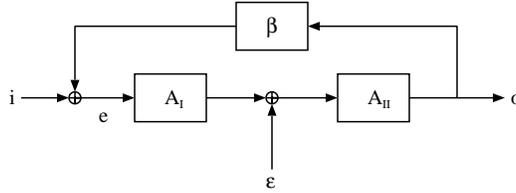


Figure 4.2: Negative-feedback amplifier with injected disturbance ϵ .

degree, depending on the place where it first appears. To determine its transfer to the output, the modified equation for the signal at o ,

$$o = A_{II}(\epsilon + A_I e), \quad (4.14)$$

is solved together with (3.13). This yields an expression for the combined output signal:

$$o = \frac{A_I A_{II}}{1 - A_I A_{II} \beta} \left(i + \frac{\epsilon}{A_I} \right). \quad (4.15)$$

So, for large $A_I A_{II}$, the transfer function of ϵ to the output of the amplifier becomes:

$$\frac{o}{\epsilon} \approx -\frac{1}{A_I \beta}. \quad (4.16)$$

Clearly, negative feedback is best able to compensate for the appearance of ϵ if the latter occurs close to the output of the amplification chain. So, for a fixed $A_I A_{II}$ product, the ratio $\frac{A_I}{A_{II}}$ should be maximised to obtain maximal suppression of ϵ . This agrees with the conclusions already drawn in Chapter 3.

4.2.2 Behaviour at high frequencies

The frequency response of the forward gain, A , is analysed, as it may effectively determine the amount of exposure to an out-of-band interference signal. Consider the amplification chain of a negative-feedback amplifier consisting of one or more cascaded gain stages. Each stage providing net signal gain is regarded as contributing a dominant pole to the overall transfer function of the amplifier. Its frequency response is modelled as the first-order function (4.1). The general form of the frequency-dependent forward gain is given by:

$$A(j\omega) = \frac{A_{01}}{1 + \frac{j\omega}{p_1}} \cdot \frac{A_{02}}{1 + \frac{j\omega}{p_2}} \cdots \frac{A_{0n}}{1 + \frac{j\omega}{p_n}}, \quad (4.17)$$

where

$$\frac{A_{0m}}{1 + \frac{j\omega}{p_m}}, \quad m \in [1, n], \quad (4.18)$$

is the individual transfer function of the m -th gain stage. At DC, $A(j\omega)$ is at its maximum, i.e., $A_{01}A_{02} \cdots A_{0n}$. As the frequency increases, so do the denominators of the different terms of $A(j\omega)$, and the total gain diminishes. The signal at the input of the forward gain section is the difference of the input signal to the amplifier and the feedback signal. This is denoted by e in Figure 3.4 and is known as the error term of the amplifier. It can be shown from 3.13 and 4.17 that:

$$e = \frac{\left(1 + \frac{j\omega}{p_1}\right) \left(1 + \frac{j\omega}{p_2}\right) \cdots \left(1 + \frac{j\omega}{p_n}\right) i}{\left(1 + \frac{j\omega}{p_1}\right) \left(1 + \frac{j\omega}{p_2}\right) \cdots \left(1 + \frac{j\omega}{p_n}\right) - A_{01}A_{02} \cdots A_{0n}\beta}. \quad (4.19)$$

In the intended mode of operation of a negative-feedback system, the error term approaches zero due to the large forward gain:

$$\lim_{A(j\omega) \rightarrow \infty} e = 0. \quad (4.20)$$

This is typically the case at DC and low frequencies, where $e \approx -\frac{i}{A_{01}A_{02} \cdots A_{0n}\beta}$. However, in the out-of-band region, where the loop gain is significantly below unity, i.e., $A_{01}A_{02} \cdots A_{0n}\beta \ll \left(1 + \frac{j\omega}{p_1}\right) \left(1 + \frac{j\omega}{p_2}\right) \cdots \left(1 + \frac{j\omega}{p_n}\right)$, it follows from (4.19) that the ratio $\frac{e}{i}$ approaches unity:

$$\lim_{A(j\omega) \rightarrow 0} e = i. \quad (4.21)$$

As $e \approx i$ and $o = A(j\omega)e$, the transfer function of the amplifier becomes:

$$o \approx A(j\omega)i. \quad (4.22)$$

In other words, the amplifier no longer behaves as a negative-feedback loop and its transfer function can be approximated by the straight gain of the forward gain section. This can significantly simplify the analysis of the system at high frequencies.

4.3 Non-linear analysis approach

The general form of a negative-feedback amplifier comprising a multistage non-linear forward gain section is depicted in Figure 4.3. Each amplifying stage

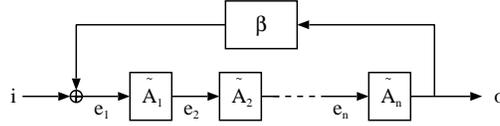


Figure 4.3: Negative-feedback amplifier with non-linear forward gain.

\tilde{A}_x , with $x \in [1, n]$, is represented by the frequency-dependent non-linear model developed in Section 4.1. The transfer function of the amplification chain can be calculated from:

$$e_{x+1} = \tilde{A}_x(e_x), \quad x \in [1, n-1], \quad (4.23)$$

with

$$o = \tilde{A}_n(e_n). \quad (4.24)$$

As shown in Figure 4.1, the amplifying stages are regarded as comprising a linear frequency-dependent component, H , and a non-linear frequency independent component, \tilde{G} . The schematic of Figure 4.3 can be expanded to include this detail and, in particular, the intermediate quantities m_x , $x \in [1, n]$, between the linear and non-linear subsections. This is seen in Figure 4.4. To determine

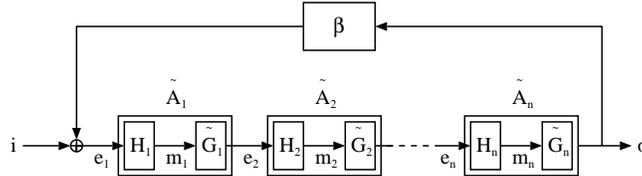


Figure 4.4: Linear and non-linear components of the forward gain stages.

the impact of out-of-band interference entering the circuit through the input, first the signal transfer to the intermediate nodes is calculated. As discussed in Section 4.2.2, due to the low open loop gain at high frequencies the negative feedback may be neglected and the transfer function from the input to the output approximates that of the forward gain, i.e., $o \approx \tilde{A}_n(\tilde{A}_{n-1}(\dots \tilde{A}_1(i)))$. Since high-power effects, such as desensitization and blocking, are beyond the scope of this study, a linear analysis is sufficient to calculate the transfer functions, $\frac{m_x}{i}$, of the out-of-band interference signal. For this purpose, the non-linear functions \tilde{G}_x are assumed linear (affine) by taking the first two terms of their Taylor decomposition (4.2):

$$G_x(m) = g_{0_x} + g_{1_x} m, \quad (4.25)$$

with

$$\tilde{G}_x(m) = g_{0_x} + g_{1_x}m + g_{2_x}m^2 + g_{3_x}m^3 + \dots, \quad x \in [1, n]. \quad (4.26)$$

The problem is now reduced to analysing a cascade of affine functions. Let ω_α be the frequency of the interference signal. The transfers to the intermediate nodes can be obtained from:

$$\frac{\hat{m}_x}{\hat{i}} = |H_x(\omega_\alpha)| \prod_{y=1}^{x-1} |H_y(\omega_\alpha)| G_y, \quad x \in [2, n], \quad (4.27)$$

with $\frac{\hat{m}_1}{\hat{i}}$ being simply $H_1(\omega_\alpha)$. These give the amplitude of the interference signal at the input of each non-linear function \tilde{G}_x . Once this is known, the nonlinear distortion can be determined using (4.26). As discussed previously, the second-order intermodulation products are predominantly responsible for the frequency folding from the out-of-band range to the operating band of the amplifier. So, only the g_2 coefficients of \tilde{G}_x are used to calculate the in-band part of IM_2 . For a two-tone interference signal of frequencies ω_α and ω_β , where both ω_α and ω_β are out-of-band, this yields:

$$\hat{\epsilon}_{x+1} = g_{2_x} \hat{m}_x(j\omega_\alpha) \hat{m}_x(j\omega_\beta). \quad (4.28)$$

The in-band IM_2 product, $\hat{\epsilon}_x$, is treated as a signal injected into a linear negative-feedback loop and its input-referred magnitude, $\hat{\epsilon}_{x,in}$, is calculated using (4.15). For $\omega_\gamma = |\omega_\alpha - \omega_\beta|$, where ω_γ is in-band:

$$\hat{\epsilon}_{x,in} = \frac{\hat{\epsilon}_x}{\prod_{y=1}^{x-1} |H_y(\omega_\gamma)| G_y}, \quad x \in [2, n]. \quad (4.29)$$

This can be expressed as a function of the input signal by combining (4.27), (4.28) and (4.29):

$$\hat{\epsilon}_{x+1,in} = \frac{g_{2_x} \hat{i}_\alpha \hat{i}_\beta |H_x(\omega_\alpha) H_x(\omega_\beta)| \prod_{y=1}^{x-1} |H_y(\omega_\alpha) H_y(\omega_\beta)| G_y^2}{\prod_{y=1}^x |H_y(\omega_\gamma)| G_y}, \quad x \in [2, n], \quad (4.30)$$

where $\hat{\epsilon}_{2,in} = \frac{g_{2_1} \hat{i}_\alpha \hat{i}_\beta |H_1(\omega_\alpha) H_1(\omega_\beta)|}{|H_1(\omega_\gamma)| G_1}$ and the amplitudes of the interference signals at frequencies ω_α and ω_β are \hat{i}_α and \hat{i}_β respectively. The result is a significantly simplified and straight-forward method for determining the susceptibility of a (baseband) negative-feedback amplifier to out-of-band interference. In particular, the assumption that negative feedback is absent at high frequencies serves to reduce the complexity of the non-linear circuit analysis. This affords a quick estimate of the performance of an amplifier and identification of the dominant sources of distortion.

4.4 Example

To demonstrate the proposed approach, the individual non-linearity contribution analysis of Section 3.2.4 is repeated using the amplifier stage model developed in Section 4.1. The amplifier of Figure 3.6 is considered in open loop for

out-of-band signals and the forward gain is partitioned according to the number stages. Intermodulation products are calculated using the method outlined in Section 4.3 instead of the Volterra series analysis.

As described in Section 3.2.4, the non-linearity of each amplifier stage is evaluated separately, with the remainder of the circuit regarded as linear. In our case this amounts to analysing two distinct circuits; one with a non-linear input stage, followed by linear gain, and one with a non-linear output stage, preceded by linear gain. This is equivalent to obtaining the partial Volterra kernels (3.71) and (3.72).

4.4.1 Non-linear input stage

When a non-linear stage is present at the input of the amplifier, the forward gain section can be represented as shown in Figure 4.5. The non-linear section, \tilde{A}_1 ,

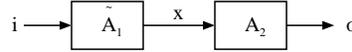


Figure 4.5: Non-linear stage at the input, followed by linear gain.

where $\tilde{A}_1 = H_1 \tilde{G}_1$, has the transfer function shown in (4.10) and (4.11). The linear frequency-dependent function, H_1 , is given by (4.1), while \tilde{G}_1 is a non-linear frequency-independent function of the form (4.26). The linear section, A_2 , is of the form:

$$A_n(j\omega) = \frac{A_{0n}}{1 + \frac{j\omega}{p_n}}, \quad (4.31)$$

with $n = 2$. Let two out-of-band sinusoidal signals with frequencies ω_α and ω_β and respective amplitudes \hat{i}_α and \hat{i}_β be present at the input of the amplifier. The amplitude, \hat{o}_α , of the output signal component at frequency ω_α can be obtained using (4.10) and (4.31):

$$\hat{o}_\alpha = \frac{H_{01} A_{02} g_{11}}{\left|1 + \frac{j\omega_\alpha}{p_1}\right| \left|1 + \frac{j\omega_\alpha}{p_2}\right|} \hat{i}_\alpha + \frac{3H_{01}^3 A_{02} g_{13}}{4 \left|1 + \frac{j\omega_\alpha}{p_1}\right|^3 \left|1 + \frac{j\omega_\alpha}{p_2}\right|} \hat{i}_\alpha^3 + \dots \quad (4.32)$$

The output signal magnitude at frequency ω_β can be calculated analogously. Due to the non-linear behaviour of \tilde{A}_1 , intermodulation products of the two signals will appear at its output, some of which may fall within the band of the system. Let ω_γ be one such signal, where the condition in (4.12) is met. The value of ω_γ is chosen well within the band of the system, so that the denominator of (4.31) at that frequency is close to unity. The intermodulation product at ω_γ is calculated using (4.28) for $x = 1$:

$$\hat{\epsilon}_\gamma = \frac{H_{01}^2 g_{21}}{\left|1 + \frac{j\omega_\alpha}{p_1}\right| \left|1 + \frac{j\omega_\beta}{p_1}\right|} \hat{i}_\alpha \hat{i}_\beta. \quad (4.33)$$

Since ω_γ is in-band, the situation becomes analogous to that in Figure 4.2, and negative feedback attempts to compensate for the injected signal. Using (4.29), the input-referred amplitude of the intermodulation product is calculated:

$$\hat{\epsilon}_{\gamma,in} = \frac{H_{01}g_{21} \left| 1 + \frac{j\omega_\gamma}{p_1} \right|}{g_{11} \left| 1 + \frac{j\omega_\alpha}{p_1} \right| \left| 1 + \frac{j\omega_\beta}{p_1} \right|} \hat{i}_\alpha \hat{i}_\beta, \quad (4.34)$$

or

$$\hat{\epsilon}_{\gamma,in} \approx \frac{H_{01}g_{21}}{g_{11} \left| 1 + \frac{j\omega_\alpha}{p_1} \right| \left| 1 + \frac{j\omega_\beta}{p_1} \right|} \hat{i}_\alpha \hat{i}_\beta. \quad (4.35)$$

It is clear that placement of additional linear gain after the non-linear stage (i.e., modifying A_{02}) does not affect $\hat{\epsilon}_{\gamma,in}$, and, therefore, also not the susceptibility to out-of-band interference of the entire system. The corresponding output amplitude of the signal at frequency ω_γ is calculated by simply multiplying (4.40) with the in-band transfer function of the amplifier, i.e.,

$$\hat{o}_\gamma \approx \frac{\hat{\epsilon}_{\gamma,in}}{\beta}. \quad (4.36)$$

Substituting the component values of the equivalent non-linear small-signal circuit of Figure 3.7 in (4.36) results in:

$$\hat{o}_\gamma \approx \frac{R_{\pi s}}{2g_{mft}v_t \left| 1 + j\omega_\alpha R_{\pi s} C_{\pi 1} \right| \left| 1 + j\omega_\beta R_{\pi s} C_{\pi 1} \right|} \hat{i}_\alpha \hat{i}_\beta, \quad (4.37)$$

where $R_{\pi s} = R_s || R_{\pi 1}$ and the influence of the Miller capacitance is disregarded. This corresponds to the IM_2 product calculated from (3.75) and is plotted in Figure 4.6, alongside the previously obtained result, as shown in Figure 3.26. The plots suggest a reasonably good match, with a slightly more pessimistic result, i.e., a larger distortion product, from the simplified approach. This seems acceptable, considering the significant reduction of complexity achieved.

4.4.2 Non-linear output stage

When the non-linearity is situated at the output of the amplifier, the forward gain section can be represented by the diagram in Figure 4.7. A_1 is a frequency-dependent linear gain of the form (4.31) and $\tilde{A}_2 = H_2 \tilde{G}_2$. Two out-of-band harmonic signals, ω_α and ω_β , of respective amplitudes \hat{i}_α and \hat{i}_β are applied at the input of the amplifier. The amplitude, \hat{o}_α , of the output signal at frequency ω_α is now given by:

$$\hat{o}_\alpha = \frac{A_{01} H_{02} g_{12}}{\left| 1 + \frac{j\omega_\alpha}{p_1} \right| \left| 1 + \frac{j\omega_\alpha}{p_2} \right|} \hat{i}_\alpha + \frac{3A_{01}^3 H_{02}^3 g_{32}}{4 \left| 1 + \frac{j\omega_\alpha}{p_1} \right|^3 \left| 1 + \frac{j\omega_\alpha}{p_2} \right|^3} \hat{i}_\alpha^3 + \dots \quad (4.38)$$

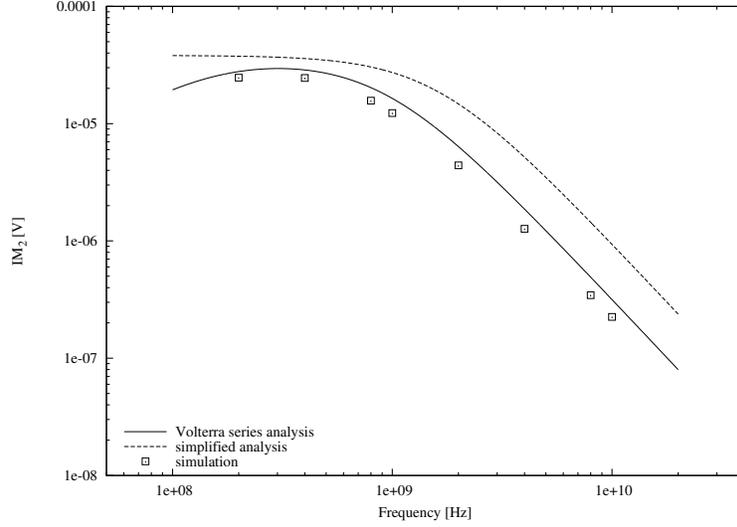


Figure 4.6: IM_2 product for the non-linear input stage obtained from the Volterra series analysis, the simplified analysis and SPICE simulation.

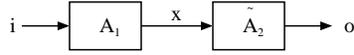


Figure 4.7: Linear input stage followed by non-linearity.

The value of \hat{o}_β is calculated analogously. The input-referred magnitude, $\hat{\epsilon}_{\gamma,in}$, of the second stage intermodulation product at frequency ω_γ is obtained as outlined in the previous case:

$$\hat{\epsilon}_{\gamma,in} = \frac{A_{0_1} H_{0_2} g_{2_2} \left| 1 + \frac{j\omega_\gamma}{p_1} \right| \left| 1 + \frac{j\omega_\gamma}{p_2} \right|}{g_{1_2} \left| 1 + \frac{j\omega_\alpha}{p_1} \right|^2 \left| 1 + \frac{j\omega_\beta}{p_2} \right|^2} \hat{i}_\alpha \hat{i}_\beta, \quad (4.39)$$

and

$$\hat{\epsilon}_{\gamma,in} \approx \frac{A_{0_1} H_{0_2} g_{2_2}}{g_{1_2} \left| 1 + \frac{j\omega_\alpha}{p_1} \right|^2 \left| 1 + \frac{j\omega_\beta}{p_2} \right|^2} \hat{i}_\alpha \hat{i}_\beta. \quad (4.40)$$

Again, the output amplitude of the signal at frequency ω_γ is calculated by multiplying $\hat{\epsilon}_{\gamma,in}$ by the in-band transfer function of the amplifier. Substituting the equivalent circuit component parameters in the expression yields:

$$\hat{o}_\gamma \approx \frac{\frac{g_{m1} R_{\pi s}}{2g_{mfb} v_t |1+j\omega_\alpha R_{\pi s} C_{\pi 1}| |1+j\omega_\beta R_{\pi s} C_{\pi 1}|}}{\frac{R_{\pi 2}}{|1+j\omega_\alpha R_{\pi 2} C_{\pi 2}| |1+j\omega_\beta R_{\pi 2} C_{\pi 2}|}}. \quad (4.41)$$

The value of (4.41) is plotted in Figure 4.8, together with the corresponding result (3.78) from the Volterra series analysis. Once more, there is a good match

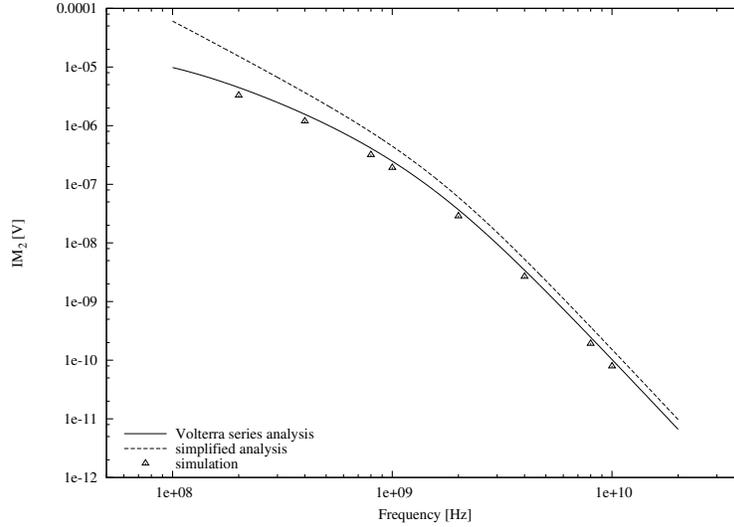


Figure 4.8: IM_2 product for the non-linear output stage obtained from the Volterra series analysis, the simplified analysis and SPICE simulation.

between the predictions of the different methods. The simplified approach converges to the trend of the Volterra series result and the full transistor simulation at the high end of the evaluated frequency range.

4.4.3 Discussion

It is expected that the simplified approach suggested in this chapter yields an acceptable result only when the assumptions it is based on are indeed fulfilled. For example, in order for the amplifier to be adequately represented as an open loop system for out-of-band signals, its open loop gain has to be sufficiently low (i.e., lower than unity) at the frequency of the interference. Consider the open loop gain plot of the amplifier analysed in this example, as shown in Figure 4.9. The unity gain frequency is at approximately 100 MHz, and the open loop gain falls below 0.1 around 1 GHz. So, the simple model is expected to yield an acceptable result for out-of-band signals beyond at least 100 MHz, and preferably (much) higher. The results plotted in figures 4.6 and 4.8 appear to support this. In both cases, the simplified analysis follows the correct trend for frequencies close to 1 GHz. This highlights a shortcoming of the proposed method, with regard to its range of applicability. It may be used only well into the out-of-band region, rather than from its onset, as defined by (3.79). It is, therefore, unsuitable to calculate the latter, as the open loop gain of the amplifier is still relatively high at that frequency and the assumption that the system may be considered in open loop is no longer valid.

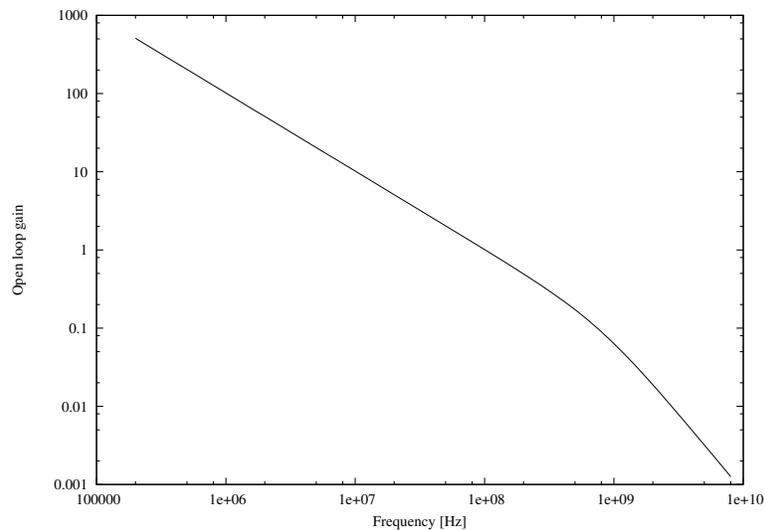


Figure 4.9: Open loop gain of the evaluated amplifier.

4.5 Conclusions

A method is proposed for simplified non-linear analysis of intermodulation-based out-of-band interference in negative-feedback amplifiers. It attempts to isolate the dominant signal processing mechanisms across the frequency range of interest in order to achieve the highest degree of simplicity. By definition, it is based on a number of approximations, so its predictions are by no means as accurate as the Volterra series approach, or a SPICE model simulation. However, the proposed method does predict the correct trends, which makes it useful for a quick initial estimation and evaluation of non-linear effects. Due to the limited set of parameters it considers, it makes it easier to gain insight into the non-linear interactions in the circuit and focus on the dominant factors. The assumed absence of feedback at high frequencies simplifies the analysis significantly, compared to the Volterra series treatment outlined in Chapter 3.

Chapter 5

Design for immunity

“In the middle of difficulty lies opportunity.”

Albert Einstein

The text so far outlines the mechanism of out-of-band interference in negative-feedback amplifiers and the most commonly used methods to alleviate the issue. An optimised non-linear small-signal model is developed in Chapter 3 to represent the active devices in an amplifier circuit. Circuit analysis is carried out using the Volterra series, and the dominant distortion path is identified. A reduced complexity analytical method is proposed in Chapter 4, which simplifies the calculations significantly. This chapter attempts to expand on the existing design techniques for reducing the susceptibility to out-of-band interference outlined in Chapter 2. New approaches are suggested, such as frequency-dependent local feedback and non-linear local-feedback compensation. All solutions focus on reducing the non-linear distortion signal products in the first stage of the amplifier, since this stage is found to be its most susceptible part.

5.1 Pole positions and interference

Instead of introducing additional frequency selectivity in order to deal with out-of-band interference, the inherent frequency selectivity of the active devices in a circuit can be exploited. The active devices possess a certain finite bandwidth, which, in turn, limits the maximally attainable bandwidth of the circuit constructed with them. A negative-feedback amplifier of finite bandwidth comprises a certain amount of poles and zeroes. The position of these, as encountered by the input signal of the system, is dependent on the system’s loop gain at DC. For low values of the loop gain, poles tend to their “open loop” positions, i.e., where they would be if the feedback network was disconnected from the input. As the loop gain increases, the poles appear to move along the root locus and are found at their “system” positions [17]. The transfer function of the input

signal to the output of the amplifier is based on the system poles. However, this is not the case for the signal at the input of the first amplifier stage, denoted by e in Figure 3.4, which is the sum of the input signal and the output of the negative-feedback network. The transfer function of e to the output of the amplifier is equal to the gain of the amplifying section and is, therefore, determined by the open loop poles. Since the signal level at the input of the first stage is ultimately responsible for the distortion products of the entire amplification chain, the poles of the system are considered in open loop. It can be shown that certain pole configurations yield negative-feedback amplifiers with increased immunity to out-of-band interference.

5.1.1 Loop versus system poles

Consider a frequency-dependent negative-feedback configuration. Without loss of generality, let the system have a Butterworth transfer function, or one that could be brought to Butterworth through frequency compensation. This accounts for the dominant subset of (baseband) negative-feedback amplifiers and will be the focus of this investigation. Let the amplifier comprise two dominant

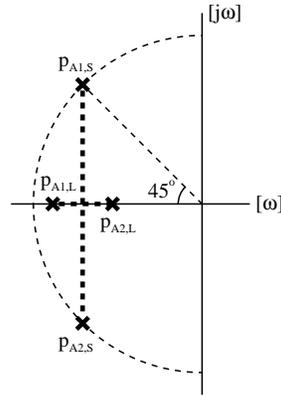


Figure 5.1: Pole-zero diagram and root locus of a two-pole system.

poles, p_{A1} and p_{A2} , and no (dominant) zeroes, as shown in the pole-zero diagram of Figure 5.1. The root locus is represented by the thick dotted line in the figure and depicts how the poles move from the open loop positions, $p_{A1,L}$ and $p_{A2,L}$, to the system positions, $p_{A1,S}$ and $p_{A2,S}$. The input signal of the system will encounter poles at $p_{A1,S}$ and $p_{A2,S}$, while for the input signal of the amplification chain the poles will be observed at $p_{A1,L}$ and $p_{A2,L}$. Let the amplifier be implemented with two non-linear frequency-dependent stages, each of which accounts for one of its poles, and a feedback network that is frequency independent. A schematic of the system is shown in Figure 5.2. There, stages \tilde{A}_1 and \tilde{A}_2 contribute poles p_{A1} and p_{A2} , respectively. The simplified approach

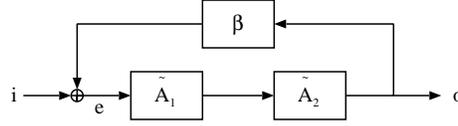


Figure 5.2: Schematic of a two-pole non-linear negative-feedback amplifier.

developed in Chapter 4 is used to analyse the amplifier, since identifying the general trends is sufficient to illustrate this example. Each stage is represented using the model shown in Figure 4.1. An out-of-band interference signal is applied at the input, i . As outlined in Section 4.2.2, it is assumed that the loop gain of the system at the frequency of the interference is sufficiently low, so that the input signal of the amplifier essentially appears unmodified at the input of the first stage, i.e., $e \approx i$. So, for out-of-band frequencies, the amplifier can be approximated by the schematic shown in Figure 5.3. This means that the

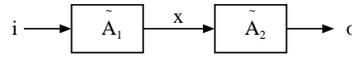


Figure 5.3: Equivalent topology of the amplifier for out-of-band interference signals.

transfer function of the input signal to the output tends to the transfer function of the forward gain section, $\tilde{A}_1\tilde{A}_2$, and can be regarded as a function of the loop poles.

5.1.2 Filtering of the first stage pole

Let an out-of-band interference signal consisting of two discrete frequencies, ω_α and ω_β , be present at the input, i . The amplitude, \hat{x}_α , of the harmonic component of frequency ω_α appearing at Node x may be derived from (4.10) and is given by:

$$\hat{x}_\alpha = \frac{N_{1,A1}}{\left|1 + \frac{j\omega_\alpha}{p_{A1}}\right|} \hat{i}_\alpha + \frac{N_{3,A1}}{\left|1 + \frac{j\omega_\alpha}{p_{A1}}\right|^3} \hat{i}_\alpha^3 + \dots \quad (5.1)$$

Using (5.1), \hat{x}_β can be determined similarly. Using (4.10) and (5.1), the amplitude, \hat{o}_α , of the signal component of frequency ω_α at the output node, o , is calculated, as shown in (5.2). The latter may also be used to derive \hat{o}_β .

$$\hat{o}_\alpha = \frac{N_{1,A1}N_{1,A2}}{\left|1 + \frac{j\omega_\alpha}{p_{A1}}\right| \left|1 + \frac{j\omega_\alpha}{p_{A2}}\right|} \hat{i}_\alpha + \frac{N_{3,A1}N_{1,A2}}{\left|1 + \frac{j\omega_\alpha}{p_{A1}}\right|^3 \left|1 + \frac{j\omega_\alpha}{p_{A2}}\right|} \hat{i}_\alpha^3 + \frac{N_{1,A1}^3N_{3,A2}}{\left|1 + \frac{j\omega_\alpha}{p_{A1}}\right|^3 \left|1 + \frac{j\omega_\alpha}{p_{A2}}\right|^3} \hat{i}_\alpha^3 + \dots \quad (5.2)$$

Due to the non-linear behaviour of \tilde{A}_1 , intermodulation products of the input signals appear at x . According to (4.11), the magnitude of the intermodulation product ϵ at frequency $\omega_\gamma = |\omega_\alpha - \omega_\beta|$ appearing at x is as follows:

$$\hat{\epsilon}_\gamma = \frac{N_{2,A1}}{\left|1 + \frac{j\omega_\alpha}{p_{A1}}\right| \left|1 + \frac{j\omega_\beta}{p_{A1}}\right|} \hat{i}_\alpha \hat{i}_\beta + \frac{N_{4,A1}}{\left|1 + \frac{j\omega_\alpha}{p_{A1}}\right|^3 \left|1 + \frac{j\omega_\beta}{p_{A1}}\right|} \cdot \frac{3\hat{i}_\alpha^3 \hat{i}_\beta}{2} + \frac{N_{4,A1}}{\left|1 + \frac{j\omega_\alpha}{p_{A1}}\right| \left|1 + \frac{j\omega_\beta}{p_{A1}}\right|^3} \cdot \frac{3\hat{i}_\alpha \hat{i}_\beta^3}{2} + \dots \quad (5.3)$$

The amplitude, $\hat{\epsilon}_{\gamma,in}$, of the input-referred signal at frequency ω_γ is derived using (4.15) and the first term of (4.10):

$$\hat{\epsilon}_{\gamma,in} = \frac{N_{2,A1} \left|1 + \frac{j\omega_\gamma}{p_{A1}}\right|}{N_{1,A1} \left|1 + \frac{j\omega_\alpha}{p_{A1}}\right| \left|1 + \frac{j\omega_\beta}{p_{A1}}\right|} \hat{i}_\alpha \hat{i}_\beta + \frac{N_{4,A1} \left|1 + \frac{j\omega_\gamma}{p_{A1}}\right|}{N_{1,A1} \left|1 + \frac{j\omega_\alpha}{p_{A1}}\right|^3 \left|1 + \frac{j\omega_\beta}{p_{A1}}\right|} \cdot \frac{3\hat{i}_\alpha^3 \hat{i}_\beta}{2} + \frac{N_{4,A1} \left|1 + \frac{j\omega_\gamma}{p_{A1}}\right|}{N_{1,A1} \left|1 + \frac{j\omega_\alpha}{p_{A1}}\right| \left|1 + \frac{j\omega_\beta}{p_{A1}}\right|^3} \cdot \frac{3\hat{i}_\alpha \hat{i}_\beta^3}{2} + \frac{N_{2,A2} N_{1,A1} \left|1 + \frac{j\omega_\gamma}{p_{A1}}\right| \left|1 + \frac{j\omega_\gamma}{p_{A2}}\right|}{N_{1,A2} \left|1 + \frac{j\omega_\alpha}{p_{A2}}\right| \left|1 + \frac{j\omega_\beta}{p_{A2}}\right| \left|1 + \frac{j\omega_\alpha}{p_{A1}}\right| \left|1 + \frac{j\omega_\beta}{p_{A1}}\right|} \hat{i}_\alpha \hat{i}_\beta + \dots \quad (5.4)$$

Since ω_α and ω_β are out-of-band frequencies and, therefore, greater than either p_{A1} or p_{A2} , it is expected that:

$$\frac{1}{\left|1 + \frac{j\omega_{\{\alpha,\beta\}}}{p_{\{A1,A2\}}}\right|^2} \ll 1, \quad (5.5)$$

while ω_γ is typically (much) lower than the system poles, so that the following applies:

$$\left|1 + \frac{j\omega_\gamma}{p_{\{A1,A2\}}}\right| \approx 1. \quad (5.6)$$

The above implies that for moderate magnitudes of the out-of-band interference signal one can safely conclude that (5.4) reduces to:

$$\hat{\epsilon}_{\gamma,in} \approx \frac{N_{2,A1}}{N_{1,A1} \left|1 + \frac{j\omega_\alpha}{p_{A1}}\right| \left|1 + \frac{j\omega_\beta}{p_{A1}}\right|} \hat{i}_\alpha \hat{i}_\beta. \quad (5.7)$$

Analysis of (5.7) suggests that the loop pole of the first stage of a negative-feedback amplifier is predominantly responsible for determining the susceptibility to out-of-band interference of the entire system. It seems, therefore, beneficial to place the stage with the lowest pole first in the amplifying chain, so as to obtain better immunity. Alternatively, the pole product of the system can be distributed sufficiently asymmetrically, so that the stage with the lowest pole appears at the input. Combined with maintaining the original loop

gain, this would ensure reduced susceptibility to out-of-band interference and, at the same time, conserve the maximum attainable bandwidth of the amplifier. While arbitrary distribution of the loop gain pole product would not influence the bandwidth of the system, other aspects, such as noise and distortion, might be affected (adversely). Due consideration must, therefore, be given to possible trade-offs.

The above conclusion could be applied to the decision process in structured electronic design. There, noise optimisation is carried out on the first stage of a negative-feedback amplifier. For a bipolar transistor common-emitter stage, the equivalent input noise power spectral density typically resembles the curve shown in Figure 5.4 [57, 58]. The noise density, S_N , is a function of the col-

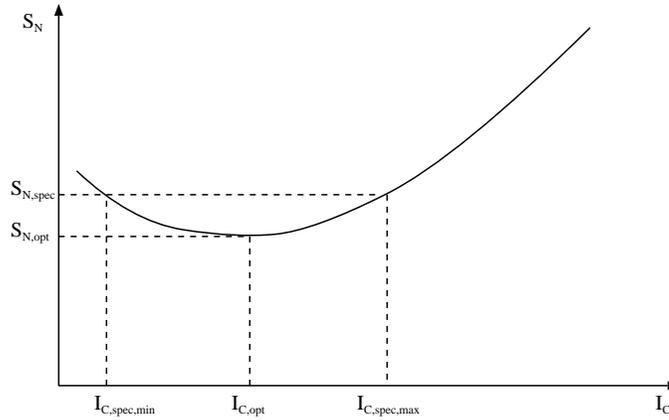


Figure 5.4: Typical BJT equivalent input-referred noise as a function of the collector bias current.

lector current, I_C , and has a minimum value, $S_{N,opt}$, at bias point $I_{C,opt}$ [17]. It can be observed that for noise power density specification $S_{N,spec}$, such that $S_{N,spec} > S_{N,opt}$, there exists a range of the collector bias current, $I_{C,spec,min}$ to $I_{C,spec,max}$, for which the specification would be met or exceeded. Assuming that the source impedance remains fixed, this gives the designer some freedom in choosing I_C , which is normally set to $I_{C,opt}$ for robustness. At a later stage of the design process, the LP product may need to be increased in order to achieve a certain bandwidth. In such cases, the designer may either choose to increase the bias current of the first stage or to add an extra stage. Increasing the collector bias current of the first stage to a value between $I_{C,opt}$ and $I_{C,spec,max}$, so as not to violate the noise performance requirement, would generally increase the frequency of the system pole it contributes but decrease that of the corresponding loop pole. This is expected to improve the out-of-band interference immunity of the system, as suggested by (5.7).

5.1.3 Example

A two-stage BJT negative-feedback amplifier is investigated in order to verify the theory and conclusions outlined in the previous section. The circuit of the amplifier is shown in Figure 5.5. A current-to-current transfer function

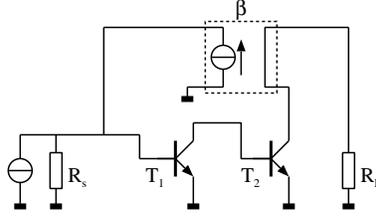


Figure 5.5: Circuit of the investigated amplifiers.

is implemented with a gain of $\frac{1}{\beta}$ in the pass band, where $\beta = 0.2$. Apart from defining the gain, the controlled source β also provides inversion in order to complete the negative-feedback loop. It is assumed that each stage of the amplifier contributes one dominant pole. For the first stage, this is calculated by considering R_s and the equivalent r_π and C_π of T_1 . The resulting pole lies at approximately 1.25 GHz. The pole of T_2 is similarly found to be at 2.6 MHz. This large difference allows lowering the first stage pole without significantly affecting the stability of the circuit. The DIMES03 npn2x1 device ($f_t = 1.4$ GHz, $\beta = 105$ at $I_C = 10 \mu\text{A}$ and $V_{CE} = 1$ V) is used for both T_1 and T_2 . The DC gain of each stage is set as the product of its base-emitter resistive component and its transconductance. Using these values, the forward gain chain is represented by the model developed in Section 4.1, as shown in Figure 5.2. The resulting open loop gain of the amplifier is plotted in Figure 5.6 and compared to a simulation of the full transistor model. After applying feedback, the transfer function of the amplifier is obtained using the non-linear frequency-dependent model and is likewise plotted in the figure. The corresponding result from the full transistor model simulation is also included.

In this example, the resistive component of the input impedance of T_1 is dominated by the source resistor, R_s . A convenient way to lower the pole of the first stage, while retaining the same LP product, is to scale up the size (and bias current) of the input transistor. This decreases the frequency of the first stage pole by the scaling factor. Assuming that the current density is kept the same, the transconductance of T_1 and, therefore, the DC loop gain are increased by the same factor. The size of the input transistor is tripled, which, according to (5.7), should result in a reduction of the output IM_2 figure of approximately an order of magnitude. The second-order intermodulation product predicted by (5.7) is plotted in Figure 5.7 for both the reference amplifier and that with the lowered input pole. The transistor circuits of the reference amplifier as well as the correspondingly modified variant are simulated with a two-tone signal at the input. The amplitude of the detected output signal at the difference frequency is

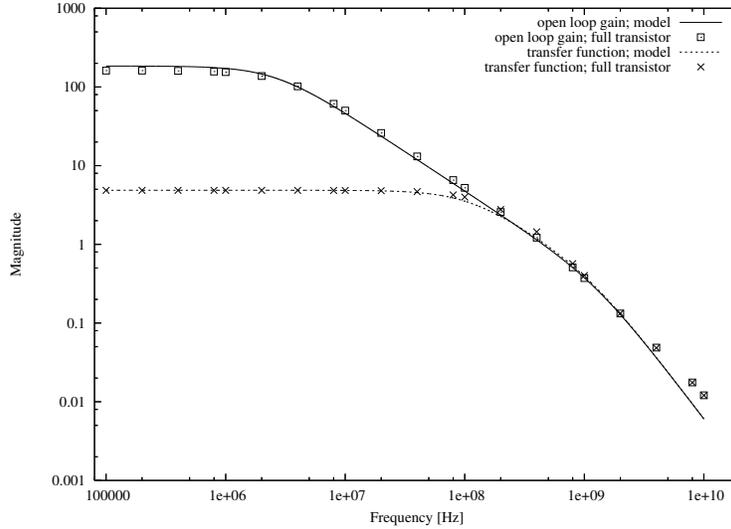


Figure 5.6: Transfer function and loop gain of the amplifier.

also shown in the figure. The difference frequency is chosen as high as possible, i.e., at 100 MHz, so as to minimize the simulation time, while remaining in the band of the amplifier. The simulation result appears to agree with the one derived from the model. There is a roughly constant offset between the predicted IM_2 value and that obtained from the full transistor model. This is an expected shortcoming of the simplified approach, as demonstrated in sections 4.4.1 and 4.4.2. Nevertheless, both the trend and the relative improvement factor are in agreement, which implies that the approximation of (5.7) is valid and can be usefully applied to the design of amplifiers with reduced susceptibility to out-of-band interference.

5.2 Local feedback

As discussed in Chapter 2, the sensitivity of a negative-feedback amplifier to out-of-band interference may be lowered by applying local feedback to individual components or larger sub-circuits. Consider a general case of local feedback in a negative-feedback configuration consisting of frequency-dependent non-linear forward gain stages $\tilde{A}_1(j\omega)$, $\tilde{A}_2(j\omega)$, etc., and feedback factor β depicted in Figure 5.8. As derived in Chapter 3, the input stage of a negative-feedback amplifier characterises its susceptibility to out-of-band interference. Local feedback of $\tilde{A}_1(j\omega)$ is, therefore, considered here. This is implemented through a linear gain β_{local} . Two situations are considered subsequently: $\beta_{local} > 0$, i.e., local feedback is present, and $\beta_{local} = 0$, i.e., local feedback is absent. Let $Y(\omega)$ be the frequency-dependent attenuation factor relating the respective magni-

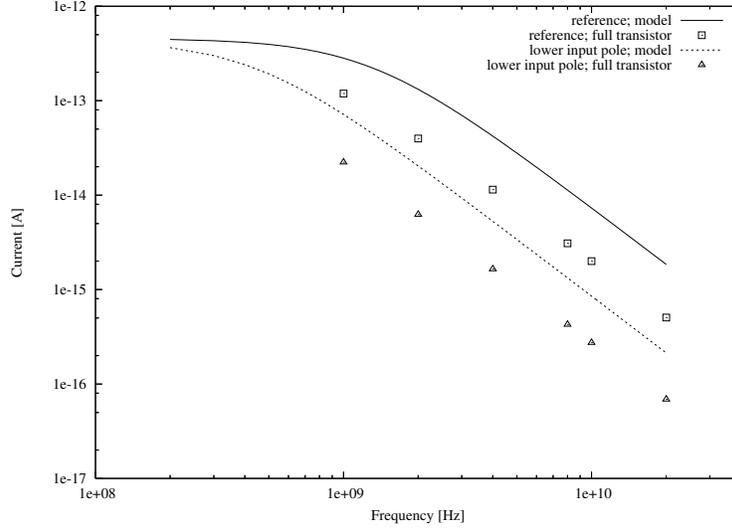


Figure 5.7: Calculated and simulated IM_2 current for the two amplifier variants.

tudes $|X_{LF}(j\omega)|$ and $|X_{NOLF}(j\omega)|$ of the signal at Node x in each of the two configurations. Then, for a frequency ω_α , the following applies:

$$\frac{|X_{LF}(j\omega_\alpha)|}{|X_{NOLF}(j\omega_\alpha)|} = Y(\omega_\alpha). \quad (5.8)$$

According to (4.15) and (4.11), for an out-of-band signal consisting of two tones of frequencies ω_α and ω_β it holds:

$$\hat{x}_{\gamma,LF} \approx \frac{Y(\omega_\alpha)Y(\omega_\beta)N_{2,A1}}{N_{1,A1} \left|1 + \frac{j\omega_\alpha}{p}\right| \left|1 + \frac{j\omega_\beta}{p}\right|} \hat{x}_{\alpha,NOLF} \hat{x}_{\beta,NOLF}, \quad (5.9)$$

$$\hat{x}_{\gamma,NOLF} \approx \frac{N_{2,A1}}{N_{1,A1} \left|1 + \frac{j\omega_\alpha}{p}\right| \left|1 + \frac{j\omega_\beta}{p}\right|} \hat{x}_{\alpha,NOLF} \hat{x}_{\beta,NOLF}. \quad (5.10)$$

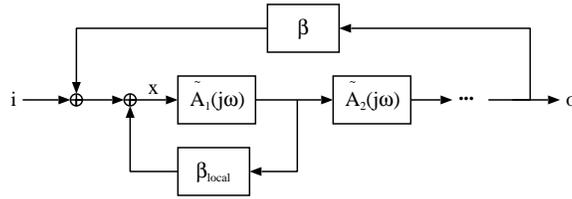


Figure 5.8: Local feedback in a negative-feedback configuration.

The equivalent input-referred signal due to $\hat{x}_\gamma \cos(\omega_\gamma t)$ can be derived using (4.15). Taking the quotient of the thus obtained \hat{i}_γ for each case results in:

$$\frac{\hat{i}_{\gamma,LF}}{\hat{i}_{\gamma,NOLF}} = Y(\omega_\alpha)Y(\omega_\beta). \quad (5.11)$$

Substituting the attenuation factors in (5.11) with (5.8) yields:

$$\frac{\hat{i}_{\gamma,LF}}{\hat{i}_{\gamma,NOLF}} = \frac{\hat{x}_{\alpha,LF}\hat{x}_{\beta,LF}}{\hat{x}_{\alpha,NOLF}\hat{x}_{\beta,NOLF}}. \quad (5.12)$$

If ω_γ is sufficiently small relative to ω_α and ω_β then $\hat{x}_\alpha \approx \hat{x}_\beta$ for $\hat{i}_\alpha = \hat{i}_\beta$, and the following applies:

$$\frac{\hat{i}_{\gamma,LF}}{\hat{i}_{\gamma,NOLF}} \approx \left(\frac{\hat{x}_{\alpha,LF}}{\hat{x}_{\alpha,NOLF}} \right)^2. \quad (5.13)$$

Equations (5.12) and (5.13) quantify the effect on susceptibility to out-of-band interference of local feedback in the first stage of a negative-feedback amplifier. Note that this (approximate) result is achieved through linear analysis of the circuit under investigation thereby eliminating the need for a more involved non-linear treatment. This can simplify the circuit analysis and allow immunity consideration at an early stage of the design process.

5.2.1 Frequency-dependent local feedback

As already mentioned, applying local feedback in a negative-feedback amplifier degrades its distortion performance unless performed at a specific location. Typically, the linearity of the amplifier is determined by the stage experiencing the largest signal swing. For topologies with uniform gain along the signal chain this is the output stage [49]. However, to address the susceptibility to out-of-band interference, local feedback should be applied to the input stage. This is generally expected to be detrimental to the in-band distortion performance. To avoid that and still benefit from the advantages of local feedback at out-of-band frequencies, it is possible to introduce frequency selectivity to the local-feedback signal transfer. An example of this approach is shown in Figure 5.9 for a degenerated bipolar transistor stage. The resistive degeneration of Figure 5.9a will function at all frequencies, with the corresponding potential loss of performance in the base band. Substituting the resistor by an inductor (Figure 5.9b) could ensure that the local feedback is insignificant at low frequencies and becomes operational only for out-of-band signals. Other implementations of the degeneration impedance that enhance the frequency selectivity or avoid the use of an inductor are possible [60]. In general, the resulting filtering action serves to keep the information signal out of the local-feedback loop, rather than preventing the interference from reaching the non-linear device.

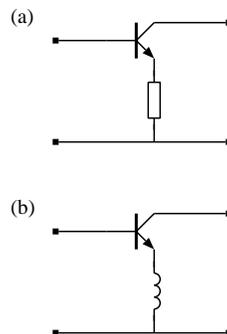


Figure 5.9: Resistive (a) and inductive (b) degeneration of a common-emitter stage.

5.2.2 Filtering versus local feedback

It can be demonstrated that in cases where an active (sub)circuit is being protected by a filter, some of the gain of the former can be expended to augment the action of the latter. This approach may be useful where limited resources are available, such as chip area or component cost. In effect, it constitutes a transition from filtering to frequency-dependent local feedback. The circuits of Figure 5.10 serve as an example. There the filter is represented by a complex impedance Z . It is assumed that this consists of capacitances, inductances and resistances, so that the real and imaginary parts of Z are positive. In general,

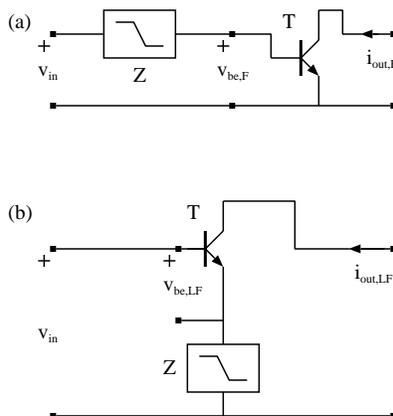


Figure 5.10: Transistor stage with input filter (a) and frequency dependent local feedback (b).

the role of Z is to modify the signal transfer function from the input voltage,

v_{in} , to the controlling voltage of the transistor (v_{be}). This transfer should be reduced (ideally to zero) at out-of-band frequencies, while in-band signals should remain unaffected. Consider the circuit of Figure 5.10a where the filter is placed in series with the input. Let Z_{be} be the input impedance of the transistor, i.e., the impedance between its base and emitter terminals. The controlling voltage $v_{be,F}$ can be expressed as function of the input voltage, v_{in} , according to:

$$v_{be,F} = \frac{Z_{be}}{Z + Z_{be}} v_{in}, \quad (5.14)$$

i.e., v_{in} is simply divided between Z and Z_{be} . In the circuit of Figure 5.10b, Z defines the local-feedback coefficient. The transfer between the input and the controlling voltage $v_{be,LF}$ is given by:

$$v_{be,LF} = \frac{Z_{be}}{Z + Z_{be}} (v_{in} - i_{out,LF} Z). \quad (5.15)$$

A first-order approximation of the input impedance, Z_{be} , is the combination of the equivalent hybrid- π model capacitance, C_π , and resistance, r_π , i.e., $Z_{be} = C_\pi || r_\pi$. The output current of the transistor can be regarded as the product of the controlling voltage, v_{be} , and the transconductance, g_m . Under these assumptions, (5.14) can be rewritten as:

$$\frac{v_{be,F}}{v_{in}} = \frac{r_\pi}{Z + r_\pi + sr_\pi C_\pi Z}. \quad (5.16)$$

Similarly, (5.15) then yields:

$$\frac{v_{be,LF}}{v_{in}} = \frac{r_\pi}{Z + g_m r_\pi Z + r_\pi + sr_\pi C_\pi Z}. \quad (5.17)$$

Consider the ratio between the two transfers:

$$\frac{v_{be,F}}{v_{be,LF}} = \frac{Z + r_\pi + sr_\pi C_\pi Z}{Z + g_m r_\pi Z + r_\pi + sr_\pi C_\pi Z} \approx \frac{Z + r_\pi + sr_\pi C_\pi Z}{(1 + g_m r_\pi) Z + r_\pi + sr_\pi C_\pi Z}. \quad (5.18)$$

For positive real and imaginary parts of Z , the value of the modulus of (5.18) is always less than or equal to unity. This demonstrates how the impact of the filtering impedance can be increased by including it in a local negative-feedback loop.

5.2.3 Example

To illustrate the above and verify the conclusions of (5.12) and (5.13), the effect of local feedback in a practical case is evaluated. The circuit depicted in Figure 5.11 is analysed. This implements a negative-feedback voltage amplifier with local feedback, Z_{LF} , in the first (non-linear) stage. The amplifier consists of two BJT stages and a linear voltage controlled voltage source, E , to determine the gain factor and provide inversion. Biasing is present but omitted from the circuit

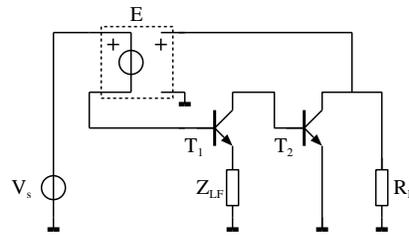


Figure 5.11: Example of a negative-feedback amplifier with local feedback.

diagram in the figure. Several alternative situations are investigated. The circuit without local feedback, i.e., $Z_{LF} = 0$ is used as a base for comparison. The impedance Z_{LF} is consequently made either resistive ($Z_{LF} = R_{LF}$) or inductive ($Z_{LF} = j\omega L_{LF}$). Resistive local feedback is active over the entire frequency range considered and may have an adverse effect on the overall in-band distortion performance unless it is applied to the stage dominating the non-linear behaviour of the system. This is not the case for an inductive Z_{LF} which is essentially a short-circuit at DC and will not influence the circuit at low frequencies. It has the added advantage that its impact becomes increasingly noticeable with frequency. The value of the inductor L_{LF} is chosen such that its impedance is equal to the impedance of R_{LF} at approximately 1 GHz. Figure 5.12 shows

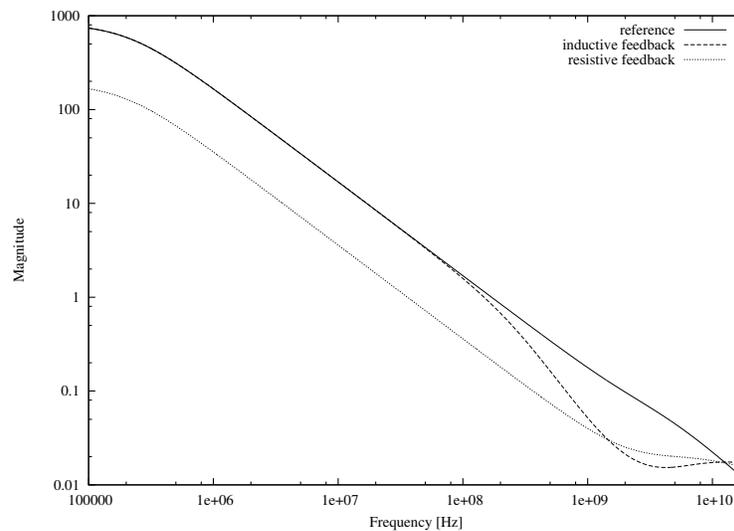


Figure 5.12: Loop gain of the circuits investigated.

the loop gain of the unmodified circuit as well as that of the circuits with

resistive and inductive local feedback. From the plots it can be observed that resistive local feedback results in a sustained decrease of loop gain throughout the evaluated frequency range. The loop gain of the circuit with inductive local feedback is unaffected in the base band. As expected, it coincides with that of the circuit with resistive local feedback around 1 GHz. The transfer functions of the different amplifier variants are given in Figure 5.13. The value of the

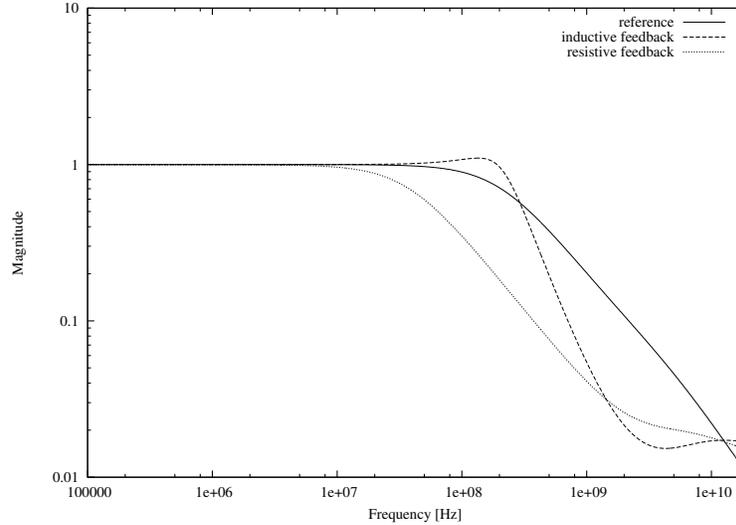


Figure 5.13: Transfer functions of the circuits investigated.

feedback coefficient E is set to unity, so that a voltage gain of 1 is obtained. The bandwidth of the circuit with inductive local feedback is roughly the same as the reference. Due to the lower in-band loop gain, a lower bandwidth is obtained for the circuit with resistive local feedback.

A two-tone signal consisting of frequencies ω_α and ω_β is applied at the input of each amplifier and swept between 100 MHz and 10 GHz. The difference frequency, ω_γ , where $\omega_\gamma = |\omega_\alpha - \omega_\beta|$, is chosen such that it falls within the bandwidth of the amplifiers. The input-referred magnitude, \hat{i}_γ , of the signal at the difference frequency is determined from a simulation of the full transistor model. This is plotted in Figure 5.14 for each amplifier variant. From the plots it can be observed that the circuit with inductive local feedback behaves similarly to the reference at in-band frequencies, and matches the performance of the circuit with resistive local feedback at 1 GHz, as expected. Beyond 1 GHz, due to the steadily increasing impedance of the inductor, it gives the lowest second-order intermodulation product and, therefore, the best immunity to out-of-band interference.

To verify the prediction of (5.13), the ratio is taken between the IM_2 product of the control circuit and that of the circuits with resistive and inductive Z_{LF} .

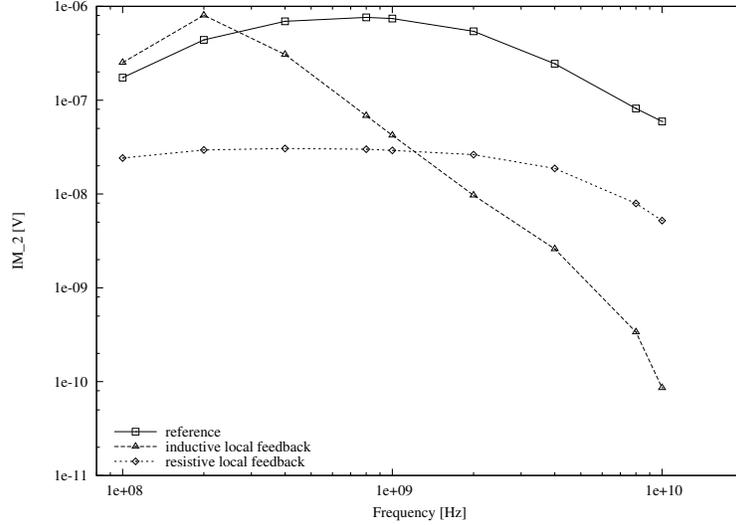


Figure 5.14: Simulated results for the different amplifier variants.

This is compared to the square of the ratio $\hat{x}_{\alpha,LF}/\hat{x}_{\alpha,NOLF}$ obtained from a linear (i.e., AC) analysis of the amplifiers. The result is plotted in Figure 5.15. Since the relationship with the control circuit is depicted, values above unity represent higher levels of distortion and, therefore, undesirable behaviour. Values below unity, particularly in the out-of-band region, indicate an enhanced immunity to interference. The results obtained with both methods show close agreement and verify the inferences made in (5.12) and (5.13).

5.3 Dummy stage placement considerations

As outlined in Section 2.2.5, it is possible to base a distortion cancellation scheme on single-ended input drive while accepting the fact that the circuitry involved is not ideal and will be influenced by parasitics. A form of error feed-forward is used which is also known as dummy circuit compensation. In this case, the focus shifts from improving the performance of a symmetrical circuit to replicating it as faithfully as possible, together with its associated non-idealities. This does come at a price, however, as additional functionality has to be implemented. To keep the amount of extra circuitry to a minimum, typically only the first stage of an amplifier is replicated [74]-[76]. This scheme is shown topologically in Figure 5.16. There, \tilde{M} is an arbitrary non-linear polynomial representing the first stage (or, without loss of generality, a larger segment) of the circuit. The remaining stages of the forward gain are represented by \tilde{N} . In order not to affect the stability of the entire system, the compensation should not introduce

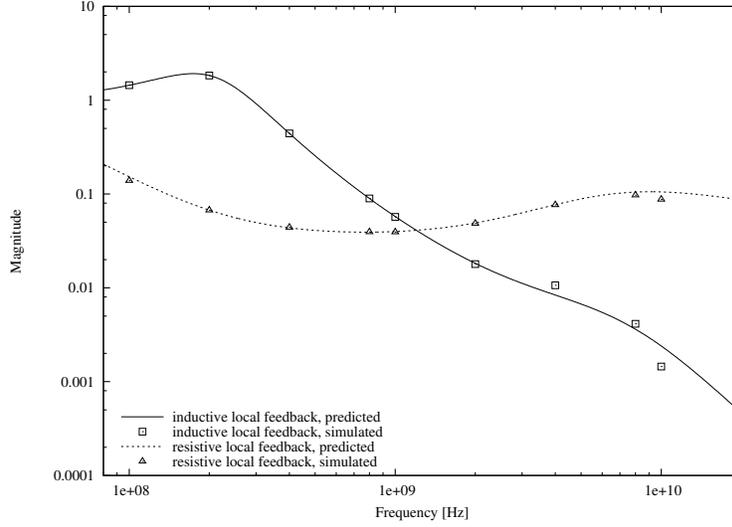


Figure 5.15: Predicted and simulated results for the intermodulation ratio.

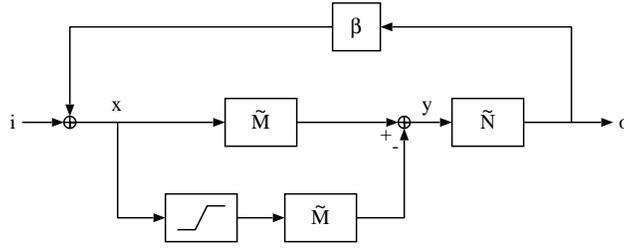


Figure 5.16: Negative-feedback amplifier with an input dummy stage.

any dominant poles to the negative-feedback loop. To evaluate that, we assume $M(s)$ to be the small-signal Laplace domain transfer function of \tilde{M} . Taking $F(s)$ as the frequency response of the high-pass filter, we can obtain the overall compensated stage transfer function from Node x to Node y :

$$Y(s) = X(s) [M(s) - M(s)F(s)]. \quad (5.19)$$

Taking both $N(s)$ and $F(s)$ as arbitrary frequency domain functions, of the form

$$M(s) = \frac{\sum_0^m a_m s^m}{\sum_0^n b_n s^n}, \quad a_m, b_n \in \mathfrak{R}, \quad m, n \in \mathfrak{N}, \quad (5.20)$$

and

$$F(s) = \frac{\sum_0^p c_p s^p}{\sum_0^q d_q s^q}, \quad \begin{array}{l} c_p, d_q \in \Re \\ p, q \in \mathbb{N} \end{array}, \quad (5.21)$$

respectively, the overall transfer function of the compensated stage assumes the form:

$$\frac{Y(s)}{X(s)} = \frac{\sum_0^m a_m s^m}{\sum_0^n b_n s^n} \cdot \frac{\sum_0^q d_q s^q - \sum_0^p c_p s^p}{\sum_0^q d_q s^q}. \quad (5.22)$$

Note that the second part of the right-hand side of (5.22) now defines a low-pass transfer, comprising the poles of the original high-pass filter. These poles also participate in the combined transfer function and, therefore, must be larger than the dominant loop poles.

Let us compare this situation with placing a filter in the negative-feedback loop between the input and the first stage, as discussed in Section 2.1.2. There, the inserted frequency-dependent circuit also participates in the transfer of the entire negative-feedback loop. Therefore, the additional poles it introduces should not be dominant, or the designed bandwidth of the amplifier will be affected. A low-pass transfer function is required, which admits the in-band information signal but prevents the out-of-band interference from reaching the input stage. The opposite is true for the dummy stage, where the desired filter characteristic is high-pass. There, the introduced frequency selectivity serves to block the in-band signal, while the out-of-band interference is allowed to propagate. Apart from having different stop bands, the filters that need to be implemented in each case can also differ in another respect. In a low-pass filter, the poles are generally concentrated at the high end of the conduction band, while in the case of a high-pass filter these are found around the low end of the conduction band. This means that in order to satisfy the condition for non dominance of filter poles, in otherwise identical circumstances, the filter required at the input of the negative-feedback loop needs to be steeper than that employed if a dummy stage is implemented. A high-pass filter might also be easier to integrate as chip area is typically at a premium. Of course, a dummy stage adds additional overhead in terms of circuitry, power consumption and noise, so a choice between the two methods remains an optimisation problem.

5.4 The complementary differential stage

As deduced from (2.15), the presence of a tail current source parasitic capacitance is a major contributing factor towards the deviation from the expected distortion behaviour of a differential stage. In an integrated circuit, the devices used for an amplifier stage and those in the biasing circuitry are likely to be of the same technology. Limited immunity performance gain can thus be achieved by optimisation of the biasing circuit for minimal parasitic capacitance. To overcome this problem, a topology is considered where the tail current bias source is eliminated by replacing it with a symmetrical complementary differential pair. This is shown schematically in Figure 5.17. Biasing is not included

in the schematic for clarity. The sensitive tail node is now connected to de-

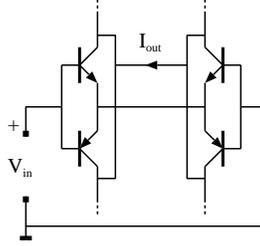


Figure 5.17: Principal circuit of the complementary differential stage.

vice terminals with minimal parasitic capacitance to ground/substrate, and it is expected that this arrangement results in improved distortion performance. The configuration of Figure 5.17 requires more voltage headroom and possibly a more complicated biasing circuit than a differential stage. It does, however, provide double the transconductance for the same supply current.

A complementary differential stage is set up, as shown in Figure 5.18, and simulated in order to compare its performance to that of the regular differential pair. To ensure the comparison is consistent, the same technology, stimuli and modelling of parasitic components is used as in the circuit of Figure 2.7. Similarly, transistors are biased at the same operating point with ideal voltage and current sources. These are omitted from the schematic in the figure to avoid clutter. A two-tone signal is applied at the input of the complementary

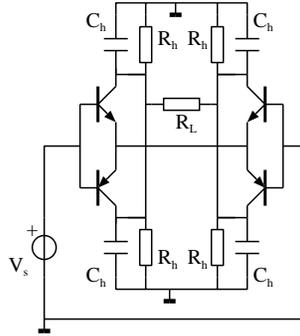


Figure 5.18: Experimental circuit of the complementary differential stage (biasing not shown).

differential stage. The same amplitude and frequency composition are chosen as with the setup of Figure 2.7. The circuit is simulated, and the second-order intermodulation product current through the load resistor, R_L , is determined. The results obtained are plotted against the frequency of the carrier, as shown

in Figure 5.19. The similarly obtained responses of the ordinary NPN and PNP

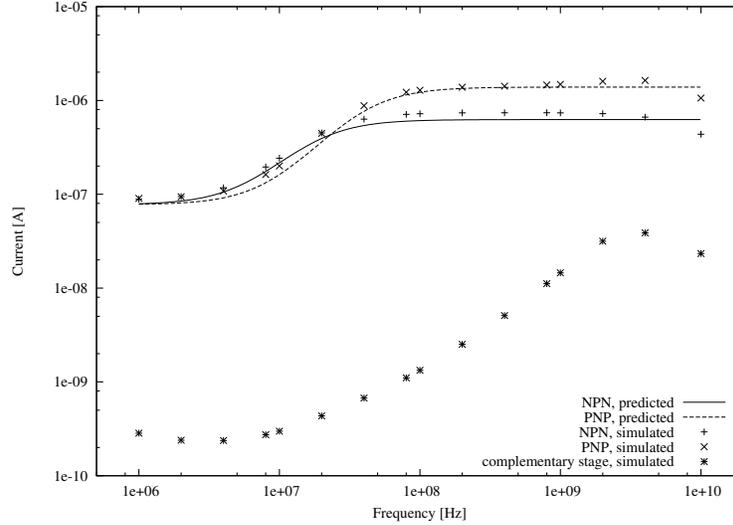


Figure 5.19: Simulated offset current of the complementary differential stage.

differential stages are also included in the figure for comparison. The simulation data indicates that the complementary differential stage achieves a lowering of even order distortion by at least an order of magnitude. This applies without taking into consideration its higher relative gain which would otherwise increase its effective linearity even further.

5.5 Non-linear local-feedback compensation

Consider a typical negative-feedback transimpedance amplifier, as shown in Figure 5.20. This topology is commonly used as a front-end amplifier in sensor interfaces processing current or charge [78]–[82]. It consists of an input differential stage, T_{1a} – T_{1b} , single-ended output stage, T_2 , and feedback resistor, R_f . The load impedance is represented by R_L . The biasing of the output stage is not shown and is assumed ideal. The differential stage at the input is expected to ensure a high IP_2 figure of the amplifier. However, due to parasitics and imperfections of the active devices, there will always be IP_2 degradation in practice, especially when going from single-ended to balanced configurations and vice versa. Various methods have been proposed to compensate for such second-order distortion effects, as discussed previously in Chapter 2. While the emphasis in these studies is invariably placed on ensuring that the differential output is free of down-converted distortion, the effect of the distortion on the input of the stage is often overlooked. Here, it will be shown that local feedback

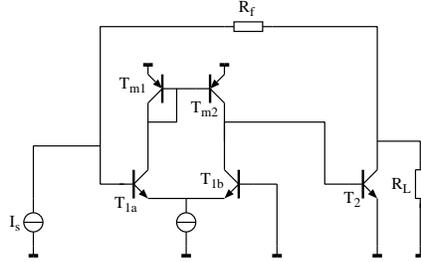


Figure 5.20: Circuit of negative-feedback amplifier.

of non-linear products in a differential stage is a prime contributor to the overall IM_2 distortion. Thus, a structural improvement in the baseband amplifier's immunity to out-of-band interference must address the design of the differential stage itself.

The Volterra series method is used to estimate the IM_2/IP_2 generated by the amplifier of Figure 5.20 in response to an out-of-band interferer. Since Volterra series analysis can result in expressions with a very large number of terms, especially when feedback is present, a simplified model is employed for the active devices in the circuit, as outlined in Section 3.1. This is shown in the amplifier equivalent circuit of Figure 5.21. PNP current mirror $T_{m1}-T_{m2}$ is replaced by an ideal current-controlled current source with input impedance R_e . The system will be represented as a set of admittance node equations, so the input current source is replaced by a voltage source, V_s , in series with the (large) source resistor, R_s . Using the admittance matrix, $\mathbf{Y}(s)$, of the circuit

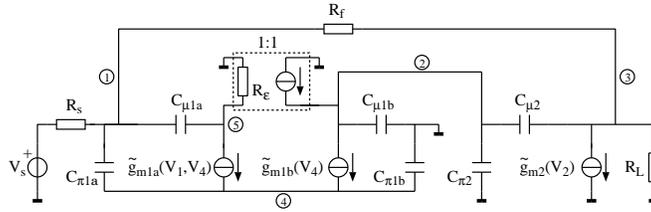


Figure 5.21: Equivalent circuit of the negative-feedback amplifier.

and its normalized input voltage linear current source vector, \mathbf{IN}_1 , given by:

$$\mathbf{IN}_1 = \begin{bmatrix} R_s^{-1} \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix}, \quad (5.23)$$

the linear Volterra kernel vector, $\mathbf{H}(s_1)$, of the system can be calculated from:

$$\mathbf{Y}(s_1) \times \mathbf{H}(s_1) = \mathbf{IN}_1. \quad (5.24)$$

In order to simplify the resulting expressions, we assume $R_e \rightarrow 0$ and $C_{\mu 2} \rightarrow 0$. After computing the first-order Volterra kernel, $\mathbf{H}(s_1)$, of the system, we obtain:

$$H_{1,1}(s_1) = 2H_{1,4}(s_1), \quad (5.25)$$

or

$$H_{1,1}(s_1) - H_{1,4}(s_1) = H_{1,4}(s_1). \quad (5.26)$$

In other words, the steady-state base-emitter voltages of the differential pair transistors are equal but have opposite signs. This is essential for the following analysis and will be referred to again later. The equality of (5.26) can also be determined directly from inspection of the circuit. From Kirchhoff's current law at Node 4, it follows that the current delivered by g_{m1a} and $C_{\pi 1a}$ must flow into g_{m1b} and $C_{\pi 1b}$. For a symmetrical input differential pair:

$$g_{m1a} = g_{m1b}, \quad (5.27)$$

$$C_{\pi 1a} = C_{\pi 1b}, \quad (5.28)$$

and all current sourced by g_{m1a} flows into g_{m1b} . All current flowing out of $C_{\pi 1a}$ is sunk by $C_{\pi 1b}$. This condition is fulfilled only if (5.26) is valid.

To study the interference scenario, a two-tone signal comprising discrete out-of-band frequency components ω_α and ω_β is applied at the amplifier input, such that

$$\omega_\alpha = \omega_\beta + \omega_\gamma, \quad (5.29)$$

where ω_γ represents the (low) in-band radian difference frequency and $s = j\omega$ (i.e., sinusoidal steady state). The second-order intermodulation product at ω_γ that appears at the output of the amplifier due to the interaction between ω_α and ω_β is given by $H_{2,3}(s_\alpha, -s_\beta)$. It is obtained from the second-order Volterra kernel, $\mathbf{H}(s_1, s_2)$, which is calculated using

$$\mathbf{Y}(s_1 + s_2) \times \mathbf{H}(s_1, s_2) = \mathbf{IN}_2, \quad (5.30)$$

where \mathbf{IN}_2 is the second-order non-linear current source vector

$$\mathbf{IN}_2 = \begin{bmatrix} 0 \\ -I_{NL2, g_{m1b}}(s_1, s_2) \\ -I_{NL2, g_{m2}}(s_1, s_2) \\ I_{NL2, g_{m1a}}(s_1, s_2) + I_{NL2, g_{m1b}}(s_1, s_2) \\ -I_{NL2, g_{m1a}}(s_1, s_2) \end{bmatrix}. \quad (5.31)$$

Individual non-linear current contributions are given by [9]:

$$I_{NL2, g_{m1a}}(s_1, s_2) = \frac{I_{C1a}}{2V_t^2} (H_{1,1}(s_1) - H_{1,4}(s_1)) \times (H_{1,1}(s_2) - H_{1,4}(s_2)), \quad (5.32)$$

$$I_{NL2,g_{m1b}}(s_1, s_2) = \frac{I_{C1b}}{2V_t^2} H_{1,4}(s_1) H_{1,4}(s_2), \quad (5.33)$$

$$I_{NL2,g_{m2}}(s_1, s_2) = \frac{I_{C2}}{2V_t^2} H_{1,2}(s_1) H_{1,2}(s_2). \quad (5.34)$$

If the transistors of the differential pair are biased identically, so that $I_{C1a} = I_{C1b} = I_{C1}$, then it follows from (5.26) that

$$I_{NL2,g_{m1a}}(s_1, s_2) = I_{NL2,g_{m1b}}(s_1, s_2) = I_{NL2,g_{m1}}(s_1, s_2) \quad (5.35)$$

with

$$I_{NL2,g_{m1}}(s_1, s_2) = \frac{I_{C1}}{2V_t^2} H_{1,4}(s_1) H_{1,4}(s_2). \quad (5.36)$$

Equation (5.30) must be solved in order to calculate $H_{2,3}(s_\alpha, -s_\beta)$:

$$\mathbf{H}(s_1, s_2) = \mathbf{Y}^{-1}(s_1 + s_2) \times \mathbf{IN}_2. \quad (5.37)$$

Note that \mathbf{IN}_2 can be represented as a linear combination of the non-linear current sources of each amplifier stage:

$$\mathbf{IN}_2 = \mathbf{IN}_{2,g_{m1}} + \mathbf{IN}_{2,g_{m2}}, \quad (5.38)$$

where, from (5.31) and (5.35),

$$\mathbf{IN}_{2,g_{m1}} = \begin{bmatrix} 0 \\ -I_{NL2,g_{m1}}(s_1, s_2) \\ 0 \\ 2I_{NL2,g_{m1}}(s_1, s_2) \\ -I_{NL2,g_{m1}}(s_1, s_2) \end{bmatrix} \quad (5.39)$$

and

$$\mathbf{IN}_{2,g_{m2}} = \begin{bmatrix} 0 \\ 0 \\ -I_{NL2,g_{m2}}(s_1, s_2) \\ 0 \\ 0 \end{bmatrix}. \quad (5.40)$$

From (5.37) and (5.38):

$$\mathbf{H}(s_1, s_2) = \mathbf{Y}^{-1}(s_1 + s_2) \times \mathbf{IN}_{2,g_{m1}} + \mathbf{Y}^{-1}(s_1 + s_2) \times \mathbf{IN}_{2,g_{m2}}. \quad (5.41)$$

$\mathbf{H}(s_\alpha, -s_\beta)$ can now be obtained by substituting ω_α and ω_β into equation (5.41). Since both ω_α and ω_β are out-of-band, the first stage is expected to yield the dominant non-linearity due to the low-pass characteristic of the amplification chain. We, therefore, concentrate on the first term of (5.41):

$$\mathbf{H}(s_\alpha, -s_\beta) \approx \mathbf{Y}^{-1}(s_\gamma) \times \mathbf{IN}_{2,g_{m1}}. \quad (5.42)$$

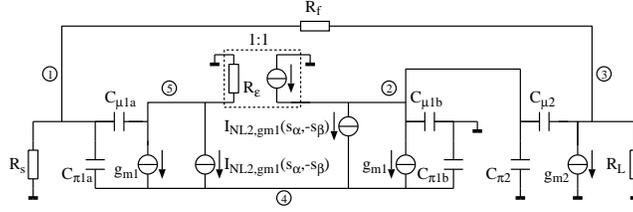


Figure 5.22: Input stage non-linear source equivalent circuit.

$I_{NL2,gm1}(s_\alpha, -s_\beta)$ is the non-linear current component of each of the differential pair transistors (5.35). Evaluating this equation to find $H_{2,3}(s_\alpha, -s_\beta)$ is equivalent to determining how $I_{NL2,gm1}$ contributes to the second-order intermodulation voltage, V_3 , at Node 3 in the equivalent circuit of Figure 5.22. Dependent sources g_{m1} and g_{m2} in Figure 5.22 are the respective linear transconductances associated with the collector currents of T_1 and T_2 in Figure 5.20. Two mechanisms through which the sources $I_{NL2,gm1}(s_\alpha, -s_\beta)$ affect the output node can be identified:

- *Mechanism 1*: Direct feed-through via nodes 2 and 5, i.e., from the output of the differential pair, to the output of the amplifier.
- *Mechanism 2*: Feedback of the second-order intermodulation voltage from Node 4 to Node 1. From Node 1 this signal passes directly through the feedback network to the output, or it reaches the output after being reprocessed by the amplification chain.

It can immediately be seen from Figure 5.22 that for R_e approaching zero, the current mirror delivers the same signal to Node 2 that is subtracted by $I_{NL2,gm1}(s_\alpha, -s_\beta)$ (i.e., *Mechanism 1*). As a result, no IM_2 voltage swing appears at Node 2. This compensation is absent from Node 4, where both non-linear currents are injected (i.e., *Mechanism 2*). The injected current divides between $C_{\pi1a}$ and $C_{\pi1b}$ and appears at the outputs of the devices through their transconductances. This non-linear, local feedback can disturb the symmetry of the differential pair and thereby allow a common-mode signal to propagate to the output of the amplifier. According to (5.26), the input signal divides exactly between the two transistors in the differential stage. Furthermore, since ideal transconductors are used in the model and the current mirror is also ideal, a purely differential-mode signal is sourced by the output of the stage. Therefore, the interferer drives and loads the differential stage with perfect symmetry. Despite that, its second-order products are not handled symmetrically, and a fraction of the non-linear distortion appears at the output of the circuit.

Under certain conditions, complete cancellation of the non-linear currents $I_{NL2,gm1}(s_\alpha, -s_\beta)$ occurs at Node 2 in Figure 5.22. For example, their combined contribution to V_3 can be brought to zero if these currents divide between

$C_{\pi 1a}$ and $C_{\pi 1b}$ after being injected into Node 4. Current division is achieved by replacing the short circuit at the (grounded) inverting input of the differential stage by an impedance (Z) of the appropriate value. Alternatively, it can be shown that for a particular I_{C1} - which is the collector bias current of each of the equally biased differential stage transistors - the components of $I_{NL2,gm1}(s_\alpha, -s_\beta)$ are distributed along the amplification chain in such a way that their contributions at the output node sum to zero. Such solutions will work for a particular frequency set $\omega_\alpha, \omega_\beta$, introduce additional noise due to the real part of Z , or fix the bias and limit the design freedom for the first stage. It is interesting to note that dividing the non-linear currents $I_{NL2,gm1}(s_\alpha, -s_\beta)$ equally between $C_{\pi 1a}$ and $C_{\pi 1b}$, where $I_{NL2,gm1a}(s_\alpha, -s_\beta) = I_{NL2,gm1b}(s_\alpha, -s_\beta)$ (i.e., retaining the symmetry of the differential pair) does not result in complete cancellation of the non-linear current components at the output of the amplifier in general. This is illustrated with the aid of the schematic shown in Figure 5.23.

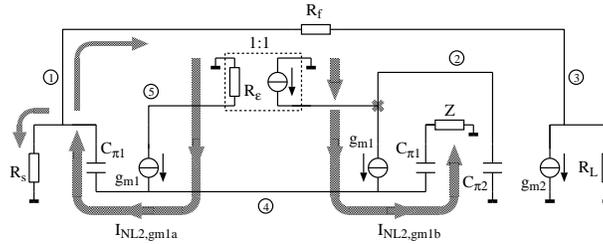


Figure 5.23: Fully symmetrical non-linear current distribution.

The non-linear current flow due to each transistor of the input differential pair is annotated. The 1:1 current mirror load ensures that perfect compensation occurs at Node 2. However, a portion of the current $I_{NL2,gm1}(s_\alpha, -s_\beta)$ injected into Node 1 is still able to reach the load via feedback resistor R_f . This is true for a single component implementation of Z , or if a dummy output stage and a symmetrical feedback network are used to realize impedance Z across a broader bandwidth. In both cases, it is possible to develop a differential signal between two internal nodes that is free of second-order intermodulation. However, we are interested in developing a single-ended output without passive baluns (e.g., avoiding use of a transformer balun to convert an internal, differential signal to a single-ended output).

A new method to reduce the undesired local feedback of even-order distortion components and IP_2 limitations in baseband amplifiers with single-ended input/output is proposed. The principle is illustrated in Figure 5.24. Unity-gain current mirrors $G_{1..4}$ copy all of the current components (linear and non-linear) at the outputs of the differential stage. Mirrors G_1 and G_2 pass the difference between the output currents on to the second stage. The non-linear currents are identical and common to both outputs, as indicated by arrows in Figure 5.24. Their difference is zero, which prevents these currents

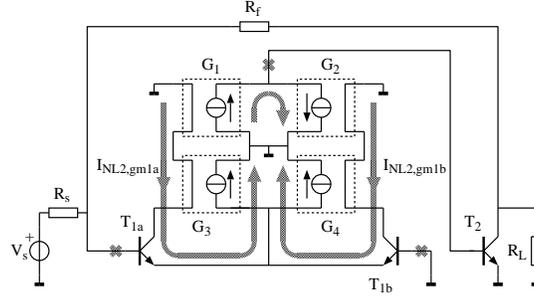
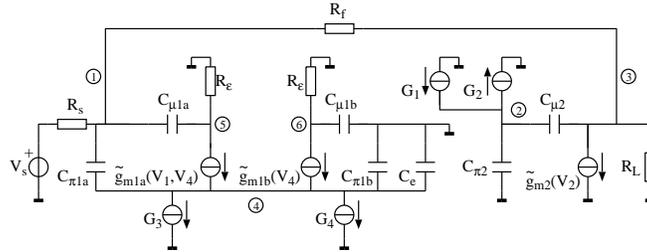


Figure 5.24: Proposed non-linear local-feedback compensation topology.

$I_{NL2,gm1a}(s_1, s_2) = I_{NL2,gm1b}(s_1, s_2)$ (5.35) from reaching the base of T_2 . The function of G_1 and G_2 is, therefore, analogous to the current mirror in Figure 5.20 and addresses *Mechanism 1* as outlined in the previous section. Additionally, G_3 and G_4 subtract the sum of the non-linear currents from the common node of T_{1a} and T_{1b} in the proposed circuit, thereby preventing any even-order voltages from developing at this node. This eliminates local feedback to the input through *Mechanism 2* (also outlined in the previous section). In the example of Figure 5.24, the non-linear currents are sensed at the collectors of the differential pair transistors T_{1a} and T_{1b} and then pulled from their emitters by G_3 and G_4 . Conceptually, it is possible to combine both sensing and feeding at the emitters of T_{1a} and T_{1b} by grounding the emitters. This results in a push-pull pair [83]. However, the amplifier inputs would then have to be driven differentially which is not possible in this case (i.e., a single-ended input is assumed).

The amplifier of Figure 5.24 is analyzed in greater detail by considering its simplified non-linear equivalent circuit shown in Figure 5.25. Currents sourced


 Figure 5.25: Equivalent circuit of the proposed amplifier with IM_2 compensation.

by G_1 to G_4 model the outputs of the unity-gain current mirrors and resistors R_e model the (arbitrarily low) mirror input resistance. Practical circuit param-

eter values corresponding to commercially available discrete bipolar devices are assumed. The differential pair transistors are biased identically, so that:

$$g_{m1a} = g_{m1b} = g_{m1}, \quad (5.43)$$

$$C_{\pi1a} = C_{\pi1b} = C_{\pi1} \quad (5.44)$$

and

$$C_{\mu1a} = C_{\mu1b} = C_{\mu1}. \quad (5.45)$$

The first-order Volterra kernel of the system is calculated using (5.23) and (5.24). From this can be shown that:

$$\lim_{R_\epsilon \rightarrow 0} \frac{H_{1,1}(s_1)}{H_{1,4}(s_1)} = \frac{C_{\pi1a} + C_{\pi1b}}{C_{\pi1a} + C_{\mu1a}}. \quad (5.46)$$

As stated previously, the condition of (5.26) is essential for second-order distortion minimization, and from (5.46) it follows that:

$$C_{\pi1b} = C_{\pi1a} + 2C_{\mu1a}. \quad (5.47)$$

Since T_{1a} and T_{1b} are expected to have the same operating point (i.e., $C_{\pi1b} = C_{\pi1a}$) in an actual implementation, (5.47) is not satisfied unless an external capacitor C_e of value $2C_{\mu1a}$ is added between Node 4 and ground in the circuit of Figure 5.25 (i.e., connected in parallel with $C_{\pi1b}$).

We proceed with the analysis under the assumption that (5.47) holds while all other parameters of the input differential pair transistors remain identical. The second-order Volterra kernel is then determined as outlined in (5.30)-(5.37). The second-order, non-linear current source vector, \mathbf{IN}_2 , is given by:

$$\mathbf{IN}_2 = \begin{bmatrix} 0 \\ 0 \\ -I_{NL2,g_{m2}}(s_1, s_2) \\ 2I_{NL2,g_{m1}}(s_1, s_2) \\ -I_{NL2,g_{m1}}(s_1, s_2) \\ -I_{NL2,g_{m1}}(s_1, s_2) \end{bmatrix}. \quad (5.48)$$

Taking $I_{NL2,g_{m1}}(s_1, s_2)$ and $I_{NL2,g_{m2}}(s_1, s_2)$ as parameters, (5.37) is solved in order to determine $H_{2,3}(s_\alpha, -s_\beta)$. If it is assumed that R_ϵ and $C_{\mu2}$ approach zero, this is given by:

$$H_{2,3}(s_\alpha, -s_\beta) = \frac{s_\gamma C_{\pi2}}{s_\gamma^3 2g_{m1}g_{m2}g_f} \cdot \frac{[s_\gamma(C_{\pi1} + 2C_{\mu1}) + 2g_f + 2g_s]}{(2C_{\mu1}C_{\pi2}g_L + C_{\pi2}C_{\pi1}g_L + 2C_{\pi2}C_{\mu1}g_f + C_{\pi2}C_{\pi1}g_f)} \cdot \frac{I_{NL2,g_{m2}}(s_\alpha, -s_\beta)}{(2C_{\pi2}g_Lg_f + 2C_{\pi2}g_s g_L - 2C_{\mu1}g_{m2}g_f + 2C_{\pi2}g_s g_f)}. \quad (5.49)$$

A similar result is obtained for a finite $C_{\mu2}$, except that the expression becomes significantly more involved. Note that (5.49) is independent of $I_{NL2,g_{m1}}(s_1, s_2)$, implying that the input stage non-linear \mathbf{IM}_2 current is completely cancelled at

the output node. Thus, if \mathbf{IN}_2 is once more considered as a linear combination of the distinct contributions of the first and second amplifier stages (5.38), evaluating (5.41) will result in zero as the first term of the equation. This suggests that the first stage is fully compensated and that any even-order intermodulation at the output arises from the output stage non-linearity.

The $H_{2,3}(s_\alpha, -s_\beta)$ computed for the amplifier of Figure 5.25 is compared to $H_{2,3}(s_\alpha, -s_\beta)$ for the reference circuit of Figure 5.21 by obtaining the IP_2 figure in each case. The latter is also derived from SPICE simulations of the two amplifiers. The results are plotted in Figure 5.26 for ω_β swept from 1 MHz to 10 GHz while ω_γ is kept constant at 1 kHz. Here, the simple transistor model

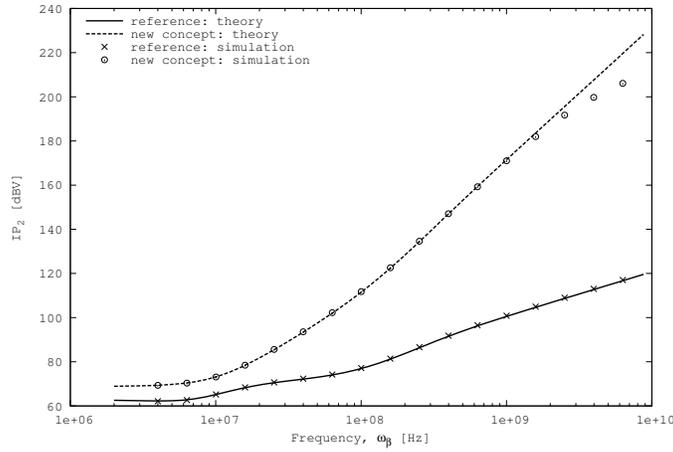


Figure 5.26: IP_2 for the equivalent circuits of Figure 5.21 (i.e., the reference) and Figure 5.25.

is used for both the Volterra series analysis and the simulations. Subsequently, this is substituted by a full transistor model as supplied by the manufacturer. Circuit biasing is implemented with ideal sources. The Volterra series analysis becomes prohibitively complex at this stage, so the circuit response is computed from SPICE simulations only. The simulation results are plotted in Figure 5.27. From the curves calculated from the Volterra series shown in Figure 5.26, it can be seen that the proposed topology yields a considerably higher IP_2 , especially for higher values of ω_β . This improvement diminishes in the simulations with the full transistor model. To determine the cause of the discrepancy, the diffusion capacitance C_π and the Miller capacitance C_μ of the full transistor model are linearised. This is obtained by setting the C_{je} , C_{jc} and T_f parameters of the SPICE model to zero, and replacing C_{je} and C_{jc} by linear capacitances of the appropriate value. The resulting IP_2 of each circuit is also plotted in Figure 5.27. From the plots it can be observed that the removal of capacitive nonlinearities yields a performance that is much more in line with the prediction of the Volterra series analysis. So, it can be concluded that the impact of

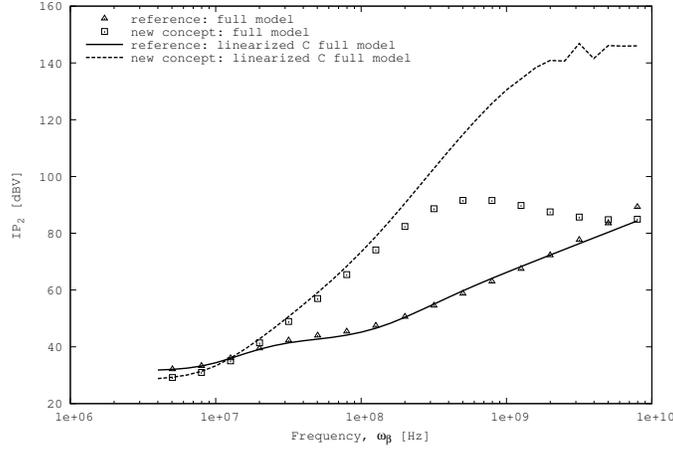


Figure 5.27: Simulated IP_2 for the reference (Figure 5.20) and proposed (Figure 5.24) circuits.

non-linear capacitances is considerable, especially at higher frequencies. They degrade the non-linear local-feedback compensation somewhat, but a superior IP_2 is still realized.

Note that there is also an offset between the simple transistor model and the linearised- C full model due to other device parasitics that are unaccounted for. Nevertheless, both models follow the same trend, thus verifying the concept.

5.6 Predistortion

The distortion cancellation methods outlined so far in this chapter rely on a symmetrical structure to achieve even-order non-linear term compensation. This approach is naturally vulnerable to disruptions of the symmetry of the circuit either through device mismatch or non-ideal behaviour. An alternative strategy is considered where a predistorted signal is first generated and subsequently presented at the input of a non-linear amplifying stage. Predistortion is typically used to linearise RF power amplifiers [84] where it is not practical to apply negative feedback. However, it can also be implemented in negative-feedback systems [77]. Figure 5.28 shows the basic topology of its application to out-of-band interference compensation. The predistorted signal is generated by a

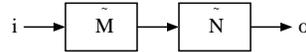


Figure 5.28: Predistortion feed-forward.

non-linear transfer, \tilde{M} , and is such that its distortion components are eliminated through intermodulation at the output of the amplifying stage, \tilde{N} . For the purpose of this work, it is not strictly necessary that the product $\tilde{M}\tilde{N}$ is a linear function. It is sufficient that its even non-linear coefficients are close to zero, so that intermodulation of an out-of-band interference signal is suppressed. This scheme relies on the non-linear behaviour of the components involved and, although not based on symmetry, will depend on absolute component parameters. The latter is a disadvantage, as the circuit may need to be calibrated.

A possible implementation of the topology outlined above is depicted in Figure 5.29. Here, the predistorted signal is provided by T_1 and R and passed on

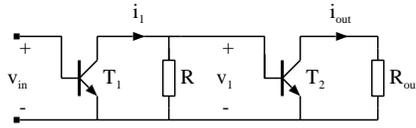


Figure 5.29: Circuit implementation of predistortion feed-forward.

to the amplifying stage, T_2 . Of course, placing a resistor in the amplification chain is undesirable and will most likely degrade the in-band performance of a negative-feedback amplifier. It is done here in order to demonstrate the concept and may have to be implemented differently in practice. To analyse the behaviour of this structure, the simplified non-linear small-signal transistor model introduced in Section 3.1 is employed. Using (3.8), the small-signal transfer of T_1 could be represented by:

$$i_1 = - \sum_1^m a_m v_{in}^m, \quad (5.50)$$

where

$$\begin{aligned} a_1 &= \frac{I_{C1}}{V_t} = g_{m1} \\ a_2 &= \frac{1}{2!} \cdot \frac{I_{C1}}{V_t^2} \\ a_3 &= \frac{1}{3!} \cdot \frac{I_{C1}}{V_t^3} \\ &\dots \end{aligned} \quad (5.51)$$

Similarly, for T_2 it applies:

$$i_{out} = - \sum_1^n b_n v_1^n. \quad (5.52)$$

Assuming that the impedance of R is sufficiently small relative to the input impedance of T_2 and the output impedance of T_1 , the output signal could be expressed in terms of the input as follows:

$$i_{out} = - \sum_1^n b_n \left(-R \sum_1^m a_m v_{in}^m \right)^n. \quad (5.53)$$

Evaluating (5.53) yields:

$$i_{out} = \frac{Ra_1b_1v_{in} + R(a_2b_1 - Ra_1^2b_2)v_{in}^2 + R(a_3b_1 - 2Ra_1a_2b_2 + R^2a_1^3b_3)v_{in}^3 + \dots}{R(a_3b_1 - 2Ra_1a_2b_2 + R^2a_1^3b_3)v_{in}^3 + \dots} \quad (5.54)$$

For small-signal levels of v_{in} , the out-of-band distortion of the structure would be determined predominantly by the quadratic term in (5.54). The latter can be eliminated by solving

$$a_2b_1 = Ra_1^2b_2. \quad (5.55)$$

Substituting the values from (5.51) for the Taylor expansion coefficients of T_1 and similarly expanding these of T_2 allows (5.55) to be simplified to the form:

$$R = \frac{1}{g_{m_1}}, \quad (5.56)$$

i.e., the voltage gain of the first stage is unity. Of course, satisfying the condition in (5.56) will not compensate non-linearities originating from the higher order terms of the Taylor polynomial. This method will, therefore, only be effective at sufficiently low signal levels, where second-order distortion is still dominant. Furthermore, since this implementation consists of two cascaded stages, an extra pole will be introduced in the overall system transfer.

Note that so far no parasitics are considered of the active devices used in this example. These will invariably affect the solution (5.56) and must be accounted for as a next step. A logical development would then be to evaluate whether the effective input impedance of T_2 is not sufficient to obtain a solution thereby dispensing of the need for an extra resistor in the amplification chain. Alternatively, the resistor R could be implemented by a diode-connected transistor which may result in cancellation of higher-order distortion components. These could be a topics for further research.

5.7 Conclusions and discussion

An attempt is made in this chapter to expand the scope of out-of-band interference immunity enhancement methods for negative-feedback amplifiers. Whenever possible, the developed methods are evaluated in the context of structured amplifier design [17]. In this way, the impact of design decisions is derived not only for the immunity to interference but also for performance in the information band. With due consideration of the trade-offs, one can combine the design rules relevant in each case to develop an overall optimised system.

Several new strategies are proposed to address the issue of out-of-band interference. The inherent low-pass behaviour of semiconductor devices can be exploited to filter an interference signal. Frequency-dependent local feedback can be used to reduce the impact of interference without a penalty to baseband performance. The operation of a differential stage can be improved through non-linear local-feedback compensation. An analog predistortion method is also

suggested. These developments are mapped according to the classification outlined in Chapter 2, and Figure 2.1 is revised to include them. The modified solution tree is shown in Figure 5.30. The various design methods are subse-

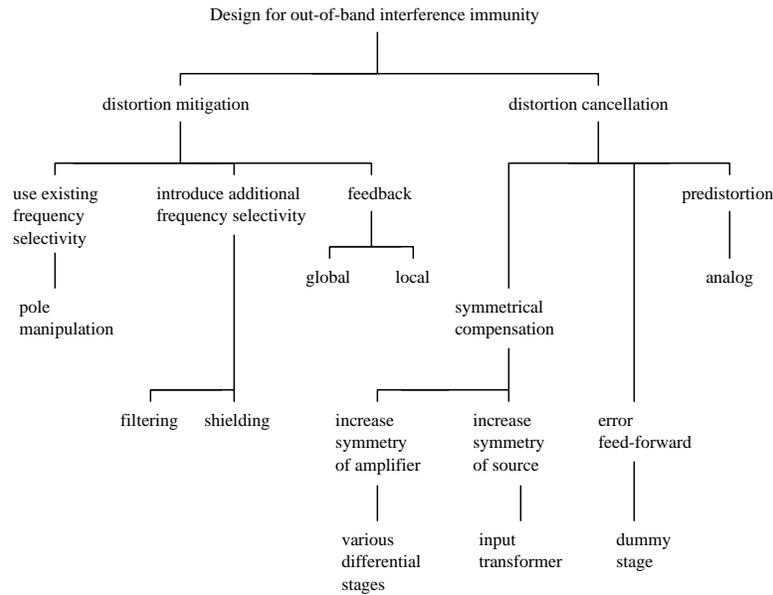


Figure 5.30: Design methods for improving out-of-band interference immunity.

quently placed on a cost-effectiveness grid in order to obtain some measure of their relative merit. This is shown in Figure 5.31. Grading is done according to the performance of the specific implementations analysed in this chapter, where applicable. Of course, other implementations will exist of the same principle that may position the solution otherwise on the graph. Different design methods are placed on the grid according to their effectiveness in lowering sensitivity to interference against implementation cost. Here, cost is loosely defined as the combined impact of additional hardware, design effort, power consumption and performance trade-off. So, for instance, a dummy stage would be most effective in compensating out-of-band interference but at a price of double the hardware, noise and power consumption, and additional filtering. This is further complicated by the requirement that both parts of the circuit receive identical interference signals. On the other hand, pole manipulation is very simple to achieve and does not cost any extra hardware or power. However, the expected immunity enhancement depends on the amount of freedom to modify the biasing of the input stage and could be marginal. The example of predistortion discussed here is costly in terms of loss of in-band performance, while it is able to compensate only the second-order intermodulation product. The cost could be decreased if a biasing condition exists for which the two stages can

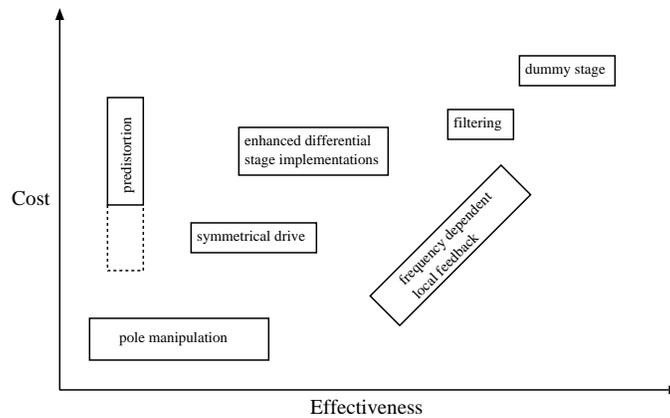


Figure 5.31: Cost-effectiveness of design strategies.

be cascaded without the need for an extra resistor. Hence, the extension of the position occupied by predistortion in the figure. It is also shown that frequency-dependent local feedback utilises the available impedance better than filtering. So, depending on the complexity of the frequency selectivity, the former can be made as effective as the latter but at a relatively lower cost. Similarly, the remaining techniques developed are positioned on the chart. Bearing in mind the advantages and trade-offs of each approach, the designer is now free to proceed with implementation.

Chapter 6

Design example

“Recipes are, by definition, documentation of what works for their authors.”

Jeff Potter, *Cooking for Geeks*

The non-linear local-feedback compensation developed in Section 5.5 is demonstrated experimentally by implementing it in a practical circuit. The transimpedance amplifier topology shown in Figure 5.20 is used as reference. To reduce the prototyping time, the circuit is built with discrete components. While easier to work with, this approach does have certain disadvantages. Device matching is normally quite poor compared to what can be achieved with monolithic integration. Additionally, the physical size of a discrete component circuit is orders of magnitude larger than an integrated solution and can result in a structure that is not electrically small at the frequencies of interest. These issues are addressed before proceeding with the design.

6.1 Signal source

As seen in Figure 5.20, the amplifier configuration chosen for this experiment requires a current source as the input driver. The signal source should furthermore be well characterised across a wide frequency range. To satisfy the latter requirement, it is chosen to work in the $50\ \Omega$ domain wherever possible in the experimental set-up. Broadband $50\ \Omega$ signal sources are readily available but are not suitable to drive the circuit directly due to their low output impedance. This is solved by considering the Thevenin equivalent of a current source [85], as shown in Figure 6.1a. Ideally, the source resistance, R_s , of the current source is infinite. The primary voltage source, V , can be substituted by a characteristically terminated $50\ \Omega$ source. This is illustrated in Figure 6.1b and results in an equivalent output impedance of $R_s + 25\ \Omega$ which approximates R_s for $R_s \gg 25\ \Omega$. The advantage of such a configuration is that the system

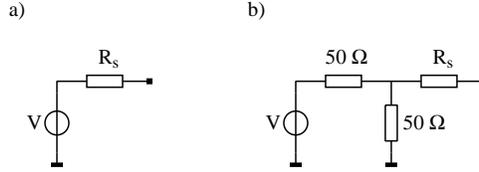


Figure 6.1: Current source implementation.

impedance can remain $50\ \Omega$ up to the termination resistor, while the effective output impedance is largely determined by R_s . It should be noted that for a particular output current, increasing R_s results in a corresponding increase of the power dissipated in the termination resistor. This is accounted for when selecting components for the final design.

6.2 Electrical size verification

To ensure that distributed effects do not have a significant effect on the circuit, the electrical size of a potential printed circuit board (PCB) implementation is investigated. Of particular interest here is the interface between the $50\ \Omega$ signal generator and the input of the amplifier. This combines several complementary functions. First, a stable, frequency-independent characteristic-impedance load must be presented to the $50\ \Omega$ subsystem. Additionally, the voltage to current conversion by the Thevenin resistor, R_s , as shown in Figure 6.1, must proceed reliably across a wide frequency range. Finally, the input signal must reach the first stage of the amplifier in a predictable and repeatable manner. To evaluate this set of requirements, a concept PCB layout of the termination resistance, R_s and the input of the first stage differential pair is simulated in a 3-dimensional electromagnetic (3-D EM) solver [86]. The electrical circuit of the experimental set-up is shown in Figure 6.2. This comprises an ideal $50\ \Omega$ signal source, a

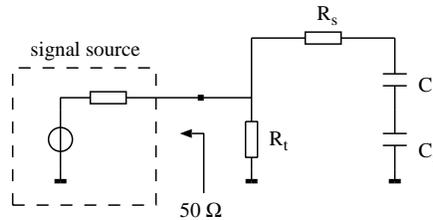


Figure 6.2: Current source implementation.

termination resistor, R_t , likewise of $50\ \Omega$, the Thevenin resistor and two capacitors, C_1 and C_2 , that model the (high-frequency) input impedance of each of the

differential pair transistors. It is assumed that R_s is significantly larger than R_t , so that the latter effectively determines the load impedance presented to the signal source. In reality, the availability of high-frequency resistors is somewhat limited to the sub-k Ω range. As a compromise between physical size and resistance value, it is chosen to compose R_s of three series connected 1 k Ω RF resistors. Figure 6.3 shows the 3-dimensional model of the physical structure.

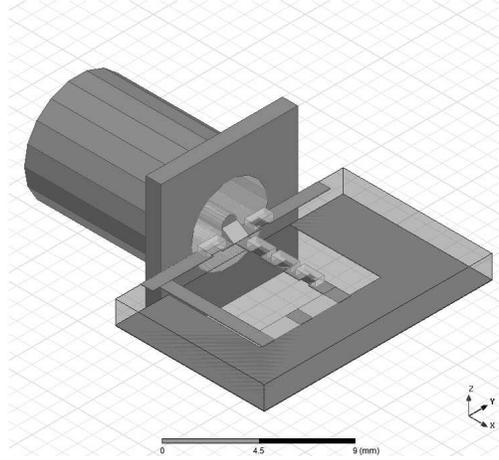


Figure 6.3: 3-D model of the input section of the PCB.

This includes a representation of the connector to the signal generator, so that the transition from a coaxial to a planar arrangement can be considered. For better symmetry, R_t is split into two 100 Ω sections connected in parallel. The resistors are modelled as a thin conducting layer on an alumina substrate of the dimensions supplied by the manufacturer [87]. Since the exact composition of the conductor is proprietary, 1 μm thick carbon track is used. This is sufficiently thin to ensure that skin effect does not influence its resistance at the frequencies of interest. To obtain a high impedance structure, the ground plane under the series implementation of R_s is removed. Ideal capacitance boundaries are used for C_1 and C_2 , with $C_1 = C_2$. Their physical size is derived from commercially available RF components. As suggested by (5.47), a balancing capacitor will be placed at the input of the differential pair. So, a discrete component will invariably be present at that point in the final circuit. Figures 6.4 and 6.5 show the real and imaginary parts of the input impedance of the structure predicted by the EM simulation. It may be concluded that the structure provides a reasonably good characteristic termination to the 50 Ω equipment up to several gigahertz. The current through the capacitors C_1 and C_2 is also derived from the analysis. This is plotted in Figure 6.6, together with the corresponding result from a lumped component SPICE simulation. The results suggest that the current is well defined up to approximately 1 GHz. Beyond that, the lumped

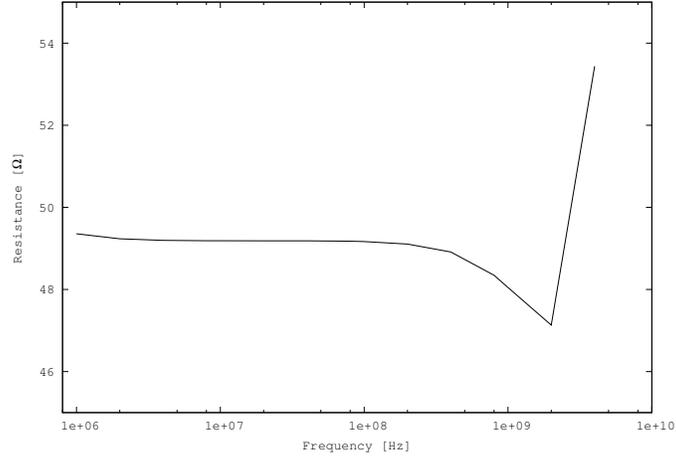


Figure 6.4: Real part of the input impedance.

component approach is clearly inadequate to model the behaviour of the circuit, and a more elaborate characterization is needed. It is furthermore noted from the EM simulation results that there is a difference between the individual currents through C_1 and C_2 at high frequencies. An essential requirement of the proposed nonlinear compensation scheme is that the input voltage of the first stage is divided equally between the two differential pair transistors, as stipulated by (5.26). In the present arrangement, this translates to an equal division in the capacitive voltage divider formed by C_1 and C_2 . To verify that, the voltage drop across each capacitor is calculated and the mismatch is determined. This is expressed as a percentage of the total voltage across the divider and is plotted in Figure 6.7. It can be observed in the graph that the voltage mismatch approaches 1% at 200 MHz and increases sharply beyond that. Since an error of 1% is significant in the proposed compensation method, it can be concluded that the evaluated PCB solution will provide a controlled environment for the design experiment up to around 100 MHz. Therefore, the amplifier under test should have a bandwidth well within this range, for example 1 MHz, so that both in-band and out-of-band measurements can be performed.

6.3 Circuit implementation

One of the disadvantages of using discrete components to implement the circuit is that the device matching can be rather poor. To address that, matched transistor arrays are used. These provide a number of individually accessible transistors integrated on the same die so as to achieve a very low relative spread. Intersil's HFA3046/3127 (5 x NPN, $f_t = 8$ GHz, $\beta = 130$ at $I_c = 10$ mA) and HFA3128 (5 x PNP, $f_t = 5.5$ GHz, $\beta = 60$ at $I_c = 10$ mA) parts are chosen [88].

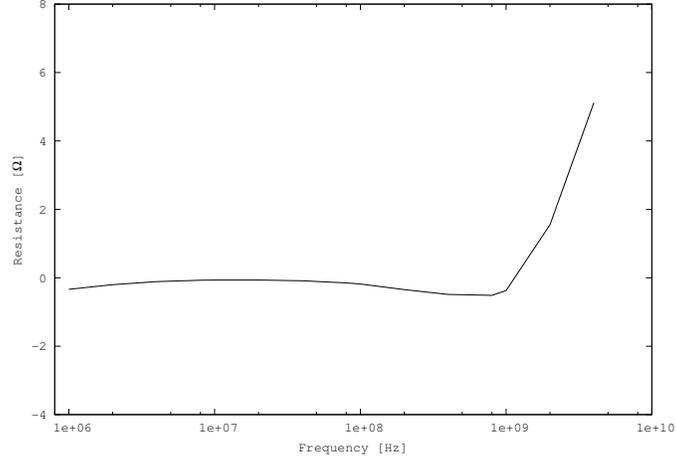
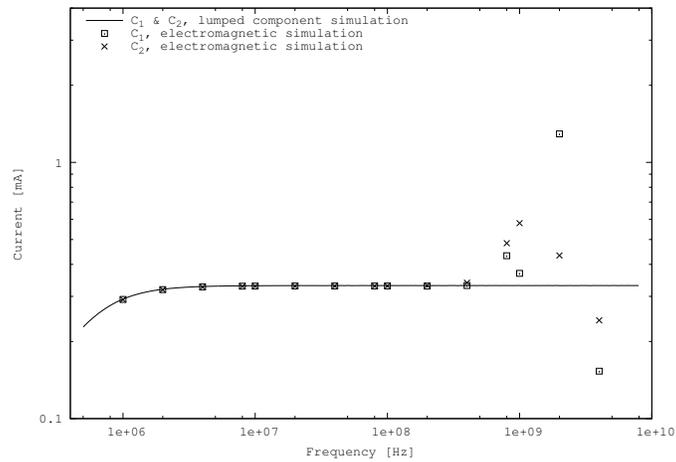
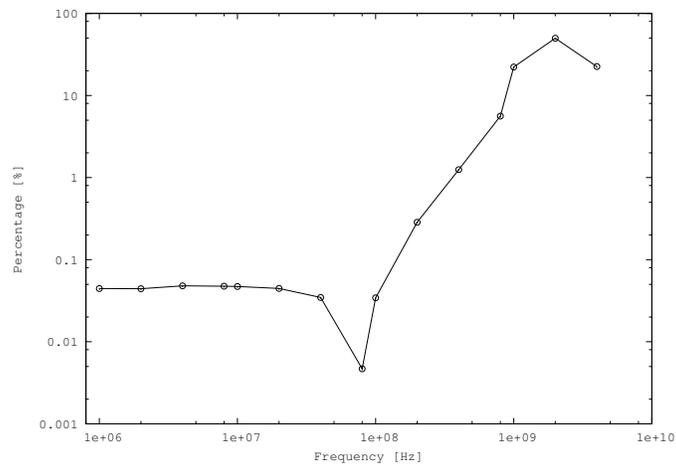


Figure 6.5: Imaginary part of the input impedance.

These UHF components could result in an amplifier with an out-of-band range in the gigahertz region. To ensure the experimental frequencies are within the operating range of a PCB implementation, the decision is made to artificially degrade the bandwidth of the transistors by placing fixed capacitors across the base-emitter junctions of selected devices. The bandwidth of the amplifier and its out-of-band region can thereby be scaled down to the workable levels outlined in Section 6.2. The proposed concept of Figure 5.24 is subsequently implemented with the reduced frequency transistors. This is shown in Figure 6.8. Biasing is omitted from the figure for clarity. The controlled current sources G_1 , G_2 , G_3 and G_4 of Figure 5.24 are implemented by current mirrors $T_{11a} - T_{15a}$, $T_{11b} - T_{12b}/T_{13b} - T_{15b}$, $T_{11a} - T_{12a}/T_{13a} - T_{14a}$ and $T_{11b} - T_{12b}/T_{13b} - T_{14b}$, respectively. To obtain a well defined current gain (i.e., unity), the components of each current mirror are chosen from the same matched transistor array chip. Table 6.1 shows how the circuit is distributed across a number of these chips. Capacitors C_d serve to limit the bandwidth of the transistors in the main signal path. They are chosen to achieve an amplifier bandwidth of around 200 kHz and the out-of-band region above 10 MHz. This does not affect the validity of

Table 6.1: Device allocation per matched array.

	chip	allocated devices
1	HFA 3046, 5xNPN	$T_{1a}, T_{1b}, T_{13a}, T_{14a}$
2	HFA 3127, 5xNPN	$T_2, T_{13b}, T_{14b}, T_{15b}$
3	HFA 3128, 5xPNP	$T_{11a}, T_{11b}, T_{12a}, T_{12b}, T_{15a}$

Figure 6.6: Current through C_1 and C_2 .Figure 6.7: Mismatch of the voltages across C_1 and C_2 .

the concept, but only ensures that additional design effort is not expended to account for the electrical size of the final implementation.

An issue of repeatability arises with the reference circuit. Implementing this on a separate PCB means that there will be a mismatch between the two amplifier variants due to component spread. As a result, for example, each circuit will be subjected to a slightly different input signal. To eliminate this source of error and ensure that an exact comparison is achieved down to the device level, it is decided to implement the reference amplifier by reconfiguring

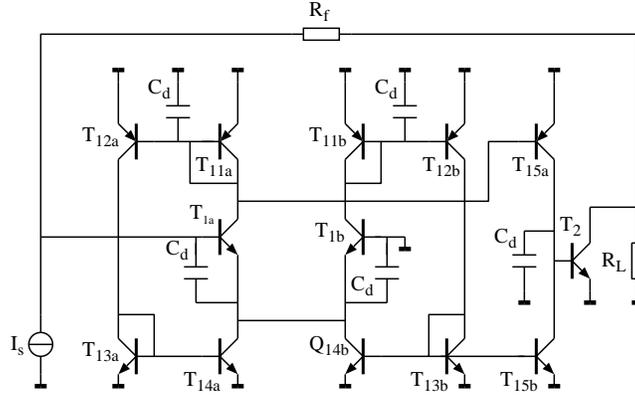


Figure 6.8: Transistor signal circuit of the proposed concept of Figure 5.24.

the circuit of Figure 6.8. This is obtained by deactivating selected devices, i.e., T_{12a} , T_{13a} , T_{14a} and T_{14b} . The result is shown in Figure 6.9. This is identical

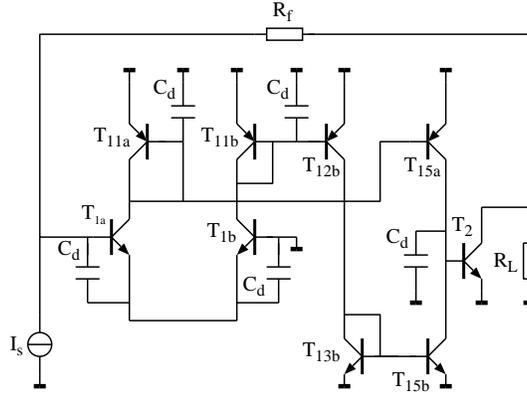


Figure 6.9: Signal circuit of the reference amplifier.

to the reference circuit of Figure 5.20, except that the output of T_{1b} is not connected directly to the input of the second stage transistor, T_2 , but passes through two unity gain current mirrors. Ultimately, the same signal transfer function is achieved in both cases.

The final implementation of the combined circuit is shown in Figure 6.10. A split power supply is used, so that the internal nodes 1 through 5 are biased at 0 V. Therefore, there is no objection to ground any of them without affecting the DC operating point of the circuit. This is made use of when switching between

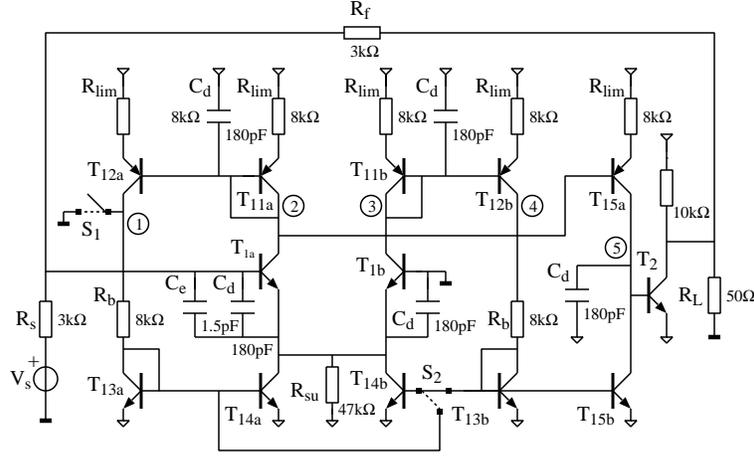


Figure 6.10: Full circuit of the combined amplifier design.

the two amplifier configurations. Closing switch S_1 and toggling S_2 reconfigures the circuit from the new concept to the reference. This grounds the collector of T_{12a} and the bases of T_{13a} , T_{14a} and T_{14b} , effectively eliminating the nonlinear local-feedback compensation mechanism. At the same time, the bias point of all transistors in the circuit remains the same in both configurations. In the present implementation of the proposed concept, transistors $T_{11} - T_{14}$ form a positive feedback loop that is stable across a wide range of signal levels. To regulate the bias of the input differential pair, current limiting resistors R_{lim} are used as degeneration at the emitters of T_{11} and T_{12} . These resistors also increase the output impedance of each PNP current source which is a beneficial side effect. To ensure that the circuit does not remain in an undefined state at power-up, a start-up resistor R_{su} is connected between the common node of T_{14a} , T_{14b} and the negative supply rail. This can be nearly arbitrarily large in a MOS transistor implementation, but in the present situation it also serves to balance the currents in the loop. Due to the limited current gain of the bipolar transistors, the mirroring ratio of the current mirrors $T_{11} - T_{12}$ and $T_{13} - T_{14}$ is not exactly unity. For example, in case of the latter, the following approximation applies:

$$I_{C,14a} = I_{C,12a} \frac{2\beta_{NPN}}{1 + 2\beta_{NPN}}, \quad (6.1)$$

where β_{NPN} is the current amplification factor of the NPN transistors and $I_{C,12a}$ and $I_{C,14a}$ the collector currents of T_{12a} and T_{14a} , respectively. So, the output signal of the current mirror, $I_{C,14a}$, is lower than the reference signal at the input, i.e., $I_{C,12a}$. Likewise, the current gain in the loop $T_{11} - T_{14}$ is less than unity. This means that the emitter current, $I_{E,1a}$, of T_{1a} is always larger than $I_{C,14a}$, and the difference must flow through R_{su} . Let the current, I_{Rsu} ,

through R_{su} be expressed as the sum of the contributions from each half of the input stage:

$$I_{Rsu} = I_{Rsu,a} + I_{Rsu,b}, \quad (6.2)$$

where $I_{Rsu,a} = I_{E,1a} - I_{C,14a}$ and $I_{Rsu,b} = I_{E,1b} - I_{C,14b}$. The structure is not perfectly symmetrical because of the base currents of T_{15a} and T_{15b} . So, the balancing currents $I_{Rsu,a}$ and $I_{Rsu,b}$ are not exactly equal. These can be calculated by finding the equivalent expressions (6.1) of the current mirrors in the loop and are given by:

$$I_{Rsu,a} = \frac{(\beta_N + 2)(\beta_P + 3) + \beta_N(3\beta_N + 2\beta_P + 6)}{\beta_N(\beta_N + 2)(\beta_P + 3)} I_{C,1a}, \quad (6.3)$$

and

$$I_{Rsu,b} = \frac{(\beta_N + 2)(\beta_P + 2) + \beta_N(\beta_N + 2\beta_P + 4)}{\beta_N(\beta_N + 2)(\beta_P + 2)} I_{C,1b}, \quad (6.4)$$

in terms of the collector currents of T_{1a} and T_{1b} . By approximation:

$$I_{C,1a} \approx \frac{\beta_N \beta_P}{3(\beta_N + \beta_P)} I_{Rsu,a}, \quad (6.5)$$

and

$$I_{C,1b} \approx \frac{\beta_N \beta_P}{\beta_N + 3\beta_P} I_{Rsu,b}. \quad (6.6)$$

Therefore, the biasing of the input stage differential pair is strongly dependent on β_N and β_P which are process-dependent parameters and may vary considerably. Note that the value of R_{su} is fixed by I_{Rsu} and the desired collector-emitter voltage of T_{14} . The voltage drop across R_{su} effectively determines the base-emitter voltages of T_{1a} and T_{1b} . For this reason, variation of R_{su} will have an even stronger influence on the bias point of the input stage. This shortcoming is considered acceptable in the prototyping stage since both R_{lim} and R_{su} can be tuned according to the values of β_N and β_P . The current gain factors are unknown but are not expected to vary significantly between devices on the same matched transistor array.

An external balancing capacitor C_e is added to satisfy the condition of (5.26) for maximizing IP_2 at the output. This is placed on the opposite transistor of the differential stage than initially surmised by (5.47) and shown in Figure 5.25, because of the output capacitance of the tail current source $T_{14a} - T_{14b}$. This parasitic capacitance effectively adds to the balancing capacitor and overcompensates the circuit, necessitating a corresponding reduction of the former. In this case, the parasitic capacitance is larger than C_e , so a negative capacitor is needed which is equivalent to a positive C_e on the opposite transistor of the differential stage. Figure 6.11 shows a photograph of the fabricated PCB. Switches S_1 and S_2 are implemented with jumpers, as indicated on the figure. The output of the circuit which is designed to drive 50Ω is connected directly to the standard 50Ω measurement equipment. For this reason, the output load resistor, R_L , of Figure 6.10, is not placed on the PCB. Batteries are used for

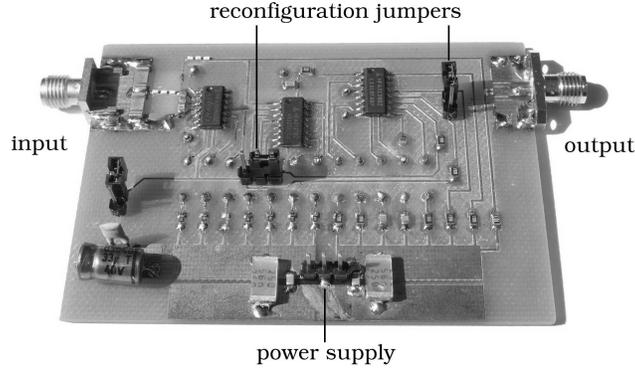


Figure 6.11: Photograph of the experimental PCB.

the split power supply to avoid any unexpected interference. Extra decoupling is added to the power supply rails to ensure any interference picked up by the wiring of the battery pack is filtered. As the biasing of the transistors is dependent on the battery voltage, this is monitored throughout the measurement. Due to the relatively low current draw of the circuit, no significant drift is observed. The bias current of the input stage transistors is verified by measuring the voltage drop across the resistors R_{lim} . To avoid temperature dependent effects, the measurements are conducted sequentially in an air-conditioned room. Self-heating of the circuit is assumed negligible due to its low power dissipation.

6.4 Measurement results

To determine the IP_2 figure of the amplifiers, they are measured with a two-tone $(\omega_\alpha, \omega_\beta)$ out-of-band signal applied to the input. The difference frequency (ω_γ) is set at 265 Hz so as not to coincide with harmonics of the 50 Hz mains. The second-order intermodulation product detected at ω_γ is measured with a spectrum analyzer connected directly to the output. The output IP_2 is subsequently calculated and is plotted in Figure 6.12 for the proposed and reference amplifier designs. The results indicate that the proposed circuit exhibits a significantly higher IP_2 - in the excess of 30 dB - at the onset of the out-of-band region. The improvement diminishes at higher frequencies due to secondary non-linear effects, as explained in Section 5.5. This drop is sharper than predicted from a lumped component analysis due to the influence of distributed effects above 50 MHz. The latter is in line with the prediction of the 3-D EM simulations. There is an approximately equal offset between the measured and simulated IP_2 values for both amplifiers. This appears to be caused by mismatch between passive components and separate transistor arrays (i.e., two NPN array ICs were needed in the set-up).

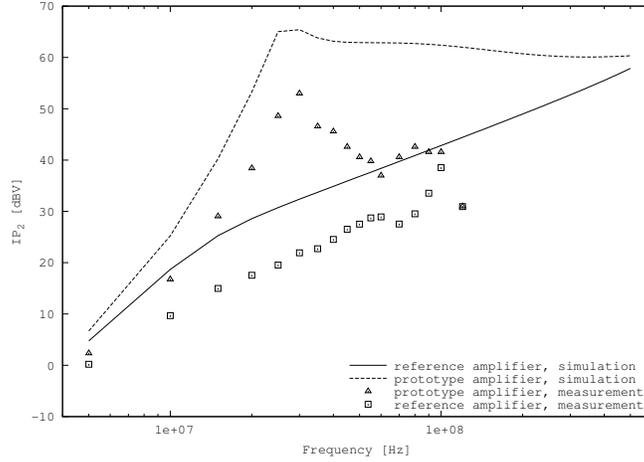


Figure 6.12: Simulated and measured output IP_2 for the reference and prototype amplifiers.

The performance of both circuits is also investigated with respect to noise and bandwidth. In Figure 6.13 the frequency response of the two amplifiers is shown. The plots reveal a close match between the simulation results and the measurements up to around 40 MHz. Beyond that, the latter start to diverge due to the commencement of distributed effects. It can furthermore be observed from the figure that the two amplifier variants have essentially the same frequency response. The input-referred noise density of the circuits is also simulated and compared to the corresponding result from the measurements. The latter is obtained by determining the output noise spectral density of the amplifier, using a spectrum analyzer. To ensure that the output noise level is above the noise floor of the measurement instrument, it is first boosted with an RF amplifier (30 dB gain, 50 Ω input/output characteristic impedance). The input-referred noise density is subsequently calculated from the measured frequency response of the amplifier, as seen in Figure 6.13, and is shown in Figure 6.14. Again, there is a close match between the predicted behaviour and the actual measured performance. The results from figures 6.13 and 6.14 suggest that neither bandwidth nor noise behavior are affected significantly by the activation of the proposed non-linear, local-feedback compensation loop in the prototype. Since both amplifiers have identically configured and biased output stages and implement the same transfer function, their dynamic range is also nearly identical (i.e., approximately 85 dB). It should also be noted that the proposed design method does not place any requirements on the biasing of the differential stage. Noise optimization can, therefore, be carried out without affecting the IP_2 performance.

The IM_3 response of the circuits is also simulated and is compared to the corresponding result from the measurements. Table 6.2 lists that for an input

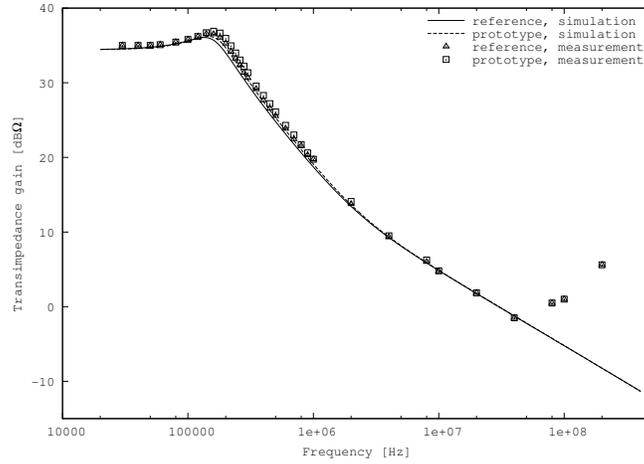


Figure 6.13: Simulated and measured transfer function of the amplifiers.

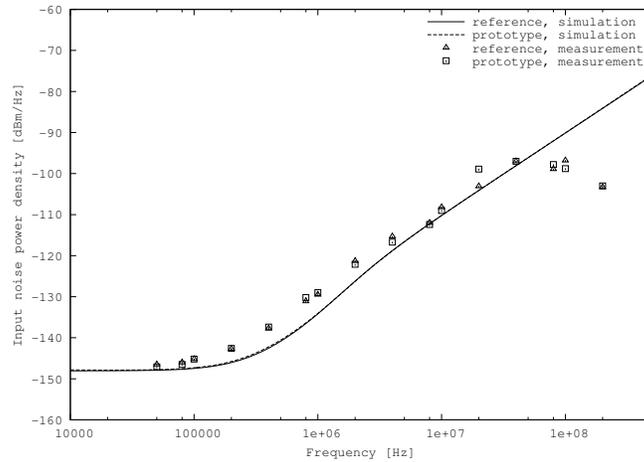


Figure 6.14: Simulated and measured input noise of the amplifiers.

signal level of -30 dBm. The fundamental frequency, f_0 , is varied between 300 kHz and 600 kHz. The IIP_3 is also evaluated and found to be approximately -10 dBm for both circuits.

6.5 Benchmarking and conclusions

The out-of-band interference immunity improvement obtained with the proposed method is compared to examples reported in the recent literature in Table

Table 6.2: IM₃ response of the circuits.

f_o [kHz]	simulated IM ₃ [dBm]		measured IM ₃ [dBm]	
	reference	new concept	reference	new concept
300	-57.7	-56.7	-59	-58
400	-72.9	-72.4	-75	-72
500	-86.2	-85.9	-90	-87
600	-97.3	-97.4	-98	-96

6.3. In each case, the EMI susceptibility reduction is given relative to a circuit with a classical differential stage at the input. The frequency (range) of the im-

Table 6.3: Comparison between immunity enhancement approaches

Source	Improvement	Frequency
fully symmetrical topology [10]	> 20 dB	1 MHz - 4 GHz
filtered dummy stage [11]	18 dB	30 - 40 MHz
complementary differential pair [12]	18 dB	100 MHz
double differential stage [13]	60 dB	1 GHz
source buffering [14]	14 dB	200 - 800 MHz
this design	31 dB	30 MHz

provement registered is also noted in the table. Source buffering [14] attempts to reduce the RFI-induced offset voltage at the common node of the differential pair. The other approaches [10]-[13] all aim to cancel distortion products at the output of the differential stage. The proposed method, on the other hand, modulates the voltage at the common node of the differential pair so that cancellation of the distortion products occurs throughout the circuit. While this comparison puts the current example in perspective, it should be noted that the IM₂ cancellation approach proposed in Section 5.5 can be combined with many of the other methods to yield an even greater improvement in immunity to second-order intermodulation distortion.

Overall, the design strategy outlined here enables IP₂ compensation of practical differential amplifiers without compromising low-noise performance or other electrical parameters in the design space. The simulation and measurement results indicate that the differences between the performance of the proposed amplifier and the reference are marginal for all the evaluated aspects. Compared to the classical differential stage, the one with nonlinear local-feedback compensation requires several additional current mirrors. This results in higher power dissipation as well as a larger physical size. Furthermore, in the present implementation, the voltage headroom between supply rails is reduced slightly by resistive degeneration. Considering that all these shortcomings apply to the

input stage of the amplifier, it seems unlikely that they will determine either the power consumption or the maximum signal swing of the whole circuit.

Chapter 7

Conclusions and recommendations

“All’s well that ends ...”

William Shakespeare

As the operating frequencies of electronic equipment and the diversity of concurrently deployed technologies increase, there is a greater risk of the occurrence of out-of-band interference. This phenomenon is caused by non-linearities in the transfer function of circuit components and, in particular, active devices such as transistors. Through intermodulation, a frequency component can appear in the information band of a negative-feedback amplifier that is absent from both the legitimate input spectrum and that of the (high frequency) interference. This spurious component will appear at the output of the amplifier and will interfere with the information signal that is currently being processed. Therefore, we focus on the non-linear behaviour of circuit components, the relative impact on the overall susceptibility profile and ways to reduce it or mitigate its effect. The Volterra series are used to perform circuit analysis. This is a recursive method to obtain the intermodulation products of a non-linear system, yielding an additional order of non-linear terms at each iteration. It is a general approach to non-linear system analysis and results in a complete expansion of the non-linear terms. Unfortunately, this makes Volterra series calculations very complex, especially when multiple non-linear components are present. Strictly speaking, only the low-order even intermodulation products are sufficient to determine the out-of-band interference level, so the Volterra series analysis results in an unnecessary level of detail. In this thesis, a simplified analysis method is proposed that is developed especially for negative-feedback amplifiers. It assumes that the negative-feedback loop is inactive at the frequency of the out-of-band interference and results in significantly simpler calculations. Of course, its predictions are not as accurate as these of the Volterra series analysis, but it is

nevertheless able to identify the correct trends and relative impact of different non-linear components. This can speed-up the choice of negative-feedback amplifier topology and give more insight of the dominant factors. Both the Volterra series analysis and the simplified approach identify the input stage of a negative-feedback amplifier as the most sensitive to out-of-band interference. Various methods are discussed to design the input stage so as to improve the interference immunity of the amplifier. These can be divided into two broad categories: distortion mitigation and distortion cancellation.

Frequency-dependent local feedback When distortion mitigation is applied, no attempt is made to manipulate the non-linearities of the circuit but to reduce the signal swing across them. This results in an exponential decrease of non-linear signal components which is more pronounced for higher order terms and intermodulation products. Applying filtering to the controlling parameter of a non-linearity is an example of this approach. Another example is local feedback which trades off some of the overall gain of an active device for a lowering of the amplitude of its input quantity. However, local feedback is typically detrimental to the in-band operation of an amplifier. To address this, a method of frequency-dependent local feedback is proposed in this thesis. It is shown that this makes better use of the available frequency selectivity than filtering of the input signal. Furthermore, as the local feedback is inactive at low frequencies, the in-band performance is not compromised. The proposed solution, therefore, combines the advantages of both approaches and gives a better result than either of them applied separately.

Pole-position manipulation Another distortion mitigation method involves employing the inherent frequency selectivity of transistors to benefit the out-of-band interference immunity. Their frequency-dependent behaviour causes poles and zeros to appear in the transfer function of a negative-feedback amplifier. It is shown that reducing the frequency of the amplifier's input stage pole results in better filtering of out-of-band signals and yields a circuit with improved interference immunity.

Improved differential stages When distortion cancellation is applied, an arrangement of circuit elements is pursued that results in partial or full cancellation of the resulting non-linear signal components. This can yield an improved linearity throughout the frequency band, which may also benefit the in-band performance. Numerous methods exist to achieve such linearisation, based on symmetry, feedback or feed-forward compensation. Some of the best-known techniques are outlined and several new ones are suggested. Many of these employ differential transistor stages to eliminate the even intermodulation products that cause out-of-band interference. However, the symmetry of these circuits is often degraded by various device parasitics. Therefore, emphasis is given on ensuring that symmetry is maintained with sufficient fidelity throughout the operating range. For example, this can be achieved by driv-

ing a differential transistor stage with a perfectly differential signal, but the requirement it imposes on the signal source is seldom feasible in practice. To accommodate single-ended actuation, a novel approach is proposed in this thesis that retains symmetry through non-linear local-feedback compensation. The non-linear signal components are detected and fed back using a compensation loop built around the differential stage. In this way, the signal path is well defined, and parasitic currents that would otherwise disturb the symmetry of the circuit are eliminated. The non-linear local-feedback compensation concept is demonstrated by implementing it in a practical amplifier. This is compared to the equivalent classical amplifier circuit and appears to function identically in all respects, while the output IP_2 is improved by more than 30 dB. Another method is proposed which is based on a complementary differential stage architecture. This attempts to minimize the parasitic capacitance at the common node of the differential pair by eliminating the tail current bias source, thereby improving the linearity performance.

Recommendations and future work This investigation attempts to give an overview of the mechanism of out-of-band interference in negative-feedback amplifiers and the available strategies to render a circuit insensitive to it. While the main issues have been addressed, several interesting questions arise in the process that could further advance the state of the art. One such question is the possibility to combine distortion cancellation and distortion mitigation techniques to obtain an even higher degree of interference immunity. For example, (frequency dependent) local feedback could be applied together with a cancellation technique such as a double differential stage or non-linear local feedback. A linearisation method based on (analog) predistortion is, furthermore, suggested in this thesis, and demonstrated conceptually. This could be investigated and developed further. A classical linearisation approach involving (filterless) error feed-forward also exists but does not appear to have found an application to out-of-band interference immunity enhancement. It should be determined whether it is practical to use it in this context. The biasing of the non-linear local-feedback compensation loop is another intriguing question. So far, no rigorous approach has been developed to relate the bias point to a single reference quantity, such as a current. The present solution is adequate for a proof of concept implementation but may not be practical for manufacturing. This is another possible topic for further research.

Appendix A

Biasing non-linear local-feedback loops

It is clear that the present implementation of a non-linear local-feedback compensation loop in a negative-feedback amplifier, as illustrated in Chapter 6, does not offer a robust solution for biasing the input differential pair. The current through transistors T_{1a} and T_{1b} of Figure 6.10 is dependent on transistor parameters, resistor values, power supply voltage and temperature. This is acceptable for a proof of concept with a restricted number of active devices and the possibility to measure and replace every resistor. However, should the circuit have to be fabricated, such an implementation may result in a large spread of performance parameters after manufacture and during operation. The biasing scheme could be streamlined by including a control loop, as shown in Figure A.1. This

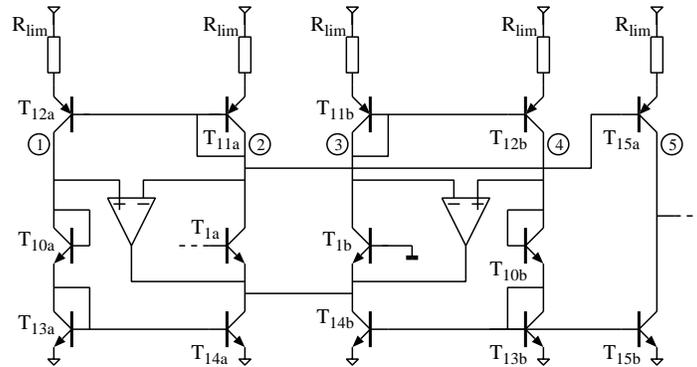


Figure A.1: Alternative biasing scheme of the input stage.

removes the dependence on the value of R_{su} , but the operating point is still a function of R_{lim} , transistor parameters, supply voltage and temperature. As

the loops T_{11} - T_{14} process both common-mode and differential mode signals it does not appear possible to define the biasing of T_1 in a frequency independent manner. A filter must, therefore, be used in a bias loop to separate the signal from the bias quantity should the biasing of the differential stage have to be set accurately.

Bibliography

- [1] International Telecommunication Union, *World Telecommunication/ICT Indicators database 2016*, 20th ed., June 2016 (online). Available: <http://www.itu.int/ITU-D/ict/statistics>
- [2] C. E. Shannon, "Communication in the Presence of Noise", *Proceedings of the IEEE*, vol. 86, no. 2, pp. 447-457, Feb. 1998.
- [3] H. S. Black, "Stabilized Feedback Amplifiers", *Bell System Technical Journal*, vol. 13, no. 1, pp. 1-18, Jan. 1934.
- [4] D. A. Neamen, *Semiconductor Physics & Devices*, 2nd ed., Chicago, IL, USA, Irwin, 1997.
- [5] Nederlandse Amateur Vereniging voor Raket-Onderzoek, *home page*, Oct. 2016 (online). Available: <http://www.navro.nl>
- [6] M. Uitendaal, *private correspondence*, May 2010.
- [7] D. A. Weston, *Electromagnetic compatibility: principles and applications*, 2nd ed., New York, NY, USA, Marcel Dekker, 2001.
- [8] J. J. Goedbloed, *Elektromagnetische compatibiliteit*, 3rd ed., Deventer, The Netherlands, Kluwer, 1993.
- [9] P. Wambacq, W. Sansen, *Distortion analysis of analog integrated circuits*, 2nd ed., Dordrecht, The Netherlands, Kluwer Academic Publishers, 2001.
- [10] A. Richelli, "Design considerations for an ultra-low voltage amplifier with high EMI immunity", *IEEE International Conference on Electronic Circuits and Systems*, pp. 558-561, Sept. 2008.
- [11] A. Richelli, "CMOS OpAmp Resisting to Large Electromagnetic Interferences", *IEEE Transactions on Electromagnetic Compatibility*, vol. 52, no. 4, Nov. 2010.
- [12] F. Fiori, P. S. Croveti, "Complementary differential pair with high immunity to RFF", *Electronics Letters*, vol. 38, no. 25, pp. 1663 - 1664, Dec. 2002.

- [13] F. Fiori, "Design of an Operational Amplifier Input Stage Immune to EMI", *IEEE Transactions on Electromagnetic Compatibility*, vol. 49, no. 4, pp. 834-839, Nov. 2007.
- [14] J. M. Redoute, M. S. J. Steyaert, "EMI-Resistant CMOS Differential Input Stages", *IEEE Transactions on Circuits and Systems*, vol. 57, no. 2, pp. 323-331, Feb. 2010.
- [15] V. Balasubramanian, P. Ruedi, Y. Temiz, A. Ferretti, C. Guiducci, C. C. Enz, "A 0.18 μm Biosensor Front-End Based on 1/f Noise, Distortion Cancellation and Chopper Stabilization Techniques", *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 5, pp. 660-673, Oct. 2013.
- [16] M. Atef, H. Zimmermann, "Optical Receiver Using Noise Cancelling With an Integrated Photodiode in 40 nm CMOS Technology", *IEEE Transactions on Circuits and Systems*, vol. 60, no. 7, pp. 1929-1936, Feb. 2013.
- [17] C. J. M. Verhoeven, A. van Staveren, G. L. E. Monna, M. H. L. Kouwenhoven, E. Yildiz, *Structured electronic design*, Dordrecht, The Netherlands, Kluwer Academic Publishers, 2003.
- [18] M. J. van der Horst, A. C. Linnenbank, W. A. Serdijn, J. R. Long, "Systematic Design of a Transimpedance Amplifier With Specified Electromagnetic Out-of-Band Interference Behavior", *IEEE Transactions on Circuits and Systems*, vol. 57, no. 3, pp. 530-538, Mar. 2010.
- [19] J. S. Scott, C. van Zijl, *Introduction to EMC*, Oxford, UK, Newnes, 1997.
- [20] B. Razavi, *RF Microelectronics*, Upper Saddle River, NJ, USA, Prentice Hall, 1998.
- [21] G. G. A. Black, K. C. Smith, "A JFET Circuit for Instrumentation Applications", *IEEE Transactions on Instrumentation and Measurement*, vol. 22, no. 1, pp. 2-8, Mar. 1973.
- [22] A. S. Sedra, K. C. Smith, *Microelectronic Circuits*, New York, NY, USA, Oxford University Press, 2004.
- [23] H. E. Abraham, R. G. Meyer, "Transistor Design for Low Distortion at High Frequencies", *IEEE Transactions on Electronic Devices*, vol. 23, no. 12, pp. 1290-1297, Dec. 1976.
- [24] A. I. Zverev, *Handbook of Filter Synthesis*, New York, NY, USA, John Wiley, 1967.
- [25] F. Fiori, P. S. Crovetti, "Nonlinear Effects of RF Interference in MOS Operational Amplifiers", *IEEE International Conference of Electronics, Circuits and Systems*, pp. 201-204, Feb. 2001.

- [26] F. Fiori, P. S. Crovetto, "Nonlinear Effects of Radio-Frequency Interference in Operational Amplifiers", *IEEE Transactions on Circuits and Systems*, vol. 49, no. 3, pp. 367-372, Mar. 2002.
- [27] J.-M. Redoute, M. Steyaert, "EMI resisting CMOS differential pair structure", *IET Electronics Letters*, vol. 42, no. 21, pp. 1217-1218, Oct. 2006.
- [28] J.-M. Redoute, M. Steyaert, "A CMOS source-buffered differential input stage with high EMI suppression", *34th European Solid-State Circuits Conference*, pp. 318-321, Oct. 2008.
- [29] H. S. Black, "Inventing the negative feedback amplifier", *IEEE Spectrum*, vol. 14, no. 12, pp. 5560, Dec. 1977.
- [30] P. Quinn, "Feed-forward Amplifier", *United States Patent 4146844*, Mar. 1979.
- [31] H. C. D. Graaff, F. M. Klaassen, *Compact Transistor Modelling for Circuit Design*; New York, NY, USA, Springer-Verlag, 1990.
- [32] Y. Tsvividis, *Operation and Modeling of the MOS Transistor*, 2nd ed., Boston, MA, USA, WCB/McGraw-Hill, 1998.
- [33] C. Enz, E. A. Vittoz, *Charge-Based MOS Transistor Modeling*, Chichester, England, John Wiley, 2006.
- [34] G. Merckel, J. Borel, N. Z. Cupcea, "An Accurate Large-Signal MOS Transistor Model for Use in Computer-Aided Design", *IEEE Transactions on Electron Devices*, vol. 19, no. 5, pp. 681-690, May 1972.
- [35] A. Vladimirescu, S. Liu, *The simulation of MOS integrated circuits using SPICE2*, Berkeley, CA, USA, University of California, 1980.
- [36] Keysight Technologies, Inc., "Advanced Design System (ADS)", *Home page*, Nov. 2018 (online). Available: <http://www.keysight.com/en/pc-1297113/advanced-design-system-ads>
- [37] Cadence Design Systems, Inc., "Cadence", *Home page*, Nov. 2018 (online). Available: <http://www.cadence.com>
- [38] C. C. McAndrew, J. A. Seitchik, D. F. Bowers, M. Dunn, M. Foisy, I. Getreu, M. McSwain, S. Moinian, J. Parker, D. J. Roulston, M. Schroter, P. van Wijnen, L.F. Wagner, "VBIC95, the Vertical Bipolar Inter-Company Model", *IEEE Journal of Solid-State Circuits*, vol. 31, no. 10, pp. 1476-1483, Oct. 1996.
- [39] J. C. J. Paasschens, W. J. Kloosterman, *The Mextram Bipolar Transistor Model*, Eindhoven, The Netherlands, Koninklijke Philips Electronics N.V., 2002.

- [40] B. J. Sheu, D. L. Scharfetter, P.-K. Ko, M.-C. Jeng, "BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors", *IEEE Journal of Solid-State Circuits*, vol. 22, no. 4, pp. 558-566, Aug 1987.
- [41] L. J. Giacoletto, "Study of P-N-P Alloy Junction Transistor from D-C through Medium Frequencies", *RCA Review*, vol. 15, no. 4, pp. 506-563, Dec. 1954.
- [42] D. J. Roulston, *An Introduction to the Physics of Semiconductor Devices*, New York, NY, USA, Oxford University Press, 1999.
- [43] P. R. Gray, R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed., New York, NY, USA, Wiley, 1993.
- [44] C. C. Ens, F. Krummenacher, E. A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications", *Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 83-114, Jul. 1995
- [45] W. A. Serdijn, C. J. M. Verhoeven, A. H. M. van Roermund, *Analog IC Techniques for Low-Voltage Low-Power Electronics*, Delft, The Netherlands, Delft University Press, 1995.
- [46] H. C. Poon, H. K. Gummel, "Modeling of emitter capacitance", *Proceedings of the IEEE*, vol. 57, no. 12, pp. 2181-2182, Dec. 1969.
- [47] E.H. Nordholt, *Design of High-Performance Negative-Feedback Amplifiers*, Delft, The Netherlands, VSSD, 1983.
- [48] M. Schetzen, *The Volterra and Wiener Theories of Nonlinear Systems*, New York, NY, USA, Wiley, 1980.
- [49] M. Lantz, *Systematic design of linear feedback amplifiers*, Lund, Sweden, Bloms i Lund, 2002.
- [50] Maplesoft, "Maple - The Essential Tool for Mathematics", *Product review page*, Feb. 2019 (online). Available: <https://www.maplesoft.com/products/maple/>
- [51] W. Sansen, "Distortion in Elementary Transistor Circuits", *IEEE Transactions on Circuits and Systems - II*, vol. 46, no. 3, pp. 315-325, Mar. 1999.
- [52] E. H. Nordholt, *Design of High-Performance Negative Feedback Amplifiers*, Delft, The Netherlands, Delft University Press, 2000.
- [53] P. L. Kirby, "The Non-linearity of Fixed Resistors", *Electronic Engineering*, vol. 37, no. 453, pp. 722-726, Nov. 1965.
- [54] P. Gonon, C. Vallée, "Understanding capacitance-voltage nonlinearities in microelectronic metal-insulator-metal (MIM) capacitors", *11th International Conference on the Properties and Applications of Dielectric Materials*, 2015.

- [55] D. S. Campbell, J. A. Hayes, *Capacitive and resistive electronic components*, Yverdon, Switzerland, Gordon and Breach, 1994.
- [56] H. W. Bode, *Network Analysis and Feedback Amplifier Design*, Princeton, NJ, USA, D. van Nostrand, 1945.
- [57] D. J. Roulston, *An Introduction to the Physics of Semiconductor Devices*, New York, NY, USA, Oxford University Press, 1999.
- [58] K. R. Laker, W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems*, Hightstown, NJ, USA, McGraw-Hill, 1994.
- [59] J. M. Redouté, A. Richelli, "A Fundamental Approach to EMI Resistant Folded Cascode Operational Amplifier Design", *Proceedings of the 2013 International Symposium on Electromagnetic Compatibility*, pp. 203-208, Sept. 2013.
- [60] P. S. Crovetto, F. Fiori, "A CMOS Opamp Immune to EMI with no Penalty in Baseband Operation", *IEICE International Symposium on Electromagnetic Compatibility*, pp. 533-536, July 2009.
- [61] M. Reisch, *High-Frequency Bipolar Transistors*, Berlin, Germany, Springer-Verlag, 2003.
- [62] F. Fiori, "Investigation on the Susceptibility of Two-Stage Voltage Comparators to EMF", *8th Workshop on Electromagnetic Compatibility of Integrated Circuits*, pp. 241-244, Nov. 2011.
- [63] F. Fiori, "A New Nonlinear Model of EMI-induced Distortion Phenomena in Feedback CMOS Operational Amplifiers", *IEEE Transactions on Electromagnetic Compatibility*, vol. 44, no. 4, pp. 495-502, Nov. 2002.
- [64] A. Richelli, L. Colalongo, Z. M. Kovács-Vajna, "Increasing the Immunity to Electromagnetic Interferences of CMOS OpAmps", *IEEE Transactions on Reliability*, vol. 52, no. 3, pp. 349-353, Sept. 2003.
- [65] G. Setti, N. Speciale, "Design of a Low EMI Susceptibility CMOS Transimpedance Operational Amplifier", *Microelectronics Reliability*, vol. 38, no. 6, pp. 1143-1148, Aug. 1998.
- [66] A. Richelli, "Design Considerations for an Ultra-Low Voltage Amplifier With High EMI Immunity", *15th IEEE International Conference on Electronics, Circuits and Systems*, pp. 558-561, Aug. 2008.
- [67] A. M. Niknejad, R. G. Meyer, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF IC's", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1470-1481, Oct. 1998.
- [68] J. R. Long, "On-Chip Transformer Design and Application to RF and mm-Wave Front-Ends", *2017 IEEE Custom Integrated Circuits Conference*, pp. 1-43, Apr. 2017.

- [69] C. J. Galbraith, T. M. Hancock, G. M. Rebeiz, "A Low-Loss Double-Tuned Transformer", *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 11, pp. 772-774, Nov. 2007.
- [70] T. Biondi, A. Scuderi, E. Ragonese, G. Palmisano, "Analysis and Modeling of Layout Scaling in Silicon Integrated Stacked Transformers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 5, pp. 2203-2210, May 2006.
- [71] A. H. M. van Roermund, H. Casier, M. Steyaert, *Analog Circuit Design*, Dordrecht, The Netherlands, Springer, 2006.
- [72] G. P. Reitsma, M. H. L. Kouwenhoven, A. Mosterd, "A Low-Power Microphone Preamplifier with EMI Canceling", *Proceedings of the 26th European Solid-State Circuits Conference*, pp. 296-299, Sept. 2000.
- [73] F. Fiori, "Operational Amplifier Input Stage Robust to EMI", *Electronics Letters*, vol. 37, no. 15, pp. 930-931, July 2001.
- [74] P. S. Croveti, "Operational Amplifier Immune to EMI with no Baseband Performance Degradation", *Electronics Letters*, vol. 46, no. 3, pp. 207-208, Feb. 2010.
- [75] A. Richelli, "Increasing EMI Immunity in Novel Low-Voltage CMOS OpAmps", *IEEE Transactions on Electromagnetic Compatibility*, vol. 54, no. 4, pp. 947-950, Aug. 2012.
- [76] A. Richelli, "EMI Susceptibility of DTMOS Opamps", *Electronics Letters*, vol. 49, no. 2, pp. 98-99, Jan. 2013.
- [77] B. E. Hofer, "Distortion Reduction Circuit for an Inverting Feedback Amplifier", *United States Patent 4296381*, Oct. 1981.
- [78] G. Ferrari, F. Gozzini, M. Sampietro, "A Current-Sensitive Front-End Amplifier for Nano-Biosensors with a 2 MHz BW", *IEEE International Solid-State Circuits Conference*, pp. 164-165, Feb. 2007.
- [79] J. Hu, Y. B. Kim, J. Ayers, "A low power 100 M Ω CMOS front-end transimpedance amplifier for biosensing applications", *53rd IEEE International Midwest Symposium on Circuits and Systems*, pp. 541-544, Aug. 2010.
- [80] J. Salvia, P. Lajevardi, M. Hekmat, B. Murmann, "A 56 M Ω CMOS TIA for MEMS applications", *IEEE Custom Integrated Circuits Conference*, pp. 199-202, Sept. 2009.
- [81] Y. Tang, Y. Zhang, G. K. Fedder, L. R. Carley, "A Dual Probe STM Imaging System and a Low Noise Switched-Capacitor Transimpedance Amplifier", *IEEE Sensors Journal*, vol. 13, no. 8, pp. 2984-2992, Jul. 2013.

- [82] R. Budhiraja, P. Pundir, S. M. R. Hasan, "A 90nm CMOS transimpedance amplifier design for nanopore based DNA nucleotide sequencer", *19th International Conference on Mechatronics and Machine Vision in Practice*, pp. 146-149, Nov. 2012.
- [83] W. M. Snelgrove, A. Shoval, "A Balanced 0.9- μm CMOS Transconductance-C Filter Tunable over the VHF Range", *IEEE Journal of Solid-State Circuits*, vol. 27, no. 3, pp. 314-323, Mar. 1992.
- [84] A. Katz, D. Chokola, J. Wood, "The Evolution of PA Linearization: From Classic Feedforward and Feedback Through Analog and Digital Predistortion", *IEEE Microwave Magazine*, vol. 17, no. 2, pp. 32-40, Feb. 2016.
- [85] F. L. Neerhoff, *Elektrische Circuits*, vol. 2, Delft, The Netherlands, Delftse Universitaire Pers, 1996.
- [86] ANSYS, Inc., "ANSYS HFSS: High Frequency Electromagnetic Field Simulation", *Product review page*, Apr. 2018 (online). Available: <http://www.ansys.com/products/electronics/ansys-hfss>
- [87] Vishay Intertechnology, Inc., "High Frequency Resistor, Thin Film Surface Mount Chip", *Data sheet*, Feb. 2015 (online). Available: <http://www.vishay.com/resistors-fixed/list/product-60093>
- [88] Intersil Corporation, "HFA3046, HFA3096, HFA3127, HFA3128", *Data sheet*, Aug. 2015 (online). Available: <http://www.intersil.com/content/dam/Intersil/documents/hfa3/hfa3046-3096-3127-3128.pdf>

Summary

A study of the out-of-band interference of negative-feedback amplifiers is carried out in this thesis. Several design methods to reduce the susceptibility to interference are identified and developed. The proposed techniques are based on robust circuits and topologies that are suitable for monolithic integration.

Out-of-band interference is caused by the non-linear behaviour of the components in amplifier circuits, as detailed in Chapter 1. To address that, it is necessary to develop amplifiers with a low IP_2 figure, i.e., apply linearisation. Chapter 2 gives an overview of the existing linearisation techniques and other methods to reduce the effect of non-linear behaviour. A mathematical analysis of a generic negative-feedback amplifier is conducted in Chapter 3 using the Volterra series. As this method often involves complex, cumbersome calculations, a simplified approach is introduced in Chapter 4. Using both the classical and the simplified non-linear analysis tools, a number of new design methods for out-of-band interference immunity enhancement are developed in Chapter 5. These make use of frequency-dependent local feedback, pole position manipulation and non-linear local-feedback compensation. Finally, a design example of non-linear local-feedback compensation in a negative-feedback amplifier is presented in Chapter 6.

Samenvatting

In dit proefschrift is de gevoeligheid van tegengekoppelde versterkers voor storingen afkomstig van buiten de signaalband behandeld. Om de storingsgevoeligheid te verlagen, zijn enkele ontwerptechnieken geformuleerd en uitgewerkt. De voorgestelde technieken zijn gebaseerd op robuuste schakelingen en topologieën die geschikt zijn voor monolithische integratie.

Het niet-lineaire gedrag van de componenten in versterkercircuits is de oorzaak van de storingsgevoeligheid voor signalen afkomstig van buiten de signaalband, zoals beschreven in Hoofdstuk 1. Daarom is het noodzakelijk om versterkers met een laag IP_2 getal oftewel gelineariseerde versterkers te ontwikkelen. Hoofdstuk 2 geeft een overzicht van de bestaande linearisatiemethoden en andere technieken om niet-lineair gedrag te onderdrukken. Een wiskundige analyse van een generieke tegengekoppelde versterker is uitgevoerd in Hoofdstuk 3 met behulp van de Volterra reeksen. Omdat zulke berekeningen vaak zeer complex en onoverzichtelijk kunnen zijn, is een vereenvoudigde rekenmethode ingevoerd in Hoofdstuk 4. Met behulp van zowel de klassieke als de vereenvoudigde rekentechnieken, zijn nieuwe ontwerpregels opgesteld in Hoofdstuk 5, die tot een verminderde storingsgevoeligheid leiden. Deze maken gebruik van frequentieafhankelijke lokale terugkoppeling, poolfrequentie manipulatie en compensatie van niet-lineaire lokale terugkoppeling. Tot slot is een praktische toepassing van de compensatie van niet-lineaire lokale terugkoppeling in een tegengekoppelde versterker gedemonstreerd in Hoofdstuk 6.

About the author

Emil Totev was born on May 24, 1975 in Sofia, Bulgaria. In 2002 he received the Ir. degree in Electrical Engineering from Delft University of Technology in the Netherlands. He has been involved in development of analog and mixed-signal circuitry, as well as RF electronics. Currently, he is occupied with research and development of sensor interface circuitry for biochemical analysis and other medical applications at Philips Research in the Netherlands.