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Characterization, Modeling and Test of Synthetic Anti-Ferromagnet Flip Defect in STT-MRAMs

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***Abstract*—Understanding the manufacturing defects in magnetic tunnel junctions (MTJs), which are the data-storing elements in STT-MRAMs, and their resultant faulty behaviors are crucial for developing high-quality test solutions. This paper introduces a new type of MTJ defect: synthetic anti-ferromagnet flip (SAFF) defect, wherein the magnetization in both the hard layer and reference layer of MTJ devices undergoes an unintended flip to the opposite direction. Both magnetic and electrical measurement data of SAFF defect in fabricated MTJ devices is presented; it shows that such a defect reverses the polarity of stray field at the free layer of MTJ, while it has no electrical impact on the single isolated device. The paper also demonstrates that using the conventional fault modeling and test approach fails to appropriately model and test such a defect. Therefore device-aware fault modeling and test approach is used. It first physically models the defect and incorporate it into a Verilog-A MTJ compact model, which is afterwards calibrated with silicon data. The model is thereafter used for fault analysis and modeling within an STT-MRAM array; simulation results show that a SAFF defect may lead to a transient passive neighborhood pattern sensitive fault (tPNPSF) when all neighboring cells are in logic '1' state. Finally, test solutions for such fault are discussed.**

***Index Terms*—Device-aware test, STT-MRAMs, manufacturing defects, fault models**

I. Introduction

As one of the most promising non-volatile memory technologies, spin-transfer torque magnetic random access memory (STT-MRAM) offers competitive write/read performance, endurance, density, retention, and power consumption [1]. The tunability of these aspects makes it customizable as both embedded and discrete memory solutions for a variety of applications such as Internet-of-Things (IoT), automotive, aerospace, and last-level caches [2]. Therefore, STT-MRAM technology has received a large amount of attention for commercialization from major semiconductor companies such as TSMC [2], Samsung [3], Intel [4], and SK hynix [5]. To enable STT-MRAM mass production, high-quality yet cost-efficient manufacturing test solutions are crucial to ensure the required quality of products being shipped to end customers. The STT-MRAM manufacturing process involves not only conventional CMOS process but also MTJ fabrication and integration [3]. The latter is more vulnerable to defects as it requires deposition, etch, and integration of magnetic materials with new tools [6]. A blind application of conventional tests for existing memories such as SRAMs and DRAMs to STT-MRAMs may lead to test escapes and yield loss. Therefore, understanding the unique MTJ defects and modeling them accurately for high-quality test solutions is of great importance.

STT-MRAM testing is still an on-going research topic. Several fault models such as multi-victim, kink, and write destructive faults [7,8] were proposed for field-driven MRAMs. However, these fault models are not applicable to current-driven STT-MRAMs. Chintaluri *et al.* [9] derived fault models such as transition faults and read disturb faults in STT-MRAM arrays by simulating the impact of resistive defects in the presence of process variations; a March algorithm and its built-in-self-test implementation were also introduced. Nair *et al.* [10] performed layout-aware defect injection and fault analysis, whereby they observed dynamic incorrect read fault. Nevertheless, all these papers assumed that STT-MRAM defects including those in MTJ devices are equivalent to linear resistors without any justification. Recently, Wu *et al.* [11] presented both experimental data and simulation results of pinhole defects in MTJ devices, and demonstrated that modeling pinhole defects as linear resistors is inaccurate and results in wrong fault models. As a solution to address the limitations of the traditional fault modeling approach, Fieback *et al.* [12] proposed the concept of *Device-Aware Test* (DAT), a step beyond cell-aware test. The DAT approach models physical defects accurately by incorporating the impact of such defects into the technology parameters and subsequently into the electrical parameters of the device. With the obtained defective device model, a systematic fault analysis can be conducted to develop realistic fault models; these are then used to develop test solutions.

This paper discovers (based on silicon data measurements) a new unique defect in MTJ devices, referred to as *Synthetic Anti-Ferromagnet Flip (SAFF)*, and applies the device-aware test approach to develop accurate fault models presenting the way the defect manifests itself at the functional level. The synthetic anti-ferromagnetic structure [1,13] is widely-used in MTJ stack designs to strongly pin the magnetization in the reference layer (RL), which is anti-ferromagnetically coupled to the hard layer (HL). A SAFF defect occurs when the magnetization of the HL undergoes an undesired flip, which in turn leads to a flip in the magnetization in the RL due to their anti-ferromagnetic coupling relation. The main contributions of this paper are as follows.

- Discover a new STT-MRAM-specific defect based on *silicon measurements*; the defect is referred to as SAFF.
- Present magnetic and electrical characterization of MTJ devices with the SAFF defect.

- Demonstrate the conventional fault modeling approach fails to derive fault models which accurately represent the SAFF defect; Hence, this approach cannot result in a test which guarantees the detection of this defect.
- Apply the device-aware test approach to develop a unique and accurate fault model for the SAFF defect, and appropriate test solutions.

The rest of this paper is organized as follows. Section II provides a background for STT-MRAM technology. Section III presents characterization results of SAFF defect. Section IV discuses the testing of the SAFF defect using the conventional approach which models defects as linear resistors. Section V, Section VI, and Section VII use the DAT approach to physically model the SAFF defect, generate associated fault models, and develop test solutions, respectively. Section VIII concludes this paper.

II. Background

A. MTJ Device Organization

Magnetic Tunnel Junction (MTJ) is the fundamental component of STT-MRAMs acting as the data-recording element where one-bit data is coded into the relative magnetization directions of ferromagnetic layers. Fig. 1a shows its stack organization which fundamentally comprises four layers [13].

1) ***Free Layer (FL)****:* This is the top layer which is composed of CoFeB-based materials. The typical thickness of FL is 1.5 nm [13]. The FL's magnetization can be reversed by a spin-polarized current going through it. The *saturation magnetization* $M_{\rm s}$ and *magnetic anisotropy field* $H_{\rm k}$ are two key technology parameters determining the *thermal stability factor* Δ as well as the switching characteristics of the FL [14], as listed in Table I.

2) ***Tunnel Barrier (TB)****:* This is the MgO dielectric layer below the FL. As the TB layer is ultra-thin, typically ∼1 nm [13], electrons have chance to tunnel through it overcoming its *potential barrier height* $\bar{\varphi}$ [6]. This makes the device behave as a tunneling-like resistor. To compare the sheet resistivity of different MTJ designs, the *Resistance-Area* (RA) product [14] is used. This is a figure of merit which is commonly used in MRAM community, and it is independent on device size.

3) ***Reference Layer (RL)****:* This layer is also based on the CoFeB material, typically 2 nm in thickness. The RL has a fixed magnetization at certain direction to provide a reference to the magnetization in the FL, as shown in the device schematic. Due to the *Tunneling Magneto-Resistance* (TMR) effect [14], the MTJ's resistance is relative low ($R_{\rm P}$) when the magnetization of the FL is parallel to that of the RL, and it is relative high ($R_{\rm AP}$) when in anti-parallel state.

4) ***Hard Layer (HL)****:* This is the bottom Co/Ni-based layer (∼5 nm) and its function is to strongly pin the magnetization in the RL by means of the *Anti-Ferromagnetic Coupling* (AFC) effect [13]. In addition, the stray field from the HL is utilized to partially cancel out the stray field from the above RL.

It is worth noting, and as Fig. 1a shows, that the RL and HL together form a *Synthetic Anti-Ferromagnet* (SAF) structure [13], which sometimes is also referred to as *Pinned Layer* (PL) as a whole. Despite the SAF structure ensures better compensation of stray fields from RL and HL at FL, a net *intra-cell stray field* $\boldsymbol{H_{\rm s\_intra}}$ may still exist at FL. Its magnitude depends on the stack design, device size, etc [15]. It has been shown that its out-of-plane component $H^z_{\rm s\_intra}$ (see Fig. 1a) has a significant impact on the device's performance, while its in-plane component $H^{x-y}_{\rm s\_intra}$ has a negligible influence [15]. Additionally, the *inter-cell stray field* $H^z_{\rm s\_inter}$ (out-of-plane component) from neighboring cells also plays a role in dense STT-MRAM arrays [16,17]. Thus, the overall stray field $H^z_{\rm stray} = H^z_{\rm s\_intra} + H^z_{\rm s\_inter}$ at the FL of MTJ device is also a key technology parameter.

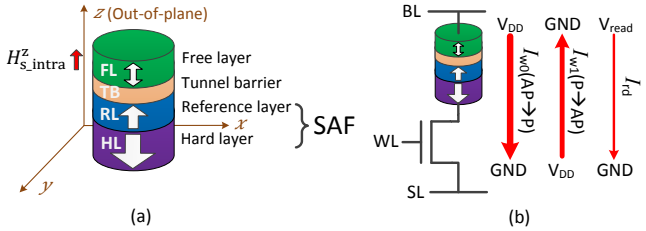

Fig. 1. (a) Simplified MTJ stack, (b) 1T-1MTJ cell and its access operations.

TABLE I
STT-MRAM KEY PARAMETERS.

Technology Parameters		Electrical Parameters	
$M_{\rm s}$	Saturation magnetization of the FL	$R_{\rm P}$	Resistance in P state
$H_{\rm k}$	Magnetic anisotropy field of the FL	$R_{\rm AP}$	Resistance in AP state
$\bar{\varphi}$	Potential barrier height of the TB	$I_{\rm c}$(P→AP)	P→AP critical switching current
RA	Resistance-area product	$I_{\rm c}$(AP→P)	AP→P critical switching current
TMR	Tunneling magneto-resistance ratio	$t_{\rm w}$(P→AP)	P→AP switching time
$H^z_{\rm stray}$	Stray field at the FL	$t_{\rm w}$(AP→P)	AP→P switching time

B. 1T-1MTJ Cell Design

Fig. 1b shows a bottom-pinned 1T-1MTJ memory cell and its corresponding voltage configurations for read/write (R/W) operations. The three-terminal cell includes an MTJ device (storage element) and an NMOS transistor (access selector). The three terminals are connected to a bit line (BL), a source line (SL), and a word line (WL), as shown in the figure.

The voltages on the BL and SL control R/W operations on the cell when the WL is asserted. For instance, a write '0' operation requires the BL at $V_{\rm DD}$ and the SL grounded, which leads to a current $I_{\rm w0}$ flowing from BL to SL. In contrast, a current $I_{\rm w1}$ with the opposite direction flows through the cell during a write '1' operation. To guarantee a successful transition of the MTJ state, the magnitude of write current (both $I_{\rm w0}$ and $I_{\rm w1}$) has to be larger than the MTJ's *critical switching current* $I_{\rm c}$. The larger the current above $I_{\rm c}$, the faster the switching can be. Due to the bias dependence of STT efficiency and stray fields [14], $I_{\rm c}$(P→AP) can be significantly different from $I_{\rm c}$(AP→P) in practice. It is worth noting that the *actual switching time* $t_{\rm w}$ under a fixed pulse varies from cycle to cycle since the STT-induced magnetization switching is intrinsically stochastic [1]. During a read operation, a significantly smaller voltage $V_{\rm read}$ than $V_{\rm DD}$ is applied on the BL to draw a read current $I_{\rm rd}$, which can be as small as ∼10 µA or $0.06I_{\rm c}$ [18], to read the resistive state of the MTJ device by a sense amplifier.

Table I lists the key technology and electrical parameters of MTJ device to be used for the DAT-based defect modeling.

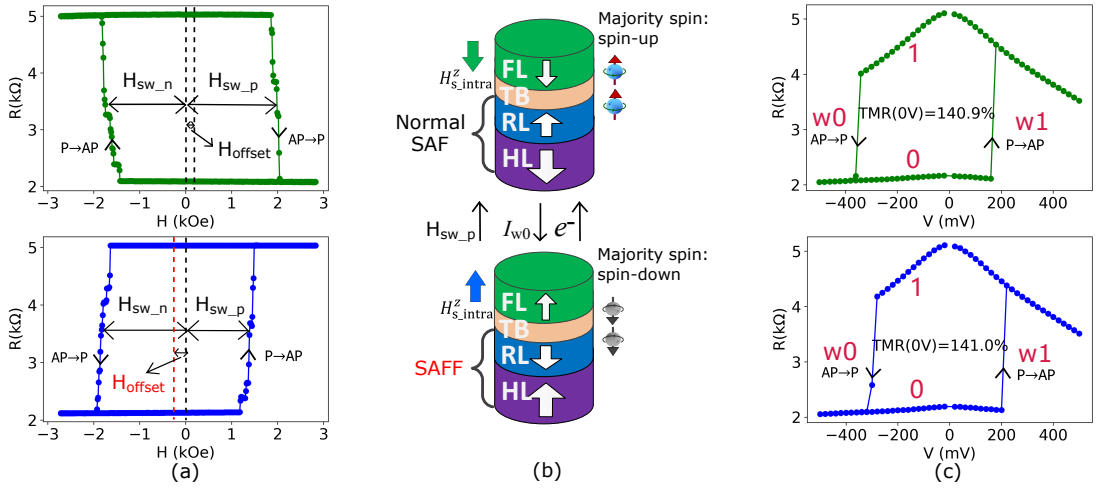

Fig. 2. Comparison between a defect-free MTJ (upper) and a SAFF-defective MTJ (lower) with the same nominal size eCD=55 nm: (a) R-H loop, (b) schematic of AP state, and (c) R-V loop.

III. Defect Characterizations of SAFF

We did comprehensive magnetic and electrical characterization on MTJs with diameters ranging from 35 nm to 175 nm on four wafers. We observed a small fraction of devices across different sizes with *horizontally* flipped R-H loops and *normal* R-V loops. We attribute the root cause to the flip of magnetization in both HL and RL, which we name as *Synthetic Anti-Ferromagnet Flip* (SAFF) defect in this paper. Next, we will present both magnetic and electrical measurement data of a representative SAFF-defective device as well as a defect-free device for the purpose of comparison. Thereafter, we briefly review the SAFF defect and its potential causes.

A. Magnetic Characterization

Measurement of the R-H hysteresis loop of MTJ device is a useful and fast technique to characterize the device's magnetic properties such as the *coercivity* H_c (defined as the reverse field needed to drive the magnetization of a ferromagnet to zero [15]) and $H^z_{s\_intra}$. In this measurement, a perpendicular magnetic field is applied to the device and swept in the range of +/-3 kOe. We monitor the resistance of the MTJ device at every value of the applied field using a small sense current. At certain threshold field, the magnetization of the FL reverses from its initial direction resulting in an abrupt shift in the resistance of the MTJ (i.e., $R_P \rightarrow R_{AP}$ or $R_{AP} \rightarrow R_P$).

Fig. 2a shows the measured R-H hysteresis loops (averaged over ten cycles) of a defect-free device (upper) and a defective device (lower), with the same size eCD=55 nm; eCD stands for *electrical Critical Diameter* which is used to describe the MTJ size as a common practice in the MRAM community [2,19]. Due to the existence of $H^z_{s\_intra}$ at the FL, the *positive* switching field H_{sw_p} and the *negative* switching field H_{sw_n} are asymmetric. The R-H loop of the defect-free device shifts to the right side, which is reflected by the offset field $H_{offset} = \frac{1}{2}(H_{sw\_p} + H_{sw\_n})$ marked in the figure. Therefore, $H^z_{s\_intra} = -H_{offset}$ and $H_c = \frac{1}{2}(H_{sw\_p} - H_{sw\_n})$. In contrast, the defective device shows a horizontally flipped R-H loop which shifts to the left side rather than the right side. This indicates that the *polarity* of $H^z_{s\_intra}$ *reverses* for the defective device while its *coercivity* H_c is *not influenced*. In addition, the switching direction (i.e., AP→P or P→AP) also flips for a given switching field. For example, a positive field H_{sw_p} induces a P→AP transition for the defective device while it leads to an AP→P transition for the defect-free device, as illustrated in the figure. Based on these observations, it is clear that the magnetization in the RL of the defective device flips to the opposite direction in comparison to the defect-free device, as illustrated with the device schematics in Fig. 2b. Due to the AFC relation between the RL and HL, the latter also flips to the opposite direction.

B. Electrical Characterization

Apart from the R-H loops, we also measured the R-V loops of the same devices; the results are shown in Fig. 2c. During the measurements, a ramped DC current was applied flowing through the device under test to switch its state. It can be seen that the R-V loop of the SAFF-defective device has the same shape and follows the same switching directions as the defect-free device; their R_P, R_{AP}, and TMR values at 0 V are almost the same. However, one can clearly see there is a marginal shift in the switching voltage, which could be attributed to the intrinsic switching stochasticity and process variations.

The STT-switching mechanisms in both cases can be explained theoretically as follows. Fig. 2b shows the schematics of a defect-free device (upper) and a SAFF-defective device (lower) with both in AP state. In case of AP→P switching, a write current I_{w0} is applied from the FL to HL; note that electrons flow in the opposite direction from the HL to FL as illustrated in the figure. For the defect-free MTJ device, the RL polarizes the incoming electrons to align with its magnetization direction, making spin-up the majority spin. Once the spin-up electrons tunnel through the MgO-based TB, they exert a torque on the FL, thereby switching its magnetization to the opposite direction. For the SAFF-defective device, spin-down becomes the majority spin, as the magnetization in the

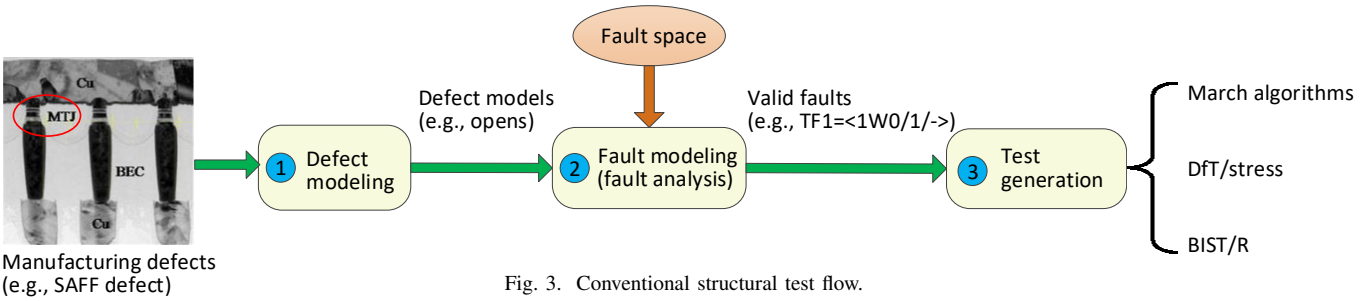

Fig. 3. Conventional structural test flow.

RL (spin polarizer) flips with the HL. Therefore, it is the majority spin which switches the magnetization of the FL in both cases. This indicates that the critical switching current I_c would not change if the magnetizations in the RL and HL flipped for a single MTJ device. More details about the STT-switching principle can be found in [1].

C. SAFF Defect Mechanism and Potential Causes

Given the strong AFC strength between the HL and RL (>10 kOe measured by vibrating sample magnetometer (VSM) [1]) for our devices and the RL flip observed in Fig. 2a, a probable cause of the SAFF defect is an initial HL reversal. Due to inhomogeneities arising during device fabrication steps, HL with significantly reduced H_c may exist in certain outlier devices. Based on the measurement results presented previously, the SAFF defect has no impact on the switching current direction. However, the polarity of $H^z_{s\_intra}$ is reversed by the defect, compared to defect-free devices. This may affect the way the SAFF-defective MTJ manifests itself at the functional level in an STT-MRAM array. Hence, modeling the SAFF defect and analyzing its impact at the behavior level is a must in order to develop appropriate test solutions if needed.

IV. Conventional Test Development for SAFF Defect

Fig. 3 shows the conventional structural approach used to develop test solutions for memories and integrated circuits in general; it consists of three steps: 1) defect modeling, 2) fault modeling, and 3) test generation. Next, we will apply this test approach to a SAFF defect by following these three steps; note that this approach assumes that a defect can be modeled as a series or parallel resistor. We will analyze the faulty behavior of memory cell in the presence of resistive defects and derive fault models, and thereafter a test solution. Finally, we will show the generated test solution fails to detect the SAFF defect, meaning that the traditional test approach is inappropriate for SAFF defect.

A. Defect Modeling

Defect modeling abstracts physical defects and presents them at electrical level so as to be processed by circuit simulators such as SPICE. Conventionally, the most prevalent defect models are linear resistors, namely opens, shorts, and bridges, as can be found in [7–10,20]. An open represents an undesired extra resistor within a connection. Similarly, a short represents an undesired resistive path between a node

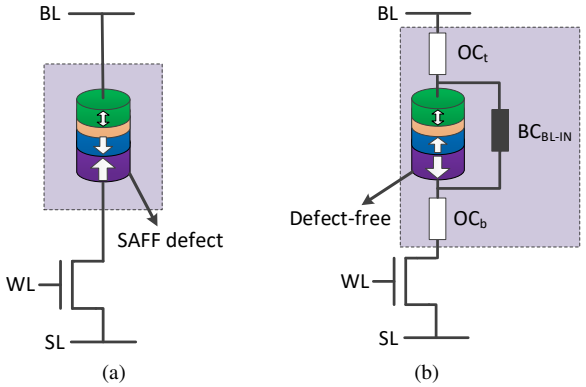

Fig. 4. STT-MRAM cell with (a) a SAFF defect in the MTJ device and (b) its resistive models.

and the power supply (i.e., GND or V_{DD}) whereas a bridge connects two individual nodes excluding the power supply. In all these resistive models, the resistance value is used to represent the physical defect size or strength. Fig. 4a shows an STT-MRAM cell with a SAFF-defective MTJ device. As the SAFF defect resides in the MTJ device, we can model it by the following three resistive models as shown in Fig. 4b: 1) an open OC_t between the MTJ device and BL, 2) an open OC_b between the MTJ device and the NMOS selector, and 3) a bridge $BC_{BL\text{-}IN}$ between the two terminals of the MTJ device. Note that the MTJ device here is considered defect-free. In other words, resistive models assume that the physical defects in MTJ devices manifest themselves as the linear resistors shown in the figure.

B. Fault Modeling

The second step is fault modeling, which develops appropriate fault models describing the faulty behavior of a memory cell in the presence of a given defect. Typically, the fault modeling process consists of two sub-steps: 1) fault space definition and 2) fault analysis/validation. The former defines all possible faults theoretically. The latter validates realistic faults in the presence of the defect under investigation in the pre-defined fault space using SPICE-based circuit simulations. Next, we will work out these two steps for SAFF defect.

*1) **Fault space definition**:* Depending on the number of cells involved, memory faults can be classified into three classes as shown in Fig. 5 [21]: single-cell faults, two-cell faults (i.e., coupling faults), and multi-cell faults (i.e., neighborhood pattern sensitive faults). These faults can be systematically

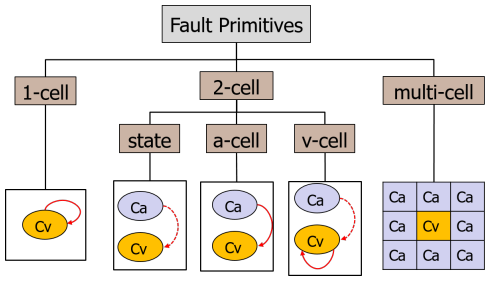

Fig. 5. Memory fault space considered for SAFF defect.

described by *fault primitive* (FP) notation [22]. An FP describes the deviation of the observed memory behavior from the expected one. For a *single-cell fault*, an operation on the addressed cell which is considered as the victim sensitizes this fault irrespective of neighboring cells. A single-cell fault can be denoted as a three-tuple $\langle S/F/R\rangle$, where

- S (sensitization) denotes the operation sequence that *sensitizes* the fault. $S\in\{0, 1, 0w0, 0w1, 1w0, 1w1, 0r0, 1r1\}$; '0' and '1' are logic values, 'r' and 'w' denote a read and a write operation, respectively.
- F (faulty effect) describes the value of the faulty cell after S is performed; $F\in\{0, 1\}$.
- R (readout value) describes the output of a read operation in case the last operation in S is a read. $R \in \{0, 1, -\}$ where '$-$' denotes that R is not applicable.

The following two examples illustrate the usage of this notation. $\langle$0w1/0/-$\rangle$ denotes a w1 operation to a cell containing '0' (S=0w1) fails, the cell remains in its initial value '0' (F=0), and the read output is not applicable (R=$-$). $\langle$0r0/0/1$\rangle$ denotes a r0 operation on a cell that holds '0' (S=0r0), where the cell remains in its correct state '0' (F=0) while the read output is '1' (R=1) instead of the expected '0'.

Coupling Faults (CFs) can be denoted as $\langle S_a; S_v/F/R\rangle$, where S_a denotes the sensitizing sequence or the state (i.e., 0 or 1) of the aggressor cell (Ca) while S_v denotes the sensitizing sequence or the state of the victim cell (Cv). CFs can be further divided into three groups as shown in Fig. 5: 1) state CFs, 2) a-cell CFs, and 3) v-cell CFs. A state CF has the property that the state of Ca (rather than an operation applied to Ca) pins Cv at a faulty state. An a-cell CF indicates that an operation to Ca causes a fault in Cv. A v-cell CF means that an operation applied to Cv while Ca is in a certain state induces a fault in Cv itself. An example of CF is $\langle$0w1;0/1/-$\rangle$, meaning that applying an up-transition operation ($S_a = 0w1$) to Ca causes Cv to flip from '0' to '1'; read (R=$-$) is not applicable.

For *Neighborhood Pattern Sensitive Faults* (NPSFs) which involve m cells (m>2), the above FP can be extended to $\langle S_{a_0}; ...; S_{a_{m-2}}; S_v/F/R\rangle$, where S_{a_i} ($i\in[0, m-2]$) indicates the sensitizing sequence or state of the aggressor cell a_i and S_v describes the sensitizing sequence or state of the Cv.

Given the above FP theory, the *entire* fault space can be obtained. It can be easily derived that the total number of possible *static* faults consist of 12 single-cell faults, 36 CFs and 15360 NPSFs. Static faults are faults caused by a sensitizing sequence consisting of *at most* one operation; otherwise, the fault is called dynamic fault [22].

TABLE II
STATIC FAULT MODELING RESULTS OF SAFF DEFECT USING RESISTIVE MODELS.

Defect model	Resistance (Ω)	Sensitized FP	FP name and abbreviation	Detection Condition
OC_t & OC_m	(466, 870]	⟨0r0/0/1⟩	Incorrect Read Fault: IRF0	⇕ (...0, r0, ...)
	(870, 1.6k]	⟨0r0/0/1⟩	Incorrect Read Fault: IRF0	⇕ (...0, r0, ...)
		⟨1w0/1/-⟩	Transition Fault: TF1	⇕ (...1, w0, r0, ...)
	(1.6k, +∞]	⟨0r0/0/1⟩	Incorrect Read Fault: IRF0	⇕ (...0, r0, ...)
		⟨1w0/1/-⟩	Transition Fault: TF1	⇕ (...1, w0, r0, ...)
		⟨0w1/0/-⟩	Transition Fault: TF0	⇕ (...0, w1, r1, ...)
$BC_{BL\text{-}IN}$	[0, 1.1k)	⟨1r1/1/0⟩	Incorrect Read Fault: IRF1	⇕ (...1, r1, ...)
		⟨1w0/1/-⟩	Transition Fault: TF1	⇕ (...1, w0, r0, ...)
		⟨0w1/0/-⟩	Transition Fault: TF0	⇕ (...0, w1, r1, ...)
	[1.1k, 3.1k)	⟨1r1/1/0⟩	Incorrect Read Fault: IRF1	⇕ (...1, r1, ...)
		⟨1w0/1/-⟩	Transition Fault: TF1	⇕ (...1, w0, r0, ...)

*2) **Fault analysis**:* Once the SAFF defect is modeled and the complete fault space is defined, the STT-MRAM netlist or layout with an injected defect model is simulated in a SPICE-based circuit simulator to validate corresponding fault models. Our fault analysis consists of seven steps: 1) circuit generation, 2) defect injection, 3) stimuli generation, 4) circuit simulation, 5) fault analysis, 6) fault primitive identification, and 7) defect strength sweep and repetition of step 2 to 6 until all defects are covered. To this end, we built up a 3×3 STT-MRAM array along with all necessary peripheral circuits. Each memory cell is composed of an MTJ device and an NMOS selector as shown in Fig. 1b. In our simulations, we used the Verilog-A MTJ compact model with eCD=35 nm presented in [11]; this model has been calibrated with silicon data. For the NMOS selector, we adopted the predictive technology model (PTM) [23] on 45 nm node. This transistor model was also utilized for building up peripheral circuits such as write drivers, sense amplifiers, and address decoders.

We first simulated the obtained netlist in Cadence's circuit simulator Spectre to verify the design as a defect-free case. Thereafter, we performed static fault analysis and validation of the static fault space defined previously (i.e., single-cell faults, CFs and NPSFs). We assume that the defective cell is located in the center of a 3×3 memory array; the other eight surrounding cells are defect-free. The data pattern in these eight cells were swept from 0 to 255 (in decimal form) to investigate NPSFs. As the SAFF defect resides in the MTJ device, we injected this defect into the netlist by adding one of the three resistors: OC_b, OC_t, and $BC_{BL\text{-}IN}$, as explained previously. The resistance was swept from 10^0 to $10^9\,\Omega$ using 45 steps which are equally distributed on a logarithmic scale. The same simulation was repeated for all sensitizing sequences before moving to the next resistive model.

Table II shows the results of static fault analysis; only a small subset of single-cell faults have been observed, no CF, neither NPSF. For each defect (e.g., OC_t) and strength/size (e.g., between $466\,\Omega$ and $870\,\Omega$), the sensitized FP (e.g., $\langle$0r0/0/1$\rangle$) and its name (e.g., *Incorrect Read Fault* (IRF)) as defined in [22] is given. Note that a single defect may cause different FPs, depending on its strength.

In conclusion, applying the conventional fault modeling approach to SAFF defect results in four FPs: IRF0, IRF1, TF1, and TF0.

C. Test Generation

The fault modeling results from the previous step are used to generate test solutions such as March algorithms. First, each sensitized FP is assigned its own detection condition, as shown in the last column in Table II. For instance, IRF0 requires a read operation on the faulty cell at state '0' to guarantee its detection, denoted as $\Updownarrow(...0, \mathrm{r0}, ...)$, where $\Updownarrow$ means that the detection condition does not depend on the addressing direction. The detection condition for TF1 is $\Updownarrow(...1, \mathrm{w0}, \mathrm{r0}, ...)$, meaning that a down-transition write followed by a read is enough to detect this fault, regardless of the addressing direction. The detection conditions of all sensitized FPs are compiled into the following optimal March test with three march elements:

$$\{\Updownarrow(\mathrm{w0}); \Uparrow(\mathrm{w1}, \mathrm{r1}); \Downarrow(\mathrm{w0}, \mathrm{r0})\}.$$

Note that different versions of March tests can be generated (e.g., with two march elements) as long as the test satisfies all the detection conditions.

D. Limitations of the Conventional Test Approach

We verified the effectiveness of the generated March algorithm on our fabricated devices. However, we observed that the test is not able to distinguish the SAFF-defective MTJs from defect-free ones. This conclusion can also be drawn by comparing the two R-V loops in Fig. 2c. In both defect-free and defective cases, the MTJ devices were initialized to state '0' with w0 operations. The loop starts with an up-transition (w1) operation followed by a down-transition (w0) operation. All the points in the two R-V loops are readout resistance (r0 or r1) under a voltage of 20 mV. It is clear that these two loops have the same shape and switching directions.

The above suggests that the FPs in Table II generated using the conventional fault modeling approach (and covered by our test) are *not qualified* to describe the actual faulty behavior of an STT-MRAM cell with the SAFF defect. As these FPs are derived by circuit simulations with the injection of resistive models, we can infer that the SAFF defect cannot be simply modeled as a linear resistor. As explained in Section III-C, the main change induced by the SAFF defect is that the polarity of the stray field at the FL is reversed. To capture the changes in the MTJ's magnetic properties, we need a more sophisticated defect modeling approach in replacement of the conventional resistor-based defect modeling approach.

V. Device-Aware Defect Modeling of SAFF

As an alternative to the conventional test approach, we will apply the Device-Aware Test (DAT) approach [12] to the SAFF defect in the remainder of this paper. The DAT approach consists of three steps as follows.

- ***Device-aware defect modeling***. Instead of modeling manufacturing defects in MTJs as linear resistors, the DAT approach integrates the defect effects into MTJ device model. This is achieved by first identifying and modifying the affected technology parameters of MTJ; thereafter, the impact is mapped into device's electrical parameters.

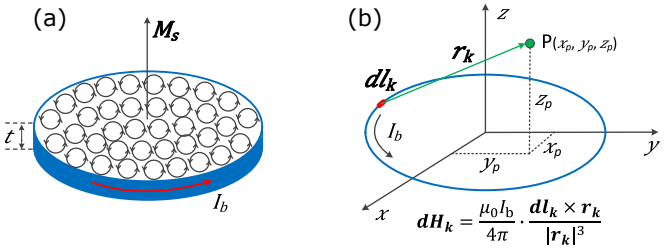

Fig. 6. Intra-cell stray field modeling principles: (a) Bound current theory and (b) Biot-Savart law.

- ***Device-aware fault modeling.*** This step defines the complete fault space for STT-MRAMs by expanding the conventional fault primitive notation. Subsequently, a systematic fault analysis based on circuit simulations is performed to validate realistic faults in the space in the presence of a device defect.
- ***Device-aware test development.*** The obtained accurate and realistic faults from the previous step are utilized to develop high-quality test solutions.

In this section, we will work out the first step for the SAFF defect. It consists of three sub-steps [12]: 1) physical defect modeling, 2) electrical modeling of defective device, 3) fitting and model optimization. Next, we will follow these three sub-steps to develop a physics-based model for the SAFF defect. To this end, we first model the impact of SAFF defect on the overall stray field H^z_{stray} (including both intra- and inter-cell stray fields) at the FL of the defective cell within a memory array; the rest of technology parameters in Table I are not impacted as suggested in Section III. Thereafter, its impact is mapped to MTJ's electrical parameters I_{c} and t_{w}; the MTJ resistance is not influenced by this defect. Finally, we calibrate the SAFF-defective MTJ compact model with silicon data.

A. Physical Defect Analysis and Modeling

1) Intra-cell stray field modeling: $H^z_{\mathrm{s\_intra}}$ in a single MTJ device can be physically modeled based on the bound current theory and Biot-Savart law [17,24]. For a thin ferromagnet (i.e., HL, RL, or FL), the generated field is identical to the field that would be produced by the bound current I_{b} [24], under the assumption that it is uniformly magnetized. I_{b} is a macroscopic current flowing around the boundary of the ferromagnet, as all internal molecular current loops cancel each other out while those at the edge are left uncanceled, as illustrated in Fig. 6a. The magnetic moment m of the ferromagnet is $m{=}I_{\mathrm{b}}{\cdot}A$, where A is the cross-sectional area. In addition, m can also be expressed as in [24]: $m{=}M_s{\cdot}A{\cdot}t$, where M_s is the saturation magnetization and t is the thickness of this ferromagnet. Therefore, one can easily derive $I_{\mathrm{b}} = M_s{\cdot}t$. Here, the $M_s{\cdot}t$ product can be measured at blanket film level by VSM measurements [1].

With the derived bound current I_{b} for each ferromagnet in the MTJ stack, the generated stray field at any point in the space can be calculated by the Biot-Savart law [17], as shown in Fig. 6b. In this way, we can calculate the out-of-plane component of the stray field at the FL from both HL ($H^z_{\mathrm{s\_HL}}$) and RL ($H^z_{\mathrm{s\_RL}}$). Thus, the net intra-cell stray field: $H^z_{\mathrm{s\_intra}} = H^z_{\mathrm{s\_HL}} + H^z_{\mathrm{s\_RL}}$.

2) Inter-cell stray field modeling: In addition to the intra-cell stray field from the device itself, all neighboring cells also produce stray fields acting on each other in a memory array. The magnitude of the inter-cell stray field $H^z_{\text{s\_inter}}$ depends on device size as well as array pitch [16,17]. Therefore, it is crucial to model and take into account $H^z_{\text{s\_inter}}$ especially when it comes to high-density STT-MRAM arrays at advanced technology nodes. To the end, we built up two 3×3 memory arrays (defect-free vs. defective) in Cartesian Coordinates to calculate $H^z_{\text{s\_inter}}$ at the FL of the central cell from all the eight neighboring cells. Fig. 7a shows a memory array consisting of nine defect-free MTJ devices, while Fig. 7c shows an array composed of eight defect-free devices (C0-C7) and a SAFF-defective device (C8) in the center. In both cases, C0-C3 are considered as *direct* neighbors with the same distance to C8; each of them produces an inter-cell stray field H_{dir} acting on C8 as illustrated in the figure. Similarly, C4-C7 are in symmetric *diagonal* positions; each of them exerts a field H_{dia} on C8. With the previously introduced stray field modeling approach, we can also calculate $H^z_{\text{s\_inter}}$ at the FL of victim cell C8 from C0-C7 as follows:

$$H^z_{\text{s\_inter}} = \sum_{i=0}^{7} (H^z_{\text{s\_HL}}(\text{C}i) + H^z_{\text{s\_RL}}(\text{C}i) + H^z_{\text{s\_FL}}(\text{C}i)). \quad (1)$$

For each cell, both the polarity and magnitude of $H^z_{\text{s\_HL}}$ and $H^z_{\text{s\_RL}}$ are fixed for a given design (i.e., device size and array pitch). However, the polarity of $H^z_{\text{s\_FL}}$ changes dynamically depending on the data stored in the MTJ device although its magnitude remains the same. As a result, $H^z_{\text{s\_inter}}$ depends on the *Neighborhood Pattern* (NP) in the eight neighboring cells C0-C7, denoted as NP_8. In the binary form, NP_8 can be expressed as: $[d_0, ..., d_7]_2$, where $d_i \in \{0, 1\}$ represents the data stored in cell Ci. NP_8 can also be denoted in the decimal form: $[n]_{10}$, where $n \in [0, 255]$.

3) Overall stray field: Fig. 7b shows the overall stray field ($H^z_{\text{stray}} = H^z_{\text{s\_intra}} + H^z_{\text{s\_inter}}$) at the FL of the defect-free cell C8 for the configuration of Fig. 7a at varying pitches with respect to three different eCD values representing device sizes. In our simulations, we set the minimum pitch to 1.5×eCD according to [25] for high-density STT-MRAMs and the maximum pitch to 200 nm which is adopted by Intel [4]. The shaded areas indicate all possible H^z_{stray} values depending on the NP_8 in C0-C7; the uppermost curve of each shaded area represents NP_8=255 (all in AP state), while the lowermost curve represents NP_8=0 (all in P state). It can also be seen that the magnitude of H^z_{stray} increases as eCD decreases (i.e., smaller MTJs) and the variation range of H^z_{stray} increases as the pitch goes down (i.e., MTJs become closer to each other). The red dotted lines mark $H^z_{\text{s\_intra}}$ for isolated devices.

In contrast, Fig. 7d shows H^z_{stray} at the FL of the SAFF-defective cell C8 in the configuration of Fig. 7c. It can be seen that the SAFF-defective cell experiences a *positive stray field* rather than a negative one in the defect-free case. In absolute number, H^z_{stray} in the presence of SAFF defect is much larger than that of the defect-free case, especially for smaller pitches; e.g., for eCD=20 nm at pitch=30 nm, H^z_{stray} increases by up to

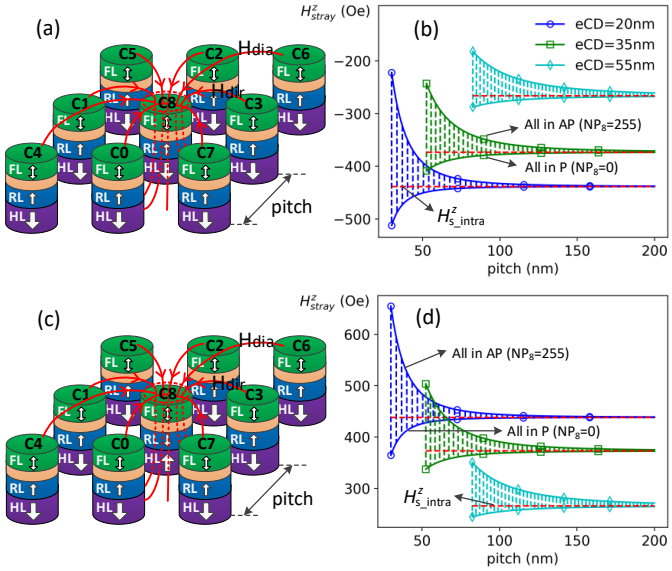

Fig. 7. (a) 3×3 array of all defect-free MTJs, (b) the overall out-of-plane stray field H^z_{stray} at the FL of the defect-free cell C8, (c) 3×3 array of eight defect-free MTJs (C0-C7) and a SAFF-defective cell C8 in the center, and (d) H^z_{stray} at the FL of the SAFF-defective cell C8.

70%. Furthermore, the magnitude of H^z_{stray} reaches the peak when NP_8=255 in the defective case, whereas the maximum H^z_{stray} occurs when NP_8=0 in defect-free case.

B. Electrical Modeling of SAFF-Defective MTJ Devices

With the obtained physics-based model of H^z_{stray}, we can map the SAFF-induced change in H^z_{stray} to the two key electrical parameters: I_{c} and t_{w}. Under the influence of stray field H^z_{stray}, I_{c} can be expressed as follows [14]:

$$I_{\text{c}}(H^z_{\text{stray}}) = \frac{1}{\eta}\frac{2\alpha e}{\hbar} M_{\text{s}} \cdot V \cdot H_{\text{k}} \cdot (1 + T \cdot \frac{H^z_{\text{stray}}}{H_{\text{k}}}), \quad (2)$$

$$T = (-1)^{j+l}, \quad j, l \in \{0, 1\}. \quad (3)$$

In Equation 2, η is the STT efficiency, α the magnetic damping constant, e the elementary charge, $\hbar$ the reduced Planck constant, M_{s} the saturation magnetization, V the volume of the FL, H_{k} the magnetic anisotropy field. We added the term T (see Equation 3) to identify the switching direction for both defect-free and defective devices; j=1(0) indicates a defective (defect-free) MTJ device. In addition, l=1(0) represents an AP→P (P→AP) switching direction. Consequently, one can derive I_{c}(AP→P)>I_{c}(P→AP) in both defect-free and defective cases, which is consistent with the experimental results and theoretical analysis in Section III-B. Note that the magnitude of I_{c}(AP→P) (or I_{c}(P→AP)) in the defective case differs from that in the defect-free case, since the H^z_{stray} magnitudes in the two cases are not same for a given eCD, pitch, and NP_8, as shown in Fig. 7b and Fig. 7d.

Furthermore, the switching time t_{w} in the precessional regime (namely, switched by the STT-effect) can be estimated

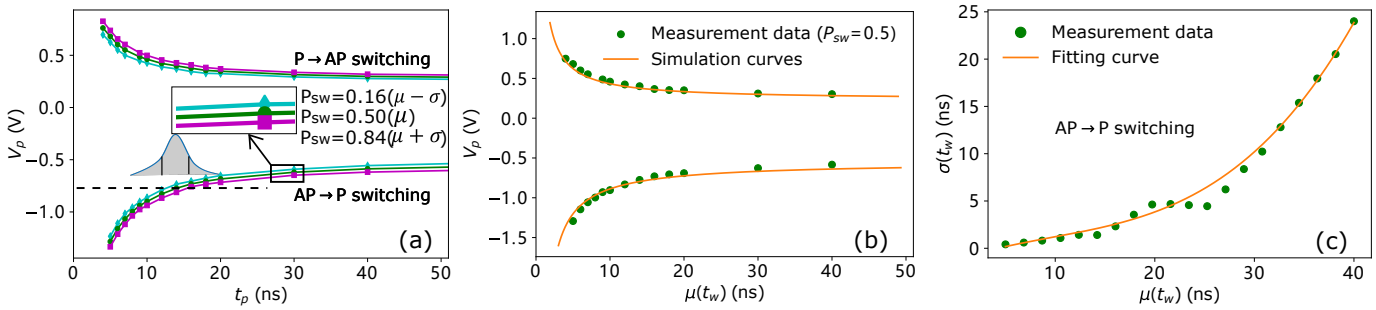

Fig. 8. (a) Measured pulse amplitude $V_{\rm p}$ vs. pulse width $t_{\rm p}$ in determining the switching behavior at switching probability $P_{\rm sw}$=0.16, 0.50, 0.84 for a SAFF-defective MTJ with eCD=35 nm, (b) Simulation results vs. measurement data at $P_{\rm sw}$=0.50, and (c) the extracted mean $\mu(t_{\rm w})$ and standard deviation $\sigma(t_{\rm w})$ of the AP→P switching time at different $V_{\rm p}$.

using the Sun's model as follows [11]:

$$\mu(t_{\rm w}) = \left(\frac{2}{C+\ln(\frac{\pi^2\Delta}{4})}\cdot\frac{\mu_{\rm B}P}{e\cdot m\cdot(1+P^2)}\cdot I_{\rm d}\right)^{-1}, \quad (4)$$

$$I_{\rm d} = \frac{V_{\rm p}}{R(V_{\rm p})} - I_{\rm c}(H^z_{\rm stray}), \quad (5)$$

$$t_{\rm w} \sim \mathcal{N}(\mu(t_{\rm w}),\, \sigma(t_{\rm w})^2). \quad (6)$$

Here, $C{\approx}0.577$ is Euler's constant, Δ the thermal stability factor, $\mu_{\rm B}$ the Bohr magneton, P the spin polarization, and m the FL magnetic moment. $V_{\rm p}$ is the voltage applied on the MTJ device to switch its state. $R(V_{\rm p})$ is the resistance of the MTJ device; it shows a non-linear dependence on $V_{\rm p}$ [11]. In addition, we assume that $t_{\rm w}$ obeys a normal distribution for a given $V_{\rm p}$ (Equation 6).

C. Fitting and Model Optimization

Finally, the obtained electrical model of SAFF-defective MTJ device (Equations 2-6) has to be calibrated with silicon data. To this end, we performed comprehensive pulsed-switching characterization on the identified SAFF-defective MTJ devices at IMEC. In the measurements, the pulse width $t_{\rm p}$ was swept from 5 ns to 40 ns; these $t_{\rm p}$ values represent the typical write speed for STT-MRAM designs in practice. The interval of pulse amplitude $V_{\rm p}$ at each $t_{\rm p}$ point was carefully tuned to cover the entire switching spectrum, namely *switching probability* $P_{\rm sw}$ from 0% to 100%, as the switching events are intrinsically stochastic. To obtain a statistical result of the stochastic switching characteristics with an acceptable accuracy, we applied 1k-cycle pulses for each combination of $V_{\rm p}$ and $t_{\rm p}$. For instance, we observed that the number of successful P→AP switching events is 63 out of 1k pulses at $V_{\rm p} = 0.4$ V, $t_{\rm p} = 10$ ns, leading to $P_{\rm sw} = 6.3\%$. As $V_{\rm p}$ increases to 0.5 V at the same $t_{\rm p}$, 885 successful switching events were observed, resulting in $P_{\rm sw} = 88.5\%$. In this way, we obtained the three-dimensional statistics of $P_{\rm sw}$ vs. $V_{\rm p}$ vs. $t_{\rm p}$ for both P→AP and AP→P switching directions.

Fig. 8a shows the measured $V_{\rm p}$ vs. $t_{\rm p}$ at switching probability $P_{\rm sw}$=0.16, 0.50 and 0.84 for a SAFF-defective MTJ with eCD=35 nm. These three $P_{\rm sw}$ values are the outputs of the cumulative distribution function $F(\mu{-}\sigma)$, $F(\mu)$, and $F(\mu{+}\sigma)$ of normal distribution, respectively. The two curves with $P_{\rm sw}$=$F(\mu)$=0.50 in Fig. 8a are used to calibrate $\mu(t_{\rm w})$ (see Equations 4-5). By carefully tuning some physical parameters such $M_{\rm s}$ and $H_{\rm k}$, we are able to fit our device model to the measurement data. Fig. 8b shows the final fitting results; it can be seen that our simulation results match the silicon data very well. In addition, the measurement data in Fig. 8a also allows us to extract the standard deviation $\sigma(t_{\rm w})$ for a given $V_{\rm p}$, which is marked with the dashed line in the figure. Fig. 8c shows the extracted data for $\sigma(t_{\rm w})$ vs. $\mu(t_{\rm w})$ as well as the fitting curve with a three-degree polynomial for the AP→P switching direction. The data corresponding to the other switching direction is similar, thus not presented due to space limitation.

The output of device-aware defect modeling is a calibrated Verilog-A SAFF-defective MTJ compact model. After verifying and calibrating the MTJ model in Python as presented previously, we moved this model to Verilog-A so as to make it compatible with analog circuit simulations for subsequent fault modeling. To integrate the inter-cell magnetic coupling effect, we added four ports to the Verilog-A MTJ model: $H_{\rm dir\_in}$[0:3], $H_{\rm dia\_in}$[0:3], $H_{\rm dir\_out}$, and $H_{\rm dia\_out}$; $H_{\rm dir\_in}$[0:3] are input inter-cell stray fields from the four direct neighbors C0-C3 while $H_{\rm dia\_in}$[0:3] are input inter-cell stray fields from the other four diagonal neighbors C4-C7 (see Fig. 7c). $H_{\rm dir\_out}$ and $H_{\rm dia\_out}$ are the output stray fields from C8 itself; they go to direct neighbors and diagonal neighbors of C8, respectively. This enables us to simulate the SAFF-defective MTJ device in the presence of magnetic coupling effect in a circuit simulator.

VI. Device-Aware Fault Modeling of SAFF

Device-aware fault modeling consists of two sub-steps: 1) fault space definition, 2) fault analysis. Compared to the conventional fault modeling as introduced in Section IV-B, some upgrades are made in both sub-steps to make them suitable for non-volatile memories such as STT-MRAMs.

A. Fault Space Definition

In device-aware fault modeling, we also use the fault primitive notation $\langle S/F/R\rangle$ to describe STT-MRAM faults. However, the fault space needs to be expanded to covered all possible memory faults that we have observed in STT-MRAMs based on measurement data. Although S (sensitizing sequence) remains the same as the one described in Section IV-B, F and R have to be extended as follows.

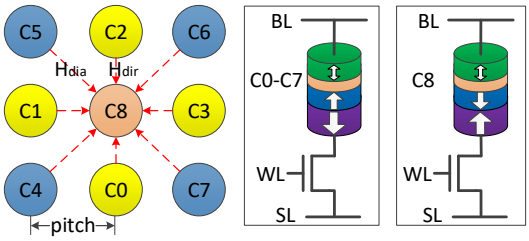

Fig. 9. DAT defect injection.

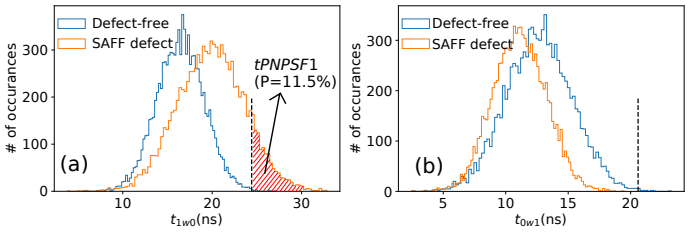

Fig. 10. tPNPSF1 with an occurrence rate of 11.5% for write '0' operations.

- F (faulty effect). $F\in\{0,1,U,L,H\}$, where the additional states 'U', 'L', and 'H' denote undefined, extreme low, and extreme high resistive states, respectively, as have been observed in real fabricated devices [20]. In STT-MRAMs, data is stored in MTJ devices whose pre-defined resistance ranges determine the logic states '0' and '1'. Due to defects or extreme process variations, the MTJ's resistance can be outside of these ranges, as demonstrated with measurement data presented in [20].
- R (readout value). $R\in\{0,1,?,-\}$, where the additional '?' denotes a *random* readout value in case the sensing current is very close to sense amplifier's reference current (e.g., the cell under read is in a 'U' state).

For example, *write transition fault* W0TFU=$\langle$1w0/U/-$\rangle$ means that a down-transition operation (S=1w0) turns the accessed memory cell to an undefined state (F=U); more details about notation and naming can be found in [12,20].

Based on the above expansion in the FP notation, the *entire* fault space can be redefined. It can be derived that the total number of *static faults* consists of 52 single-cell faults, 152 CFs, and 62464 NPSFs.

B. Fault Analysis

For the fault analysis we used the same experimental set-up as that used in Section IV-B but with some modifications as follows. First, for defect injection we replaced the defect-free MTJ model in the victim cell C8 with our SAFF-defective MTJ compact model, as shown in Fig. 9. As the SAFF defect does not affect the magnitude of the magnetizations of the RL and HL (only their directions are flipped), the SAFF defect size or strength plays no role here. Second, two array pitches were selected: 200 nm [4], 52.5 nm (=1.5×eCD) [25], representing high-performance and high-density STT-MRAM designs, respectively. Third, each sensitizing sequence S was simulated 10k cycles using Monte Carlo simulations, as the MTJ model has the stochastic switching property (see Fig. 8c and Equations 4-6).

Simulation results reveal interesting observations. For pitch=200 nm, no faults were observed in the presence of the SAFF defect; no single-cell, no two-cell, neither nine-cell faults. This clearly indicates that the inter-cell magnetic coupling and SAFF defect effects are negligible at this pitch.

For pitch=52.5 nm the results show some interesting fault behaviors in some cases. No single-cell and two-cell faults were observed at all. However, C8 failed to undergo a 0w1 transition in 1150 cycles out of the simulated 10k cycles, when all neighborhood cells were in state '1' (i.e., NP_8=255). This corresponds to an occurrence rate of 11.5%. Although the observed fault looks like the known fault model: *Passive Neighborhood Pattern Sensitive Fault* (PNPSF) for DRAMs [26], its nature is different; the fault is transient rather than permanent, due to the STT-switching stochasticity. Thus, we refer to the observed fault as *transient* PNPSF, denoted as tPNPSF1=$\langle 1;1;1;1;1;1;1;1;1\mathrm{w}0/1/-\rangle$. As this fault is a type of hard-to-detect fault [12], testing it is not quite easy!

Fig. 10a compares the switching time $t_{1\mathrm{w}0}$ histograms for 10k-cycle 1w0 operations in defect-free (blue) and defective (yellow) cases; the write pulse width is set long enough to cover the 3σ corner, as demarcated with the vertical dotted line in the figure. However, due to the SAFF defect, the $t_{1\mathrm{w}0}$ histogram shifts towards the right side. This means that tPNPSF1 takes place in those cycles where the required switching time is larger than the applied write pulse width. Fig. 10b shows the results for 0w1 operations; the $t_{0\mathrm{w}1}$ histogram of SAFF-defective device shifts towards the left side, indicating a faster transition on average in comparison to the defect-free device. Therefore, no faults were observed for 0w1 operations.

VII. Device-Aware Test Generation of SAFF

The last step of DAT is to develop appropriate test solutions for the derived fault tPNPSF1. Next, two test solutions will be discussed. One straightforward test solution could be a March algorithm such as:

$$\{\Updownarrow(\mathrm{w}1);\Updownarrow(\mathrm{w}0,\mathrm{r}0,\mathrm{w}1)^n\}.$$

In the above algorithm, n ($n\in\mathbb{Z}^+$) denotes the number of times that the second march element should be repeated. The first march element $\Updownarrow(\mathrm{w}1)$ initializes all memory cells to state '1', while the second applies three operations: w0 to sensitize the fault, r0 to *probabilistically* detect it, and w1 to reset the cell back to state '1'. As our experiments showed that tPNPSF1 occurs with a probability of 11.5% (when NP_8 is 255), the detection probability P_{dt}=$1-(1-11.5\%)^n$; hence the higher n, the higher P_{dt}. E.g., P_{dt}=90% requires n=19, while P_{dt}=99.99% requires n=76. Clearly, getting high confidence in the detection comes at the cost of long test time (large n); 100% detection is hard to guarantee.

The second test solution aims at guaranteeing the detection by incorporating *magnetic* write operations in the March test:

$$\{\Updownarrow(\mathrm{w}0_{\mathrm{H}});\Updownarrow(\mathrm{r}0)\},\ \text{or}\ \{\Updownarrow(\mathrm{w}1_{\mathrm{H}});\Updownarrow(\mathrm{r}1)\}.$$

Here, the first element $\mathrm{w}0_{\mathrm{H}}$ ($\mathrm{w}1_{\mathrm{H}}$) indicates a magnetic write '0' ('1') operation; i.e., an *external* field H_{ext} is applied to switch the MTJ state rather than driving an electric current

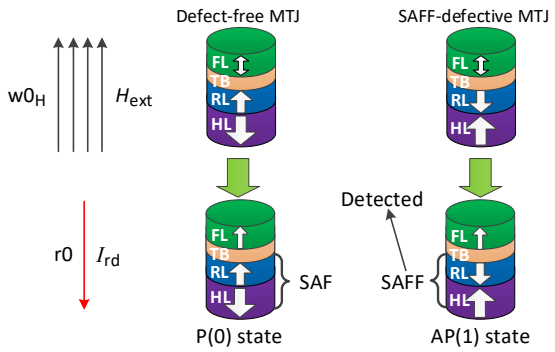

Fig. 11. Testing SAFF defects using a magnetic write '0' operation ($w0_H$).

through the MTJ device. Note that H_{ext} should be set higher than the coercivity of the FL but smaller than that of the RL and HL (i.e., H_c(FL)< H_{ext}<H_c(RL)<H_c(HL)) to avoid switching of the RL and HL. This can be realized by adding a perpendicular magnetic generator to a test chamber, similar to the wafer-level magnetic characterization tool developed by Hprobe [27]. As an entire STT-MRAM chip or even multiple chips can be reset to certain state by an external field in one shot, the additional cost due to this handling is limited. Fig. 11 illustrates the test process with a $w0_H$ operation to guarantee the detection of SAFF defect. Irrespective of the initial state, a $w0_H$ operation sets the magnetization of the FL to the same direction as the field H_{ext}. This makes the defect-free MTJ stay in P(0) state, while the SAFF-defective MTJ goes to AP(1) state, as shown in the figure. Thereafter, a r0 operation can easily distinguish defective devices from defect-free ones.

VIII. Conclusion

This paper has demonstrated the existence of a unique type of defect, referred to as synthetic anti-ferromagnet flip defect, in STT-MRAMs. In addition, it has shown that applying the traditional fault modeling and test development approach fails to accurately model the defect at the functional behavior; hence it fails in detecting such a defect during manufacturing tests. Moreover, It has demonstrated the power of device-aware test approach in being able to appropriately model the defect and develop test solutions to detect such a defect.

Emerging memory technologies such as STT-MRAM, R-RAM, and PCM require unique manufacturing steps which could cause *unique* defect mechanisms. These may not be detected by traditional memory tests, neither can be modeled with traditional fault modeling approaches. This calls for a better understanding of new defect mechanisms and better fault modeling and test approaches such as device-aware test.

References

[1] D. Apalkov *et al.*, "Magnetoresistive random access memory," *Proceedings of the IEEE*, vol. 104, no. 10, pp. 1796–1830, Aug. 2016, doi:10.1109/JPROC.2016.2590142.

[2] W.J. Gallagher *et al.*, "22nm STT-MRAM for reflow and automotive uses with high yield, reliability, and magnetic immunity and with performance and shielding options," in *IEEE Int. Electron Devices Meeting*, Dec. 2019, pp. 2.7.1–2.7.4, doi:10.1109/IEDM19573.2019.8993469.

[3] K. Lee *et al.*, "1Gbit high density embedded STT-MRAM in 28nm FDSOI technology," in *IEEE Int. Electron Devices Meeting*, Dec. 2019, pp. 2.2.1–2.2.4, doi:10.1109/IEDM19573.2019.8993551.

[4] L. Wei *et al.*, "A 7Mb STT-MRAM in 22FFL FinFET technology with 4ns read sensing time at 0.9V using write-verify-write scheme and offset-cancellation sensing technique," in *IEEE Int. Solid-State Circuits Conf.*, Feb. 2019, pp. 214–216, doi:10.1109/ISSCC.2019.8662444.

[5] S.W. Chung *et al.*, "4Gbit density STT-MRAM using perpendicular MTJ realized with compact cell structure," in *IEEE Int. Electron Devices Meeting*, Dec. 2016, pp. 27.1.1–27.1.4, doi:10.1109/IEDM.2016.7838490.

[6] L. Wu *et al.*, "Electrical modeling of STT-MRAM defects," in *IEEE Int. Test Conf.*, Oct. 2018, pp. 1–10, doi:10.1109/TEST.2018.8624749.

[7] C.L. Su *et al.*, "MRAM defect analysis and fault modeling," in *IEEE Int. Test Conf.*, Oct. 2004, pp. 124–133, doi:10.1109/TEST.2004.1386944.

[8] J. Azevedo *et al.*, "A complete resistive-open defect analysis for thermally assisted switching MRAMs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 11, pp. 2326–2335, Nov. 2014, doi:10.1109/TVLSI.2013.2294080.

[9] I. Yoon *et al.*, "EMACS: efficient MBIST architecture for test and characterization of STT-MRAM arrays," in *IEEE Int. Test Conf.*, Nov. 2016, pp. 1–10, doi:10.1109/TEST.2016.7805834.

[10] S.M. Nair *et al.*, "Defect injection, fault modeling and test algorithm generation methodology for STT-MRAM," in *IEEE Int. Test Conf.*, Oct. 2018, pp. 1–10, doi:10.1109/TEST.2018.8624725.

[11] L. Wu *et al.*, "Pinhole defect characterization and fault modeling for STT-MRAM testing," in *IEEE European Test Symp.*, May 2019, pp. 1–6, doi:10.1109/ETS.2019.8791518.

[12] M. Fieback *et al.*, "Device-aware test: a new test approach towards DPPB," in *IEEE Int. Test Conf.*, Nov. 2019, pp. 1–10, doi:10.1109/ITC44170.2019.9000134.

[13] G.S. Kar *et al.*, "Co/Ni based p-MTJ stack for sub-20nm high density stand alone and high performance embedded memory application," in *IEEE Int. Electron Devices Meeting*, Dec. 2014, pp. 19.1.1–19.1.4, doi:10.1109/IEDM.2014.7047080.

[14] A.V. Khvalkovskiy *et al.*, "Basic principles of STT-MRAM cell operation in memory arrays," *J. Phys. D: Appl. Phys*, vol. 46, no. 13, p. 139601, Feb. 2013, doi:10.1088/0022-3727/46/13/139601.

[15] G. Han *et al.*, "Control of offset field and pinning stability in perpendicular magnetic tunnelling junctions with synthetic antiferromagnetic coupling multilayer," *J. Appl. Phys.*, vol. 117, no. 17, p. 17B515, Mar. 2015, doi:10.1063/1.4913942.

[16] C. Augustine *et al.*, "Numerical analysis of typical STT-MTJ stacks for 1T-1R memory arrays," in *IEEE Int. Electron Devices Meeting*, Dec. 2010, pp. 22.7.1–22.7.4, doi:10.1109/IEDM.2010.5703416.

[17] I. Yoon *et al.*, "Modeling and analysis of magnetic field induced coupling on embedded STT-MRAM arrays," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 37, no. 2, pp. 337–349, Feb. 2018, doi:10.1109/TCAD.2017.2697963.

[18] W. Zhao *et al.*, "Design considerations and strategies for high-reliable STT-MRAM," *Microelectronics Rel.*, vol. 51, no. 9-11, pp. 1454–1458, Sep.-Nov. 2011, doi:10.1016/j.microrel.2011.07.001.

[19] L. Thomas *et al.*, "Perpendicular spin transfer torque magnetic random access memories with high spin torque efficiency and thermal stability for embedded applications," *J. Appl. Phys.*, vol. 115, no. 17, p. 172615, Apr. 2014, doi:10.1063/1.4870917.

[20] L. Wu *et al.*, "Defect and fault modeling framework for STT-MRAM testing," *IEEE Trans. Emerg. Topics Comput.*, pp. 1–1, Dec. 2019, doi:10.1109/TETC.2019.2960375.

[21] S. Hamdioui *et al.*, "Memory fault modeling trends: a case study," *J. Electronic Testing*, vol. 20, no. 3, pp. 245–255, Jun. 2004, doi:10.1023/B:JETT.0000029458.57095.bb.

[22] S. Hamdioui *et al.*, "An experimental analysis of spot defects in SRAMs: realistic fault models and tests," in *Asian Test Symp.*, Dec. 2000, pp. 131–138, doi:10.1109/ATS.2000.893615.

[23] Nanoscale Integration and Modeling (NIMO) Group at ASU, "Predictive technology model," *http://ptm.asu.edu/*, retrieved in 2018.

[24] D.J. Griffiths, *Introduction to electrodynamics*. Pearson, 2013.

[25] V.D. Nguyen *et al.*, "Towards high density STT-MRAM at sub-20nm nodes," in *Int. Symp. VLSI Technol., Syst. Appl.*, Apr. 2018, pp. 1–2, doi:10.1109/VLSI-TSA.2018.8403867.

[26] A.J. Van de Goor, *Testing semiconductor memories: theory and practice*. J. Wiley & Sons, 1991, vol. 225.

[27] M. Shulaker *et al.*, "Special session (new topic): emerging computing and testing techniques," in *VLSI Test Symp.*, Apr. 2019, pp. 1–2, doi:10.1109/VTS.2019.8758598.