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Resistor-based Temperature Sensors in CMOS Technology

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Resistor-based Temperature Sensors in CMOS Technology

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for the purpose of obtaining the degree of doctor

at Delft University of Technology

by the authority of the Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen

Chair of the Board for Doctorates

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Chapter 1

Introduction

Temperature plays an essential role in many physical, chemical, and biological processes. Therefore, temperature sensors are widely used for their monitoring and control. Traditionally, temperature sensors are based on discrete components, such as thermistors [1.1][1.2] or thermocouples [1.3]. In the last few decades, however, smart temperature sensors, i.e., integrated temperature sensors with on-chip readout circuits and digital outputs, have become increasingly popular due to their low cost, small size, and ease of use [1.4].

This thesis describes the design of smart temperature sensors for a specific application, the temperature compensation of frequency references [1.5]-[1.10], which demands both high resolution and high energy efficiency. By using on-chip resistors as sensing elements, sensors with state-of-the-art resolution and energy efficiency were realized. Moreover, these designs achieved competitive performance in various other aspects, such as accuracy, supply sensitivity, and chip area.

This chapter is an introduction to the thesis. It starts by discussing some general aspects of integrated temperature sensors, such as their applications and specifications. Then the specific challenges associated with the temperature compensation of frequency references are presented. This is followed by an introduction and comparison of the various temperature sensing elements available in CMOS technology, which leads to the choice for on-chip resistors. The chapter ends with an overview of the targeted goals and thesis organization.

1.1 Temperature sensor applications and specifications

Smart temperature sensors can be used in numerous applications, which results in a wide variety of specifications. For example, low power consumption is a key requirement for sensors intended for use in radio frequency identification (RFID) tags, which usually do not have batteries [1.11][1.12], whereas a large temperature range is required in automotive and industrial ICs [1.13]. In general, high accuracy is desirable in most applications, and must be accompanied by commensurate resolution to facilitate practical calibration.

Resolution is defined as the minimum temperature change that can be detected by a sensor, and it is typically limited by random noise [1.4]. In many applications, high resolution is not a critical requirement, 1°C resolution, for example, is more than sufficient for cooking ovens and coffee machines. However, industrial applications, e.g., the temperature control of wafer steppers, often require much higher resolution. Because the position of wafer steppers must be controlled with nanometer precision, the thermal expansion of their mechanical components should be carefully controlled and minimized. The required temperature sensing accuracy is then at the mK level, while the sensing resolution should then be at the sub-mK level [1.14]. As will be discussed in the next section, similar levels of resolution are required for the temperature compensation of frequency references.

1.2 Challenges in frequency reference compensation

The performance of electronic systems often relies on the accuracy and noise of clock references. For instance, the USB 3.0 serial bus standard requires clocks with less than 50ppm frequency error, and less than 0.8ps (~16ppm) jitter [1.15]. For telecommunication systems, the requirements are even stricter: less than 0.1ppm frequency error and an Allan Deviation (a measure of long-term stability) below 10^{-10} in an integration time of 1s [1.5].

Typically, accurate clock references are based on quartz crystal oscillators. Recently, references based on MEMS (Micro Electro Mechanical System) [1.5] [1.6] or BAW (bulk acoustic wave) [1.16] resonators have become popular due to their small size and ease of integration with CMOS technology. However, their resonant frequencies are significantly temperature-dependent. For example, the temperature coefficient (TC) of an uncompensated MEMS oscillator is about 31ppm/°C [1.6], resulting in a 4000ppm frequency change from −40°C to 85°C. Even for quartz crystal oscillators [1.7], or BAW devices with passive compensation schemes [1.16], errors of ~200ppm may occur over the same temperature range. As a consequence, temperature compensation must be included to achieve high frequency accuracy, especially for MEMS oscillators.

Figure 1.1 shows the block diagram of a typical high-accuracy MEMS-based frequency reference [1.6]. It contains a MEMS oscillator, a fractional-N synthesizer and divider, a compensating temperature sensor, and digital processing blocks. The output of the temperature sensor is used to control the output frequency of the fractional-N synthesizer via a polynomial engine, in order to compensate for the temperature dependence of the resonator. This temperature dependence is typically significantly non-linear, and spreads over samples, thus necessitating multiple-point calibration. In [1.6], a resistor-based temperature sensor and a 5th-order polynomial

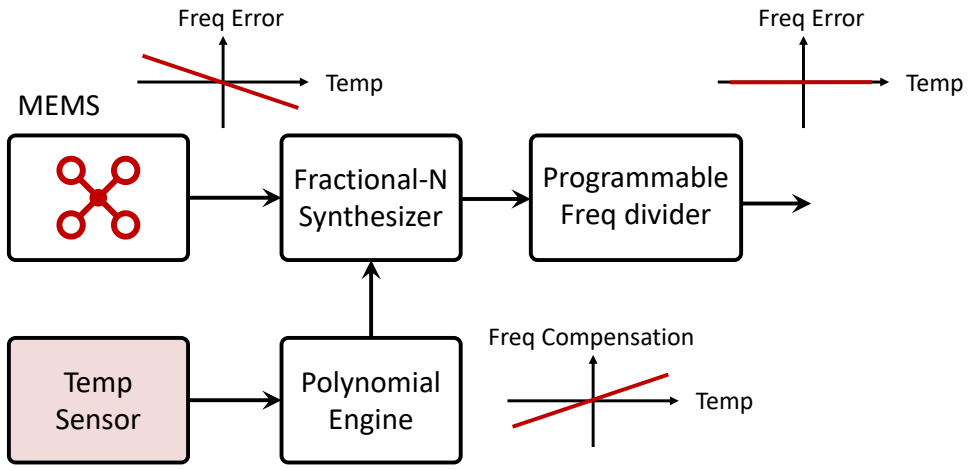


Figure 1.1: Temperature compensation of a MEMS-based frequency reference.

are used to achieve less than 0.5 ppm frequency error from −40°C to 85°C. In a more recent design [1.5], a MEMS-based temperature sensor and a 7th-order polynomial are used to reduce frequency error to the extraordinary level of 40ppb.

Since the temperature sensor's noise is injected into the fractional-N synthesizer, it appears as phase noise in the output frequency. To minimize this, a high-resolution temperature sensor is required. For example, in the 40ppb inaccuracy MEMS frequency reference reported in [1.5], better than 100μK resolution was required. In a less accurate design, with 0.3ppm frequency inaccuracy, the required resolution is still quite high: better than 650μK [1.8].

Apart from high resolution, temperature sensors intended for frequency references should also achieve a bandwidth of about 100Hz to maintain frequency accuracy in the presence of temperature variations [1.5]. Moreover, a low-power sensor is preferred to minimize its contribution to the total energy budget, meaning that its energy efficiency should be high. This also helps to reduce self-heating, which may lead to temperature compensation errors.

To reduce their overall manufacturing cost, the multiple-point calibration of temperature sensors is generally not desirable. However, since MEMS oscillators typically require multiple-point calibration anyway, the extra cost of temperature sensor calibration becomes almost negligible. The achievable accuracy of such sensors, and thus of the resulting frequency references, will then be mainly limited by their long-term drift.

1.3 Resolution and resolution FoM

Of the specifications introduced above, energy efficiency remains a vague term without a clear metric. To quantify it, a resolution figure of merit (FoM) [1.4] has been defined in the same way as the Schreier FoM for ADCs [1.17]. For temperature sensors, this can be expressed as:

$$FoM = Energy/Conversion \cdot Resolution^2 \qquad (1.1)$$

In this equation, the resolution is squared to reflect the fact that the resolution of a temperature sensor should be limited by thermal noise. Therefore, to obtain 2× more resolution, the energy consumption of a sensor should be increased by 4×. With this metric, higher energy efficiency corresponds to a smaller resolution FoM. Compared to resolution, the resolution FoM of a temperature sensor is a more fundamental specification, because as long as the sensor is thermal-noise limited, better resolution can always be obtained at the expense of increased energy consumption.

Figure 1.2 shows the resolution and the resolution FoM of various smart temperature sensors at the start of the work described in this thesis (in 2016). The plot includes sensors based on BJTs, MOSFETs, resistors, thermal diffusivity (TD), and MEMS devices. Although MEMS-based sensors [1.19] can achieve superb resolution (40μK) and energy efficiency (120fJ·K^2), their non-CMOS fabrication leads to two-die systems, greater complexity, and increased cost. Of the possible CMOS-

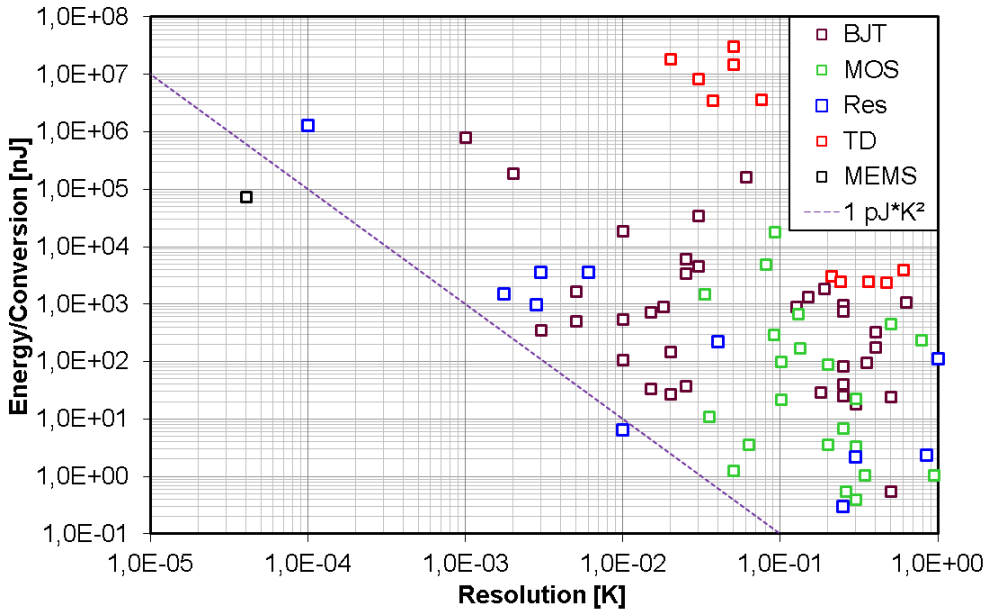


Figure 1.2: Energy per conversion vs. resolution of temperature sensors, published prior to the start of this research (in 2016) [1.18].

compatible candidates, BJT- and resistor-based sensors achieve mK-level resolution and good energy efficiency (~1pJ·K^2), while MOSFET-based sensors do not have sufficient resolution and TD sensors have relatively poor efficiency.

To understand the limitations of the different types of sensors and identify the most suitable one for the targeted frequency compensation application, the operating principles of different types of sensors will be discussed in the next section, as well as the theoretical limits on their energy efficiency.

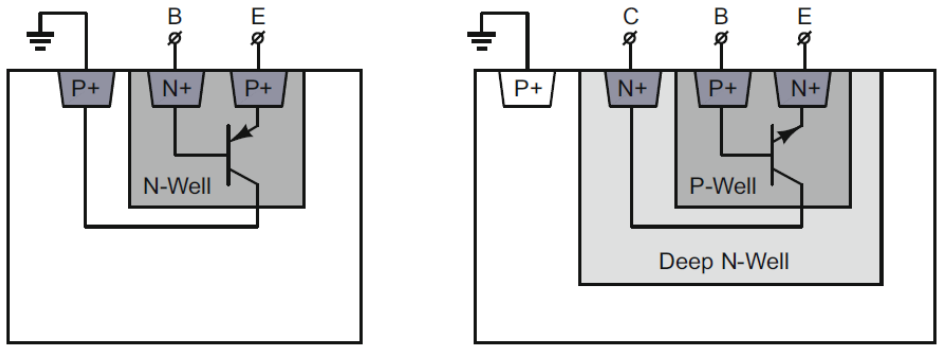
1.4 CMOS temperature sensing elements and their theoretical resolution FoMs

1.4.1 Bipolar junction transistors (BJTs)

Because of a lower sensitivity to process spread and packaging stress, vertical BJTs are preferred over lateral ones in temperature sensors [1.20]. Both PNPs [1.21] and NPNs [1.22] can be used to sense temperature. The NPN transistor is the more ideal candidate because of its larger current gain. However, it requires a deep N-well option, which is not always available in modern CMOS processes (Figure 1.3).

Regardless of the type of BJT used, its base-to-emitter voltage V_{BE} can be approximated over a wide range of collector currents as:

$$V_{BE} = \frac{kT}{q} \cdot \ln\left(\frac{I_C}{I_S}\right), \tag{1.2}$$



(a) (b)

Figure 1.3: Cross section of (a) a vertical PNP transistor in standard CMOS and (b) a vertical NPN transistor in CMOS technology with a deep N-well option.

where I_C (>> I_S) is the collector current, I_S is the saturation current, k is the Boltzmann constant, q is the electron charge, and T is the absolute temperature.

For a pair of BJTs biased with different current densities, the V_{BE} difference can be expressed as:

$$\Delta V_{BE} = \frac{kT}{q} \cdot \ln(p \cdot r), \tag{1.3}$$

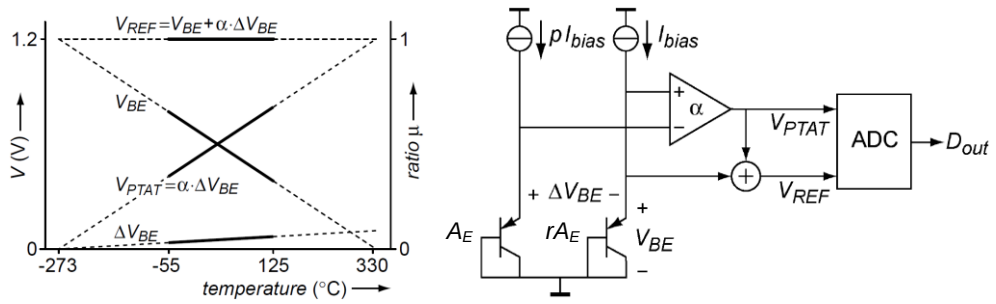
where p and r are the ratios of the collector current and emitter area between two bipolar transistors, respectively. This is known as a PTAT (proportional-to-absolute-temperature) voltage.

A reference voltage is needed to digitize ΔV_{BE}. This is usually achieved by linearly combining V_{BE} and ΔV_{BE}. The ratio of ΔV_{BE} and the well-known bandgap voltage V_{REF} (≈1.22V) is then a function of absolute temperature given by:

$$\mu = \frac{V_{PTAT}}{V_{REF}} = \frac{\alpha \Delta V_{BE}}{V_{BE} + \alpha \Delta V_{BE}}, \tag{1.4}$$

where α is the ΔV_{BE} scaling factor inversely proportional to $ln(p \cdot r)$. Using PNP transistors as an example, the relationship between the voltages mentioned above and the circuit used to provide μ is shown in Figure 1.4.

To achieve high accuracy, dynamic element matching is often used to cancel the mismatch between the BJTs and the current sources [1.21]. To avoid complex logic, the ratios (p and r) should be kept small. In most BJT sensors, $p \cdot r$ is between 2 and 10. With p=5, for example, the sensitivity of ΔV_{BE} is 0.14mV/K.



(a) (b)

Figure 1.4: (a) V_{BE}, ΔV_{BE} and V_{Ref} over temperature; (b) simplified block diagram of a BJT-based temperature sensor [1.21].

The theoretical energy efficiency of BJT sensors is limited by its front-end. As a first step, we assume that ΔV_{BE} is realized by scaling the current mirror ratio p, and that the readout circuit contributes zero power and noise. The sensor's energy consumption can then be expressed as:

$$E_{conv} = V_{DD} \cdot (1 + p) \cdot I_{bias} \cdot T_{conv}, \tag{1.5}$$

where V_{DD} is the supply voltage, I_{bias} is the biasing current of a single BJT, and T_{conv} is the sensor's conversion time.

The sensor's resolution is mainly limited by the noise present in ΔV_{BE}, as this is much smaller than V_{BE}. As in [1.23], this noise is given by:

$$v_{n,\Delta V_{BE}}^2 = \frac{4kT}{g_m} B_n \cdot (1 + \frac{1}{p}), \tag{1.6}$$

where B_n=1/(2·T_{conv}) is the noise bandwidth.

After computing the sensor's resolution, using its sensitivity and the calculated noise, and combining it with the sensor's energy consumption, both T_{conv} and I_{bias} will cancel out, resulting in the following expression for the sensor's FoM [1.23]:

$$FoM_{BJT,p} = 2 \cdot \frac{(p+1)^2}{p} \cdot V_{DD} \cdot q \cdot {V_T}^2 \cdot \alpha^2 \cdot \left(\frac{A - T}{V_{REF}}\right)^2, \tag{1.7}$$

where V_T=kT/q and A≈2T=600K. Assuming p=5 and a supply voltage of V_{DD}=1.8V, the theoretical FoM of this BJT sensor configuration is approximately 36fJ·K^2.

Alternatively, one can fix p=1 and scale the emitter area ratio r. Due to the more balanced power and noise distribution of the two BJTs, the theoretical energy efficiency improves. According to [1.23], this can be calculated as:

$$FoM_{BJT,r} = 8 \cdot V_{DD} \cdot q \cdot {V_T}^2 \cdot \alpha^2 \cdot \left(\frac{A - T}{V_{REF}}\right)^2. \tag{1.8}$$

With r=5 and the same V_{DD}=1.8V, the theoretical FoM is reduced to 20fJ·K^2.

Note that in the computation of these FoMs, the power and noise of the readout circuit have been neglected. Assuming that both the readout circuit and the BJT sensor front-end have similar power/noise levels, the FoM of a complete BJT-based temperature sensor will then be 4× larger, i.e., 80fJ·K^2. Back in 2016, the state-of-art FoM achieved by BJT-based sensors was 3.6pJ·K^2 [1.24].

1.4.2 MOSFETs

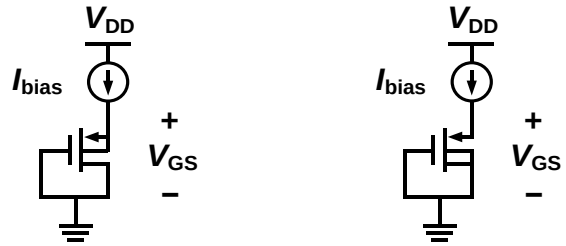
The behavior of a MOSFET device (transconductance, threshold voltage, etc.) heavily depends on temperature, and hence there are various types of MOS-based temperature sensors. They can be roughly grouped as:

1. BJT-like sensors
2. Other subthreshold region sensors
3. Saturation region sensors

In BJT-like designs, which achieve by far the best resolution and efficiency performance, two MOSFETs, biased in the subthreshold (weak-inversion) region, serve as replacements of BJT devices in Figure 1.3 [1.25]. In particular, the sensor's inaccuracy can be improved by configuring the MOSFETs as dynamic-threshold MOSTs (DTMOSTs) [1.25][1.26], in which the transistor's body is connected to its gate to provide a well-defined threshold voltage, as shown in Figure 1.5. In both cases, the V-I characteristic is similar compared to that of a BJT device, i.e.:

$$I_{DS} = I_{D0}.e^{\frac{V_{GS}-V_T}{nkT/q}}$$
$$V_{GS} = \frac{nkT}{q} \cdot \ln\left(\frac{I_{DS}}{I_{D0}}\right) + V_T, \quad (1.9)$$

where V_{GS} is the gate-source voltage, V_T is the threshold voltage, n is the slope factor, and I_{D0} is the current at V_{GS}=V_T. Therefore, the analysis in Section 1.4.1 still holds.



(a) (b)

Figure 1.5: A PMOS transistor configured as (a) a diode and (b) a DTMOST.

Compared to BJT-based sensors, two variables change in the theoretical FoM calculation: the supply voltage and the noise. Since V_{GS} (≈0.4V) is typically smaller than V_{BE} (≈0.7V), MOSFET-based sensors can work with a smaller supply voltage, potentially below 1V. However, given the same biasing current, the gm of a subthreshold MOSFET is n times smaller than that of a BJT, and the thermal noise

indicated by Equation (1.6) is proportionally worse. Also, MOSFETs typically exhibit much more 1/*f* noise. Due to these factors, the theoretical FoM of such MOSFET-based sensors is somewhat worse than that of BJT-based designs. However, back in 2016, the state-of-art FoM for MOSFET sensors was 3.2pJ·K^2 [1.27].

However, the resolution of these sensors is typically not sufficiently high for frequency compensation applications. This is mainly due to the power restriction posed by the weak-inversion operation: with the same theoretical FoM and conversion speed, the resolution of these low-power (typically <1μW) MOSFET sensors is definitely lower than their BJT-based counterparts, the exponential V-I characteristic of which can be maintained at a mW power level [1.28].

Some subthreshold MOSFET sensors are based on other temperature sensing principles. For example, [1.29] utilizes the temperature sensitivity of V_T. This linear sensitivity, denoted as κ_{VT} (i.e., $V_T(T) = V_{T0} + \kappa_{VT} \cdot \Delta T$), results in an exponential variation on I_{DS} with temperature. As shown in Figure 1.6, this current is further proportionally converted to frequency using a ring oscillator, and, with the help of a reference frequency, is digitized by a counter-based readout circuit.

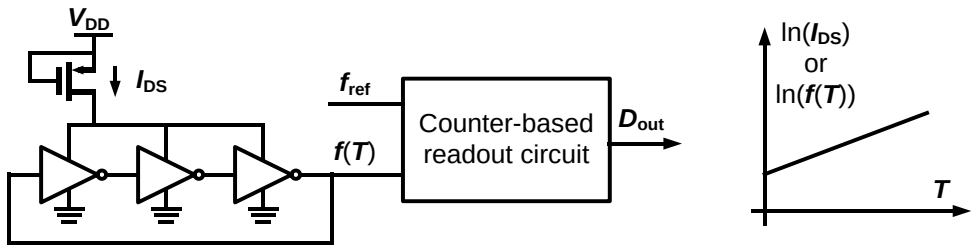


Figure 1.6. Simplified diagram of a subthreshold MOSFET temperature sensor with frequency-based readout [1.29].

To accurately determine the theoretical FoM of such sensors, the temperature dependency of I_{D0} should be also taken into account, which greatly complicates the temperature sensitivity expression of I_{DS}. For simplicity, this sensitivity κ_{IDS} is typically derived from simulations, and is roughly 4.6%/°C at room temperature [1.30].

Neglecting the power of the readout circuit circuit, the energy consumption of such sensors can be simplified as

$$E_{conv} = V_{DD} \cdot I_{DS} \cdot T_{conv}. \tag{1.10}$$

And the current noise of I_{DS} is given by:

$$i_n^2 = 4kTg_m \cdot B_n = \frac{2q \cdot I_{DS}}{n \cdot T_{conv}}. \tag{1.11}$$

After neglecting the area-dependent 1/f noise and assuming this thermal noise to be the only noise source, the theoretical FoM of the MOSFET sensor front-end can be calculated as:

$$FoM_{MOS} = \frac{q \cdot V_{DD}}{2n \cdot {\kappa_{IDS}}^2} \tag{1.12}$$

Assuming n = 1.2, and V_{DD}=1V, the theoretical FoM is roughly 0.03fJ·K^2, which is almost 1000× better than that of the BJT-like sensors.

However, these sensors are not well suited for the temperature compensation of frequency references. First, the oscillator-based readout circuit typically introduces significant excess power and noise, which severely degrades the energy efficiency. In a relatively efficient design based on a native NMOS current source, the FoM turns out to be 3200fJ·K^2 [1.30]. Second, like BJT-like sensors, the sensor's power, and thus its resolution within a certain conversion time, is limited by the subthreshold operation. Last but not the least, sensor performance, including power, resolution, and sensitivity, varies exponentially over temperature. This is not conducive to realizing frequency references with stable performance over temperature.

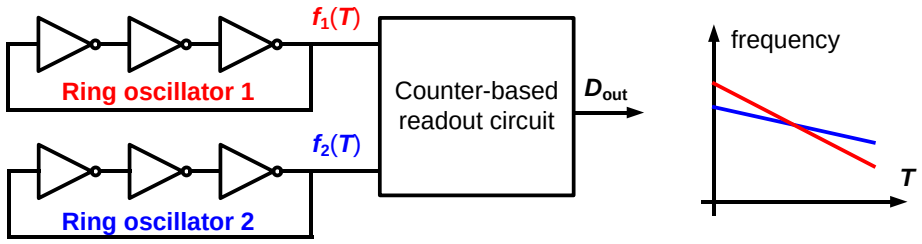


Figure 1.7. Simplified diagram of the MOSFET temperature sensor in [1.32].

The theoretical resolution of MOSFET sensors working in saturation regions is not restricted by the aforementioned power problem. However, existing designs are still not suitable for the targeted frequency compensation application. These sensors are mostly based on compact ring oscillators and counter-based readout, resulting in a small chip area [1.32][1.33]. In [1.32], for instance, the temperature is obtained by digitizing the frequency ratio $f_1(T) / f_2(T)$ of two ring oscillators, as shown in Figure 1.7. The two ring oscillators are comprised of transistors with different threshold voltages, leading to different effects on mobility variation and thus different temperature sensitivities. The temperature is then digitized by calculating the

oscillator frequency ratio using counters. Unfortunately, these sensors are extremely vulnerable to supply variations (1-10 °C/V). Also, their low resolution (>100mK) is usually limited by the counter's quantization noise instead of the thermal noise of their front-end, so that their FoM is far worse than the theoretical limit.

Due to these drawbacks, MOSFET-based temperature sensors are mainly used in system-on-a-chip (SoC) applications with limited supply voltages. Also, they typically require less chip area than BJTs, which helps to reduce the fabrication cost.

1.4.3 Electro-thermal filters (ETFs)

Temperature sensors based on electro-thermal filters make use of the well-defined and temperature-dependent speed at which heat diffuses through a silicon substrate [1.34]-[1.36]. The thermal diffusivity of silicon, denoted as D_{si}, can be approximated by the power law of $D_{si} \propto 1/T^{1.8}$ [1.37].

The structure of an electro-thermal filter is shown in Figure 1.8. It consists of a heater that generates heat pulses, and a relative temperature sensor (thermopile) located at a distance s from the heater which detects the heat propagation delay in between these two elements. The sensor has a square-wave voltage input, and the generated heat pulses are converted back to a small voltage signal by the thermopile. As a result, the ETF behaves like a low-pass filter in the time domain (Figure 1.9). Given a fixed excitation frequency f_{drive}, its phase shift can be expressed as:

$$\emptyset_{ETF} = -s\sqrt{\pi f_{drive}/D_{si}} \propto -s\sqrt{\pi f_{drive} T^{1.8}} \tag{1.13}$$

A phase-domain ADC can then be used to digitize this phase and obtain the temperature information.

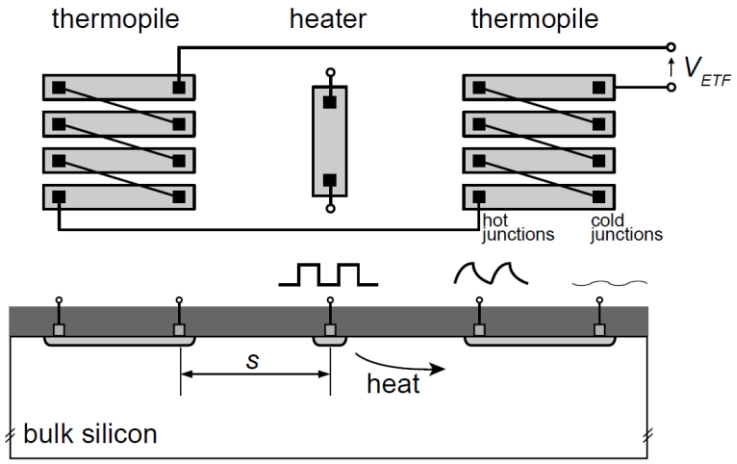


Figure 1.8. An ETF using a thermopile as its relative temperature sensor [1.35].

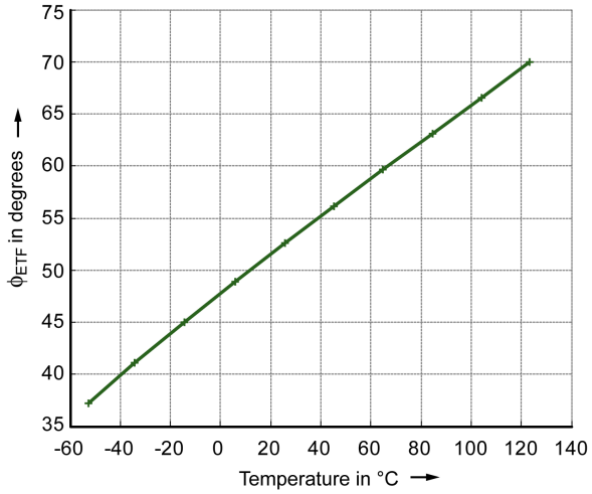


Figure 1.9. Phase shift of an ETF as a function of temperature [1.35].

Because on-chip thermopiles usually have low sensitivity (~0.5mV/K), the output level of ETFs is rather small (~1mV), which, in turn, severely limits their resolution. Together with the power dissipation of their heaters (several mWs), the result is poor energy efficiency. At the start of this research (2016), the best reported FoM for an ETF was $1.4 \cdot 10^5$ pJ·K^2 [1.36], which is about 10^5 times worse than the record FoMs obtained for BJT- and resistor-based temperature sensors at that time.

Although ETF-based temperature sensors are highly energy-inefficient, they can achieve both high accuracy and small chip area [1.36] due to the well-defined D_{si}. This makes such sensors promising in dense thermal management applications, where high power and low resolution can be tolerated.

1.4.4 Resistors

Most CMOS-compatible resistors exhibit significant temperature coefficients (TCs). According to [1.39], the temperature dependence of a resistor can be well modeled as:

$$R_S(T) = R_S(T_0) \cdot (1 + TC_{S1} \cdot \Delta T + TC_{S2} \cdot \Delta T^2) \qquad (1.14)$$

where $R_S(T_0)$ is the nominal resistance at a reference temperature T_0, TC_{S1} and TC_{S2} are its 1st and 2nd order TCs, and ΔT is the temperature with respect to T_0. Figure 1.10 shows the temperature characteristics of different resistors in a standard 0.18µm CMOS technology. Depending on the resistor type, the 1st-order TC at room temperature (~25°C) ranges from −0.15%/°C to 0.34%/°C.

Given a certain resistor type, $R_S(T_0)$, TC_{S1} and TC_{S2} all spread, which necessitates a multi-point calibration [1.6][1.10]. Among those variables, $R_S(T_0)$ spreads the most (~±20% over corners), TC_{S1} spreads less, while the spread of TC_{S2} is often negligible. As a result, a well-designed sensor should achieve good accuracy with only 2 trimming points.

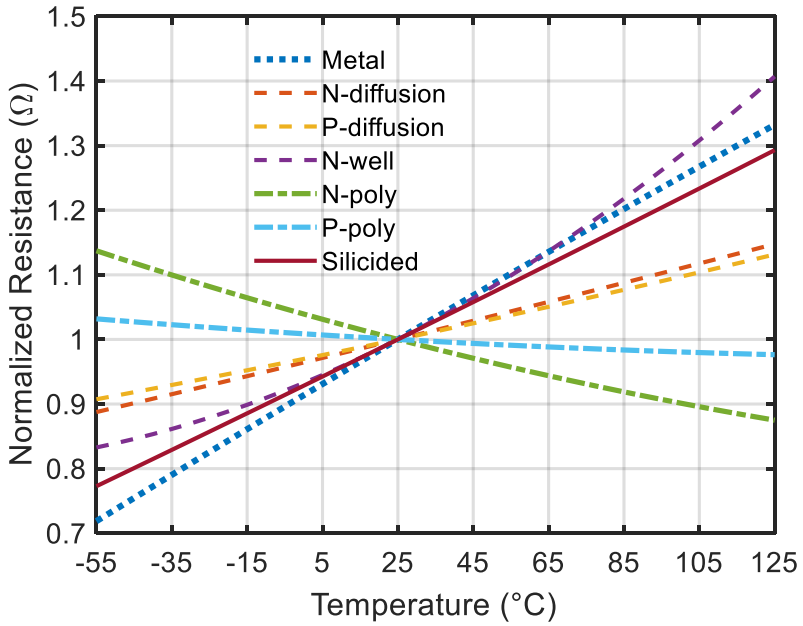


Figure 1.10. Temperature characteristics of different resistors in a standard 0.18μm CMOS technology.

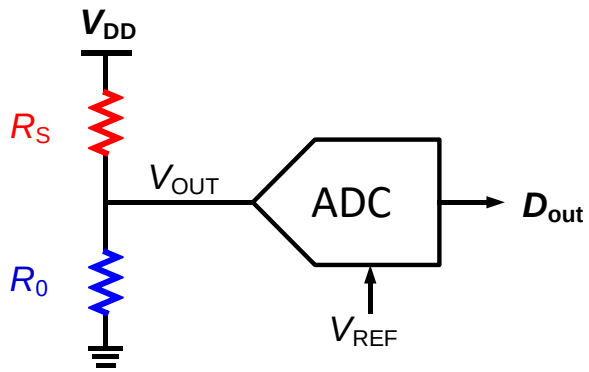


Figure 1.11. Temperature sensor based on a resistor divider.

Figure 1.11 shows a simple temperature sensor that consists of a temperature-sensitive resistor (thermistor) R_S and a reference resistor R_0. The temperature-dependent voltage output of the resistor divider is then digitized by an ADC. Here it is assumed that R_0 has a zero TC and the temperature dependence of R_S is given by equation (1.14). With a small temperature difference of ΔT, the voltage output under a supply voltage of V_{DD} can then be expressed as:

$$V_{OUT} = V_{DD} \cdot \frac{1}{2 + \Delta T \cdot TC_{S1}}. \tag{1.15}$$

With V_{DD}=1.8V and TC_{S1}=0.3%/°C, the V_{OUT} sensitivity is 1.35mV/°C. In the case of a balanced bridge (i.e., ΔT=0), the resolution FoM of the sensor front-end can be calculated as [1.38]:

$$FoM_{RES} = \frac{8kT}{{TC_{S1}}^2}. \tag{1.16}$$

With TC_{S1}=0.3%/°C, the theoretical FoM is about 3.7fJ·K^2. Considering the 4× factor from the ADC's power and noise, the practical FoM limit becomes 15fJ·K^2, which is 5× better compared to that of BJT-based sensors. Note that, unlike BJT-based sensors, the theoretical FoM of a resistor-based sensor only depends on the thermistor's TC, but is independent of its supply voltage or biasing current. At the start of this research (2016), the best reported FoM for a resistor-based sensor was 0.65pJ·K^2 [1.39].

Other than the high-resolution FoM, resistor-based sensors can be easily scaled along constant-FoM lines to achieve either high-resolution or low-power requirements. Also, there is no minimum supply limitation. A drawback of these sensors, as mentioned before, is the need for multi-point calibration.

1.5 Choice of the sensing element

After reviewing the principles and limitations of different CMOS temperature sensing elements, resistor-based sensors are the most suitable choice for the targeted application of compensating the temperature dependency of frequency references. Their practical energy efficiency is the best among all CMOS candidates. Although the need for multi-point calibration is a disadvantage, it can be tolerated as such calibration is needed anyway for the oscillator.

It would be interesting to investigate energy-efficient sensors built with other sensing elements, such as BJTs or MOSFETs working in saturation regions. However, this is beyond the scope of this thesis.

1.6 Goals and thesis organization

The main goal of this thesis is to provide a comprehensive study of different types of resistor-based temperature sensors, and to compare their pros and cons with respect to conventional BJT-based temperature sensors. In chapter 2, the critical choices involved with their design will be discussed, together with a literature review.

Another goal is the development of resistor-based temperature sensors that can be used for the temperature compensation of frequency references. Among all the structures, two major types—namely Wien bridge sensors and Wheatstone bridge sensors—have been designed, fabricated, and characterized. The Wien bridge sensors, which achieve better accuracy but worse energy efficiency, are presented in Chapter 3. The Wheatstone bridge designs, which use various design techniques to improve the sensor's resolution FoM, are presented in Chapter 4. Ultimately, a $10fJ \cdot K^2$ FoM has been achieved, which improves the state-of-the-art by 65×.

Last but not least, two resistor-based temperature sensors designed to broaden the application of resistor-based sensors are presented in Chapter 5. One is a low-power sensor designed for biomedical applications, and the other is a sensor integrated into an RC-based frequency reference.

After discussing how these results were achieved, the thesis ends with Chapter 6, which consists of conclusions and discussions of future work.

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Chapter 2

Sensor and readout topologies

2.1 Introduction

This chapter discusses some general issues involved in the design of resistor-based temperature sensors. First, the characteristics of the different sensing resistors available in standard CMOS technology are described. This is followed by a discussion of the available impedance references, which are needed to convert resistance changes into digital information. Two possible sensor structures: dual-R (with a resistor reference) and RC (with a capacitor reference), are then presented. Lastly, the requirements and architectures of various readout circuits are discussed.

2.2 Sensor design

2.2.1 Sensing resistors

In standard CMOS technology, many types of resistors are available, including metal resistors, diffusion resistors, polysilicon (poly) resistors, N-well resistors, and silicided resistors. As shown in Figure 1.11, they all are temperature-dependent to some degree and so can all be potentially used to sense temperature. Although resistors can be also realized with active devices, e.g. by biasing a MOSFET in the triode region, they suffer from a greater spread, and are much less stable.

To meet the stringent resolution, energy efficiency, and stability requirements of the targeted application - the temperature compensation of frequency references, sensing resistors with a large temperature coefficient (TC), low $1/f$ noise, and high stability (low voltage and stress sensitivities, low long-term drift) should be used.

In terms of sensitivity, metal resistors (with TCs ranging from 0.3% to 0.4%/°C) are the best choice. However, as they are optimized for high-conductivity interconnections, their sheet resistance (<100mΩ/□) is extremely low. This results in either high power consumption or a large chip area.

The sheet resistance of diffusion resistors is typically around 100Ω/□, which enables a compact and low-power sensor design. However, it is strongly voltage-dependent. As shown in Figure 2.1, the cross-sectional area of an N+ diffusion resistor will decrease as its potential increases and the depletion region boundary moves deeper into the N-diffusion region. Consequently, the resistor's sheet resistance will become larger. Another disadvantage of diffusion resistors is their relatively small TC: about 0.1%/°C to 0.2%/°C.

N-well resistors are very lightly-doped N diffusion resistors. Although their TCs are large (~0.3%/°C) and comparable to that of metal resistors, their lower doping levels result in larger voltage and stress [2.1] sensitivities.

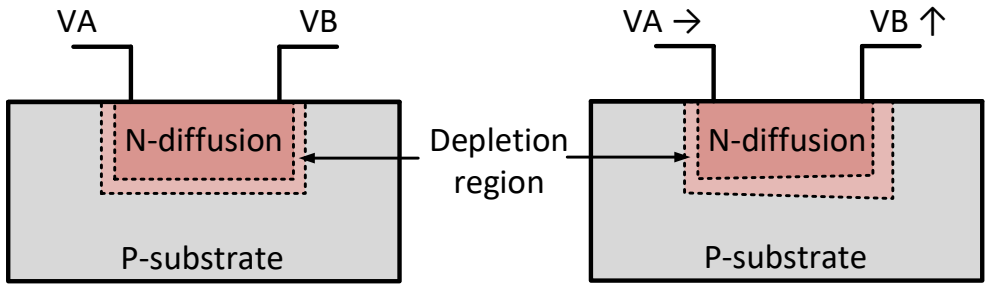


Figure 2.1: Simplified cross section of an N+ diffusion resistor and illustration of its voltage dependency.

Unlike diffusion resistors, polysilicon resistors have a fixed geometry, and thus a much smaller voltage dependency. They also have higher sheet resistance, in the order of 100Ω/□. In some processes, specially designed high-resistance poly resistors with sheet resistances of ~1kΩ/□, or even higher, are also available. Depending on the technology and process, the TCs of poly resistors can be either positive or negative, ranging from −0.2%/°C to 0.1%/°C.

Compared to diffusion resistors, however, one disadvantage of poly resistors is their relatively high levels of flicker noise (1/*f* noise). As shown in Figure 2.2, poly resistors are composed of small crystal structures which are separated by grain boundaries. These boundaries create extra energy states. When charge carriers move across such boundaries, some are trapped and later released by these states [2.2]. Such random trapping and releasing leads to noise that has a 1/*f* type spectrum [2.3]. Because the amplitude of 1/*f* noise is higher at low frequencies, it cannot be effectively suppressed by filtering or averaging. Moreover, its amplitude is proportional to the resistor's current [2.3], which means that increasing its power dissipation will not improve its SNR. Thus, 1/*f* noise represents a fundamental limit on the resolution of resistor-based sensors.

Another disadvantage of poly resistors is their significant long-term drift. This is mainly due to the presence of weakly bonded hydrogen atoms in their grain-

boundaries [2.4]. Due to excessive local heating or current, these bonds may break and then permit traps, i.e., energy states, to reform. As a result, the probability of carriers flowing through grain boundaries decreases, and so resistance increases. After being exposed to 150°C for 6 months, resistance drifts of between 0.2% to 0.8% were observed [2.5]. In comparison, the drift of diffusion resistors in the same technology is 4 to 8 times smaller [2.6], and that of metal resistors is negligible.

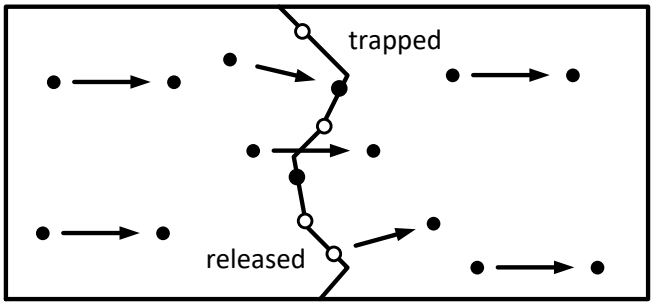


Figure 2.2: Charge carriers trapped and released at grain boundaries.

Two other types of resistors are available in most standard CMOS technologies: silicided poly and silicided diffusion resistors. Although they are not always modelled, there are always equivalent structures used to reduce the gate/source/drain resistance of MOSFETs, as shown in Figure 2.3. Silicide layers are formed on top of polysilicon (gate) or diffusion (source or drain) layers by first depositing a thin transition metal layer and then applying heat. The metal then reacts with the silicon, forming a low-resistance transition metal silicide. As a result, the characteristics of such resistors fall between those of metal and silicon resistors. Compared to silicon resistors, they have a relatively large and positive TC (~0.3%/°C), a more linear temperature dependence, and lower 1/*f* noise. However, their sheet resistance is much lower (~10Ω/□). They also have low voltage and stress sensitivities, and are quite stable, showing no electrical degradation (e.g., hysteresis) even after being heated up to 500°C [2.7]. Their long-term drift should be also much lower than that of silicon resistors. However, to the author's best knowledge, no serious reliability tests have been conducted for this type of resistor.

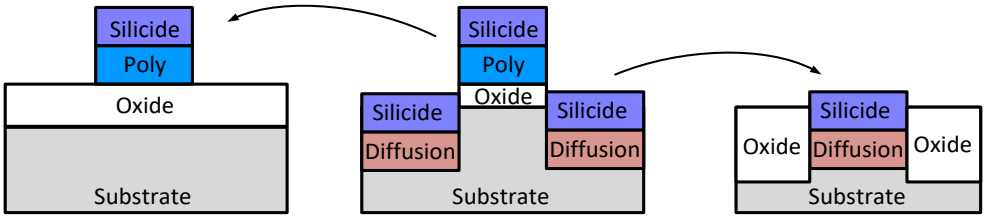


Figure 2.3: Simplified cross section of silicided poly (left) and silicided diffusion (right) resistors compared to that of a MOSFET (middle).

Since their characteristics are determined by the silicided layer, silicided poly and silicided diffusion resistors exhibit similar behavior in most respects. One subtle difference is their parasitic capacitances: silicided diffusion resistors have a large junction capacitor between the diffusion layer and its well/substrate, while silicided poly resistors do not have this issue. As a consequence, silicided diffusion resistors are less suitable for high-frequency circuits.

The performance of the commonly available CMOS resistors is summarized in Table 2.1.

Table 2.1. Resistor characteristics in standard CMOS processes.

Resistor type	Metal	Diffusion	N-well	Poly	Silicided
1st-order TC	Large	Medium	Large	Medium or Small	Large
1st-order TC sign	+	+	+	−/+	+
2nd-order TC	Medium	Medium	Large	Medium	Small
Sheet resistance	Very small	Large	Large	Large	Small
Supply dependency	Small	Medium	Large	Small	Small
1/*f* noise	Negligible	Negligible	Negligible	Large	Small or negligible
Stress sensitivity	Small	Large	Very large	Medium	Small
Drift	Very small	small	Small	large	Very small or small

At the start of this research, most resistor-based temperature sensors employed diffusion or poly sensing resistors [2.8]-[2.11]. However, as shown above, silicided resistors are better candidates. Their only disadvantage is a relatively small sheet resistance, which can be tolerated in frequency compensation applications, where the sensing resistor is typically not very large (~100kΩ) in order to achieve low thermal noise and high sensing resolution.

2.2.2 Impedance reference

2.2.2.1 Reference choices

In principle, a sensing resistor is a temperature-dependent impedance. Therefore, in order to digitize this impedance, a reference impedance is required.

The simplest reference impedance is a reference resistor. As illustrated in Figure 1.11, temperature can then be sensed by reading the voltage output of a resistive divider. Alternatively, capacitors and inductors can be used to generate an impedance reference in the presence of a fixed frequency reference, as summarized in Table 2.2.

Table 2.2. Characteristics of different references.

Type	Resistor	Capacitor	Inductor
Symbol			
V-I characteristic	$V = R \cdot I$	$I = C \cdot \frac{dV}{dt}$	$V = L \cdot \frac{dI}{dt}$
Impedance	R	$\frac{1}{j\omega C}$	$j\omega L$
Structure	Poly, diffusion, metal, etc.	Fringe, plate, MOS gate.	Planar
Quality factor	--	High	Low

The drawbacks of an on-chip inductor reference are its large area and a low quality factor (~10) at GHz frequencies. Moreover, the quality factor is frequency-dependent, and drops significantly at sub-GHz frequencies. However, designing precision readout circuits operating at GHz frequencies is extremely challenging.

Capacitors are more suitable for low-frequency readout circuits. As shown in Figure 2.4, there are three main types of on-chip capacitors: fringe capacitors (MOM, or metal-oxide-metal capacitors), plate capacitors (MIM, or metal-insulator-metal capacitors), and MOS capacitors utilizing the capacitance of the MOSFET's gate.

Benefiting from their thin gate oxide, MOS capacitors have a high capacitance density. However, their capacitance is voltage-dependent, as the space charge region of the substrate is modulated by the gate voltage. Additionally, the MOS capacitor is sensitive to temperature and process spread: when used as the impedance reference, the resistor-based sensor's accuracy will be degraded.

MIM and MOM capacitors are much more stable due to their well-defined electrode spacing and the low temperature-dependency of their oxide dielectrics. Typically, their TC is smaller than 100ppm/°C [2.12]. In some modern CMOS processes, the density of MOM capacitors is higher than that of MIM capacitors. However, in mature processes, e.g., 0.18μm CMOS, the MIM capacitor still has a higher density, and is thus preferred in area-constrained designs.

The drift of capacitors is mainly caused by electrical stress [2.13][2.14], which creates trapped charges in the oxide insulator layer. This, in turn, can generate new dipoles and so modulate the dielectric permittivity. As this is determined by the strength of the electrical field on the dielectric, operating the circuit at standard supply voltages should almost eliminate this effect. In [2.15], the 1fF/μm^2 MIM capacitor drifts by less than 0.01% with an applied voltage of 5V. This implies that, for most MIM capacitors with densities $\leqslant$ 2fF/μm^2, no observable drift will occur if the applied voltages are kept below 2.5V.

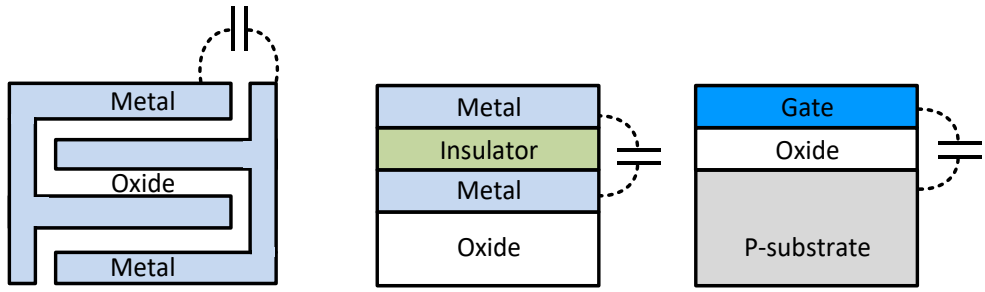


Figure 2.4: (a) Top view of a MOM capacitor. (b) Cross section of a MIM capacitor. (c) Cross section of a MOS capacitor.

2.2.2.2 Comparison

As discussed above, both resistors and capacitors are suitable references for resistor-based sensors. Both structures have their own advantages and disadvantages.

The benefits of using a resistive reference include ease of use and high efficiency. Furthermore, it does not need to operate at a well-defined frequency. Advantageously, the TC of the reference resistor may even be chosen to be opposite to that of the sensing resistor, resulting in a resistor divider with increased sensitivity. Assuming that the TCs of two resistors are TC_p (positive) and TC_n (negative), the theoretical FoM of such a resistor divider sensor (Figure 1.11) can be expressed as:

$$FoM_{WhB} = \frac{8kT}{\left(TC_p - TC_n\right)^2}, \tag{2.1}$$

which is smaller (better) than that given in Equation (1.13).

However, as shown in Table 2.1, only certain poly resistors have a negative TC, in contrast to the positive TC of silicided sensing resistors. As a result, the price for better energy efficiency is excess 1/*f* noise and worse stability.

RC sensors, on the other hand, require a well-defined frequency reference and are less energy-efficient. However, as the TC of MIM or MOM capacitors (<100ppm/°C) is much lower compared to that of resistors (typically >1000ppm/°C), these sensors suffer from less spread and can achieve higher accuracy with the same number of trimming points. Also, compared to dual-R sensors with polysilicon reference resistors, RC sensors implemented with silicided resistors are more stable.

The features of dual-R and RC temperature sensors are summarized in Table 2.3.

Table 2.3. Resistor-based sensor overview.

Type	dual-R	RC
Reference	Resistor	Capacitor + frequency
Accuracy	Medium	High
Efficiency	High	Medium
Stability	Medium	High

2.2.3 Sensor structures and readout method

2.2.3.1 Dual-R sensors

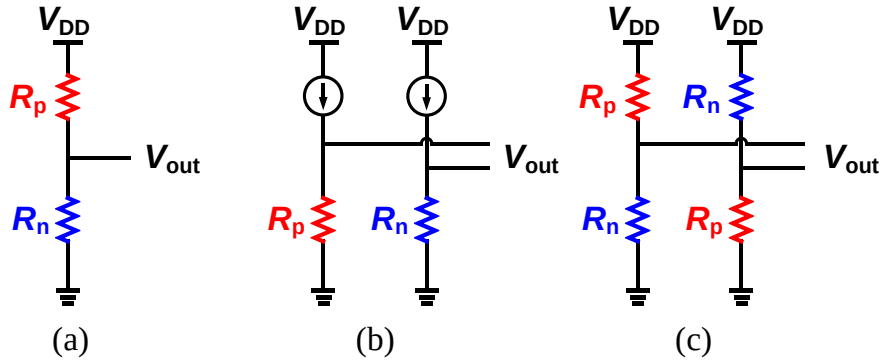


Figure 2.5: Several dual-R sensor structures. (a) Resistor divider. (b) Current-driven resistors. (c) Wheatstone bridge.

There are several ways to digitize the ratio between two resistors with different TCs (R_p and R_n). Compared to the simple resistor divider (Figure 2.5 (a)), the use of current sources allows for a small differential output that can be easily processed (Figure 2.5 (b)) [2.8]. However, the excess noise produced by the current source will limit noise efficiency. The most commonly used structure is the fully differential Wheatstone bridge (WhB) (Figure 2.5(c)). Apart from improved power supply sensitivity [2.15], it does not require matched current sources.

Other than the voltage readout methods shown in Figure 2.5, dual-R sensors can be configured to output a temperature-dependent current. The advantages and disadvantages of the two approaches will be discussed in more detail in Chapter 4.

2.2.3.2 RC sensor structures

Based on how they are driven by a frequency reference, RC sensors can be divided into two main categories: discrete-time and continuous-time. Just like dual-R sensors, their power supply sensitivity can be improved by using a fully differential topology. In the following sections, however, simple single-ended schematics will be used to illustrate their working principles.

One type of discrete-time RC sensor employs switched-capacitor resistor references, as shown in Figure 2.6 (a) [2.16]. Given a fixed input frequency f_s, the effective reference resistance R_0 can then be expressed as $R_0=1/(C_0 f_s)$. By using a large capacitor C_F to filter out switching transients, the resulting voltage output is similar to that of a real resistor divider. Figure 2.6 (b) shows an alternative topology based on the settling characteristics of a low-pass RC filter [2.17]. The capacitor C_0 is first reset to V_{DD} (φ_{RST}), while during the next phase (φ_{DCHG}), C_0 is discharged through the sensing resistor R_S. After a fixed period, the discharging stops, and the residual voltage on C_0 is a representation of the RC time constant and temperature.

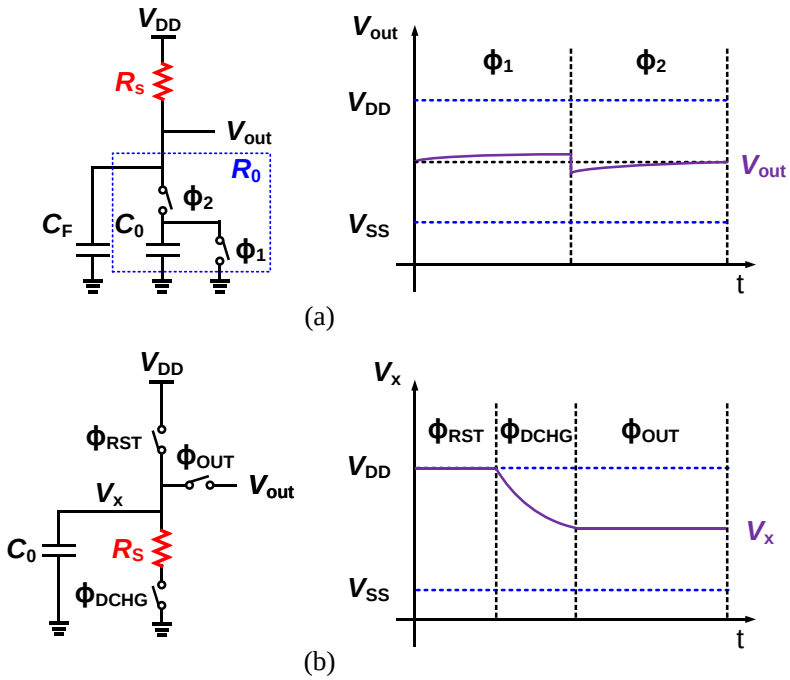


Figure 2.6. Discrete-time RC sensors: (a) Using a switched-capacitor resistor. (b) Using incomplete settling of an RC filter.

As already mentioned, one advantage of RC-based sensors over dual-R sensors is high accuracy. However, the switching operation of discrete-time sensors is accompanied by charge injection, which causes errors in the voltage stored on the capacitors. As a result, the sensor becomes less accurate.

Charge injection can be minimized if its current path to the reference capacitor is blocked by a resistor. As a result, temperature sensors built around continuous-time RC filters are potentially more accurate. Some of the filter variations, including the low-pass filter, poly-phase filter [2.18], and Wien bridge (WB) [2.10][2.11], are shown in Figure 2.7. Given a fixed frequency input, which is typically a square wave generated from inverters, the phase shift of the output waveform is determined by the temperature-dependent RC time constant.

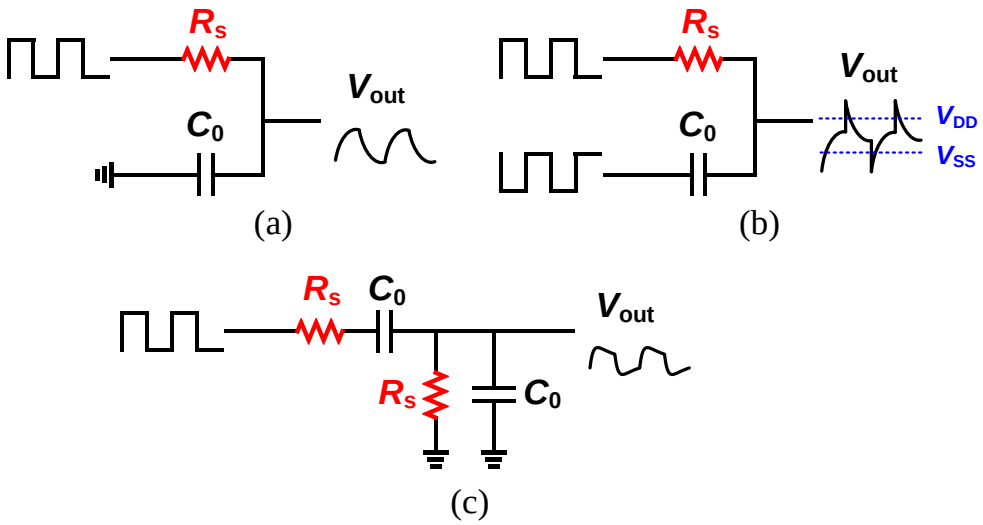
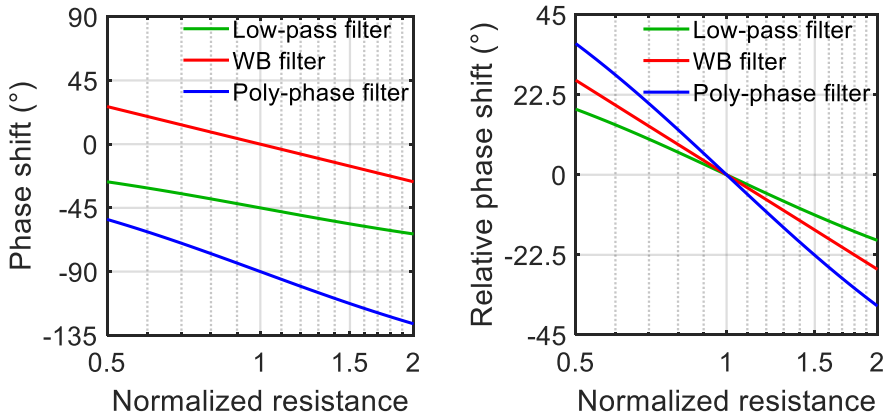


Figure 2.7: Continuous-time RC sensors: (a) Low-pass filter. (b) Poly-phase filter. (c) Wien bridge (WB) filter.

Assuming all the filters are operated around their center frequencies ($\omega R_s C_0 \approx 1$), their phase shifts as a function of normalized resistance are presented in Figure 2.8 (a). Of the three, the poly-phase filter has the highest phase sensitivity [2.18] (Figure 2.8 (b)), and thus the best theoretical FoM. At the center frequency, its phase sensitivity with respect to R_s is $1/R_s$, which is 2×/1.5× larger than that of the low-pass filter/Wien-bridge filter, respectively. However, when driven by a rail-to-rail square-wave, the output voltage of the poly-phase filter will exceed the supply rails, thus imposing a stringent requirement on the input stage of the readout circuit. Moreover, high-frequency supply noise can be directly coupled to its output signal. On the other hand, the Wien bridge filter has the second-largest sensitivity and an inherent filtering of high-frequency noise. Thus, it is the preferred building block of high-accuracy temperature sensors.



(a) (b)

Figure 2.8: (a) Phase shift and (b) relative phase shift of different RC filters as a function of normalized resistance.

2.2.3.3 RC filter Readout

An RC filter can be seen as a circuit that outputs different phases at different input frequencies. As such, there are two ways to sense its RC time constant: by fixing its input frequency and extracting the output phase, or by enforcing a certain output phase and measuring the required excitation frequency. Extracting its RC time constant by sensing its output amplitude is also possible. However, if not processed carefully, the result will be highly sensitive to the supply voltage.

The former method is depicted in Figure 2.9 (a). Typically, it requires a reference clock that generates two signals of the same frequency: a driving signal φ_{dirve}, and a reference signal φ_{ref} which serves as the input of a phase-ADC. As will be discussed in detail in Chapter 3, this usually consists of two blocks: a phase detector, which converts the filter's phase shift into a voltage or current, followed by a conventional amplitude-domain ADC.

The latter method can be implemented by a frequency-locked-loop (FLL) [2.11][2.18], as shown in Figure 2.9 (b). A phase detector first converts the phase output of the RC filter into a voltage or current signal, which, after integration, controls the driving frequency of the RC filter. The feedback loop then forces the output of the phase detector to zero, thus fixing the RC filter's output phase, and making the VCO's output frequency inversely proportional to the filter's RC time constant. Since an FLL outputs an RC-dependent frequency, a frequency reference is still required for digitization, usually with the help of a digital counter.

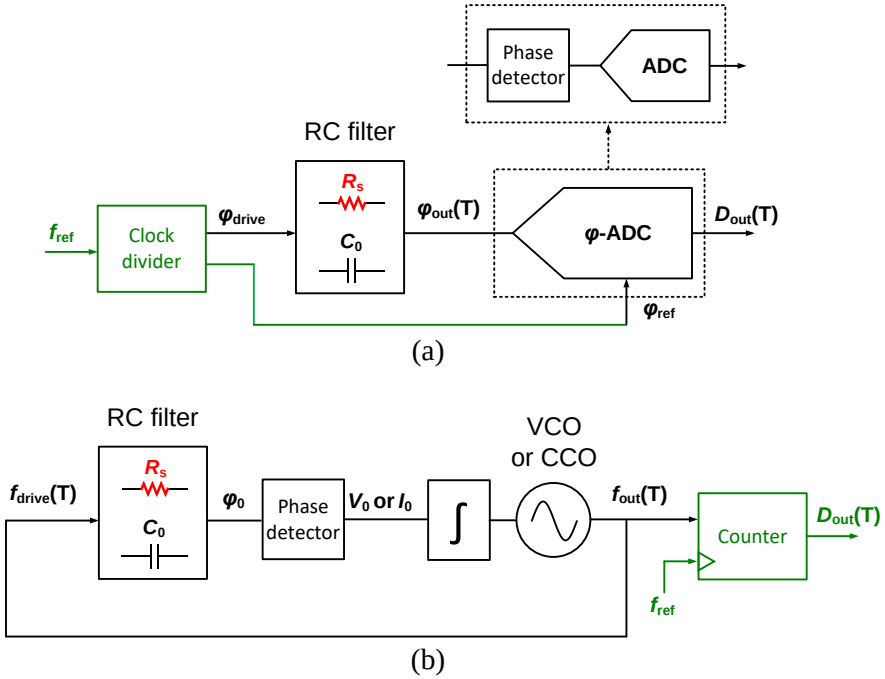


Figure 2.9: RC filter readout methods using (a) phase-ADC and (b) frequency-locked loop, with elements in green indicating the generation and processing of clock signals from an external reference.

Both structures have their advantages and disadvantages. The phase-ADC approach is simple and direct. However, the shape of the RC filter's output waveform will vary over temperature, imposing stringent nonlinearity requirements on the phase-ADC in order to obtain accurate sensor readout. The FLL-based readout, on the other hand, does not have this issue. However, its sensing resolution is typically limited by the counter's clock frequency. For example, to obtain a 0.5mK quantization-noise-limited resolution from an RC filter with a 0.3%/°C TC, the counter should count up to over 1/(0.3%·0.0005) times. Assuming a 5ms conversion time, the reference clock frequency should be greater than 133MHz. As a result, the counter will be very power hungry, especially in mature processes (e.g., 0.18µm CMOS), which limits the achievable energy-efficiency of such sensors. Thus, the phase-ADC is better suited for the high-resolution task of compensating the temperature variations of on-chip frequency references.

2.3 ADC choice

As discussed above, the FLL-based readout of RC-based sensors is not well suited to the target application, so a phase ADC will be used. This in turn requires an

amplitude-domain ADC. There are mainly three requirements for the ADC. First, to ensure sufficient sensing resolution, the ADC should have a high SNR. For example, achieving 0.5mK resolution in a 200°C temperature range requires an SNR of >112dB. Second, to achieve a high energy efficiency of the overall circuit, the ADC should have a balanced power/noise performance compared to the sensor front-end. This means that the ADC should be as efficient as possible, e.g. have a good Schreier FoM [2.19]. Last but not least, the ADC should have high linearity and accuracy, so that the sensor's trimming effort can be minimized.

2.3.1 Nyquist vs. oversampled ADCs

Many sensor readout circuits use Successive Approximation ADCs (SAR ADCs) because of their low power. However, due to the binary nature of their DAC elements, errors like non-monotonicity and missing-codes limit their resolution. As a result, this is typically limited to ~14 bits, or a ~85dB SNR, as shown in Figure 2.10 [2.20]. With state-of-the-art background calibration, their SNR can be improved to about 100dB [2.21]. However, this is still below the stringent requirement (>110dB) imposed by the targeted temperature sensing application. Another major type of Nyquist ADCs is the pipeline ADC. Although these can be extremely fast, their resolution is typically worse than that of a SAR ADC: other than DAC mismatch, additional errors are introduced during the generation of the inter-stage residue signals.

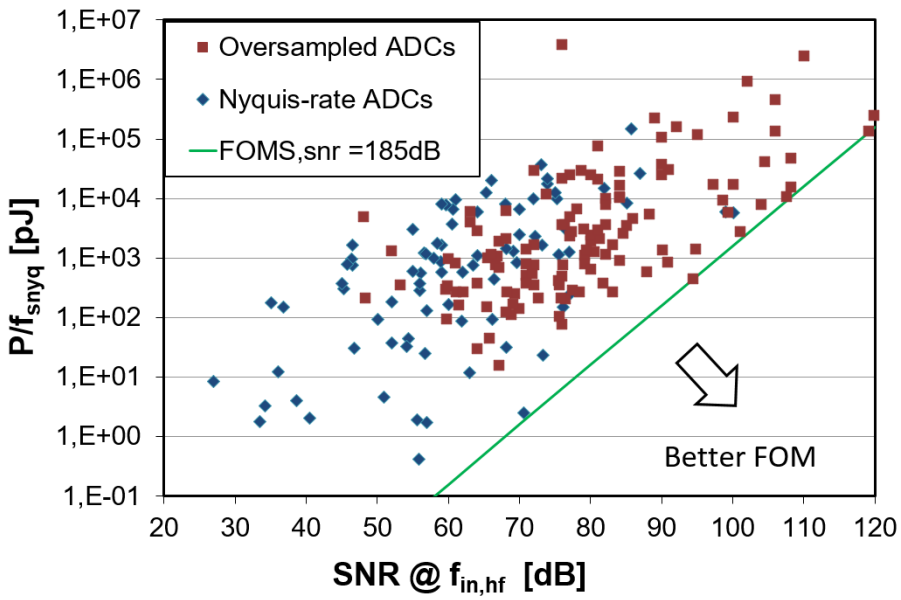


Figure 2.10: Power per bandwidth vs. SNDR of Nyquist-rate and oversampled ADCs, with a constant Schreier FoM line [2.20].

Oversampled ADCs (ΔΣ-ADCs) can achieve low quantization noise levels by shaping quantization noise away from a bandwidth of interest, and then suppressing it through filtering. This enables the use of inherently linear 1-bit quantizers and DACs. If multi-bit DACs are used, their mismatch errors can also be shaped by using algorithms like data-weighted averaging (DWA) [2.22]. As a result, oversampled ADCs can achieve higher SNR than Nyquist ADCs, and meet the resolution requirements of the temperature compensation application. Furthermore, they can also achieve excellent energy efficiency [2.20].

Due to oversampling, ΔΣ-ADCs have a lower conversion rate than Nyquist ADCs. However, this is not an issue in the targeted application, which only requires bandwidths of about 100Hz.

2.3.2. Continuous-time ΔΣ-ADC

Reading out a resistor always involves passing a current through it. As a result, a continuous-time (CT) ΔΣ-ADC (Figure 2.11) is the most natural choice. As will be shown in the following chapters, the temperature sensing resistor(s) can be reconfigured as the input resistor (R_{in}) in a CT ΔΣ-ADC, so the current flowing through the sensing resistor can be directly digitized.

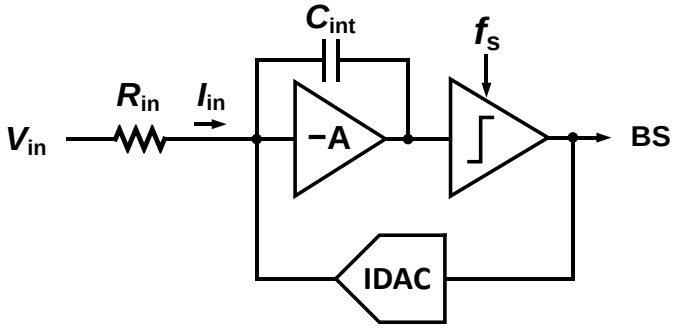


Figure 2.11: Basic structure of a CT ΔΣ-ADC.

2.4 Concluding remarks

In this chapter, major design choices for both the sensor front-end and the readout circuit have been made based on the requirements of the targeted frequency compensation application. These are summarized in Table 2.4. Of the available CMOS resistors, silicided resistors are the best choice due to their high sensitivity and high stability. Depending on application requirements, the reference impedance can be achieved using either a negative-TC poly resistor for high energy efficiency, or a stable low-TC capacitor driven at a reference frequency for high accuracy. For the

dual-R/RC type of sensor, a Wheatstone bridge/Wien bridge is preferred. As for the readout circuit, the resolution requirement can only be achieved by using oversampled ADCs. Due to the resistive sensing requirement, CT ΔΣ-ADC becomes a natural choice.

Table 2.4. Major design choices of resistor-based temperature sensors.

Sensing resistor	Silicided resistor	
Reference (sensor type)	Poly Resistor (dual-R)	Capacitor + frequency (RC)
Advantage / Focus	High efficiency	High accuracy
Preferred sensor structure	Wheatstone bridge	Wien bridge
Readout circuit	CT ΔΣ-ADC	

Having made these design choices, the following two chapters will focus on the design and characterization of both Wien bridge (Chapter 3) and Wheatstone bridge (Chapter 4) sensor prototypes.

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Chapter 3

Wien-bridge-based temperature sensors

3.1 Introduction

In Chapter 2, RC and dual-R based sensors were presented and compared. RC-based sensors rely on a stable reference capacitor, which makes them suitable for building accurate temperature sensors. This chapter discusses a particular and suitable approach: the readout of a Wien-Bridge (WB) sensor with a phase-domain ADC. It begins with a discussion of general design choices. Then, three different WB sensor prototypes are presented based on their publication sequence.

3.2 General design choices

3.2.1 WB sensor

The circuit diagram of a differential WB is shown in Figure 3.1 (a). It is a 2nd-order band-pass filter whose voltage amplitude and phase transfer functions can be expressed, respectively, by equations 3.1 and 3.2.

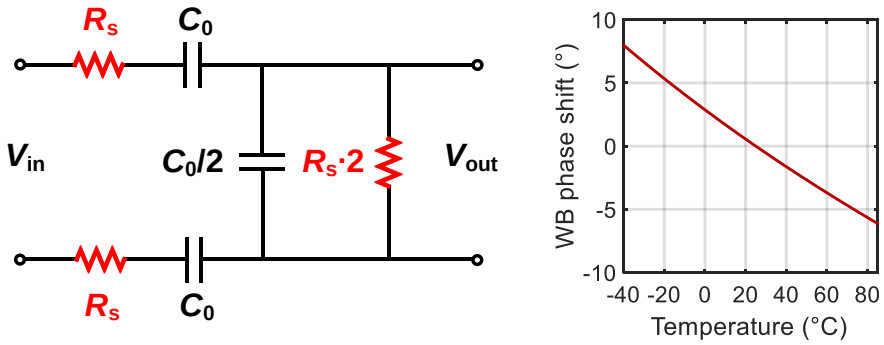
$$\mathrm{H}(j\omega) = \frac{R_s C_0 j\omega}{1 - {R_s}^2 {C_0}^2 \omega^2 + 3R_s C_0 j\omega} \tag{3.1}$$

$$\varphi_{WB}(\omega) = -tan^{-1}\left(\frac{{R_s}^2 {C_0}^2 \omega^2 - 1}{3R_s C_0 j\omega}\right) \tag{3.2}$$

Given a temperature-dependent RC time-constant but a fixed input frequency (at around the WB's center frequency), the amplitude of the WB output will remain roughly constant, while the output phase will vary over temperature.

As discussed in Chapter 2, to reduce chip area, the WB capacitors (C_0) should be realized as high-density Metal-Insulator-Metal (MIM) capacitors, and to reduce

supply sensitivity, silicided poly resistors (less parasitic capacitance) are preferred over silicided diffusion resistors. The temperature dependence of the WB phase will then be mainly determined by the silicided poly resistor, since the TC of MIM capacitors is quite low (<100ppm/°C). In the chosen 0.18µm technology, the resistor's TC is about 0.285%/°C, and so the WB phase will vary by about 15° over the industrial temperature range (−40 °C to 85 °C), as shown in Figure 3.1 (b).



(a) (b)

Figure 3.1: (a) Differential Wien-Bridge and (b) its phase output as a function of temperature.

The same temperature-dependent phase response can be obtained by measuring the current through the output resistors [3.1], as shown in Figure 3.2 (a). This facilitates the readout of a WB by a CT ΔΣ-ADC, as two of the WB resistors can be reused as the ADC's input resistors (Figure 3.2 (b)). The WB phase can then be detected by inserting a phase detector in the integrator's feedback loop, as will be discussed in section 3.2.2.

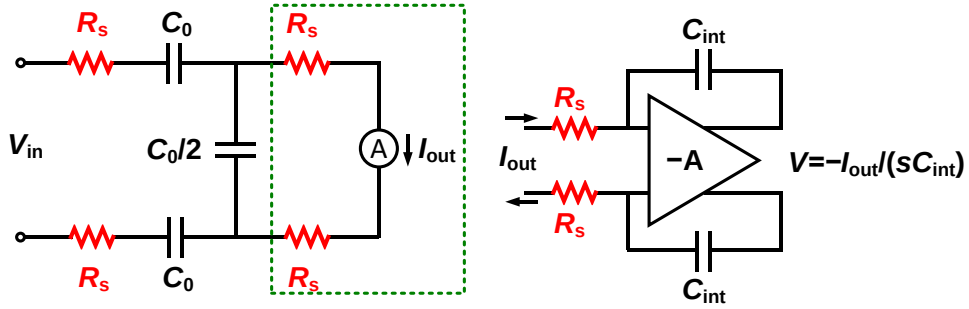


Figure 3.2: (a) Current-based readout of a WB. (b) Sensing resistors reused as input resistors in a CT ΔΣ-ADC.

3.2.2 Phase-domain ADC

3.2.2.1 Phase detector

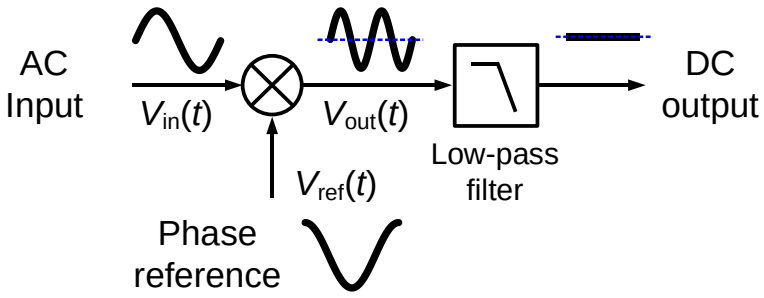


Figure 3.3: A phase detector built with an analog multiplier and a low-pass filter.

Phase detection is essential to the operation of a phase-domain ADC. For analog input signals, it can be achieved with the help of an analog multiplier and a low-pass filter, as shown in Figure 3.3. Here both the input signal and the reference signal are sine-wave signals with the same frequency f_0, i.e.,

$$\begin{aligned} V_{in}(t) &= A_{in} \cdot sin(2\pi f_0 t + \varphi_{in}) \\ V_{ref}(t) &= A_{ref} \cdot sin(2\pi f_0 t + \varphi_{ref}) \end{aligned} \tag{3.3}$$

The multiplier's output can then be expressed as:

$$V_{out}(t) = \frac{A_{in}A_{ref}}{2} \cdot \left(\cos(\varphi_{in} - \varphi_{ref}) - cos(4\pi f_0 t + \varphi_{in} + \varphi_{ref})\right). \tag{3.4}$$

It contains two terms, the first is a DC signal that contains the phase difference information, while the second contains high-frequency content that can be removed by a low-pass filter. Due to the cosine function, the DC signal achieves the maximum sensitivity and linearity when $\varphi_{in} - \varphi_{ref} \approx 90°$.

Alternatively, the reference signal may be a square-wave, allowing the analog multiplier to be replaced by an analog multiplexer, as shown in Figure 3.4. Depending on the value of the phase reference, the multiplexer outputs either the original or the inverted version of the input signal. This precisely realizes a reference square-wave signal with an amplitude $A_{ref} = 1$. As for a sine-wave reference, a low-pass filter can be used to eliminate the higher-order multiplication products, leaving a DC signal that represents the desired phase information.

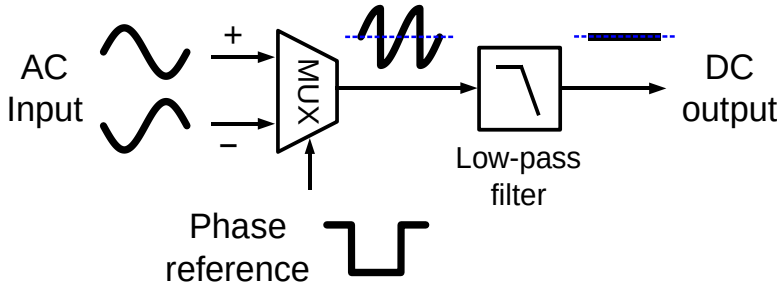


Figure 3.4: Phase detector built with an analog multiplexer and a low-pass filter.

3.2.2.2 Phase DAC and phase-domain ΔΣ-ADC

Although the multiplier approach (Figure 3.3) is quite straightforward, it requires an accurate and low-noise reference phase signal as well as a precise analog multiplier, which is often power-hungry. On the other hand, the multiplexer approach shown in Figure 3.4 can be realized by switches, and is thus much more energy-efficient. In the case of a current-mode WB sensor, the output current direction can be toggled by a chopper, effectively multiplying the WB output current by a square wave of unity amplitude, as shown in Figure 3.5. By using a multiplexer to select various phase references, the phase detector circuit can be turned into a phase DAC. Apart from the reference signal, the driving signal of the WB is also made a square wave to achieve low-noise and high energy-efficiency. The waveforms over temperature are plotted in Figure 3.6.

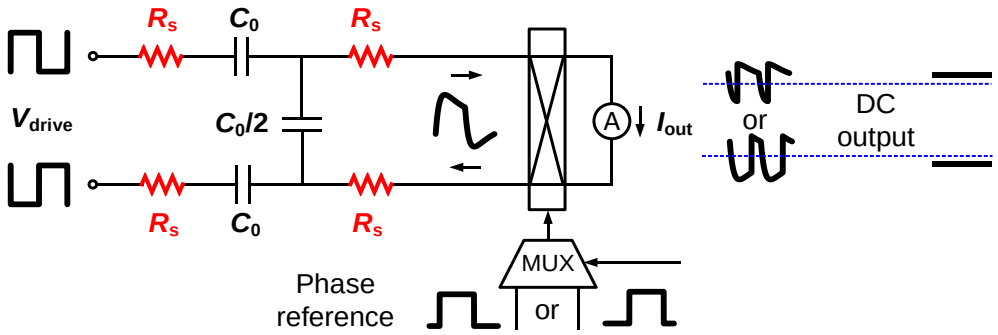


Figure 3.5: WB sensor and analog multiplexer/phase DAC achieved by a current chopper.

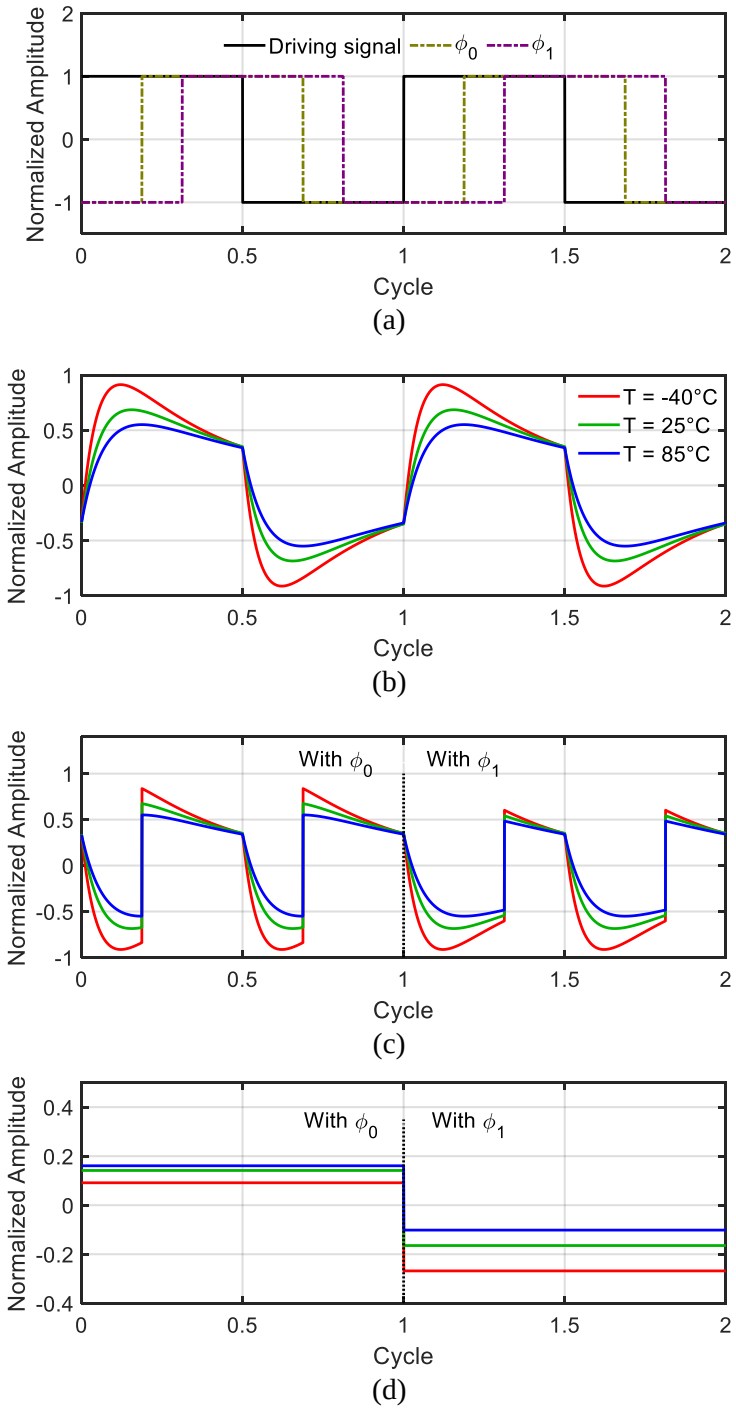


Figure 3.6: (a) WB driving and phase DAC signals. (b) WB sensor output under different temperatures. (c) WB sensor output after analog multiplexer. (d) Averaged output over one cycle.

As shown in Figure 3.7, a phase-domain Delta-Sigma ADC (PDΔΣ-ADC) can be built around a WB sensor by incorporating a phase DAC in the feedback path of a continuous-time ΔΣ-ADC [3.2]. The ADC first down-converts $\varphi_{WB}(T)$ by multiplying it by a phase reference at the same frequency (f_{demod}=f_{drive}). Depending on the chosen references φ_0 or φ_1 of the phase DAC, the multiplier's DC output is either positive or negative [3.1]. The multiplier's output is filtered by the integrator and then quantized. In a negative feedback loop, the quantizer toggles the reference phases such that the loop filter's average DC input is zero. The average of the output bit-stream is therefore a digital representation of $\varphi_{WB}(T)$.

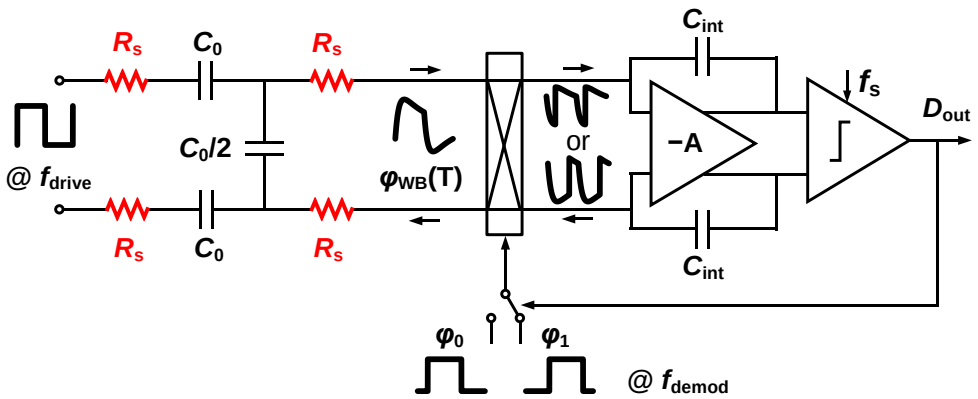


Figure 3.7: WB sensor digitized by a phase-domain ΔΣ-ADC.

3.2.3 System analysis

3.2.3.1 Resolution and FoM

Besides the promising accuracy of WB sensors, resolution and resolution FoM remain important specifications. Two simplifications are made to obtain the WB sensor's theoretical FoM, e.g, the FoM without considering the power and noise of its readout circuits. First, both the driving and the demodulating signals are assumed to be sine waves with the same frequency: $V_{in} = A\cdot\sin(2\pi f_0 t)$ and $V_{demod} = \sin(2\pi f_0 t+\varphi_{demod})$, where A is the amplitude of the driving signal. Second, the WB filter is assumed to be driven at its center frequency, i.e., $f_0 = 1/(2\pi R_S C_0)$, and φ_{demod}=90°.

The theoretical resolution of the WB sensor can then be derived by comparing the levels of the noise and the temperature-dependent DC signal present at the output of the low-pass filter. The demodulating signal is assumed to be noise-free, and thus its amplitude doesn't affect the sensor's resolution.

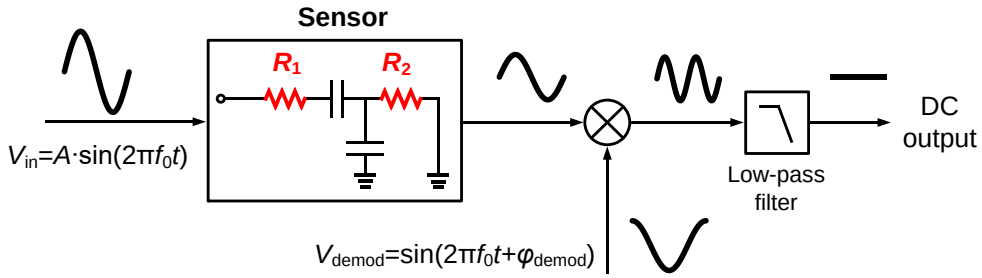


Figure 3.8: Phase detection model for WB sensor's resolution calculation.

Under the orthogonal sine wave assumption, the sensitivity of the demodulator's DC output (I_{DC}) to temperature can be expressed as:

$$S_{WB} = \frac{dI_{DC}}{dT} = \frac{dI_{DC}}{d\varphi_{WB}} \cdot \frac{d\varphi_{WB}}{dT} = \frac{A}{6R_S} \cdot \frac{2TC_s}{3} = \frac{A \cdot TC_s}{9R_S}. \tag{3.5}$$

At the driving frequency f_0, the noise spectrum densities of R_1 and R_2 in Figure 3.8 before demodulation are $i_{n,R1} = \sqrt{4kT/(9R_s)}$ and $i_{n,R2} = \sqrt{4kT \cdot 5/(9R_s)}$, respectively. After demodulation, the noise power will be reduced by 4×, as the power of the unity-amplitude demodulation sine wave is 0.5, and only half of the noise power will be demodulated to DC. Given a conversion time of t_{conv}, the amplitude of the output current noise becomes:

$$I_n = \sqrt{{i_{n,R1}}^2 + {i_{n,R2}}^2} \cdot \sqrt{\frac{1}{2t_{conv}}} \cdot \sqrt{\frac{1}{4}} = \sqrt{\frac{kTR_S}{3t_{conv}}}. \tag{3.6}$$

By combining (3.5) and (3.6), the resolution of this WB sensor can be expressed as:

$$\Delta T = \frac{I_n}{S_{WB}} = \frac{3}{A \cdot TC_S}\sqrt{\frac{3kTR}{t_{conv}}}. \tag{3.7}$$

For a differential WB sensor, however, the resolution improves by $\sqrt{2}$ due to the halved noise power, i.e.,

$$\Delta T_{diff} = \frac{3}{A \cdot TC_S}\sqrt{\frac{3kTR}{2t_{conv}}}. \tag{3.8}$$

When driven at its center frequency f_0, the power consumed by the differential bridge is $A^2/(3R_S)$. By combining this with (3.8), the sensor's FoM can be calculated as:

$$\mathrm{FoM}_{WB} = \frac{9kT}{2 \cdot {TC_S}^2}. \tag{3.9}$$

Assuming TC_S = 0.285%/°C, the theoretical resolution FoM is about 2.3fJ·K^2.

In practice, it is easier and more accurate to use square-wave drive and demodulation. In this case, the higher-order harmonics will reduce the phase sensitivity and increase the power consumption of the WB. Simulations show that the theoretical FoM will then degrade to 9.7fJ·K^2. In a real design, however, the power and noise of the readout circuit will further degrade the FoM.

3.2.3.2 Nonlinearity and trimming

To reduce the calibration costs of a temperature sensor, the number of trimming points should be minimized. In the case of a WB sensor, this is limited by the spread of the sensing resistor. As presented in Chapter 1, a 2-point trim is required to achieve good accuracy. Thus, the readout circuit should not introduce extra error after a 2-point trim.

Unfortunately, applying a 2-point trim to the bitstream average of a phase-domain ΔΣ-ADC will result in extra spread. This is because, due to RC spread, nominally identical WB sensors will output slightly different phase shifts. Since the readout system is non-linear, the transfer function of each sample will then be slightly different, as shown in Figure 3.9. As a result, the residual non-linearity will also be slightly different over samples, and so more trimming points (>2) will be required to achive high accuracy.

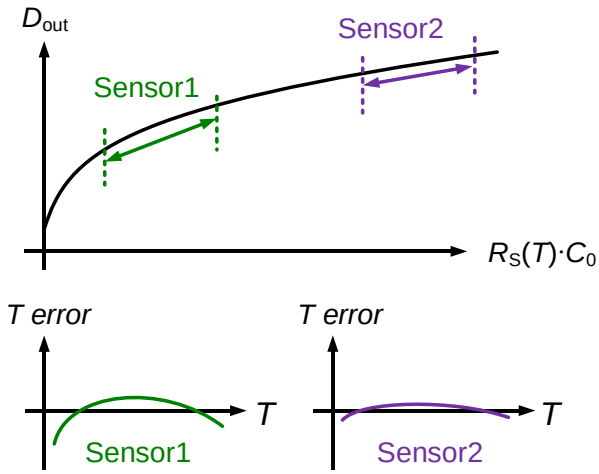


Figure 3.9: Illustration of the effect of readout nonlinearity on sensor's accuracy after a 2-point trim.

To avoid increasing the number of trimming points, the nonlinearity of the sensor readout should be compensated before trimming. This non-linearity mainly consists of two parts: a) the nonlinear RC-to-phase characteristic of the RC filter and b) the nonlinearity of the phase-domain ΔΣ ADC. Fortunately, both of these are fully deterministic and so can be corrected mathematically.

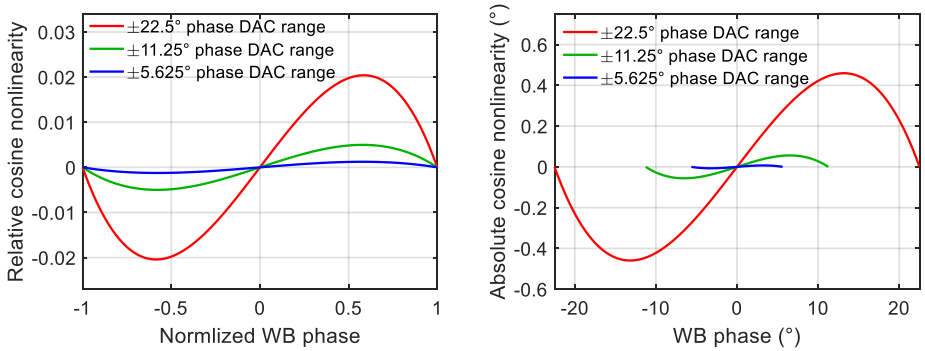
Under a sine-wave excitation/demodulation assumption, the so-called cosine nonlinearity of a phase-domain ΔΣ ADC can be readily computed [3.1][3.2]. At steady-state, the DC input of the ΔΣ-ADC's integrator has an average value of zero. Thus, the WB phase φ_{WB} and the ΔΣ-ADC's bitstream average μ are related by:

$$\frac{\mu A}{2}\cdot\cos(\varphi_1-\varphi_{WB})+\frac{(1-\mu)A}{2}\cdot\cos(\varphi_1-\varphi_{WB})=0. \tag{3.11}$$

From this equation, φ_{WB} is clearly a non-linear function of μ. After some manipulation, φ_{WB} can be expressed analytically as:

$$\varphi_{WB}=\tan^{-1}\left(\frac{\mu\cos(\varphi_1-\varphi_0)-\mu+1}{\mu\sin(\varphi_1-\varphi_0)}\right)-\varphi_0. \tag{3.12}$$

As shown in Figure 3.10, the relative error due to the cosine non-linearity decreases rapidly as the phase DAC range decreases, and the absolute error shrinks even more. Reducing the phase range by 4×, from 45° to 11.25°, suppresses the absolute error by ~70×.



(a) (b)

Figure 3.10: (a) Relative and (b) Absolute cosine nonlinearity with different phase DAC ranges.

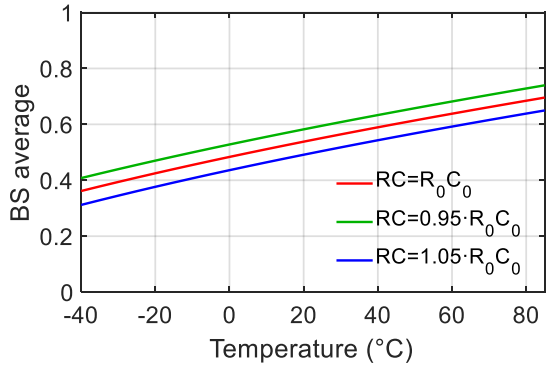


Figure 3.11: Simulated WB sensor output with a phase DAC range of ±22.5°.

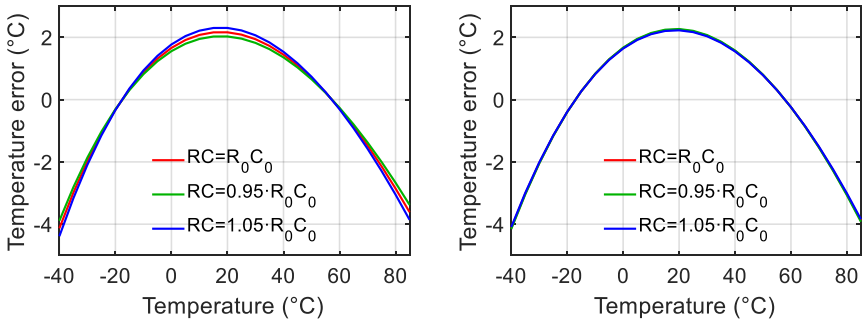


Figure 3.12: Residual error of WB sensors after a linear fit assuming an ideal phase-domain ADC: (a) without cosine nonlinearity compensation and (b) with cosine linearity compensation.

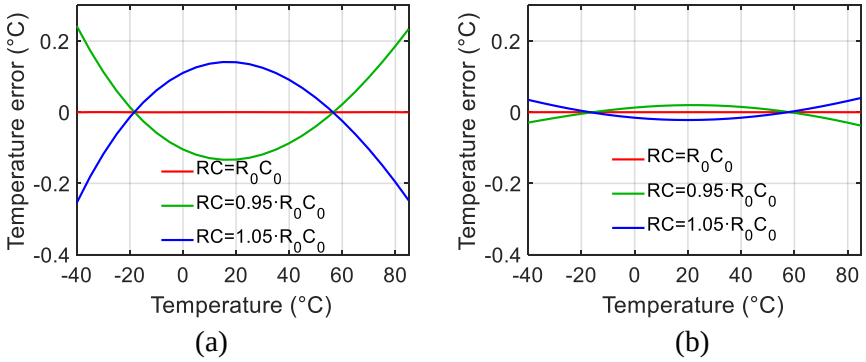


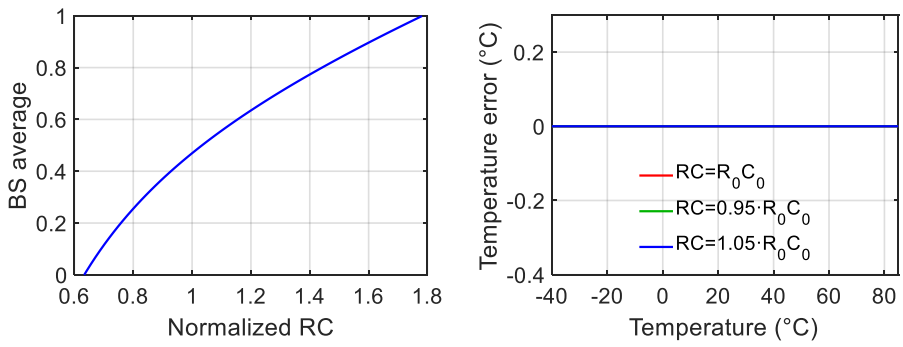
Figure 3.13: Residual error after systematic error removal: (a) without cosine nonlinearity compensation and (b) with cosine linearity compensation.

To test its effectiveness, the cosine-nonlinearity correction is tested on simulated WB sensor outputs (Figure 3.11). For simplicity, an in-batch spread of ±5% on $R_S(T_0)\cdot C_0$ is assumed, with zero no TC spread on both the silicided sensing resistor or the MIM capacitor. To facilitate operation in the presence of process and large temperature variations, the phase range is set to ±22.5°.

Without any pre-processing, a linear fit on the modulator's bitstream average results in a systematic nonlinearity of ~6°C over a 125°C temperature range, which is mainly due to the nonlinear RC-to-phase characteristic of the WB (Figure 3.12). After removing this systematic nonlinearity with a 5th-order polynomial, the maximum residual error becomes 0.24°C. After applying the cosine nonlinearity correction (Equation 3.12), the systematic nonlinearity remains roughly the same, but the spread after a linear fit can be suppressed to 0.03°C, as shown in Figure 3.13.

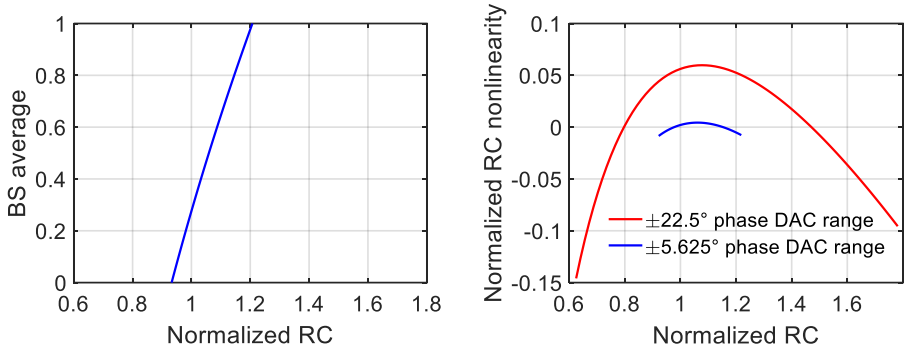
Although the method is effective, there is still significant error left, which can be further suppressed by a more complete nonlinearity correction. Since Equation (3.12) assumes the use of sine-wave excitation/demodulation, better results can be obtained by using a simulated μ to RC mapping (Figure 3.14 (a)) based on square-wave excitation/demodulation to eliminate all nonlinearity errors. After applying this mapping, represented by a 7th-order polynomial, the effect of resistor spread can be completely corrected by a linear fit, as shown in Figure 3.14 (b).

It is worth mentioning that the resulting μ to RC nonlinearity, just like the cosine-nonlinearity, decreases with the phase DAC range. E.g., with a ±5.625° DAC range, the absolute RC nonlinearity will become ~20× smaller (Figure 3.15). As a result, a nonlinearity correction is not required to achieve decent inaccuracy after trimming.



(a) (b)

Figure 3.14: (a) Normalized RC vs. BS average of WB sensors with a phase DAC range of ±22.5° (b) Residual error after applying the μ to R nonlinearity correction.



(a) (b)

Figure 3.15: (a) Normalized RC vs. BS average of WB sensors with a phase DAC range of ±5.625° (b) RC nonlinearity compared with a ±22.5° phase DAC.

3.3 Implementation I, proof of concept[1]

As a proof of concept, a WB sensor was built to investigate the potential energy-efficiency and accuracy of resistor-based sensors. However, some other importatnt parameters, e.g., chip area, and 1/*f* noise, were not optimized.

3.3.1 Circuit implementation

The block diagram of the proposed temperature sensor is shown in Figure 3.16. For high resolution, the WB resistor (silicided poly, 1μm wide) was chosen to be 32kΩ, while the WB capacitor was set to 10pF, resulting in a center frequency f_0 of 500kHz. The filter is driven by a square wave-signal at this frequency, i.e. $f_{drive} = f_0$ =500kHz. This is derived from an 8MHz external master clock by a divide-by-16 circuit. For simplicity, the PDΔΣ-ADC employs a single-bit quantizer. Its two square-wave phase references, φ_0=67.5° and φ_1=112.5°, are also generated by the divider circuitry. Their phase difference of 45° is chosen to accommodate the spread of the WB's resistors and capacitors, and hence in φ_{WB}(T).

In contrast to a previous design, which was based on a 1st-order modulator [3.1], this design employs a 2nd-order modulator to achieve sub-mK resolution in a short (5ms) conversion time. As shown in Figure 3.16, it employs a feed-forward topology [3.4], which requires only one feedback DAC, and also reduces the swing in the loop filter. To establish a low-impedance virtual ground at the input of the ADC, the first

[1] S. Pan, Y. Luo, S. H. Shalmany and K. A. A. Makinwa, "A resistor-based temperature sensor with a 0.13 pJ·K² resolution FoM," *IEEE Journal of Solid-State Circuits*. vol. 53, no. 1, pp. 164-173, Jan. 2018.

stage consists of an active integrator, while, for simplicity, the second stage consists of a gm-C integrator. The feedforward coefficient is realized by the introduction of R_{ff} in series with the integration capacitor (C_{int2}) of the second stage. Its output is sampled at f_{drive} by a comparator, which is triggered at φ_{trig} =135°.

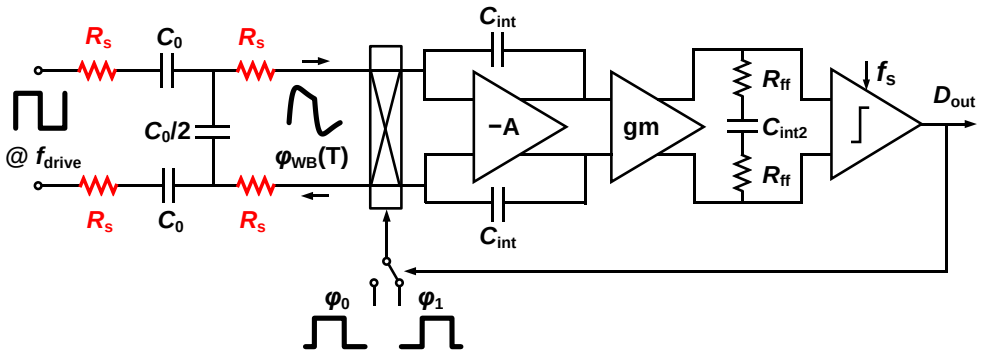


Figure 3.16: Simplified circuit diagram of the first WB sensor implementation.

3.3.1.1 Chopper and chopper merging

To suppress its 1/*f* noise, the opamp of the first stage is chopped. By making the chopping frequency f_{chop} the same as the driving frequency f_{drive}, the input chopper and the input demodulator can be merged into a single chopper in series with the integration capacitors, as shown in Figure 3.17. This chopper merging technique [3.5] simplifies the required control logic and minimizes errors due to charge injection mismatch.

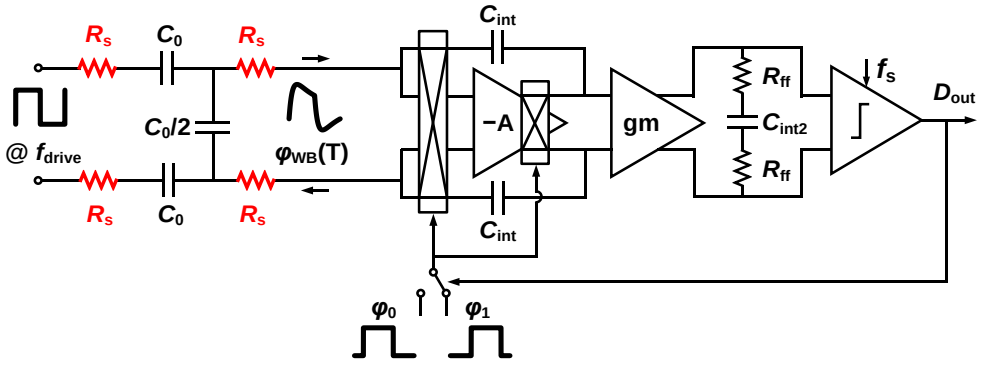


Figure 3.17: Simplified circuit diagram of the first WB sensor implementation with a merged chopper.

3.3.1.2 Amplifier design

In principle, the 1st-stage amplifier can be implemented as an energy-efficient single-stage operational trans-conductance amplifier (OTA). However, the input impedance of the resulting integrator is then approximately 1/gm, where gm is the OTA's transconductance. As shown in Figure 3.18, this resistance loads the WB, thus altering $\varphi_{WB}(T)$ and degrading its temperature-sensing accuracy. For example, with the chosen s-p-poly resistors, a 10% variation on a nominal gm of 1mS (I_d ~ 50µA, or 4× larger than the maximum output current of the WB) will translate into a temperature-sensing error of more than 0.5°C.

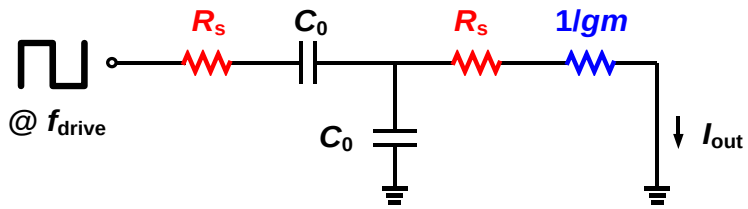


Figure 3.18: Additive resistance on the output resistor of Wien bridge sensor when using an OTA-based first stage.

In a two-stage amplifier, the input stage doesn't need to provide the output current. This helps to reduce its input swing and hence the input impedance of the first integrator, which in turn results in a smaller temperature-sensing error. For simplicity, and to avoid the need for Miller compensation capacitors, the gain of the output stage should not be large, so that the pole formed by the gm/C_{load} of the output stage, is well beyond the unity-gain frequency of the amplifier. In this work, a two-stage opamp consisting of a telescopic gm stage followed by two low-V_T PMOS source followers was used, as shown in Figure 3.19. The common-mode feedback of the gm stage is realized by two PMOS transistors in their triode region. The tail current of the telescopic gm, which is 16µA at room temperature, is optimized for low noise and power consumption. The source followers' bias current (20µA/branch at room temperature) is chosen to handle the WB's peak current (11µA at room temperature, 16µA at −40°C). The opamp's 1/*f* noise has a corner frequency of about 15kHz, and so is effectively canceled by chopping at 500kHz. To limit the 1st stage's output swing (which includes chopper ripple) and thus to relax the design of the gm-C second stage, the integration capacitor of the first stage is made quite large (180pF each).

The gm-C second stage is built around a telescopic OTA with source degenerated input pairs, which achieves a good balance between energy-efficiency and linearity. It draws 4µA, which is less than 10% of that of the first stage.

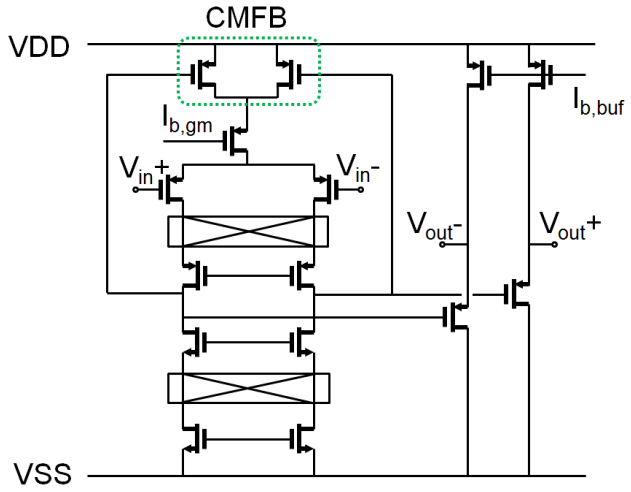


Figure 3.19: Schematic of the opamp in the first stage.

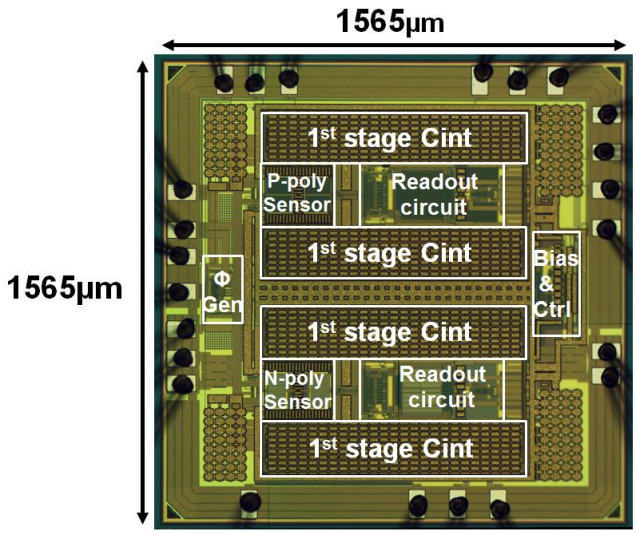


Figure 3.20: Micrograph of the first WB sensor implementation.

3.3.2 Measurement results

The sensor was fabricated in a standard 0.18µm CMOS technology, and the chip micrograph is shown in Figure 3.20. For flexibility, a $sinc^2$ decimation filter is implemented off-chip. Each sample contains two different temperature sensors: one with silicided p-poly (s-p-poly) resistors, and for the sake of comparison, the other with non-silicided n-poly resistors. These two co-integrated sensors share the same constant-gm biasing and phase generation circuits. Each sensor occupies an active die

area of 0.72mm^2, about 40% of which is consumed by the first integrator's capacitors (2×180pF). Each sensor draws 87µA from a 1.8V power supply, including the readout circuits. At room temperature, DC supply sensitivities of −0.17°C/V (s-p-poly bridge) and 0.34°C/V (n-poly bridge) were observed for supply voltages ranging from 1.6 to 2V.

3.3.2.1 Resolution and FoM

Since the phase output of the WB sensor is determined by its driving frequency, random jitter will translate into random phase noise and degrade the sensor's resolution. To prevent this, the sensors are driven by a low-jitter (1ps$_{rms}$) frequency reference, which only degrades the sensor's resolution by about 0.5%. Furthermore, the temperature of the sensors was stabilized by mounting them inside a cavity in a large (10kg) metal block, which, in turn, was placed in a temperature-controlled oven (Vötsch VT7004). More details of the setup can be found in Appendix A.1.

The power spectral densities of both sensors' output bit-streams are shown in Figure 3.21, where 0dB corresponds to 1 in the BS average amplitude, which full range is [−1, 1]. The sensor's noise floor is dominated by the RC-filters' thermal noise. The n-poly resistor exhibits a 1/*f* corner of about 10Hz, while that of the s-p-poly sensor is below 1Hz. Since the two sensors are read-out in exactly the same way, the 1/*f* noise of the n-poly sensor can be directly attributed to the sensing resistors.

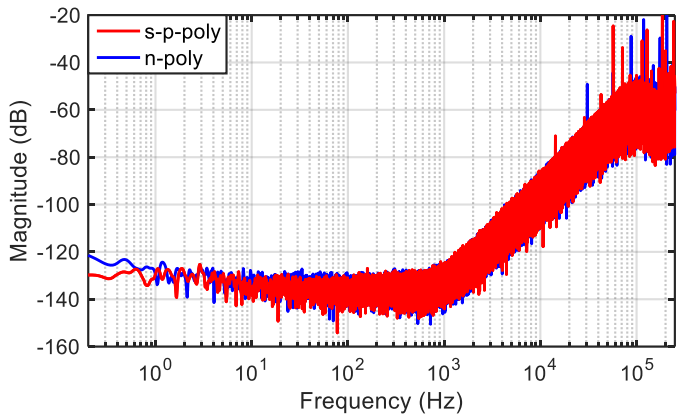


Figure 3.21: The power spectral densities of the output bit-stream of both sensors.

After decimating their bit-streams at room temperature (RT ~25°C), the sensors' resolution is plotted versus conversion time, as shown in Figure 3.22. To suppress the effects of ambient temperature drift, the resolution was determined from a two-sample Allan deviation, i.e., from the difference between two successive measurements. In a 5ms conversion time (2500 samples), the calculated resolutions of s-p-poly and the n-poly sensors are 410µK$_{rms}$ and 880µK$_{rms}$, respectively.

However, the differencing operation inherent to the Allan deviation calculation will also suppress the sensor's non-negligible 1/*f* noise (Figure 3.22). To avoid this, the standard deviation can be computed over a shorter interval (1 second), during which the temperature drift will be negligible compared to the sensor's noise. Given the same 5ms conversion time, the resolution becomes 440 μK_{rms} for the s-p-poly sensor and 990μK_{rms} for the n-poly sensor. The corresponding resolution FoM of the s-p-poly sensor is then 0.15pJ·K^2.

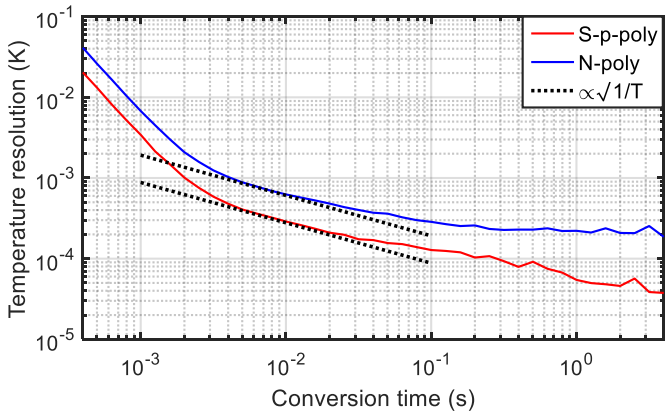
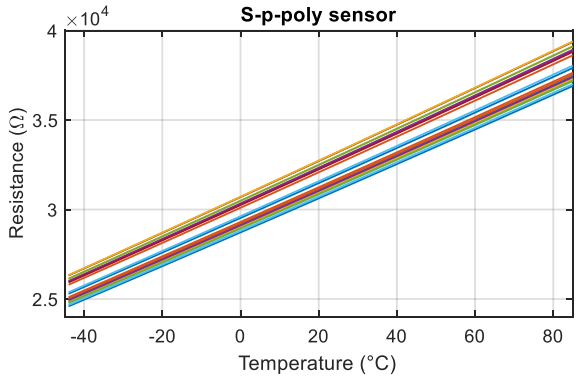


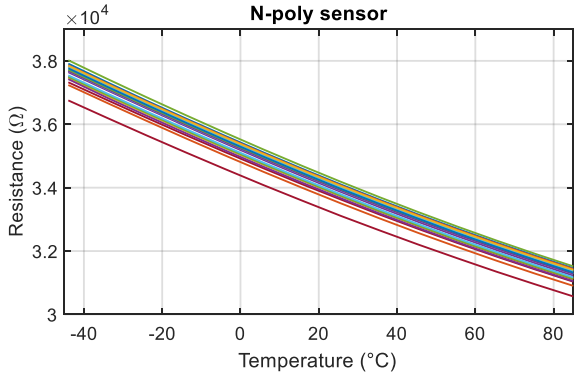
Figure 3.22: The calculated resolution using a two-sample Allan deviation.

3.3.2.2 Calibration and inaccuracy

Twenty samples from one wafer in ceramic DIL packages were characterized from −45°C to 85°C (steps of 10°C) in a temperature-controlled oven. The actual temperature was established by a calibrated Pt-100 RTD. To partially compensate for the spread of f_0 with process, f_{drive} was set to 562.5kHz (9MHz master clock) instead of the nominal 500kHz. After the fixed nonlinearity correction introduced in section 3.2.3.2, the extrapolated resistance vs. temperature plots (R-T plots) of the s-p-poly and the n-poly sensors are shown in Figure 3.23, and the corresponding average R-T plots are shown in Figure 3.24. The corresponding 1st and 2nd order TCs agree well, to within a few percent, with the models provided by the foundry, thus validating the non-linearity correction technique. After a 1st-order linear fit, the remaining non-linearity, mainly due to the nonlinearity of the sensing resistor's TC, is quite systematic (Figure 3.25), and so can be removed by a fixed 3rd-order polynomial obtained by batch calibration. After this systematic nonlinearity correction, the s-p-poly sensor achieves a 3σ inaccuracy of ±0.03°C, while the n-poly sensor's inaccuracy is about ±0.3°C, as shown in Figure 3.26. Without this correction, the accuracy of the s-p-poly sensor would have been about 2× worse.

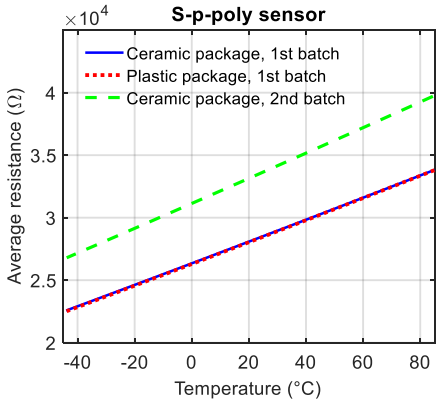


(a)

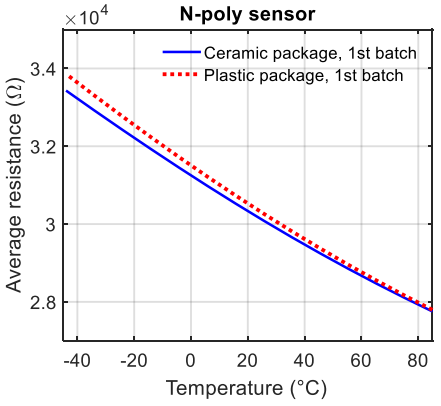


(b)

Figure 3.23: Resistance vs. temperature plots of (a) s-p-poly sensor (b) n-poly sensor in ceramic packages.

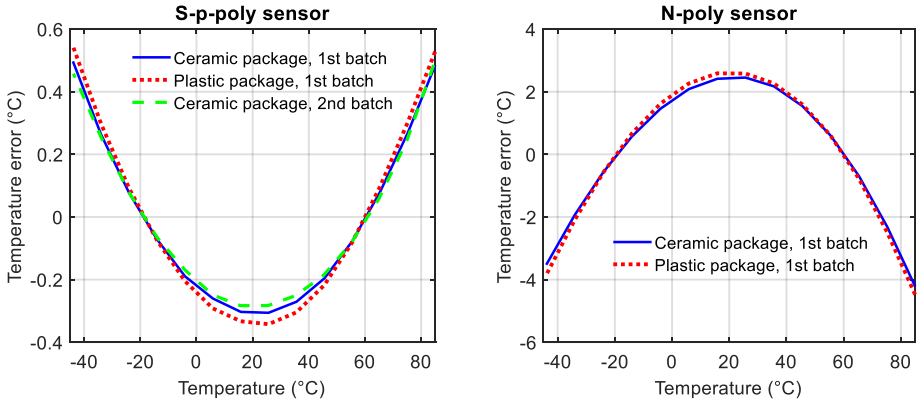


(a)



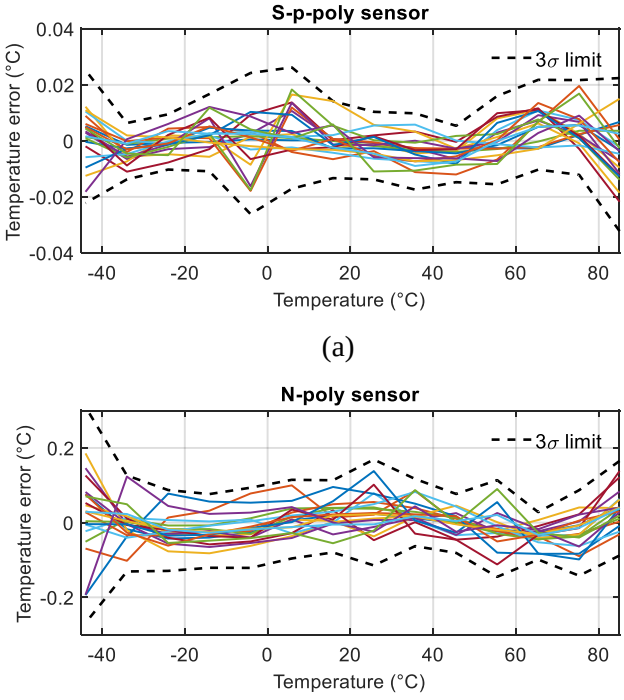
(b)

Figure 3.24: Average resistance vs. temperature of (a) s-p-poly sensor and (b) n-poly sensor.



(a) (b)

Figure 3.25: Systematic temperature nonlinearity of (a) s-p-poly sensor (b) n-poly sensor after a 1st-order fit.



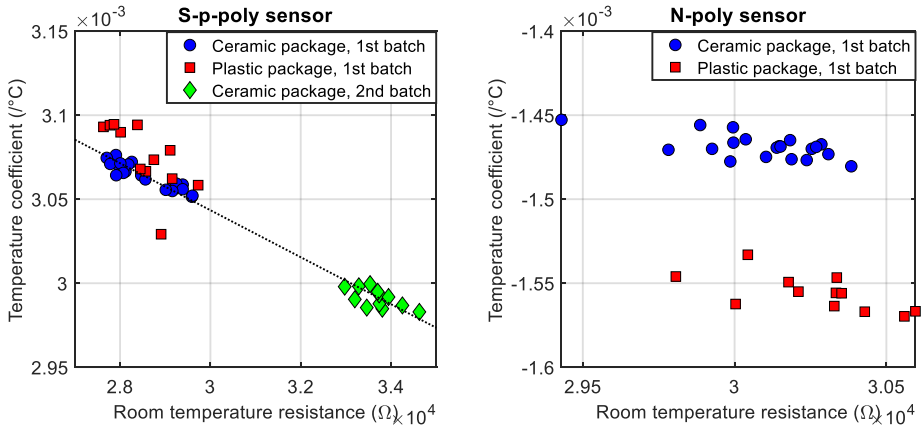
(a)

(b)

Figure 3.26: Inaccuracy of (a) s-p-poly sensor (b) n-poly sensor after a 1st-order fit and systematic nonlinearity removal.

To reduce calibration costs, the number of calibration temperatures should be reduced as much as possible. So rather than doing a 1st-order fit based on data obtained at multiple temperature points, a more straightforward two-point calibration can be done. This results in only a slight loss of accuracy: when calibrated at −15°C and 65°C, the s-p-poly sensor achieves a 3σ inaccuracy of ±0.05°C.

Serendipitously, the TC and the RT resistance (R_0) of the s-p-poly sensor were found to be correlated, as shown in Figure 3.27 (a). By exploiting this correlation, a 3σ inaccuracy of ±0.2°C could be achieved after a single-point calibration, as shown in Figure 3.28. Unfortunately, this correlation is much weaker for n-poly sensor (Figure 3.27 (b)), and the 3σ inaccuracy after a single-point calibration is only ±0.6°C.



(a) (b)

Figure 3.27: Correlation between R_0 and its TC for (a) the s-p-poly resistor and (b) the n-poly resistor.

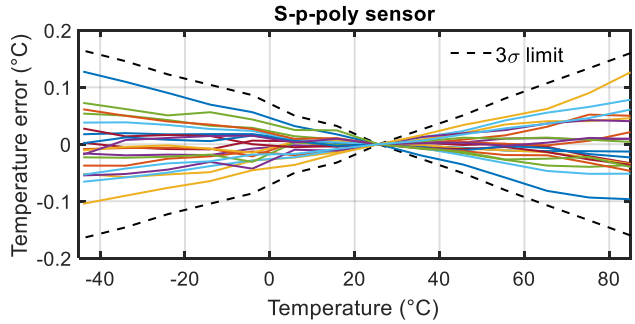


Figure 3.28: Inaccuracy of s-p-poly sensor after a correlation-assisted 1-point calibration (ceramic packaged, 1st batch).

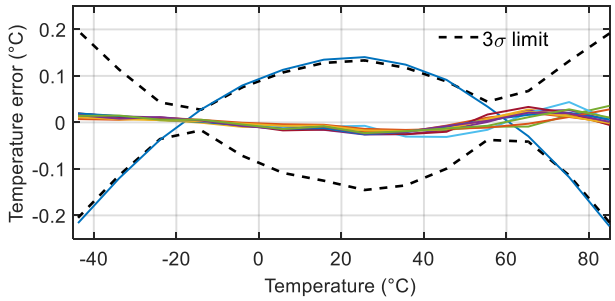


Figure 3.29: Inaccuracy of plastic packaged s-p-poly sensor after a 1st-order fit and systematic non-linearity removal.

3.3.2.3 Plastic packaging

In production, low-cost plastic packages are preferred over ceramic packages. However, the accompanying mechanical stress [3.6] impacts the sensor's accuracy. Because of the metal-like properties of silicided poly resistors, their stress sensitivity is much less than that of non-silicided poly resistors. The average resistance vs. temperature plot of 12 sensors produced in the same batch is shown in Figure 3.24. Compared to the ceramic packaged chips, both the TC and R_0 of the n-poly resistors in plastic packages change significantly, while those of the s-p-poly resistors do not.

However, compared to ceramic packaged devices, a shift was observed in the TC-R_0 correlation of the s-p-poly sensors. Even based on the limited number of samples, the correlation also appears to be weaker, as shown by an outlier in Figure. 3.27(a). After a two-point calibration, however, the change in their systematic nonlinearity is less than 0.05°C (Figure 3.25). After a packaging-specific systematic nonlinearity correction, the sensor achieves a 3σ inaccuracy of ±0.2°C, as shown in Figure. 3.29, mainly due to the outlier.

3.3.2.4 Batch-to-batch spread

To verify the effect of batch-to-batch spread on the s-p-poly sensor's inaccuracy, 12 devices from a different batch (fabricated a few months after the first batch) were characterized in ceramic packages. As shown in Figure 3.24, however, the center frequency f_0, and hence the extrapolated resistance of the s-p-poly sensors then shifted by about 16%. This resistance shift was compensated by reducing f_{drive} by 16% during characterization. The sensor's extrapolated TC-R_0 relationship is shown in Figure 3.27. Despite the significant shift in f_0, the linear correlation discussed in section 3.3.2.2 is still valid. The s-p-poly sensor achieves an estimated 3σ inaccuracy of ±0.3°C after a correlation-assisted single-point calibration. After an individual 1st-order fit, the maximum difference in the systematic nonlinearity of the two batches is 0.04°C from −40°C to 85°C (Figure 3.25).

3.3.2.5 Comparison with prior art

The performance of the s-p-poly sensor is summarized in Table 3.1 and compared with that of earlier energy-efficient CMOS temperature sensors. It achieves an energy efficiency of 0.15pJ·K^2, which is over 4× better than an earlier resistor-based sensor [3.8]. When packaged in ceramic, the sensor achieves an inaccuracy of ±0.03°C (3σ) after a 1st-order fit followed by a fixed systematic nonlinearity correction. It also achieves ±0.2°C (3σ) after a single-point calibration, which is comparable to that of most BJT-based sensors [3.7][3.11] .

Table 3.1: Performance summary of the first sensor implementation and comparison with previous work.

	ISSCC'14 [3.7]	JSSC'15 [3.8]	JSSC'15 [3.9]	Implementation I
Sensor type	BJT	Resistor WhB	Resistor WB	Resistor WB
Technology	0.7µm	0.18µm	0.18µm	0.18µm
Area [mm^2]	1.5	0.43	0.09	0.72
Temp. Range [°C]	−40─130	−40─125	−40─85	−40─85
3σ Inaccuracy [°C] (trimming points)	0.3 (1)	0.4[a] (2[b])	0.12[a] (3)	0.03 (2[c])
Relative inaccuracy	0.35%	0.48%	0.19%	0.05%
Power [µW]	160	65	31	160
Conv. time [ms]	1.8	0.1	32	5
Resolution [mK]	3	10	2.8	0.44
Res. FoM [fJ·K^2]	3200	650	8000	150

[a] Min/Max. [b] 1-point trim with a fixed 1st-order fit. [c] 1st-order fit.

3.4 Implementation II, reduced chip area[2]

Although the first implementation achieves good performance, it has a large chip area (0.72mm^2) and a limited temperature range. This section describes a compact (0.12mm^2**)** resistor-based sensor that uses a scaled WB filter to achieve 0.1°C (3σ) inaccuracy over a wider temperature range of 220°C.

[2] S. Pan, Ç. Gürleyük, M.F. Pimenta, K.A.A Makinwa, "A 0.12mm^2 Wien-bridge temperature sensor with 0.1°C (3σ) inaccuracy from −40°C to 180°C," in *ISSCC Dig. Tech. Papers*, Feb 2019, pp 184-186.

3.4.1 Circuit implementation

As shown in section 3.3, most of the chip area in the first implementation is consumed by the integration capacitor in the 1st stage (C_{int}). Since $C=Q/U=I\cdot T/U$, there are three options: reducing the WB input current, shortening its period (i.e., increasing f_{drive}), or increasing the output swing of the 1st integrator.

In this design, the WB resistor width is halved (1μm to 0.5μm) compared to that in the first implementation, leading to a doubled resistance (64kΩ) at the expense of worse resolution. The designed WB driving frequency f_{drive} is kept the same (500kHz). This is because the temperature information is embedded in the shape of the input current, and the accuracy will be degraded if the bandwidth of the readout circuit is not sufficiently higher compared to f_{drive}. As a result, the WB capacitor is also halved (5pF instead of 10pF) to accommodate the change of the WB resistance.

Increasing the 1st integrator's output swing requires a new opamp topology. The 1st integrator is based on a two-stage Miller-compensated opamp based on current-reuse amplifiers, as shown in Figure 3.30. The 1st stage provides good energy efficiency, while the 2nd uses high-V_T devices to efficiently provide a nearly rail-to-rail output swing. Compared to the conventional choice of two common-source stages, it provides twice the output current for the same bias current. Together with the doubling of R_S (e.g., halved WB current), the enlarged opamp output swing allows the value of C_{int} to be reduced from the 180pF used in the first implementation, to 23pF. At room temperature (RT), the amplifier draws 14μA, achieves 80dB gain, and has a gain-bandwidth product of 17MHz with a 500fF loading capacitor.

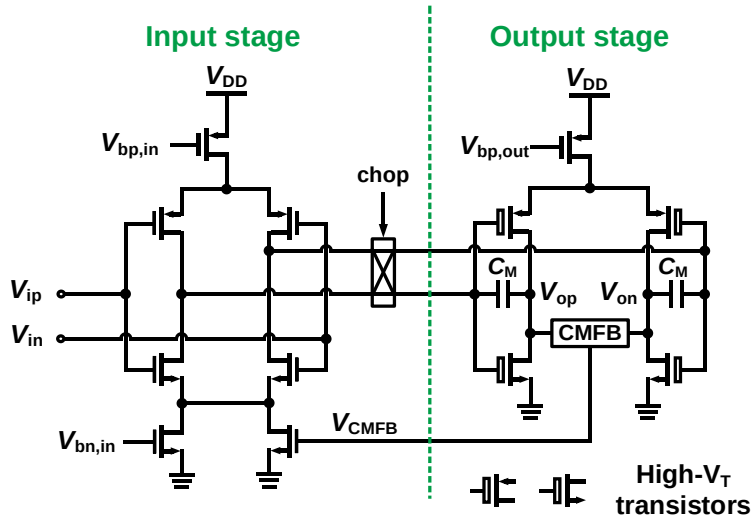


Figure 3.30: Simplified diagram of the 1st-stage amplifier.

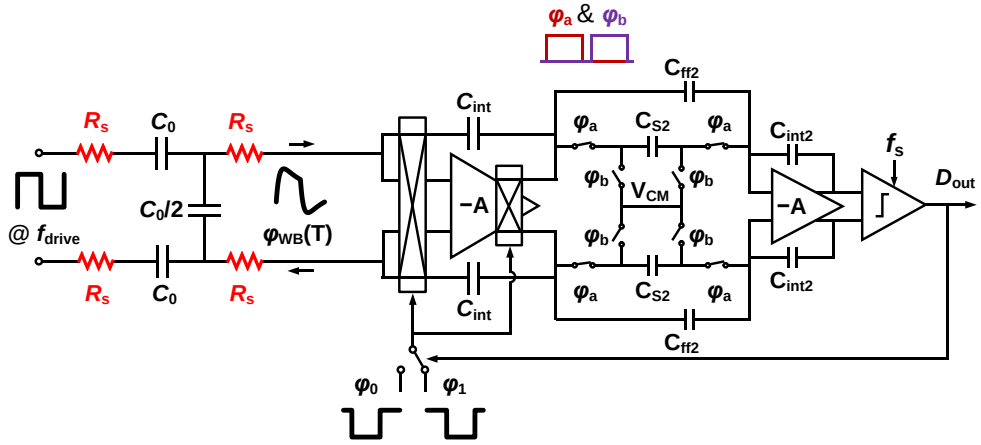


Figure 3.31: Simplified circuit diagram of the second implementation.

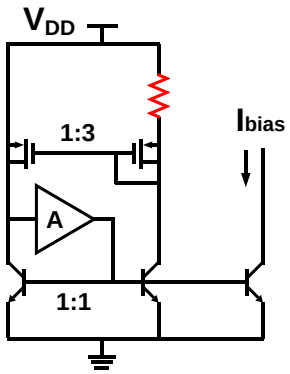


Figure 3.32: Biasing circuit.

To further reduce area, the 2nd integrator and the feed-forward coefficient are realized in a switched-capacitor manner, thus avoiding the large resistors used in the first implementation, as shown in Figure 3.31. The associated folded-cascode amplifier draws only 2.5µA at RT. The sampling capacitor C_{S2} and the feedforward capacitor C_{ff2} are 100fF and 200fF, respectively, while the 2nd stage integration capacitor C_{int2} is 1pF.

The phase references $\varphi_{0,1}$ are 90°±30° instead of 90°±22.5° to extend the measurable temperature range. Like f_{drive} and $\varphi_{a,b}$, they are derived from an external 6MHz frequency reference using on-chip logic.

However, reducing C_{int} will increase the opamp's closed-loop input impedance Z_{in} ($\propto 1/(C_{int}*GBW)$), where GBW is the opamp's gain-bandwidth product. This is in series with the WB (Figure 3.18) and is thus a source of spread and 1/*f* noise. To minimize spread, a constant-Gm biasing circuit based on the same resistor type as R_S ensures that Z_{in} tracks R_S over a wide temperature range. Although the opamp is

effectively chopped, the bias current's 1/*f* noise will modulate Z_{in}, and thus R_S, causing residual 1/*f* noise. To minimize this noise, the core of the biasing circuit was realized with large PMOS devices (W/L = 40µm/5.5µm), and critical current mirrors were realized with the standard NPN transistors available in the chosen process (Figure 3.32). Simulations show that the sensor's 1/*f* corner is then about 1Hz and that R_S is less than 1% Z_{in} over corners.

3.4.2 Measurement results

Three pairs of identical sensors based on silicided p-poly (s-p-poly), unsilicided n-poly (n-poly), and high-resistive poly (h-r-poly) resistors were fabricated on the same die in a 0.18µm CMOS process (Figure 3.33). This facilitates the use of differential measurements to reject temperature drift of the ambient environment, so that the sensor resolution can be accurately measured. Each sensor consumes 29µA from a single 1.8V supply and occupies 0.12mm^2, of which the WB occupies 25%.

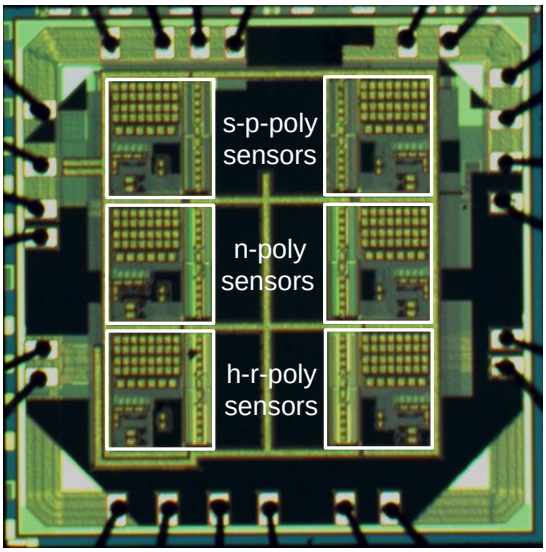


Figure 3.33: Micrograph of the second WB sensor implementation.

3.4.2.1 Resolution and FoM

PSDs of the bitstream outputs of the three sensors are shown in Figure 3.34 based on differential data captured from 100s time. The corner frequencies are ~4Hz (n-poly and h-r-poly), and ~1Hz (s-p-poly). The latter is limited by the readout electronics. Sensor resolution is derived from the standard deviation within a 1s time interval (Figure 3.35). Due to its greater TC, the silicided-p-poly sensor exhibits the best resolution: 460µK in a 10ms conversion time, corresponding to a 110fJ·K^2 resolution

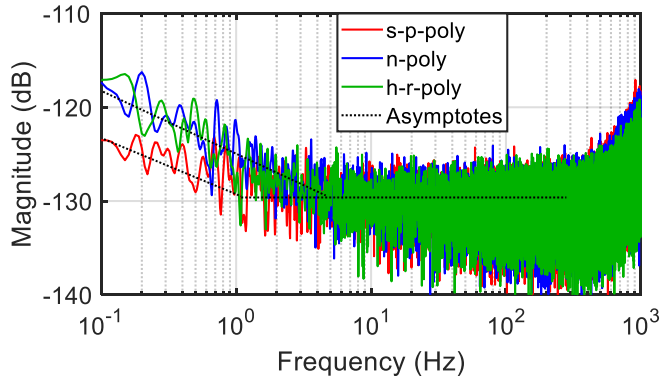


Figure 3.34: Bitstream spectra (100s interval, Hanning window) of different WB sensors.

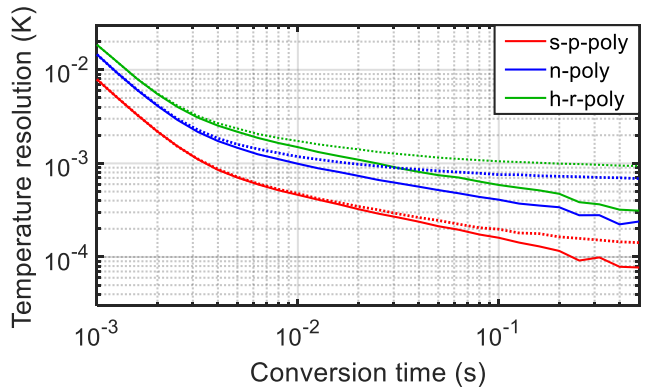


Figure 3.35: Resolution vs. conversion time of different WB sensors given a 1s (solid lines, 100× averaging) and 100s (dashed lines) time interval.

FoM. With a longer interval (100s), however, the integrated 1/*f* noise power gets larger, resulting in a worse calculated resolution.

3.4.2.2 Calibration and inaccuracy

A total of 10 chips (60 sensors) from a single batch were packaged in ceramic DIL and characterized from −40°C to 180°C. To correct for the inherent cosine nonlinearity of the PDΔΣM and the non-linear relationship between φ_{WB} and R_S (section 3.2.3.2), a 7th-order polynomial is used to translate the decimated output of each sensor into an equivalent sensor resistance R_S. Since the temperature dependency of polysilicon resistors is comparatively linear, this approach minimizes the residual error after a 1st-order fit. Figure 3.36 (left) shows the resulting temperature dependence of each resistor type. The following RT TCs were extracted: 0.31%/°C (s-p-poly), −0.15%/°C (n-poly) and −0.10%/°C (h-r-poly), which agree with the

process documentation. After a 1st-order fit to compensate for process spread, followed by a fixed 6th-order polynomial to correct for systematic non-linearity, the sensors' residual spread is shown in Figure 3.36 (right). The sensors achieve 3σ inaccuracies of 0.1°C (s-p-poly), 0.4°C (n-poly) and 0.9°C (h-r-poly) from −40°C to 180°C.

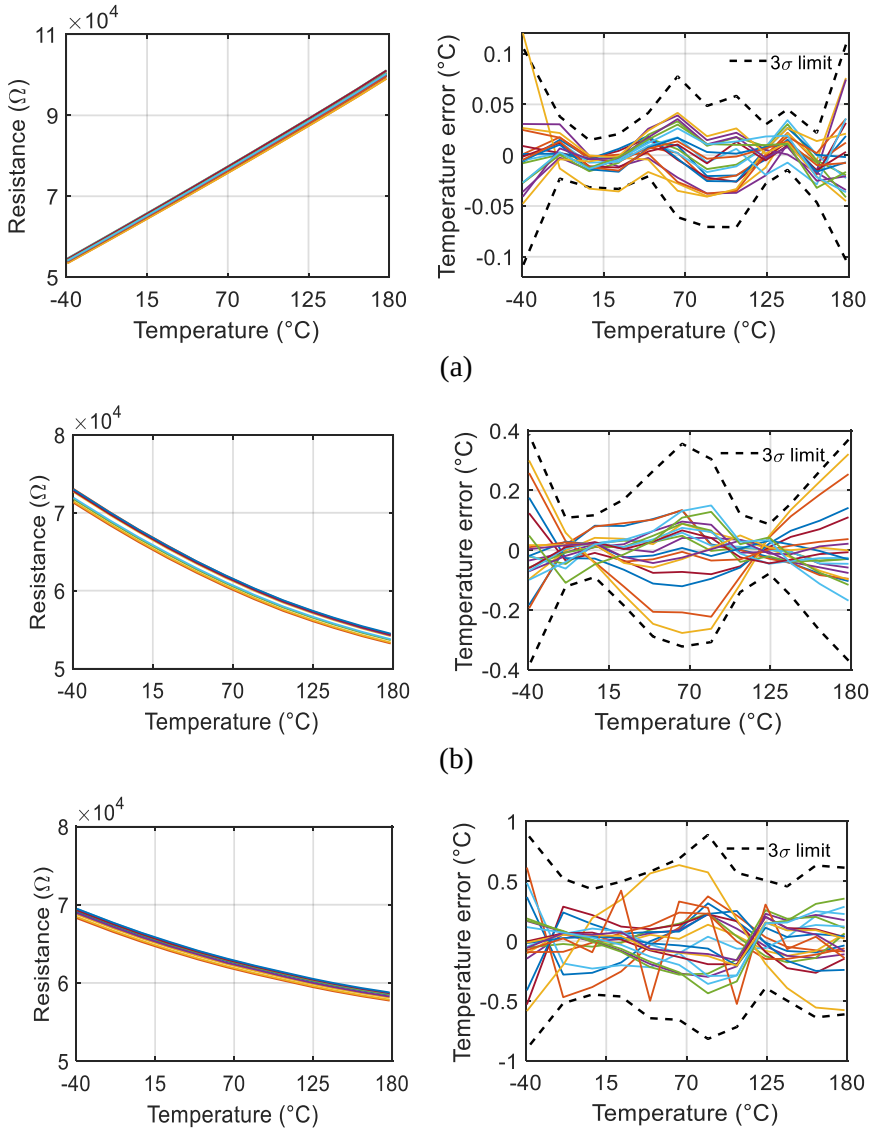


Figure 3.36: Extracted sensor resistance R_S of ceramic packaged sensors (left); Inaccuracy after a 1st-order fit and systematic non-linearity correction (right) of (a) s-p-poly (b) n-poly and (c) h-r-poly sensors.

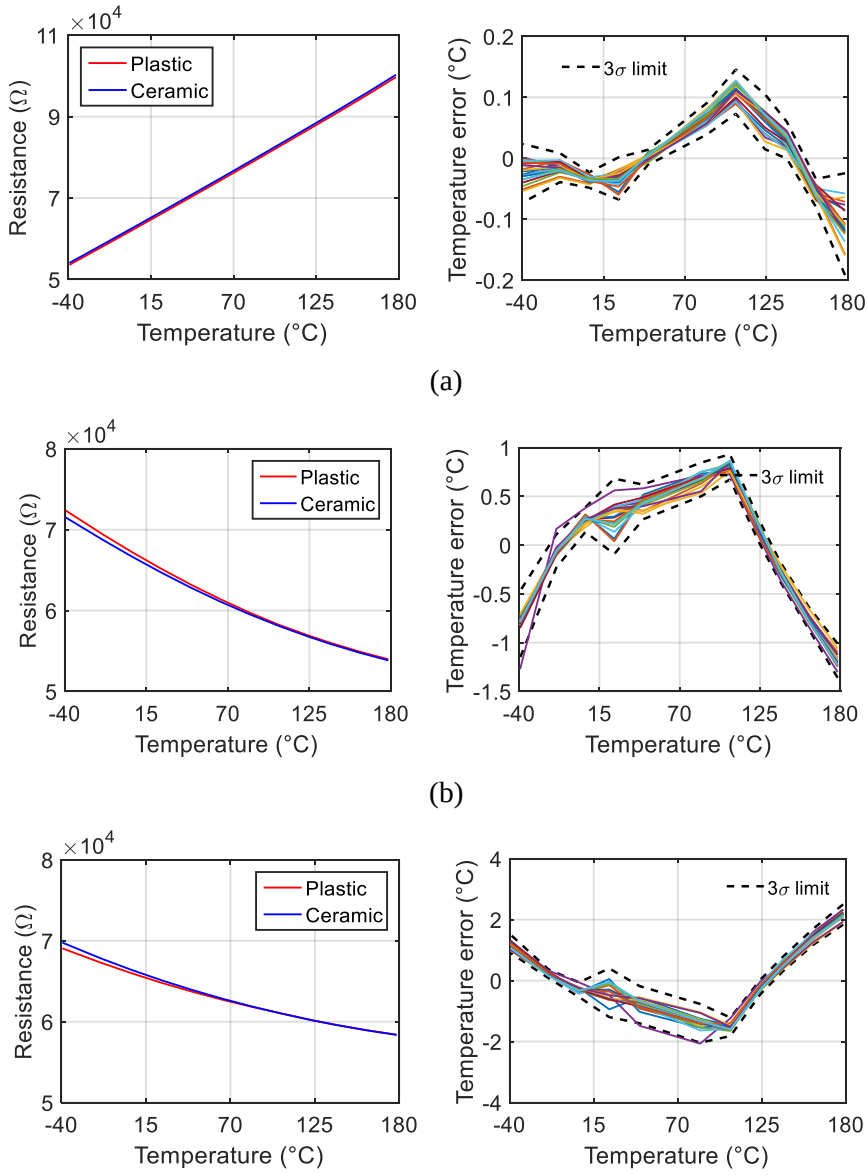


Figure 3.37: Average resistance vs. temperature of three types of resistors in different packages (left); Inaccuracy of plastic packaged sensors after a 1st-order fit and system non-linearity correction from ceramic packaged sensors (right) of (a) s-p-poly (b) n-poly and (c) h-r-poly sensors.

To observe the effects of mechanical stress, 10 chips from the same batch were characterized in injection-molded plastic QFN packages. Figure 3.37 (left) shows the average dependency of R_S for both the ceramic and plastic-packaged chips. After using the same non-linearity correction polynomials determined for the ceramic

packaged chips, the inaccuracy after a 1st-order fit increases by only 0.2°C for the s-p-poly sensors, but to 1.4°C for the n-poly sensors, and even 2.5°C for the h-r-poly sensors (Figure 3.37 (right)). The sharp inflexion in all the inaccuracy plots around 100°C is probably due to the effects of moisture on the plastic packages [3.10]. Of the three resistor types, the s-p-poly resistor is clearly the least stress-sensitive, exhibiting a packaging shift similar to that of BJT-based sensors [3.11].

3.4.2.3 Comparison to implementation I

Compared to the first implementation, this design has a 76% larger operating range and occupies 6× less area. at the expense of a somewhat worse relative inaccuracy. Also, the sensor's $1/f$ noise corner is still limited by the readout circuit. These problems will be addressed in the third implementation.

3.5 Implementation III, better accuracy and stability[3]

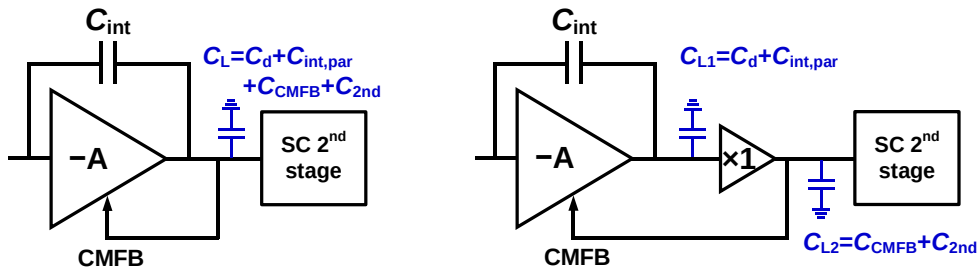
3.5.1 Circuit implementation

To provide a fair comparison, both the WB sensor (64kΩ s-p-poly resistor, 5pF capacitor) and its driving frequency (500kHz) in this third implementation are inherited from the second one. The phase DAC range is changed back to ±22.5°, as the sensor is now targeting the slightly narrower military temperature range from −55°C to 125°C.

As shown in Figure 3.18, one primary error source of a WB sensor is the input impedance of the 1st stage integrator, which is connected in series with the WB resistor. To minimize this Z_{in} ($\propto 1/(C_{int}\cdot\text{GBW})$) without enlarging the chip area, the GBW of the 1st-stage opamp needs to be extended. However, this shouldn't be at the expense of significantly increased opamp power.

In the second implementation, the opamp's GBW is limited by the current of the output stage and its load capacitor (C_L). For a sufficient phase margin, the frequency of the secondary pole (gm_2/C_L, where gm_2 is the transconductance of the opamp's output stage) should be 3× larger than that of the dominant pole (≈GBW), i.e., GBW < $3gm_2/C_L$. The load capacitor (C_L) consists of the parasitic capacitance of the integrator ($C_{int,par}$), the drain capacitance of the output stage (C_d), the input capacitance seen from the CMFB circuit (C_{CMFB}), and that of the SC-based 2nd stage (C_{2nd}).

[3] S.Pan, J.A. Angevare, K.A.A Makinwa, "A hybrid thermal-diffusivity/resistor-based temperature sensor with a self-calibrated inaccuracy of 0.25°C (3σ) from −55°C to 125°C," in *ISSCC Dig. Tech. Papers*, Feb. 2021, pp. 78-79.



(a) (b)

Figure 3.38: Opamp connections with (a) all loading capacitors and (b) reduced loading capacitors.

The first two are hard to suppress. However, the effect of both C_{CMFB} and C_{2nd} can be removed by introducing a low-power buffer, as shown in Figure 3.38, without changing the basic opamp structure (Figure 3.30). Since the 2nd stage of the ΔΣ-ADC only processes a DC signal, the speed requirement of the buffer is not stringent. In this work, the buffer is simply realized with PMOS source-followers, which only adds ~1.1μA on the designed 16μA baseline of the opamp. However, after adjusting the Miller capacitor value accordingly, the opamp's GBW is extended from ~20MHz to ~40MHz, and thus the input impedance is suppressed by 2×.

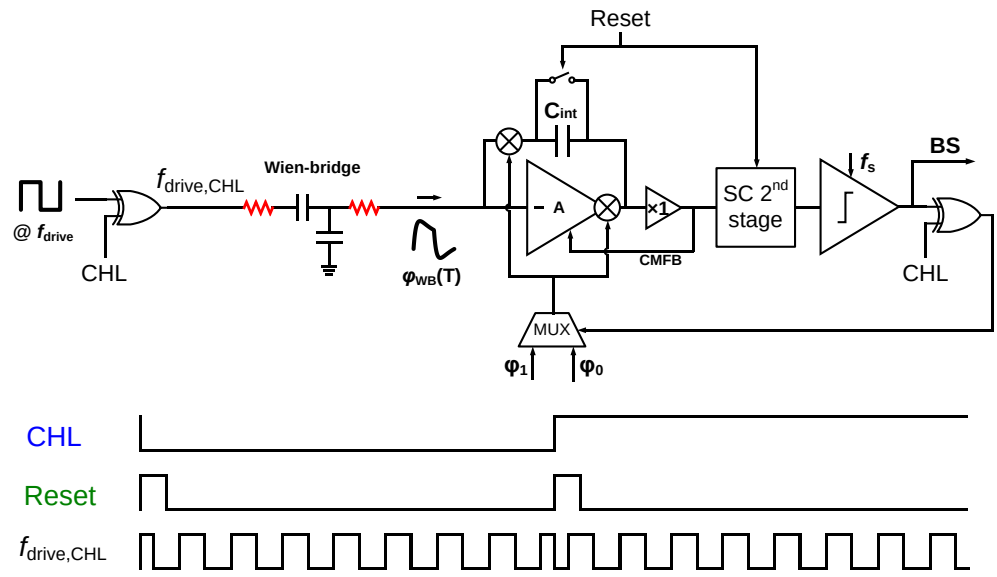


Figure 3.39: Simplified circuit schematic and timing diagram of the sensor's low-frequency system-level chopping.

This halved Z_{in} also reduces the $1/f$ noise coming from the biasing circuit. However, since only the input stage of the 1st stage opamp is chopped (Figure 3.30), the $1/f$ noise of the opamp output stage and the rest of the circuit remains. To further suppress this residual noise, XOR-gate-based low-frequency system-level choppers [3.12] are inserted to flip the entire system at 100Hz. The driving signal (f_{drive}) is switched in the middle of its half period to minimize the settling error after this low-frequency chopping, as shown in Figure 3.39. To avoid quantization noise folding, the ΔΣ-ADC works in an incremental mode, in which the integrators are reset at twice the system-level chopping frequency.

3.5.2 Measurement results

With the same standard 0.18μm process, four sensors based on s-p-poly resistors were fabricated on the same chip. Each sensor consumes 37μA under a 1.8V supply, and occupies 0.12mm^2 after neglecting the test structures (Figure 3.40), which is the same as the second implementation. For flexibility, the decimation filters (sinc^2) are implemented off-chip.

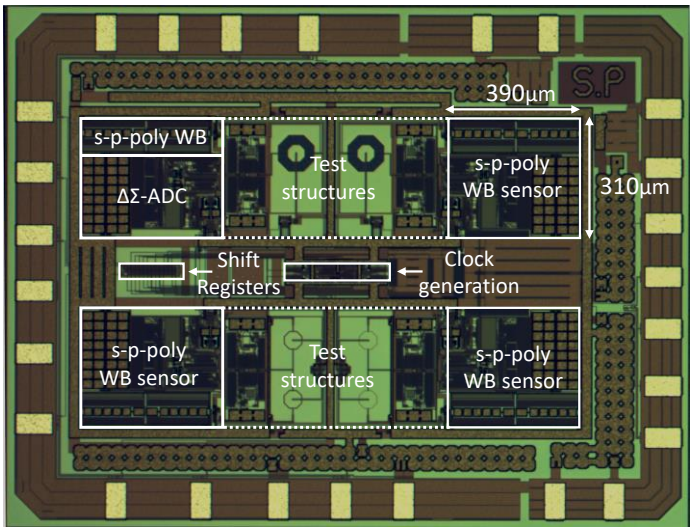


Figure 3.40: Micrograph of the third WB sensor implementation.

3.5.2.1 Resolution and FoM

Twenty samples from one wafer were characterized in a temperature-controlled oven after ceramic DIL packaging and mounting in good thermal contact with a large metal block. To reject the ambient temperature drift, the s-p-poly WB sensor's resolution is derived by computing the standard deviation of the difference in the output of two sensors from the same die. Figure 3.41 shows the s-p-poly sensor's

output spectrum after decimation (with a 5ms sinc^2 window). After enabling the system-level chopping (100Hz), the sensor's 1/f noise corner is reduced from ~1Hz to below 10mHz. As shown in Figure 3.42, over a 1s interval, the sensor achieves a 450μKrms resolution in a 10ms conversion time (T_{conv}), which corresponds to a 0.13pJ·K^2 resolution FoM.

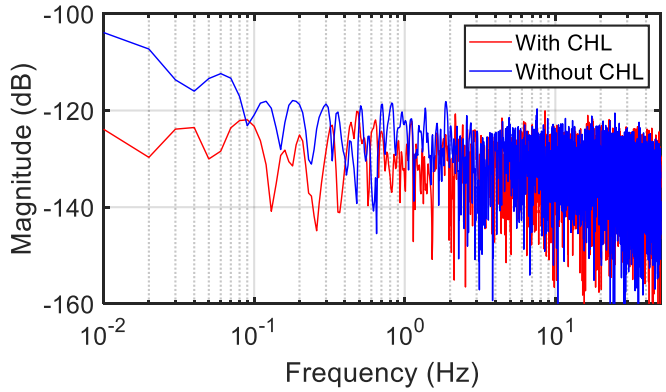


Figure 3.41: Spectra of the sensor's decimated BS output with/without system-level chopping (CHL).

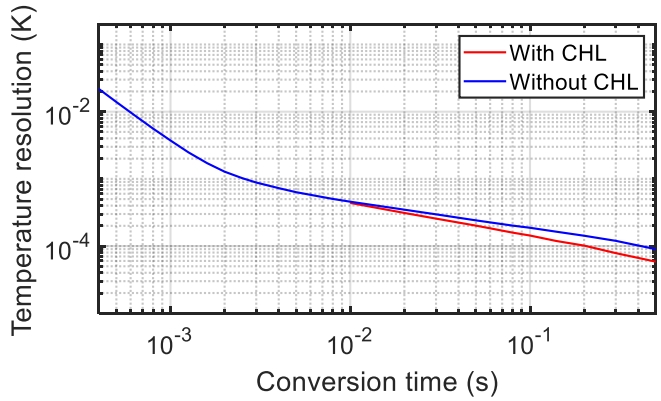
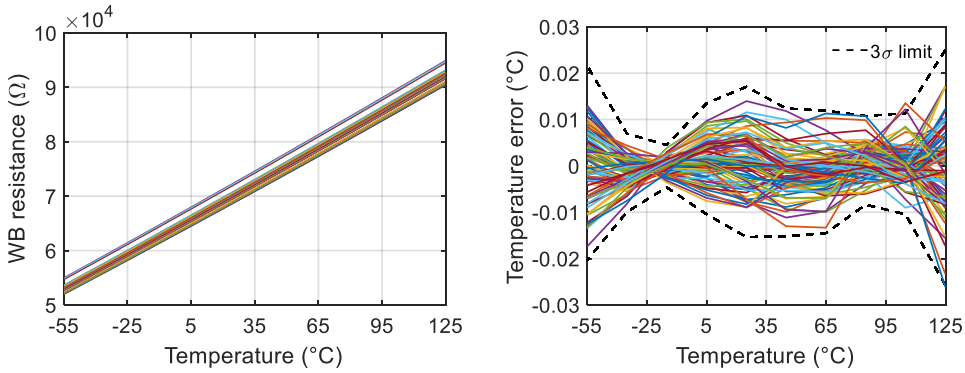


Figure 3.42: Resolution vs. conversion time over a 1s period, with/without system-level chopping.

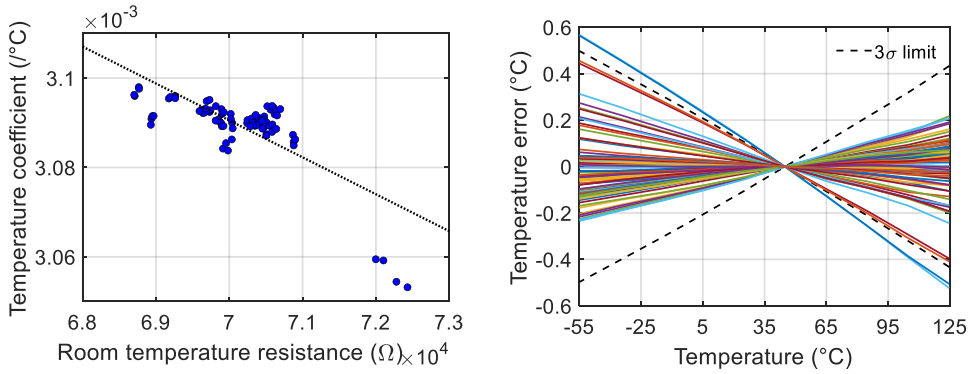
3.5.2.2 Calibration and inaccuracy

After converting the decimated ΔΣ-ADC output to WB resistance, an individual 1st-order fit is applied to remove process spread. Followed by a 5th order systematic nonlinearity removal, the s-p-poly sensor achieves a 3σ inaccuracy of 0.03°C from −55°C to 125°C, as shown in Figure 3.43. A similar inaccuracy can be achieved after replacing the 1st-order fit with a two-point trim (−35°C and 105°C).



(a) (b)

Figure 3.43: (a) Extracted sensor resistance and (b) sensor inaccuracy after a 1st-order fit and systematic non-linearity correction.



(a) (b)

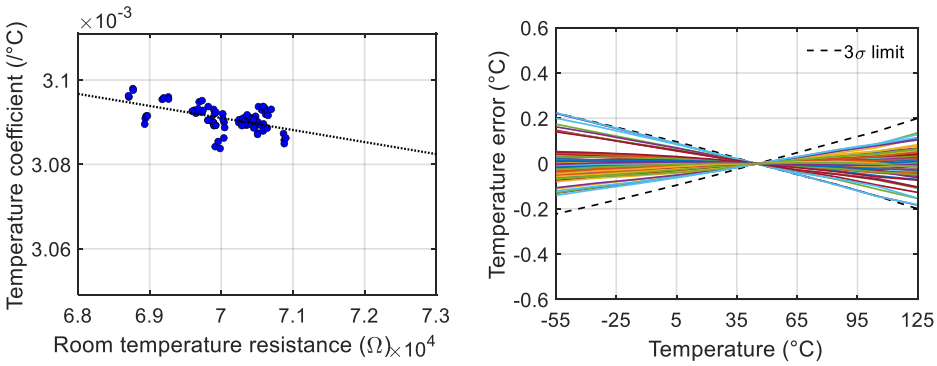
Figure 3.44: (a) Correlation between R_0 and TC (b) sensor inaccuracy after a correlation-assisted 1-point trim and systematic non-linearity correction.

The correlation between the calculated WB resistance at RT (R_0) and its TC is shown in Figure 3.44 (a). To fairly compare it with that in the first implementation, the correlation slope can be normalized by TC and R_0, i.e.,

$$k_{corr} = \frac{dTC}{dR_0} \cdot \frac{R_0}{TC}. \tag{3.13}$$

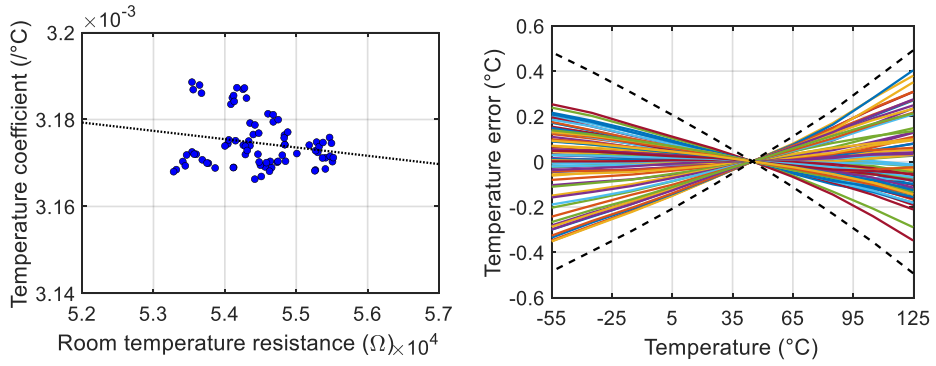
In this design, k_{corr} is roughly ~−18%, which is larger than the −11% observed in the first WB implementation (Figure 3.27 (a)). However, the correlation is less significant. Consequently, the relative 1-point trimmed inaccuracy is degraded from 0.32% to 0.55%, and the 3σ error becomes 0.5°C over the 1.4× larger temperature range, as

shown in Figure 3.44 (b). However, it is worth noticing that there are four outliers (from a single chip) that deviate from most of the samples. Without these outliers, the 1-point trimmed inaccuracy will become ~0.25°C, which is similar to that achieved by the first WB implementation. The calculated k_{corr} under this situation is ~−7%, which is smaller than that of the first WB implementation.



(a) (b)

Figure 3.45: (a) Correlation between R_0 and TC (b) sensor inaccuracy after a correlation-assisted 1-point trim and systematic non-linearity correction, with 4 outliers excluded.



(a) (b)

Figure 3.46: (a) Correlation between R_0 and TC (b) sensor inaccuracy after a correlation-assisted 1-point trim and systematic non-linearity correction for sensors in another batch.

To investigate which model is better, an almost identical WB sensor design has been fabricated in another batch and then characterized. Figure 3.46 shows its R_0-TC correlation and the temperature inaccuracy. Compared to Figure 3.45, the TC spread is larger, and the 1-point-trimmed inaccuracy is degraded to about 0.5°C (3σ). Even assuming no R_0-TC correlation, the 1-point-trimmed inaccuracy is only 5% worse. It

can be concluded that, the R_0-TC correlation is either non-existent or too weak to be relied on for the narrow (0.5μm) silicided poly resistor.

3.5.2.3 Comparison to implementation II

Compared to the second prototype, the third implementation achieves 3× better relative inaccuracy with the same chip area. This is mainly due to the improved opamp design and use of system-level chopping.

3.6 Comparisons and concluding remarks

In this chapter, three Wien-bridge-based temperature sensor prototypes were presented. All the sensors use a 2nd-order phase-domain ΔΣ ADC to digitize the temperature-dependent phase shift of the WB sensor. The characteristics of these sensors are summarized and compared to the state-of-the-art (in 2020) in Table 3.2.

Compared to the first prototype, the readout circuits in the next two implementations were further optimized, resulting in less chip area and, finally, in better relative inaccuracy. In the most recent implementation, the 0.12mm^2 WB sensor achieves a relative inaccuracy of 0.03% with only two trimming points, and a 1/*f* noise corner of below 10mHz. However, the resolution FoM of such sensors (>100fJ·K^2) is far larger than the theoretical value (2.3fJ·K^2), which is mainly due to the power and noise from the readout circuit.

Similar or even better energy efficiency (<100fJ·K^2) can be achieved with a frequency-based readout [3.13][3.14][3.15], i.e., a frequency-locked loop (FLL) followed by a frequency-to-digital converter (FDC). Like a phase-domain ΔΣ ADC, the power consumption and noise performance of an FLL are dominated by that of its integrator (Figure 2.9). By using filtering [3.13] or sampling [3.14] techniques, however, the integrator's AC input can be greatly suppressed, allowing its design to be optimized for noise. This is not the case for the sensors presented in this chapter, since their integrators must be designed to handle the maximum output current of their WB sensors. Another way to suppress the sensor's power is to digitize the front-end output before entering the FLL [3.15]. However, due to the large comparator noise, this typically results in a slightly worse energy efficiency.

Despite a better (or similar) FoM, the accuracy of FLL-based sensors is currently significantly worse, possibly due to the charge injection of the switched-capacitor circuits used in their RC front-ends. Furthermore, such sensors also require an FDC to digitize the frequency output, whose extra power consumption and area is not always presented.

Table 3.2: Performance summary of the WB sensors presented in this Chapter and that of other state-of-the art RC-based temperature sensors.

	JSSC'20 [3.13]	ISSCC'20 [3.14]	Implementation I JSSC'18	Implementation II ISSCC'19	Implementation III ISSCC'21
Sensor type	SC-WhB	RC	WB	WB	WB
ADC type	FLL+FDC	FLL+FDC	ΔΣM	ΔΣM	ΔΣM
Technology	180nm	65nm	180nm	180nm	180nm
Area [mm^2]	0.72	0.0088	0.72	0.12	0.12
Temp. Range [°C]	−40─85	−30─90	−40─85	−40─180	−55─125
3σ Inaccuracy [°C] (trimming points)	0.55 (2)	0.32[a] (2)	0.03 (2[b])	0.1 (2[b])	0.03 (2[b])
Relative inaccuracy	0.88%	0.52%	0.05%	0.1%	0.03%
Power [μW]	15.6	45	160	52	66
Conv. time [ms]	1	1	5	10	10
Resolution [mK]	2	1.43	0.44	0.46	0.45
Res. FoM [fJ·K^2]	62	92	150	110	130

[a] Min/Max. [b] 1st-order fit.

3.7 References

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[3.2] C.P.L. van Vroonhoven and K.A.A. Makinwa, "A CMOS temperature-to-digital converter with an inaccuracy of ±0.5°C (3σ) from –55 to 125°C," in *IEEE ISSCC Dig. Tech. Papers*, pp. 576 - 577, Feb. 2008.

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Chapter 4

Wheatstone-bridge-based temperature sensors

4.1 Introduction

In contrast to Wien-bridge sensors, on-chip Wheatstone bridge (WhB) sensors are less accurate, due to the lack of a stable reference resistor. However, because of the extra sensitivity that can be achieved by using resistors with opposite temperature coefficients (TCs), they can achieve better energy efficiency.

As presented in Chapter 2, the TC of silicided resistors is positive (TC_p), while that of some non-silicided poly resistors is negative (TC_n). In the chosen 0.18μm process, TC_p = 0.285%/°C for the silicided-p-poly resistor, while TC_n = −0.152%/°C for the non-silicided n-poly resistor. According to equation (2.1), the theoretical FoM of the resulting Wheatstone bridge will then be ~1.7fJ·K^2. Assuming the readout circuit dissipates the same power and contributes the same noise as the bridge, the practical FoM limit will then be ~7fJ·K^2.

Like Chapter 3, this chapter starts with a discussion of some general design choices, including the choice of readout circuit topology and the trimming method. Afterward, four Wheatstone bridge sensor implementations are presented based on their publication sequence. By systematically optimizing their circuit design, their resolution FoM improves from 65fJ·K^2 (the first implementation) to 10fJ·K^2 (the fourth implementation).

4.2 General design choices

4.2.1 Traditional readout vs. direct readout

Traditionally, a Wheatstone bridge sensor output is read out by digitizing its open-circuit voltage, as shown in Figure 4.1 (a), where R_p and R_n are resistors with positive and negative TCs, respectively. An instrumentation amplifier (IA) can be used to match the output voltage and impedance of the bridge to the input range and

impedance of the ADC, resulting in good energy efficiency. Compared to the classic 3-opamp IA [4.1], a significant improvement in energy efficiency can be achieved by using a Current Feedback Instrumentation Amplifier (CFIA) [4.2] or a Capacitively-Coupled Instrumentation Amplifier (CCIA) [4.3].

One drawback of this traditional topology is that the sensor's accuracy will be limited by the combined gain errors of the IA and the ADC. Moreover, the sensor's output range is limited to V_{DD} over the gain of the IA. To effectively suppress the input-referred noise of the ADC, the IA's gain is usually larger than 10 [4.4], which sets a maximum WhB output of $0.1V_{DD}$. In the chosen process, however, the WhB output range is roughly 14% over the industrial temperature range (−40°C to 85°C) or almost 20% over the military range (−55°C to 125°C). Consequently, the energy-efficiency of this traditional topology cannot be optimized.

A simpler and more accurate way of reading out a WhB is by directly balancing it with a resistive DAC, and hence, nulling its output current. As shown in Figure 4.1 (b), the required feedback loop can be conveniently realized as a continuous-time delta-sigma modulator (CTΔΣM) [4.5], where the modulator's bitstream output D_{out} drives the resistive DAC to null the difference I_{err}(T) between the output currents of the DAC and the bridge. The resulting bitstream average will then be proportional to the amount of parallel resistance required to balance the bridge. If R_{DAC} is also an R_n-type resistor, the bitstream average will be solely determined by the temperature-dependent values of R_n and R_p resistors. The system is also robust to supply voltage variations, since the DAC and the bridge share the same supply. Moreover, the WhB output range has no limitation, as the integration capacitor (C_{int}) can be scaled to limit the maximum output voltage of the integrator. In this chapter, this direct readout scheme is used in all four implementations.

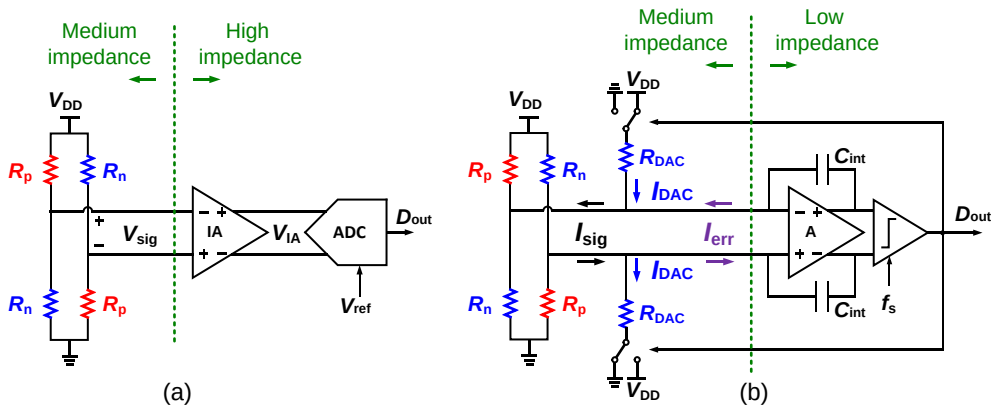


Figure 4.1: (a) Conventional WhB readout using IA and ADC and (b) CTΔΣM WhB readout with a resistive DAC.

4.2.2 Nonlinearity and trimming

As in Chapter 2, the temperature dependence of the various resistors in the WhB and the DAC can be modeled as:

$$\begin{aligned} R_p(T) &= R_p(T_0)\cdot(1 + TC_{p1}\cdot\Delta T + TC_{p2}\cdot\Delta T^2) \\ R_n(T) &= R_n(T_0)\cdot(1 + TC_{n1}\cdot\Delta T + TC_{n2}\cdot\Delta T^2) \\ R_{DAC}(T) &= R_{DAC}(T_0)\cdot(1 + TC_{n1}\cdot\Delta T + TC_{n2}\cdot\Delta T^2). \end{aligned} \tag{4.1}$$

Here $R_p(T_0)$, $R_n(T_0)$, and $R_{DAC}(T_0)$ are the resistances at a reference temperature T_0, while TC_{p1}, TC_{n1}, are their 1st order TCs, TC_{p2} and TC_{n2} are their 2nd order TCs, and ΔT is the temperature with respect to T_0. Noting that the active integrator virtually shorts the bridge's output terminals to $V_{DD}/2$, while the modulator ensures that the integrator's average input current I_{err} is zero, the bitstream average μ_{ADC} can be expressed as:

$$\begin{aligned} \mu_{ADC} &= \frac{I_{sig}(T)}{I_{DAC}(T)} = \frac{1/R_p(T) - 1/R_n(T)}{1/R_{DAC}(T)} \\ &= \frac{R_{DAC}(T_0)}{R_p(T_0)}\cdot\frac{(1 + TC_{n1}\cdot\Delta T + TC_{n2}\cdot\Delta T^2)}{\left(1 + TC_{p1}\cdot\Delta T + TC_{p2}\cdot\Delta T^2\right)} - \frac{R_{DAC}(T_0)}{R_n(T_0)} \\ &= \frac{R_{DAC}(T_0)}{R_p(T_0)}\cdot f_{pn}(\Delta T) - \frac{R_{DAC}(T_0)}{R_n(T_0)}. \end{aligned} \tag{4.2}$$

Since the TC spread of CMOS resistors is much smaller than their nominal resistance spread (Chapter 3, section 3.3.2.2), the function f_{pn}, can be approximated as a constant, but non-linear, function of temperature. The ratio R_{DAC}/R_p involves different types of resistors and so will spread significantly, while the ratio R_{DAC}/R_n involves the same type of resistors and so should spread less. So a one-point trim is definitely required to compensate for the spread of R_{DAC}/R_p. A two-point trim, on the other hand, will compensate for the spread of R_{DAC}/R_n, as well as some spread due to the varying TCs.

According to (4.2), the mapping of the main spread component R_{DAC}/R_p to μ_{ADC} is linear, so unlike WB sensors (Chapter 3, section 3.2.3.2), no nonlinearity correction polynomial is required before performing a two-point trim. This greatly simplifies the process of calibrating a WhB sensor.

4.3 Implementation I, proof of concept [1]

In this first design, a WhB sensor is built by reusing circuit blocks from the first WB sensor design (Chapter 3, section 3.3). It achieves a resolution FoM of 65fJ·K^2, which is better than that of all the WB sensors. However, due to the lack of optimization, this FoM is still almost 10× worse than the practical FoM limit.

4.3.1 Circuit implementation

As shown in Figure 4.2, the proposed Wheatstone bridge temperature sensor consists of silicided p-poly (s-p-poly, R_p=105kΩ, TC≈0.285%/°C) and a non-silicided n-poly (R_n=95kΩ, TC≈−0.152%/°C) resistors. To investigate the performance of the non-silicided p-poly resistor, a bridge made from s-p-poly and p-poly resistors (TC≈−0.02%/°C) was also realized. To reuse the same readout circuit, its bridge resistances (R_p=67.5kΩ, R_n=64kΩ) are chosen to ensure the same maximum error current levels over the industrial temperature range from −40°C to 85°C.

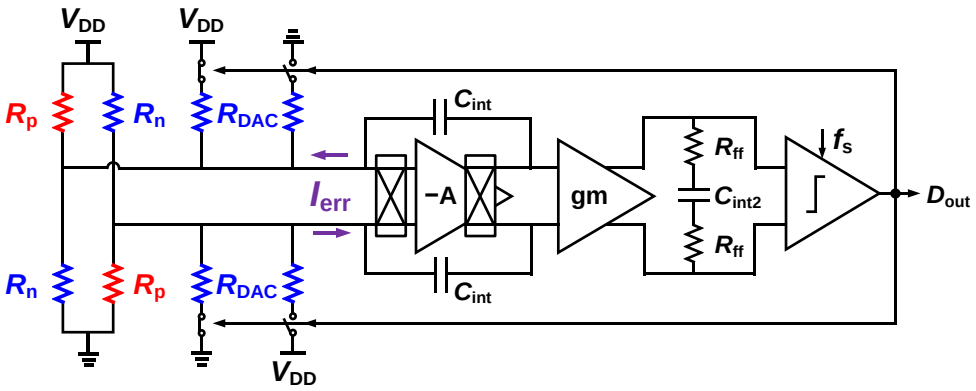


Figure 4.2: System block diagram of the first WhB sensor implementation.

As in section 4.2.1, the Wheatstone bridge sensors are read out by connecting them to the virtual ground of the 1st integrator of a CTΔΣ-ADC (Figure 4.2). The modulator's resistive DAC (R_{DAC}=140kΩ, made from the same material as R_n) will then null their output current. The DAC resistors are switched to either supply rails or left floating, so that this differential sensor has 4 DAC resistors. As will be shown in the second design, however, the same function can be performed by switching two DAC resistors between the supply rails.

[1] S. Pan, H. Jiang, and K. A. A. Makinwa, "A CMOS temperature sensor with a 49fJK^2 resolution FoM," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. C82–C83.

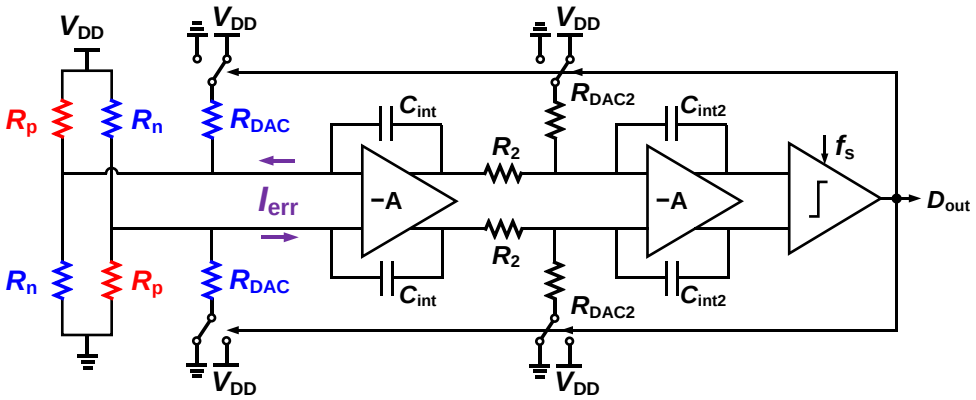


Figure 4.3: System block diagram of a previous Wheatstone bridge sensor [4.5].

In this work, in contrast to previous work [4.5] shown in Figure 4.3, the use of a feedforward architecture helps to suppress the swing of the 1st integrator. More importantly, the offset and 1/*f* noise of the 1st integrator are suppressed by chopping. To avoid aliasing high-frequency quantization noise at the chopping transitions [4.6], the chopping frequency is the same as the sampling frequency (500kHz).

Both the amplifiers used in the 1st and 2nd integrators were reused from the first WB prototype (Chapter 3, section 3.3). From simulations, the 1st and 2nd integrators dissipate 100µW and 7µW, respectively, from a 1.8V supply. The bridges dissipate 32µW (s-p/n-poly) and 25µW (s-p/p-poly).

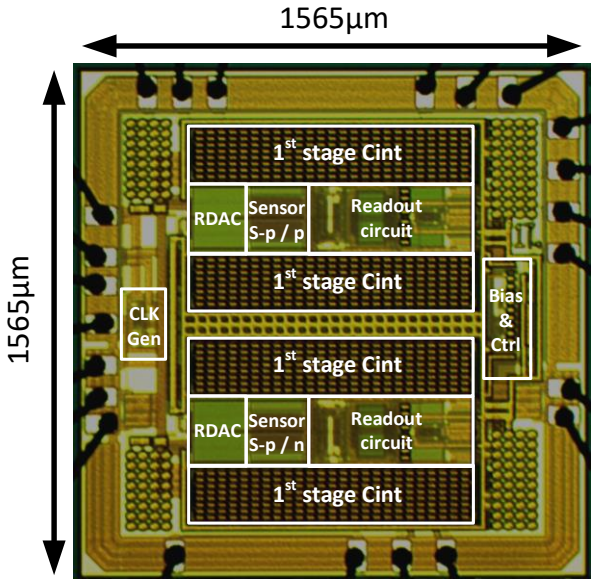


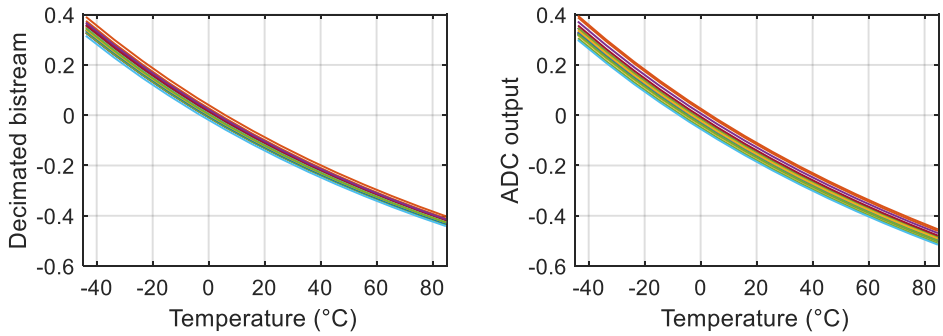
Figure 4.4: System block diagram of the first WhB sensor implementation.

4.3.2 Measurement results

The two Wheatstone bridge sensors were fabricated side-by-side, as shown in Figure 4.4. They share the same clock and constant-g_m biasing circuits and each occupies 0.72mm^2, which is dominated by the large capacitors (2 × 180pF) of the 1st integrator. For flexibility, the sinc^2 decimation filter is realized off-chip.

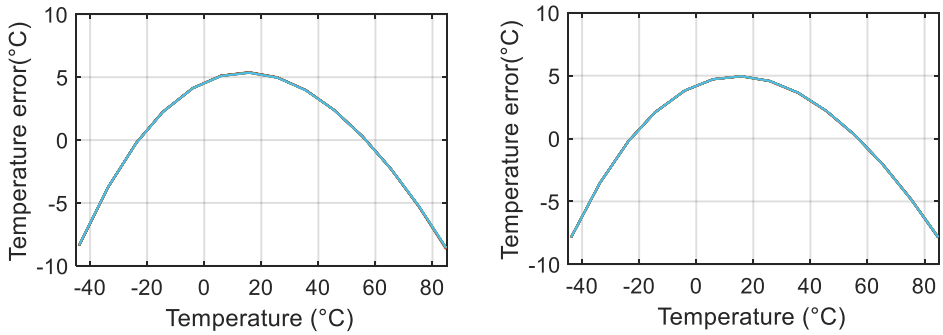
4.3.2.1 Calibration and inaccuracy

Twenty samples from one wafer were characterized in ceramic packages from −40°C to 85°C in a temperature-controlled oven. The sensor characters are shown in Figure 4.5. After a 1st-order fit, the measured nonlinearities are quite systematic (Figure 4.6), and, like those shown in Chapter 3, can be removed by a fixed polynomial. The resulting spread is below 0.07°C (3σ) for the s-p-poly/p-poly sensor, and below 0.10°C (3σ) for the s-p-poly/n-poly sensor (Figure 4.7). At room temperature, the power supply sensitivity of both sensors is less than 20mK/V.



(a) (b)

Figure 4.5: Output vs. temperature of (a) s-p-poly/n-poly WhB sensors and (b) s-p-poly/p-poly WhB sensors.



(a) (b)

Figure 4.6: Temperature error of (a) s-p-poly/n-poly WhB sensors and (b) s-p-poly/p-poly WhB sensors after individual 1st-order fit.

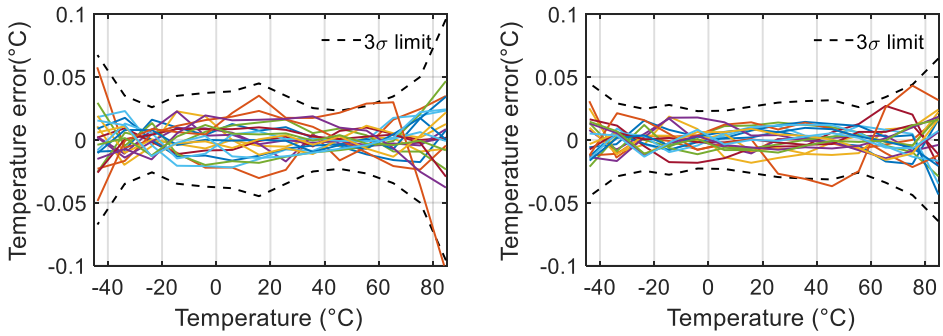


Figure 4.7: Residual temperature error of (a) s-poly WhB sensors and (b) s-diffusion WhB sensors after indiviudal 1st-order fit and systematic nonlinearity removal.

4.3.2.2 Resolution and FoM

The bitstream spectra of the sensors are shown in Figure 4.8. The observed 1/*f* noise is mainly due to the non-silicided poly resistors, resulting in a 10Hz corner frequency for both sensors. In [4.7], it was reported that the s-p-poly/n-poly sensor achieves a thermal-noise limited resolution of 164μK in a conversion time of 10ms (Figure 4.9), which corresponds to a resolution FoM of 49fJ·K^2. However, just like that in [4.8], the use of a two-sample Allan deviation underestimates the sensor's 1/*f* noise. With a more realistic estimation using standard deviation in a 1s interval (Chapter 3, section 3.3.2.1), the resolution becomes ~15% worse, and the corresponding FoM becomes 65fJ·K^2. Although the s-p-poly/p-poly sensor achieves a similar level of resolution with the same conversion time, its resolution FoM is ~10% worse due to its larger power consumption.

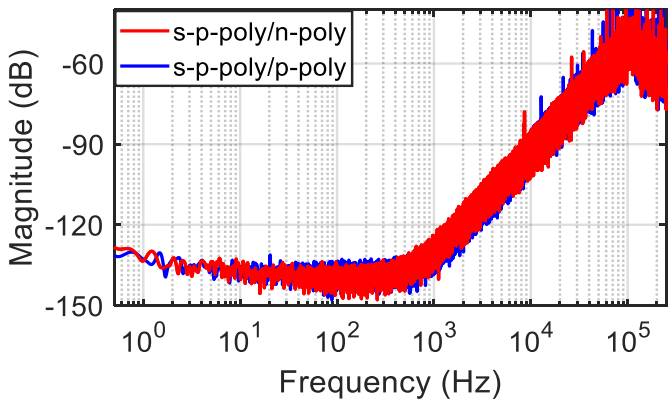


Figure 4.8: Bitstream spectra of two types of Wheatstone bridge sensors.

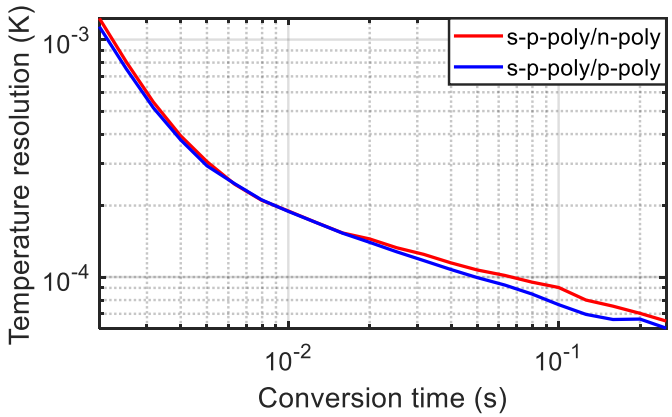


Figure 4.9: Resolution vs. conversion time of the Wheatstone bridge sensors.

4.3.2.3 Comparison with prior art

Compared to [4.5], the energy efficiency of the proposed s-p-poly/n-poly Wheatstone bridge sensor is improved by 10×, which is mainly due to the increased sensitivity from silicided-poly resistors and the reduced 1/*f* noise via chopping. As for the s-p-poly/p-poly sensor, its resolution FoM is ~10% worse than the s-p-poly/n-poly sensor, but the inaccuracy is somewhat better.

The sensor requires further optimization: its area is ~70% larger compared to [4.5], and the efficiency gap between the achieved FoM (65fJ·K^2) and the practical FoM limit (7fJ·K^2) is almost 10×.

4.4 Implementation II, smaller area and better FoM²

In this second implementation, a multi-bit CTΔΣ-ADC is proposed to replace the single-bit ADC used in the first Wheatstone bridge sensor prototype. It achieves a resolution FoM of 40fJ·K^2 and an active chip area of 0.25mm^2.

4.4.1 System-level design

Just like the first Wien-bridge implementation, the first Wheatstone bridge prototype consumes most of its power/area in the 1st stage amplifier/integration

[2] S. Pan and K. A. A. Makinwa, "A 0.25 mm^2 resistor-based temperature sensor with an inaccuracy of 0.12°C (3σ) from −55°C to 125°C," in *IEEE J. Solid-State Circuits*, vol 53, no. 12, pp. 3347-3355, Dec 2018.

capacitor. These are all limited by the large variation in the WhB output signal I_{sig} over PVT. As shown in Figure 4.10 (a), the first stage of the CTΔΣ-ADC is essentially an active-RC integrator, where the WhB is modeled by a source resistor driven by a temperature-dependent voltage $V_{in}(T)$. This has to be compensated by the output current I_{DAC} of a 1-bit DAC, resulting in an even larger error current I_{err} flowing into the 1st integrator, as shown in Figure 4.10 (b).

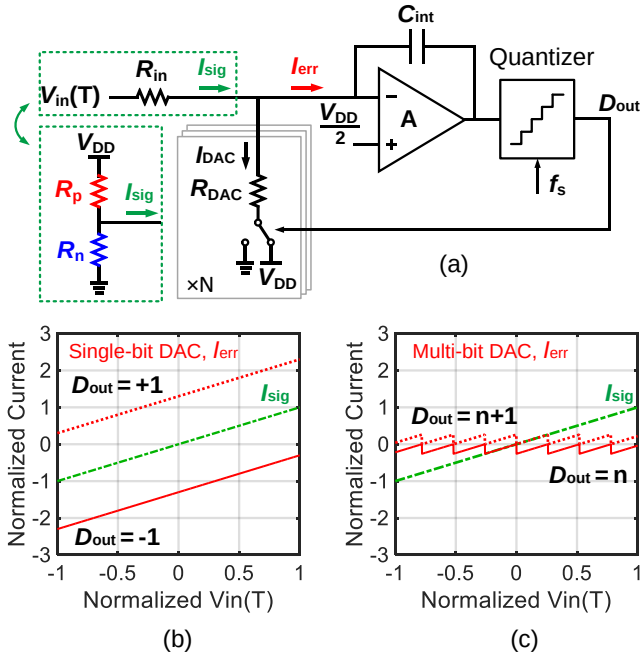


Figure 4.10: (a) A CTΔΣ-ADC based on an active integrator. (b) Error current of a single-bit CTΔΣ-ADC. (c) Error current of a multi-bit CTΔΣ-ADC.

A multi-bit resistor DAC (N > 1) can be used to reduce the magnitude of I_{err} (Figure 4.10 (c)). Since most of I_{sig} will then be compensated by I_{DAC}, the 1st integrator's supply current, as well as the size of its integration capacitors, can be significantly reduced.

Nonlinearity is a key challenge in multi-bit ΔΣMs. For CTΔΣMs with resistive DACs, the two major contributors are RDAC mismatch and the non-linearity of the 1st integrator. RDAC mismatch can be sufficiently suppressed by careful layout and dynamic element matching (DEM). The non-linearity of the 1st integrator, however, is more problematic. The input impedance of the CTΔΣM becomes signal-dependent, and so will the DAC value. As in [4.9], this creates inband-noise (IBN) that cannot be mitigated by DEM. Increasing the linearity of the 1st stage amplifier would help, but this usually comes at the expense of higher power dissipation.

This problem can be solved using a zoom-ADC [4.10]. During the fine conversion of a zoom ΔΣM, however, only two levels of its multi-bit DAC will be used. As a result, the DAC will still appear to be perfectly linear even in the presence of integrator non-linearity, and so no quantization noise folding will occur [4.11].

The proposed zoom CTΔΣM digitizes the temperature-dependent ratio $X = I_{sig}/(2I_{DAC})$ in two steps, as illustrated in Figure 4.11 (a), for the case of a 1st-order modulator. First, a coarse SAR conversion determines the integer part n of X. Then, the fractional part μ is determined by a fine ΔΣ conversion. Compared to conventional multi-bit ΔΣMs, a zoom-ADC obviates the complexity of a multi-bit quantizer and only requires a single-bit comparator, a reset switch for the 1st integrator, and some logic.

During the coarse conversion, the 1st integrator is used as a pre-amplifier for the comparator [4.12]. Each step of the SAR conversion then consists of choosing a DAC code, resetting the 1st integrator, and then integrating the resulting error current for one clock cycle. The polarity of the result is detected by the comparator and used to determine the next DAC code to test. To absorb potential errors from the SAR conversion and ensure that μ lies in the modulator's stable input range, over-ranging is used. This is implemented by switching the DAC between the codes $n-1$ and $n+1$ during the delta-sigma phase (Figure 4.11 (b)). This significantly reduces the current I_{err} flowing into the integrator so the linearity and power dissipation of the 1st integrator can be significantly relaxed.

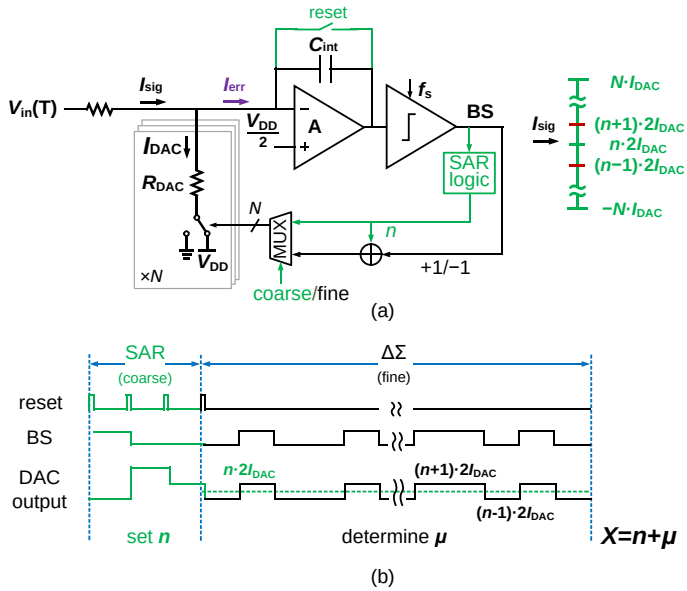


Figure 4.11: (a) Schematic of a static zoom CTΔΣM and (b) a timing diagram example in case of a 3-bit DAC.

4.4.2 Circuit implementation

4.4.2.1 Wheatstone bridge and DAC

In contrast to the first Wheatstone bridge prototype, this sensor is designed to operate over the military temperature range (−55 °C to 125 °C). As a result, the bridge is unbalanced at room temperature (RT, about 25 °C), with R_p = 100kΩ and R_n = 80kΩ. With a 1.8 V supply, this results in $|I_{sig}| < 7$ µA over PVT, which requires a minimum DAC resistance of 120kΩ. The minimum width imposes a tradeoff between the number of DAC bits and the minimum possible DAC area. To ensure that the areas of the DAC and the integrating caps C_{int} are roughly equal, a 3-bit DAC was chosen, with unit elements of 960kΩ. As in [4.12], an extra half-LSB unit element is used at the end of the coarse conversion to determine the optimal choice of the references used in the fine conversion.

4.4.2.2 Zoom ADC

Figure 4.12 shows the circuit diagram of the zoom CTΔΣ-ADC. To achieve high resolution in a reasonable conversion time, a 2nd order modulator was chosen with a feedforward architecture to reduce the swing at the output of the 1st integrator and thus further reduce the size of C_{int} (~48pF). As in the first Wien bridge sensor prototype, the loop is stabilized by a zero realized by R_{ff} at the output of the 2nd integrator.

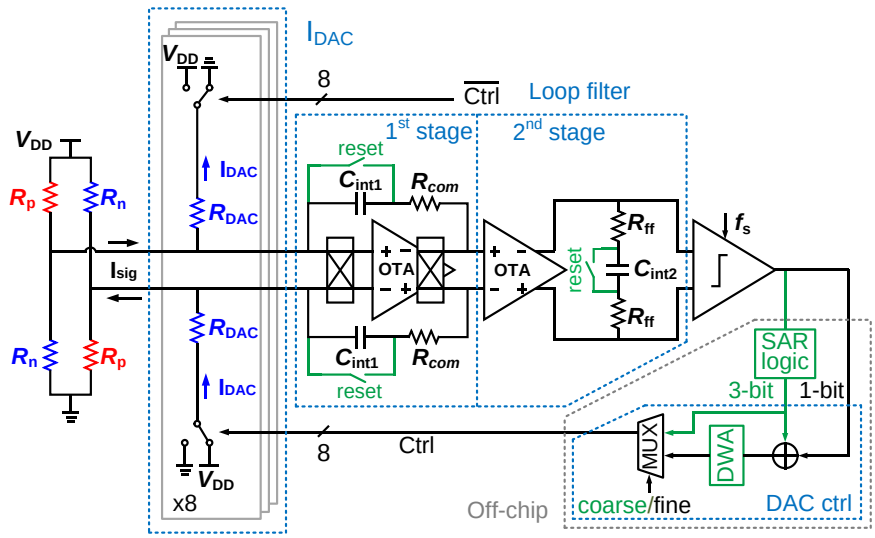


Figure 4.12: Circuit diagram of the zoom CTΔΣ-ADC.

Since the 1st integrator's non-linearity will not increase IBN, it was optimized mainly for noise. It employs an energy-efficient current-reuse OTA, rather than the two-stage opamp used in the first Wheatstone bridge prototype. High-V_T input transistors are used to achieve a reasonable output swing (~0.9 V at RT), as shown in Figure 4.13. To improve modulator stability, the zero of the OTA-based integrator is compensated by inserter $R_{com} \approx 1/g_m$ in series with C_{int}. To suppress its offset and $1/f$ noise while avoiding quantization noise fold-back, the OTA is chopped at the CTΔΣM's sampling frequency (f_s = 500kHz). It achieves over 80dB of DC gain, a GBW product of ~20 MHz with a 1pF load, and consumes 22μW at RT, which is about 60% of the power dissipated by the bridge. The 2nd stage is based on a source-degenerated cascaded telescopic OTA. It has a DC gain of 80dB and dissipates 3μW at RT.

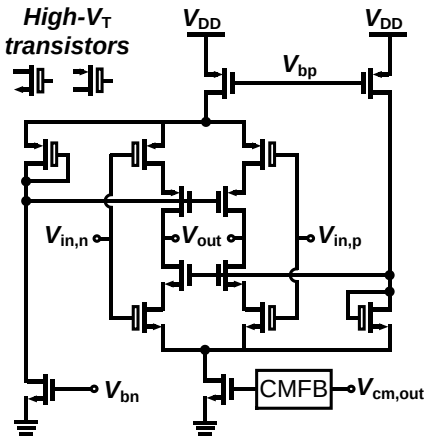


Figure 4.13: Schematic of the 1st stage OTA.

For flexibility, the SAR and DWA logic are implemented off-chip. Since the SAR conversion only involves 3-bits, its duration and power overhead are negligible, and the energy-efficiency of the bridge readout is basically defined by the fine conversion. Simulations show that, if implemented on-chip, the SAR and DWA logic would consume less than 1μW and less than 0.01mm^2 area, which are negligible compared to the other circuit blocks.

4.4.2.3 Non-linearity and segment averaging

Although the nonlinearity of the 1st integrator does not impact the IBN of a zoom ADC, it does impact its INL. The main source of non-linearity is the signal-dependent g_m of the current-reuse OTA, which can be modeled by the addition of a 3rd order term g_{m3}.

The OTA's non-linearity will cause errors in the bitstream average μ obtained after the fine conversion. These will be a weighted average of the associated errors

in the two possible values of the 1st integrator's input current I_{err}. When $\mu = 0$, however, the bitstream output BS will toggle between +1 and −1 with equal probability, and since $I_{err}(BS = +1) = -I_{err}(BS = -1)$, the resulting error in μ will be zero. This will also be the case at the extremes of the modulator's input range, because the bridge's output current I_{sig} will then be exactly canceled by I_{DAC}, and so $I_{err} = 0$. Apart from these three cases, the error of the fine ADC will be non-zero. As shown in Figure 4.14, the result is a sinusoidal error curve centered on $\mu = 0$.

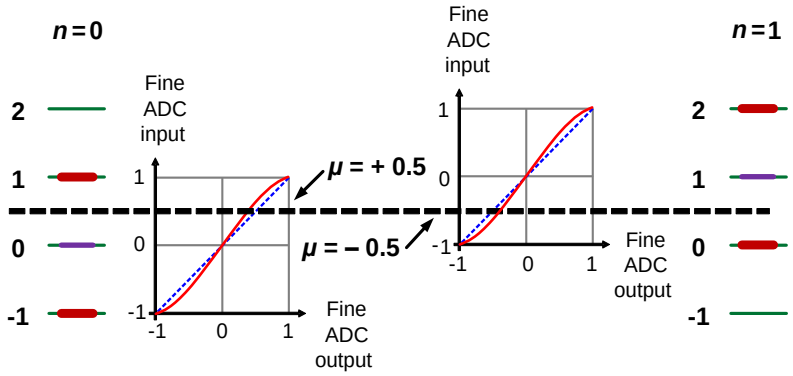


Figure 4.14: Readout error of the opposite sign with two possible coarse codes.

Choosing the range of the fine conversion to be exactly equal to two steps of the coarse conversion (2-LSB over-ranging) means that there are two different ways to convert a given input current, each corresponding to a different coarse code n. Ideally, the zoom ADC's output X would be the same in both cases. In the presence of OTA non-linearity, however, there will be an error in μ, which will be of opposite polarity in the two cases. As shown in Figure 4.15, this means that at the coarse code transitions, i.e. when $\mu = \pm 0.5$, the error in X will abruptly change polarity. Simulations show that the jumps in X at RT can be as large as 0.1°C, which is significantly larger than the sensor's expected resolution.

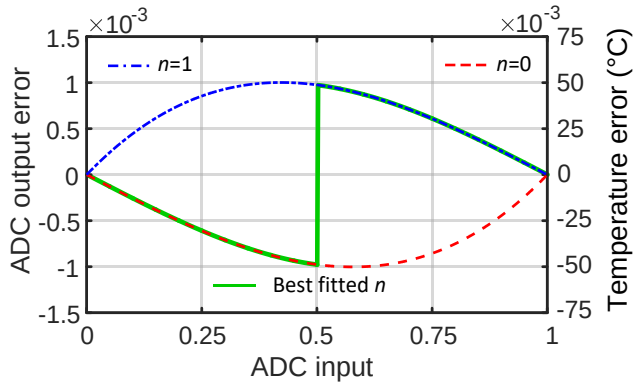
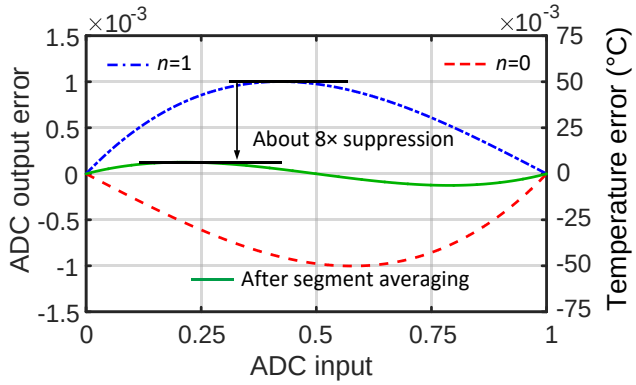


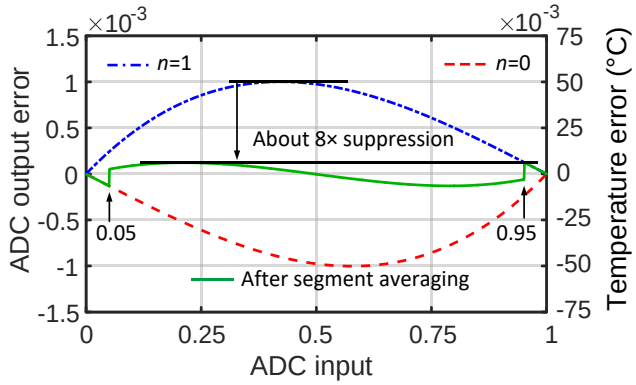
Figure 4.15: Temperature error jump when changing n.

Noting that the errors associated with the two possible n/μ combinations are of opposite polarity, they can be mitigated by simply averaging the values of X obtained from two such conversions, as shown in Figure 4.16 (a). Simulations show that this approach can reduce the error by about 8×, to about ±5mK. This approach translates to considerable power savings. Without this segment averaging technique, the bias current of the 1st integrator's OTA would have to be increased by about 2× to obtain similar linearity.

Although the stable input range of a 2nd order ΔΣM corresponds to $-1 < \mu < 1$ for DC input signals [4.14], its quantization noise becomes quite large when $|\mu| \sim 1$. To avoid degrading the sensor's resolution in such cases, segment averaging is disabled when $1 - |\mu| < 0.05$. As shown in Figure 4.16 (b), this will have little effect on the sensor's linearity, since the nonlinearity is anyway quite small in these cases and the transitions are blurred by the presence of thermal noise.



(a)



(b)

Figure 4.16: Nonlinearity suppression using segment averaging (a) without a threshold (b) with a threshold of 0.05.

4.4.3 Measurement results

The sensor is realized in the same standard 0.18µm CMOS process, with a dimension of 615 µm × 410 µm (Figure 4.17). At RT, it draws 52 µA from a 1.8 V supply, with over half of this dissipated in the WhB and the DAC. About 15% of the active area is occupied by the WhB, 30% by the DAC resistors, and another 30% by the integration capacitors of the 1st stage. For supply voltages varying from 1.6 V to 2.0 V, the sensor's supply sensitivity is 0.02 °C/V. An off-chip sinc^2 filter is used to decimate the sensor's bitstream output.

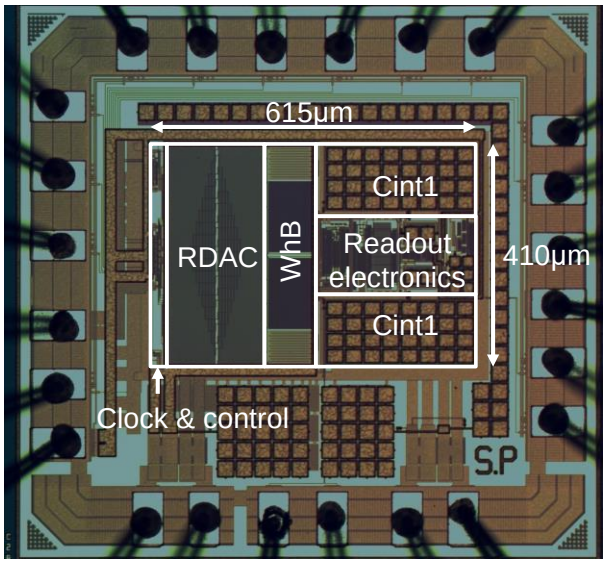


Figure 4.17: Die micrograph of the second Wheatstone sensor implementation.

4.4.3.1 Calibration and inaccuracy

Using a temperature-controlled oven (Vötsch VT7004), 19 chips from the same batch were characterized from −55 °C to 125 °C (in 10 °C steps) in ceramic DIL packages. The reference sensor was a calibrated Pt-100 resistor temperature. To minimize the effects of oven drift, both the Pt-100 and the chips were placed inside a cavity in a large block of aluminum.

Figure 4.18 shows the sensors' output vs. temperature. The opposite trend compared to that of the first WhB implementation is simply due to an inverted BS output. Due to the spread in R_p and R_n, its sensitivity is about 16% less than that in the TT corner. Over temperature, the output of the zoom ADC varies from about 0 to 3.2 over temperature, which is still within its designed full-scale range of −4 to 4.

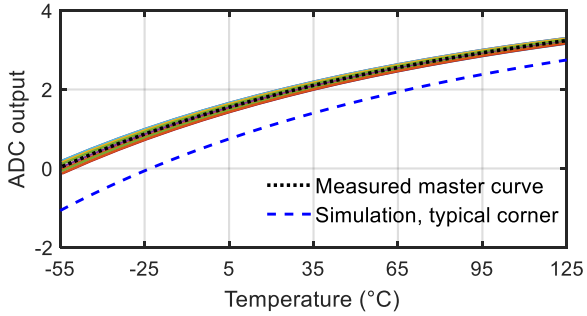
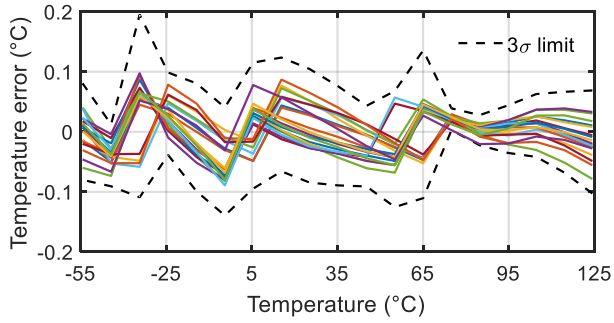
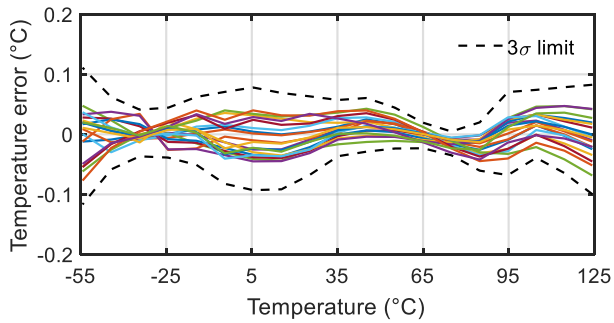


Figure 4.18: Measured and simulated sensor output vs. temperature.

An individual 1st order fit is applied to remove process spread, i.e., the spread of $R_{DAC}(T_0)/R_p(T_0)$ and $R_{DAC}(T_0)/R_n(T_0)$ in equation (4.2). The residual error is then determined by the term $f_{pn}(T-T_0)$ in equation (4.2), which turns out to be quite systematic. Despite the reduction of bridge sensitivity due to process spread, the residual error agrees well with simulations made in the TT corner (maximum error < 0.3°C). As shown before, this error can then be removed by a fixed polynomial.



(a)



(b)

Figure 4.19: Temperature error after individual 1st order fit and systematic nonlinearity removal (a) without segment averaging and (b) with segment averaging.

Without segment averaging, the 3σ inaccuracy is 0.2°C after the systematic nonlinearity is removed by a fixed 5th-order polynomial (Figure 4.19 (a)). As discussed in section 4.4.2.3, the jumps around −35 °C, 5 °C, and 55 °C (when the fine code $\mu \approx \pm 0.5$) are caused by the non-linearity of the 1st stage. With segment averaging enabled (Threshold = 0.05), the inaccuracy can be reduced to 0.12°C (3σ) within the military temperature range (Figure 4.19 (b)). The 1.6× improvement in accuracy is less than the 8× factor shown in Figure 4.14, indicating that the majority of the error is due to the spread of the sensing resistors rather than to the nonlinearity of the ADC.

4.4.3.2 Resolution and FoM

With different DEM algorithms, the power spectral densities of the sensor's output bitstream are shown in Figure 4.20. Since the ADC output range is [−4, 4], 0dB on the y-axis now corresponds to 1/8 of the full ADC range. Compared to barrel-shifting DEM, DWA is more complex, but it preserves the sensor's noise floor. Applying segment averaging of 2.5 ms/segment results in tones at multiples of 200 Hz, but not a raised noise floor. For a fixed conversion time of 5ms (Nyquist frequency of 100 Hz), the tones will be located at the notches of the sinc^2 decimation filter, and thus have no effect on the sensor's resolution. The $1/f$ noise corner is at about 20 Hz, which is mainly due to the non-silicided poly resistor.

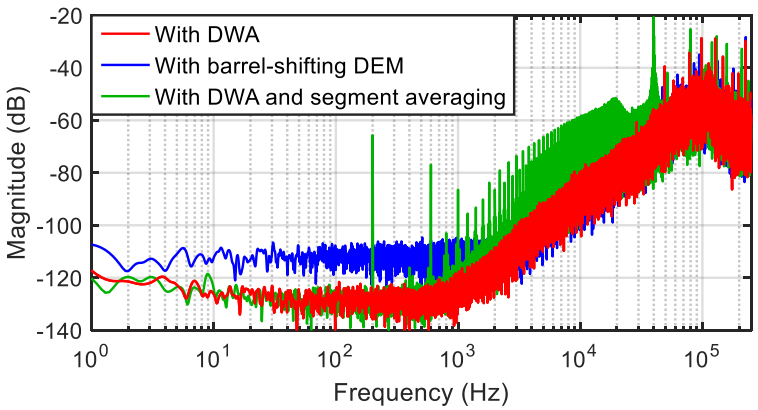


Figure 4.20: Power spectral density of the bitstream output.

After decimation and drift compensation, the sensor's resolution is derived by calculating the standard deviation in a 1s interval (Chapter 3, section 3.3.2.1). Its 290 μK_{rms} resolution in 5ms corresponds to a 40 $fJ \cdot K^2$ resolution FoM, as shown in Figure 4.21.

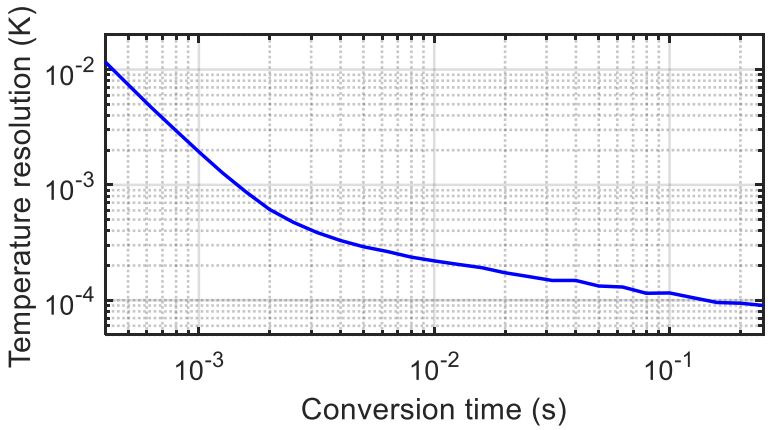


Figure 4.21: Temperature resolution vs. conversion time.

4.4.3.3 Comparison to implementation I

Compared to the first Wheatstone bridge sensor prototype, this design achieves a 40% larger temperature range and a 1.6× better energy efficiency, while occupying 3× less chip area.

4.5 Implementation III, even smaller area and better FoM[3]

In this third prototype, an FIR-DAC CTΔΣ-ADC is implemented to replace the zoom ADC used in the second Wheatstone bridge sensor design. The sensor achieves a better resolution FoM of 20fJ·K^2 with a smaller chip area of 0.12mm^2 in the same 0.18µm CMOS process.

4.5.1 System-level design

As shown in the previous sub-section, the use of a multi-bit DAC reduces the swing of the loop filter's input current I_{err}, which decreases the 1st integrator's power dissipation and the area of C_{int}. In the 2nd prototype, a zoom ADC is used, and the DAC state is determined by combining the result of an initial coarse SAR conversion with the output of a 1-bit CTΔΣM. Extra logic is then required to implement the SAR conversion, as well as the data weighted averaging (DWA) and segment averaging schemes used to mitigate DAC mismatch and amplifier non-linearity, respectively.

[3] S. Pan and K. A. A. Makinwa, "A Wheatstone bridge temperature sensor with a resolution FoM of 20fJ·K^2," in *IEEE ISSCC Dig. Tech. Papers.*, Feb 2019, pp. 186-188.

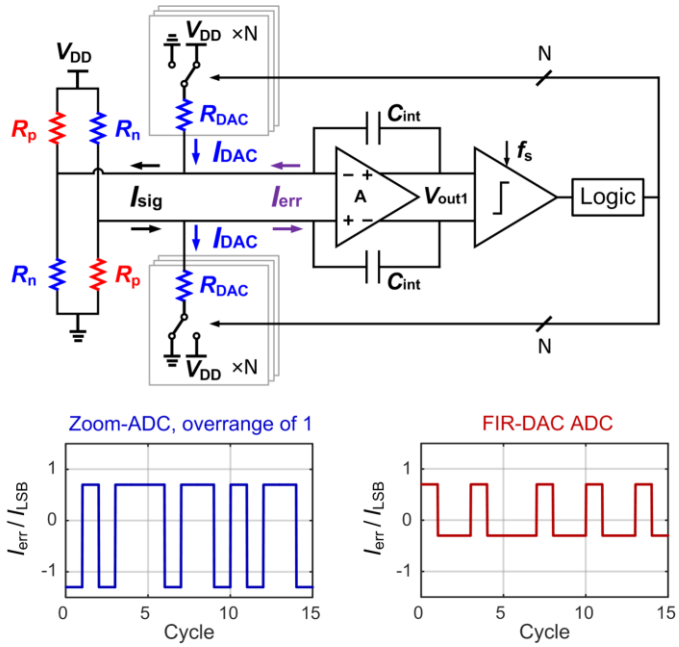


Figure 4.22: CTΔΣ readout of a differential Wheatstone bridge temperature sensor (top), error current I_{err} over time (bottom).

This design employs a 1-bit CTΔΣM with an FIR-DAC, thus ensuring 1-bit linearity without the need for extra logic [4.6]. For the same DAC resolution, the resulting I_{err} swing will then be about 2× less than that in the zoom ADC, since the FIR-DAC does not require over-ranging (Figure 4.22). As a result, both the size and area of C_{int} can be reduced, as well as the 1st integrator's power dissipation. In contrast to a zoom ADC, however, the output of an FIR-DAC may sometimes switch between three DAC levels instead of two. As a result, a more linear input stage is required to prevent quantization noise fold-back, which raises the noise floor [4.9].

Due to the uncorrelated spread of R_p and R_n, the nominal range of the WhB's output current I_{sig} will spread significantly from batch to batch. To compensate for this, and so make optimal use of the modulator's input dynamic range, a 4-bit batch trim is applied to R_p, so that R_{DAC} is only required to compensate I_{sig} over temperature. As shown in Figure 4.23, the trimming scheme ensures that only one switch is in series with the selected segment of R_p. Compared to the trimming scheme in [4.5], this minimizes temperature-sensing errors due to the switches' finite on-resistance.

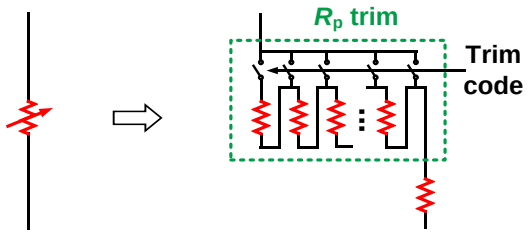


Figure 4.23: R_p trim with constant switch on-resistance.

4.5.2 Circuit implementation

This sensor is designed to operate over the military temperature range from −55°C to 125°C. With R_p=105kΩ and R_n=100kΩ, a 2-bit FIR-DAC consists of four 720kΩ unit elements results in a BS average ranging from −0.68 to 0.68 at the typical corner. With the 4-bit trimming on R_p (~5.7kΩ/step) to compensate for process spread, the BS boundary is then ±0.7. To save area, the DAC resistors are minimum-width. Compared to the zoom-based sensor with a similar R_p and the same temperature range, the total RDAC area is reduced by 2.7×.

To achieve sub-mK resolution in a short conversion time (T_{conv} = 10ms), the modulator employs a 2nd-order feed-forward architecture (Figure 4.24). This also reduces the swing at the output of the 1st integrator, and thus reduces the area of C_{int1} (27pF). The 2nd stage consists of a switched-capacitor integrator (C_{S2} = 100fF and C_{int2} = 2pF) and a feedforward path (C_{FF2} = 400fF), making it a hybrid ΔΣM [4.15]. An extra FIR filter ($C_{FIR,C}$), is used to compensate for the delay introduced by the FIR-DAC [4.6].

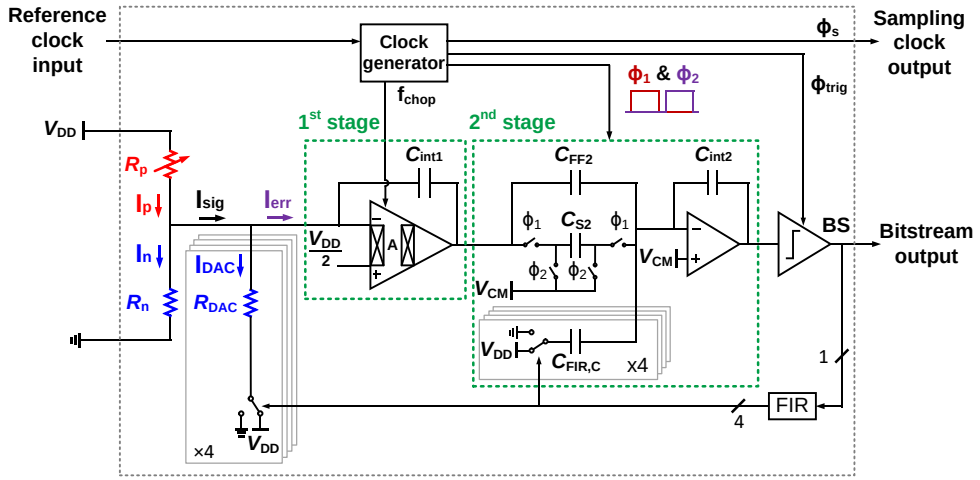


Figure 4.24: Simplified single-ended system block diagram.

The 1st integrator's opamp is a scaled version of that used in the second WB sensor prototype (Figure 3.30). Compared to an OTA, it has a reduced input swing, and thus exhibits better linearity. It consists of two current-reuse stages which maximize the noise efficiency of the input stage, and, compared to the use of two common-source amplifiers, halves the output stage's bias current for a given maximum output current. Also, the use of high threshold devices enlarges the output swing (~1.5V at room temperature). This, in turn, allows the area of C_{int1} to be further reduced. The input stage is chopped to suppress its offset and $1/f$ noise, and so the chopping frequency f_{chop} must be chosen such that quantization noise is not down-converted to DC. In this design, f_{chop} can be set to either f_s = 500kHz or, by exploiting the FIR-DAC's spectral nulls, to multiples of f_s /8 [4.6], as shown in Figure 4.25. From simulations, the chopped opamp has a residual $1/f$ corner frequency of 2Hz, a DC gain of 80dB, while its input/output stages consume 15µW/11µW, respectively. The 2nd stage is built around a cascoded telescopic OTA, which also has an 80dB gain, but consumes only 3.5µW.

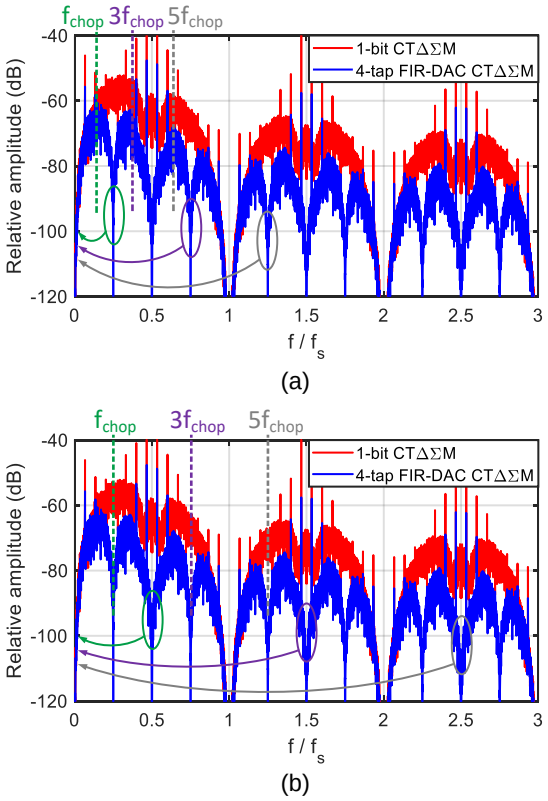


Figure 4.25: PSD of the signal at the input of the 1st integrator with a 1-bit DAC or with a 4-tap FIR-DAC. Nulls in the PSD of the FIR-DAC minimize the folded noise when (a) $f_{chop} = f_s / 8$ and (b) $f_{chop} = 2 f_s / 8$.

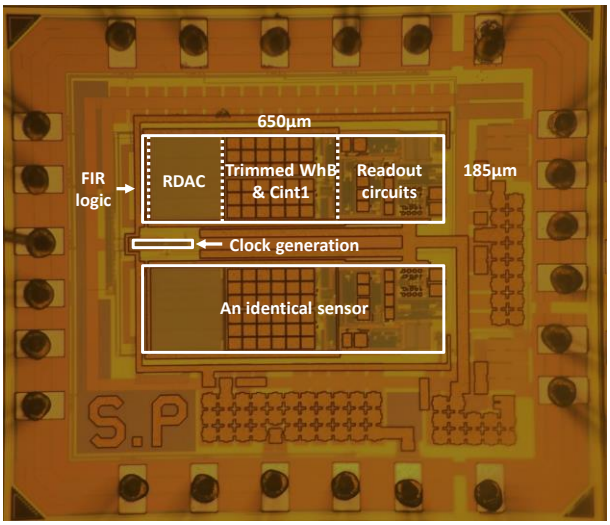


Figure 4.26: Die micrograph of the fabricated temperature sensor.

4.5.3 Measurement results

Two identical sensors were fabricated on the same die in a 0.18µm CMOS process (Figure 4.26). This allows their resolution to be accurately estimated via differential measurements, which effectively reject ambient temperature drift. Each sensor consumes about 44µA (41µA analog and 3µA digital) from a 1.8V supply, and occupies 0.12mm^2, 60% of which is occupied by the WhB and the DAC. The sensors share the same clock generation circuit (0.003mm^2). To further conserve area, C_{int1} (27pF, MIM) is located directly above the WhB. For flexibility, the sinc^2 decimation filters are implemented off-chip.

4.5.3.1 Calibration and inaccuracy

20 samples from one wafer (40 sensors) were mounted in ceramic DIL packages and characterized in a temperature-controlled oven. The packages were mounted in good thermal contact with a large aluminum block. After a batch trim, the residual spread from sample to sample is less than ± 3% full scale at RT. To mimic the effect of batch-to-batch spread, the sensor's output was characterized over temperature for two different trim code settings (Figure 4.27). After a 1st-order fit to compensate for process spread, the resulting systematic non-linearity differs by less than 3mK for the two trim code settings. It also agrees well with simulations (less than 0.1°C difference) and so can be robustly corrected by a fixed 5th-order polynomial. The sensor then achieves an inaccuracy of 0.14°C (3σ) from −55°C to 125°C for both trim code settings (Figure 4.28). The sensor also has a low supply sensitivity: ~0.03°C/V from 1.6 to 2V at RT.

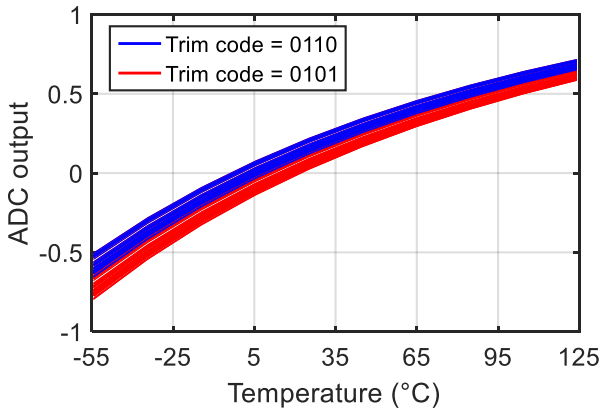


Figure 4.27: Sensor characteristic with different trimming codes.

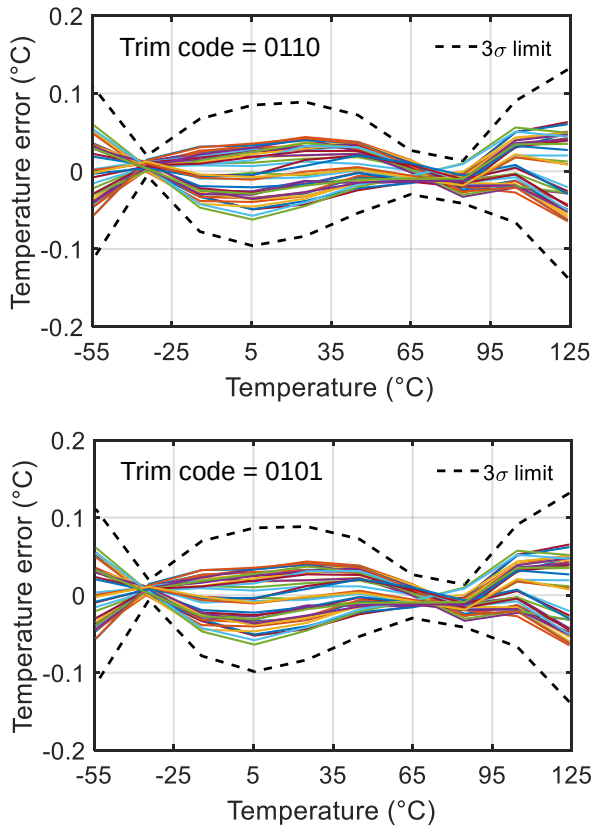


Figure 4.28: Sensor's temperature error after individual 1st-order fit and fixed nonlinearity removal with different trimming codes.

4.5.3.2 Resolution and FoM

FFTs of the sensor's bitstream output are shown in Figure 4.29. As designed, the sensor's noise is dominated by the WhB, and changing f_{chop} from f_s to $f_s/8$ has no significant effect on its resolution. The observed $1/f$ noise (~20Hz corner frequency) is mainly due to the WhB's non-silicided poly resistors. The effect of oven drift can be suppressed by computing the standard deviation from the difference in the output of the two sensors on each die. As shown in Fig. 4.30, over a 1s interval, the results of the single-ended and differential approaches agree well, resulting in a resolution of 160μK (rms) for t_{conv} = 10ms. Like that in Chapter 3, section 3.4.2.1, the effect of the sensor's own $1/f$ noise can be clearly seen by comparing the resolution derived from different time intervals.

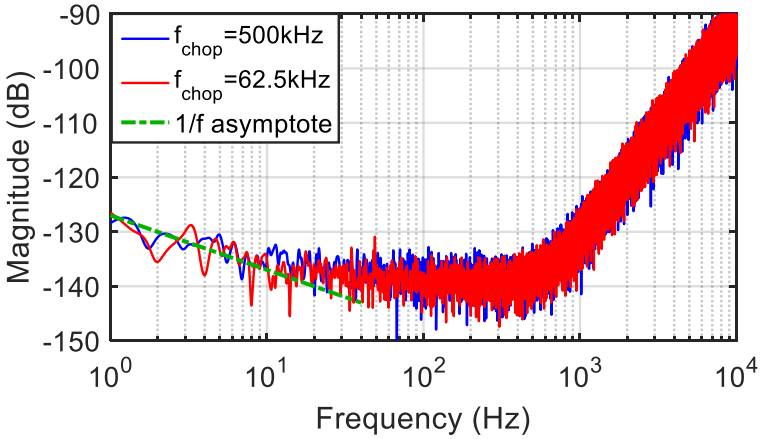


Figure 4.29: PSD of the sensor's bitstream with different chopping frequencies.

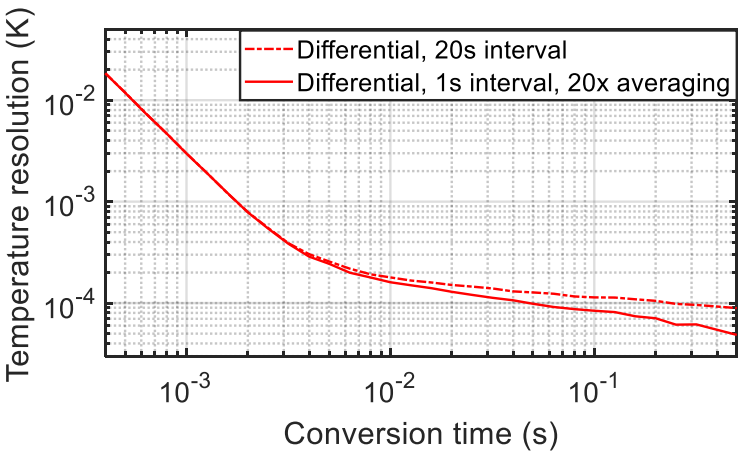


Figure 4.30: Resolution vs. conversion time with different time intervals.

4.5.3.3 Comparison to implementation II

Compared to the second prototype, this design achieves a 2× improvement in both chip area and resolution FoM, while the inaccuracy is kept almost the same.

4.6 Implementation IV, approaching the FoM limit[4]

In this design, we target at approaching the practical FoM limit of Wheatstone bridge sensors. This is done by carefully examining all the power/noise contributors and optimizing the readout circuit. This sensor achieves a resolution FoM of 10fJ·K^2, which is only 6× and 1.5× worse compared to the theoretical and practical FoM limitation, respectively.

4.6.1 Architecture and design considerations

As in the third implementation, this design is also based on the direct digitization of the current output of a Wheatstone bridge by an FIR-DAC CTΔΣ-ADC. To make the best use of ADC range, R_p (~105kΩ) is 3-bit trimmed to compensate for process spread (~40%), so that R_{DAC} is only required to compensate for the temperature dependence of I_{sig} over the targeted temperature range (−55°C to 125°C). To minimize the error from trimming switches, a unary trim is applied to ensure that only one switch is in series with the selected segment of R_p, as shown in Figure 4.23.

4.6.1.1 RDAC switching scheme

As shown in Figure 4.31 (a), in previous designs, the DAC resistors were switched between the supply rails. Some of the R_n-type DAC resistors (R_{DAC1}) will then be connected in parallel with the R_p arms while the rest (R_{DAC2}) are connected in parallel with the R_n arms. In a current readout scheme, the addition of balanced DAC resistors ($R_{DAC1} = R_{DAC2}$) will not alter the sensitivity of I_{err} to temperature. However, the added noise and power will degrade the FoM of the resistive front-end (WhB and DAC resistors). For the resistive front-end in the third prototype, the FoM will be degraded from 1.7fJ·K^2 to 3.0fJ·K^2 at room temperature (RT).

It is worth noting that, to avoid the extra supply current, a 1-bit serial DAC can be realized by using a switch to short a small segment of the R_n branch [4.16][4.17]. However, realizing a linear multi-bit DAC then requires the implementation of non-

[4] S. Pan and K. A. A. Makinwa, "A 10fJ·K^2 Wheatstone bridge temperature sensor with a tail-resistor-linearized OTA" *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 501-510, Feb. 2021.

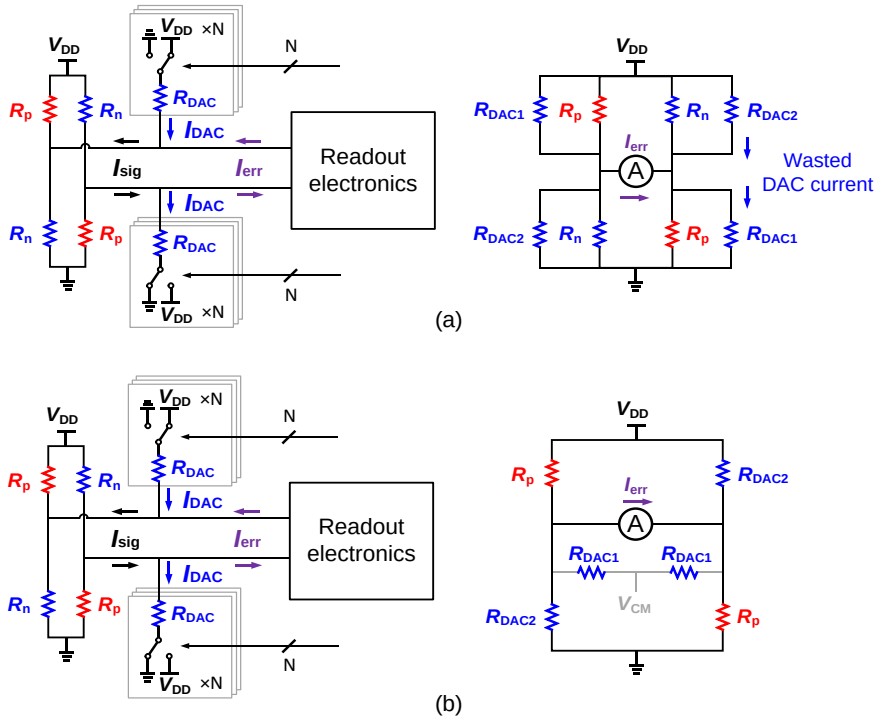


Figure 4.31: (a) Rail-to-rail DAC switching scheme of a Wheatstone bridge sensor, showing how the DAC resistors consume extra supply current. (b) Proposed return-to-CM RDAC made from unit elements.

uniform resistive segments, whose matching cannot be improved by DEM. Alternatively, the unused resistors of a parallel DAC can be switched to the output common-mode voltage of the bridge V_{CM} (=V_{DD}/2). As shown in Figure 4.31 (b), the required V_{CM} can be realized by simply shorting unused DAC pairs together, thus obviating the need for a dedicated voltage reference. Since the voltage drop across the R_{DAC} elements has now been reduced from V_{DD} to V_{DD}/2, their values must be halved to achieve the same DAC currents. For the same (minimum) resistor width, this return-to-CM (RCM) switching scheme also reduces the DAC area by half.

With an appropriately scaled DAC, the proposed RCM switching scheme improves the FoM of the resistive front-end to about 2.2fJ·K^2 at RT. Due to the noise of the unused DAC resistors (R_{DAC1}), this is somewhat more than the theoretical FoM of the bridge itself (1.7fJ·K^2). Although it might be tempting to eliminate their noise contribution by letting the unused resistors float, their parasitic capacitances will then cause slow-settling DAC currents. These, in turn, will cause inter-symbol-interference (ISI) and significantly increase the modulator's in-band noise (IBN).

4.6.1.2 DAC array and DAC range optimization

Rather than implementing the R_n and R_{DAC} arms as separate resistors, they can be implemented as a single array of N unit resistors. To balance the bridge, the modulator must drive the DAC such that, on average, $R_{DAC} = R_p$. If the modulator's bitstream average μ ranges from 0 to N, then μ is given by:

$$\mu = \frac{R_{DAC}(T)}{R_p(T)} = \frac{R_{DAC}(T_0)}{R_p(T_0)} \cdot f(T) \tag{4.3}$$

where T_0 is a reference temperature, $R_p(T_0)$ and $R_{DAC}(T_0)$ are nominal resistances, and $f(T)$ represents the combined temperature dependency of both resistors assuming no TC spread. Compared to equation (4.2), the offset trim is eliminated. This means that any spread in the nominal resistances $R_p(T_0)$ and $R_{DAC}(T_0)$ can be corrected by a 1-point trim. In practice, TC spread is present, and so a 2-point trim is required for better accuracy.

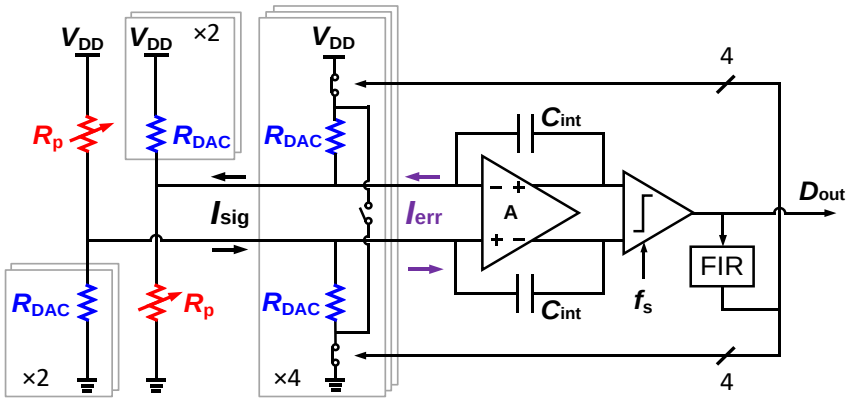


Figure 4.32: FIR-DAC CTΔΣM readout of the WhB temperature sensor after DAC range optimization.

In this work, the number of parallel DAC resistors (N=6) is a trade-off between chip area and energy efficiency: increasing N decreases I_{err}, but requires more area-consuming DAC resistors. To cover the targeted temperature range, only 4 of the 6 unit elements (each 370kΩ) are switched, as shown in Figure 4.32. Thus, the modulator's bitstream average μ ranges from 2 to 6.

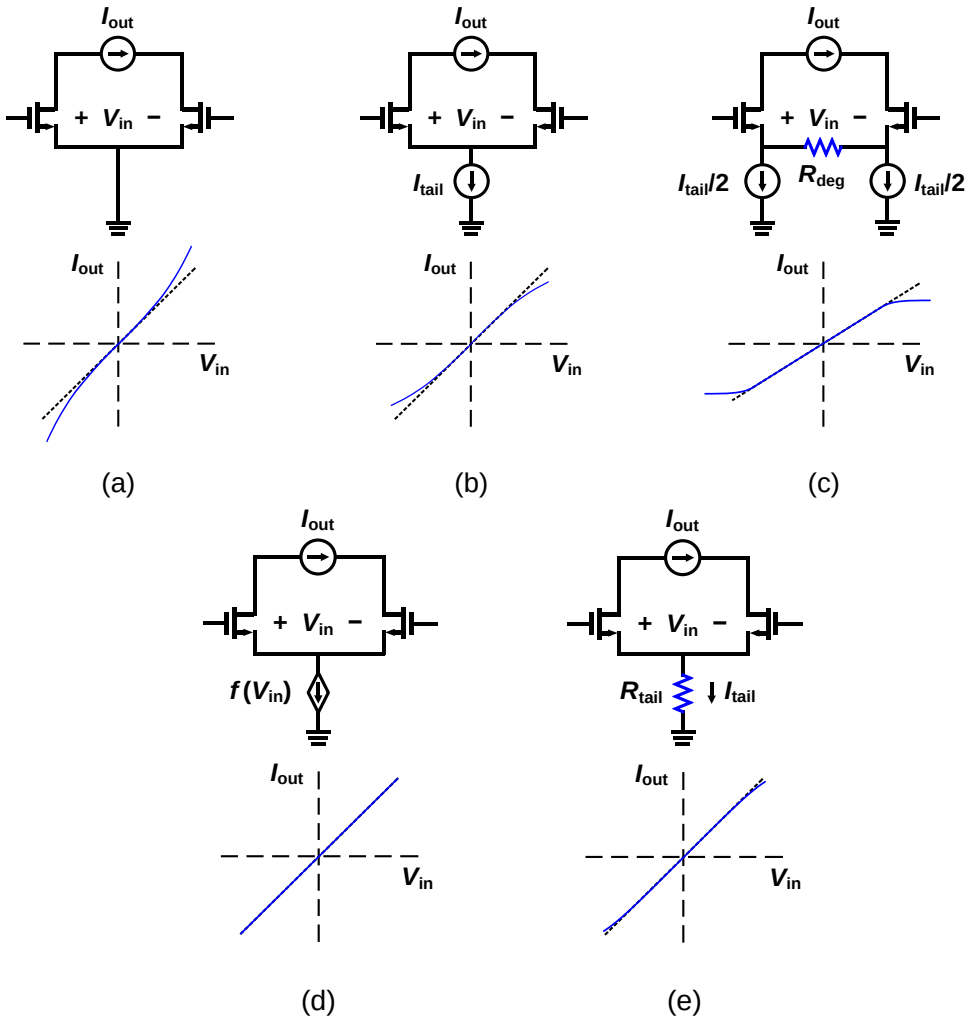


Figure 4.33: Output characteristics for OTAs with (a) zero tail impedance (b) high tail impedance (c) degeneration (d) controlled tail impedance (e) fixed tail impedance.

4.6.1.3 Integrator nonlinearity

As introduced in section 4.5.2, one challenge of the multi-bit DAC is integrator non-linearity and quantization noise fold-back. In the third Wheatstone bridge implementation, the input stage was built around a two-stage opamp, whose high gain keeps its input swing small (< 1mV) and thus mitigates the non-linearity of its input differential pair. However, the power consumed by its output stage then leads to a loss of energy efficiency.

Greater energy efficiency can be achieved by building the 1st integrator around a single-stage OTA, since all its supply current then contributes to lowering its noise. However, for the same level of output current I_{out}, this will result in a significantly larger input swing (tens of mVs) and hence non-linearity [4.18]. In a conventional differential pair, the maximum I_{out} is limited by the tail current, resulting in a compressing V-I nonlinearity (Figure 4.33 (b)). In contrast, an expanding and slightly more linear characteristic can be obtained by employing a pseudo-differential (PD) topology (Figure 4.33 (a)) [4.19]. In both cases, the effect of OTA non-linearity can be mitigated by either increasing the tail current or by resistive degeneration, as shown in Figure 4.33 (c). However, both approaches reduce energy-efficiency. In the next section, a more energy-efficient way of improving OTA linearity will be discussed.

4.6.2 Linearized OTA design

4.6.2.1 Linearization principle

From Figure 4.33 (a) and 4.33 (b), it can be seen that the impedance of the tail current source has a strong influence on OTA non-linearity. As in [4.20], it has been shown that the linearity of an OTA can be extended by making its tail current a non-linear function of its input voltage V_{in} (Figure 4.33 (d)). Although this approach results in excellent linearity, it requires two trimming knobs to compensate for process spread. As also suggested in a concurrent work [4.21], a simpler solution is to replace the tail current source by a tail resistor and then optimize its value for linearity, as shown in Figure 4.33 (e).

For input transistors biased in weak inversion, which therefore have an exponential I-V characteristic, it can be shown (Appendix A.2) that the value of R_{tail} required to cancel the OTA's dominant 3rd-order nonlinearity is given by:

$$R_{tail} = \frac{nU_T}{2I_{tail}}, \tag{4.4}$$

where I_{tail} is the tail current for V_{in}=0, n is a process-dependent slope factor, and $U_T = kT/q$ is the thermal voltage. It should be noted that this technique also works when the input transistors are biased in moderate inversion, e.g., to increase speed. In such cases, however, the required resistor will be somewhat smaller.

4.6.2.2 Biasing generation

Equation (4.4) indicates that for a fixed R_{tail}, the optimal I_{tail} should be proportional to absolute temperature (PTAT). This can easily be achieved by a

conventional constant-gm biasing circuit (Figure 4.34). Assuming that both M1 and M2 are biased in weak inversion with a current density ratio of k_1:1, and that the current mirror ratio between M3 and M5 is 1:k_2, the output reference current can be expressed as:

$$I_{ref} = \frac{nU_T}{R_{bias}} \cdot \ln(k_1) \cdot k_2. \tag{4.5}$$

Assuming a ratio of 1:k_3 between I_{ref} and I_{tail}, and combining (4.4) and (4.5) then results in

$$R_{bias} = 2R_{tail} \cdot \ln(k_1) \cdot k_2 \cdot k_3. \tag{4.6}$$

Since R_{bias} is proportional to R_{tail}, a process and temperature robust biasing scheme can thus be achieved by realizing R_{bias} and R_{tail} as a pair of ratiometrically matched resistors.

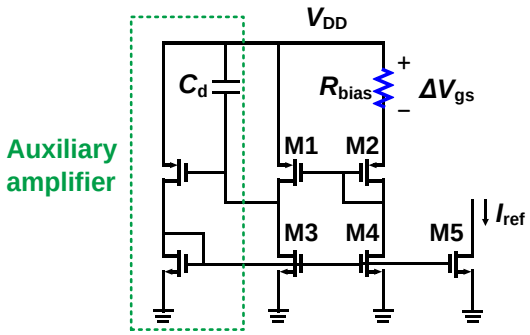


Figure 4.34: Constant-gm biasing generation.

4.6.3.3 Circuit structure

The simplified schematic of the linearized OTA is shown in Figure 4.35. To maximize its energy-efficiency, its supply current is reused by both PMOS and NMOS input pairs. Both pairs are cascoded to achieve high DC gain. For simplicity, a single PMOS-based constant-Gm biasing circuit was used to set the tail currents of both the NMOS and PMOS input transistors via large biasing resistors R_b. The input voltage is capacitively coupled to the gate of the input transistors. To minimize its noise contribution at the chopping frequency, R_b should be made quite large. This large resistance (~1GΩ) is achieved by duty-cycling. As in [4.19], the entire OTA is chopped, allowing it to amplify DC inputs despite its AC-coupled topology. This also suppresses the offset and 1/f noise of the OTA. The use of chopping also improves the OTA's low-frequency CMRR and PSRR, thus alleviating one drawback of eliminating the conventional tail current source [4.21]. A conventional

continuous-time CMFB circuit is used. To facilitate experimental comparison, extra switches (not shown) were included to short all the replicas of R_{tail} shown in Figure 4.35, thus converting the linearized OTA into a PD OTA (Figure 4.33 (a)) with the same bias current.

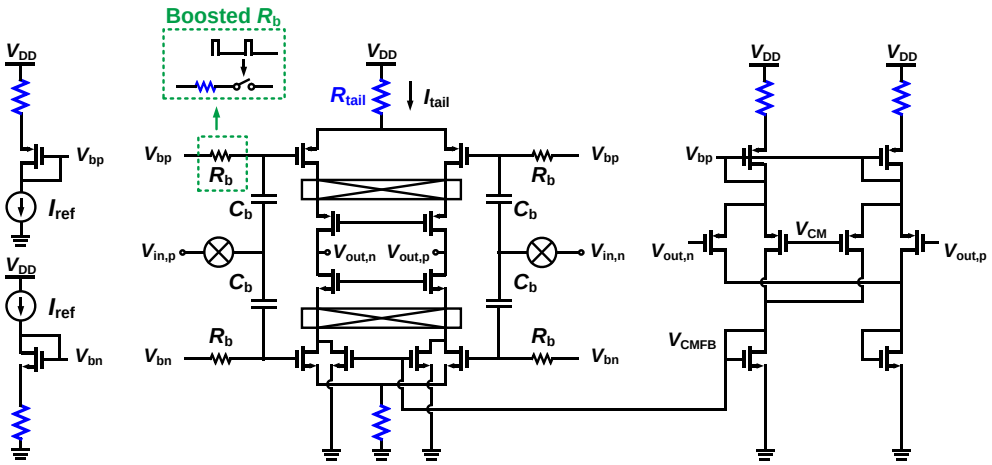


Figure 4.35: Simplified schematic diagram of the linearized OTA, including the biasing generation and CMFB circuit.

4.6.3.4 Nonlinearity simulation results

To verify its performance, the linearity of the proposed OTA was simulated and compared to that of conventional and PD OTAs biased at the same tail current. As shown in Figure 4.36, the use of a tail resistor results in significantly less nonlinearity. Even over process and temperature (−55°C to 125°C), the proposed scheme is quite robust. As shown in Figure 4.37, the worst-case nonlinearity is still 12× better than that of the PD OTA and 40× better than a conventional OTA.

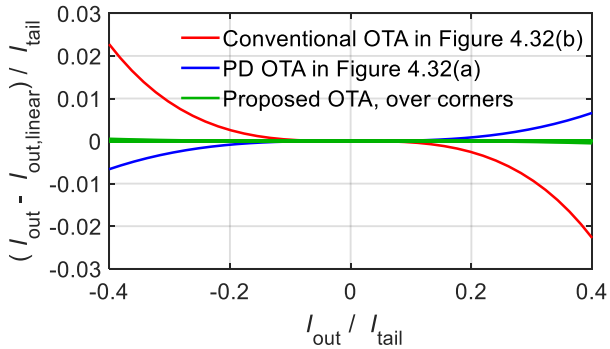


Figure 4.36: Relative nonlinearity with different OTA structures.

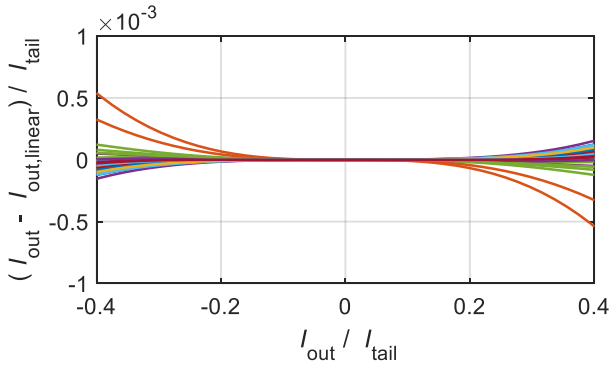


Figure 4.37: Relative nonlinearity of the proposed OTA over corners.

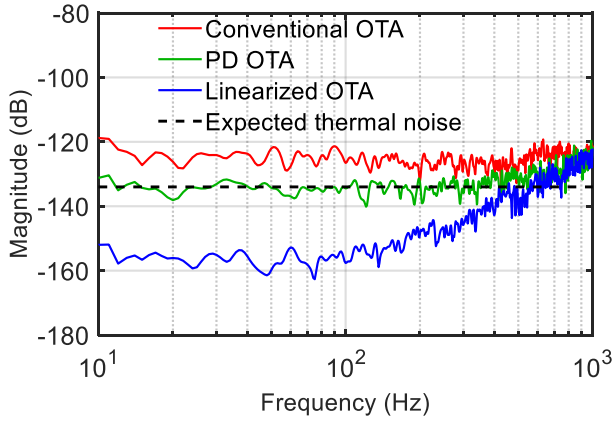


Figure 4.38: Simulated ΔΣM bitstream spectrum without noise using the same I_{tail} but different OTA configurations.

4.6.4.5 Power scaling and system-level simulation

To optimize energy efficiency, the tail current of the OTA used in the 1st stage of the CTΔΣM was set to 7.6μA at RT. The 1st stage then consumes ~9μA, including the biasing and CMFB circuit, while its input-referred noise is ~20nV/√Hz. In comparison, the resistive front-end consumes ~17μA, and its noise level is ~36nV/√Hz. Neglecting the rest of the CTΔΣM, this results in a theoretical FoM of 4.4fJ·K^2.

Figure 4.38 shows the results of system-level simulations to verify the effect of OTA non-linearity on the modulator's in-band noise. With a 4-element FIR-DAC,

the maximum swing of I_{err} at RT is about 1/3 I_{tail}. Due to quantization noise folding, the use of a conventional OTA then results in a noise floor that is about 9dB higher than the expected thermal noise. The improved linearity of a PD OTA reduces quantization noise-folding, and brings this to the same level as the thermal noise. After tail-resistor linearization, however, the sensor becomes truly thermal-noise limited, as the folded quantization noise drops to about 20dB below the thermal noise.

In the third Wheatstone bridge prototype, similar suppression of quantization noise folding is achieved by building the 1st stage around a two-stage opamp. However, for similar input noise and output current levels, this almost doubles the required supply current (~17μA including the biasing and CMFB circuits).

4.6.3 Circuit implementation

Figure 4.39 depicts the block diagram of the proposed temperature sensor. As in previous designs, a 2nd-order ΔΣM was adopted to achieve the required resolution in a reasonable conversion time, and a feedforward architecture was chosen to suppress the swing at the output of the 1st stage, so that the size of C_{int1} (27pF) can be minimized. To further improve area efficiency, C_{int1} is implemented as a high-density metal-insulator-metal (MIM) capacitor, which is placed above the WhB. The CTΔΣM's sampling frequency (f_s) is set to 500kHz, which is derived from an off-chip 2MHz master clock.

The CTΔΣM's 1st stage integrator is based on the tail-resistor linearized OTA introduced in section 4.6.2. A delay-line-based pulse generator operating at $2 \cdot f_{chop}$ is used to duty-cycle R_b with pulses of ~4ns. With $C_b \approx 2$pF and $R_b \approx 700$kΩ, the occupied chip area is quite small (<4×0.002mm^2). Meanwhile, the R_b noise is heavily filtered by C_b, and is suppressed to ~3nV/√Hz at f_{chop}, or ~2% of the OTA's total noise. The OTA achieves an 80dB gain and a unity-gain bandwidth of 18MHz with a 1pF load. To improve its phase response at high frequencies, a zero-cancellation resistor R_z is inserted in series with C_{int}. As shown in Figure 4.25, the quantization-noise folding can be avoided by choosing $f_{chop} = f_s / 4$.

As in the third Wheatstone bridge prototype, the 2nd-stage is implemented as an area-efficient switched-capacitor integrator, with a switched-capacitor FIR-DAC ($C_{FIR,C}$) is inserted to compensate for the delay introduced by the resistive FIR-DAC and stabilize the ΔΣM (Figure 4.39). Compared to the 1st stage, the noise and linearity requirements of the modulator's 2nd stage are much more relaxed, so the 2nd stage employs a conventional current-reuse OTA, whose tail current is scaled to 1μA at RT.

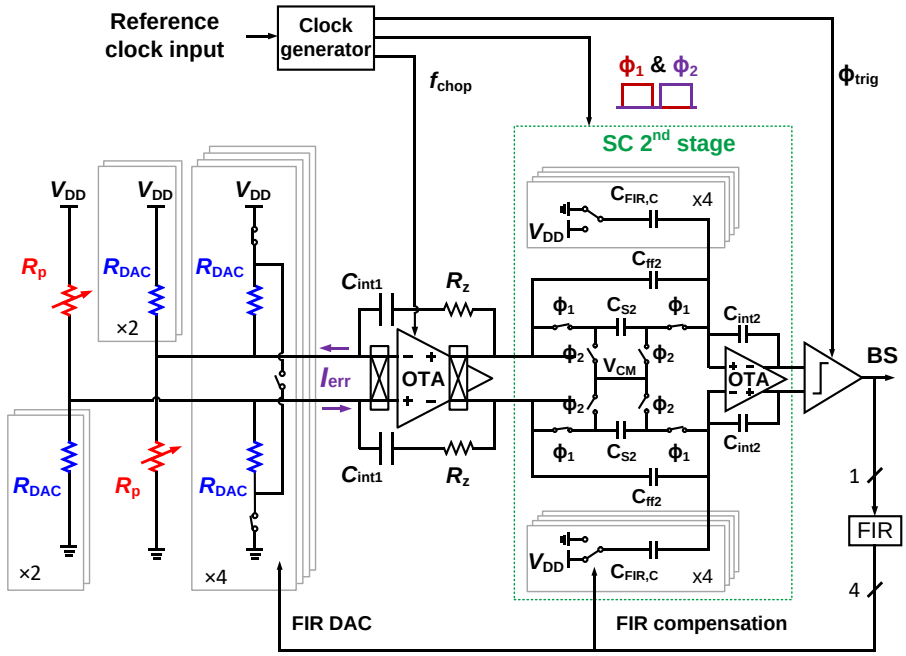


Figure 4.39: Simplified system block diagram.

4.6.4 Measurement results

As shown in Figure 4.40, four WhB temperature sensors were fabricated on the same die in a standard 0.18µm process. Two employ a silicided-p-poly/n-poly WhB (s-poly WhB), while the other two employ a silicided-p-diffusion/n-poly WhB (s-diffusion WhB). This is because the silicided diffusion resistor has ~10% higher TC and almost the same voltage dependency compared to the silicided poly resistor. Implementing pairs of sensors on the same die allows ambient temperature drift to be effectively rejected by differential measurements. Sinc^2 filters, implemented off-chip for flexibility, are used to decimate the sensors' bitstream output.

Each sensor consumes 27.5µA/3µA from a 1.8V analog/ digital power supply, and occupies 0.11mm^2, of which over 50% is occupied by the WhB and the integration capacitors. Four sensors share two clock generation circuits, each occupying 0.003mm^2. For supply voltages varying from 1.4V to 2.0V, both sensors exhibit a supply sensitivity of about 0.04°C/V at RT, which is mainly limited by the voltage-dependent R_{on} of the trimming/DAC switches.

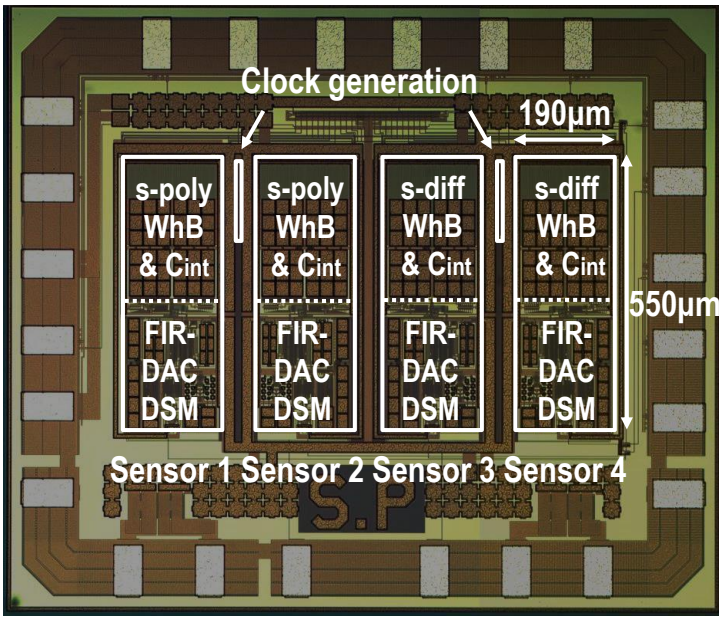


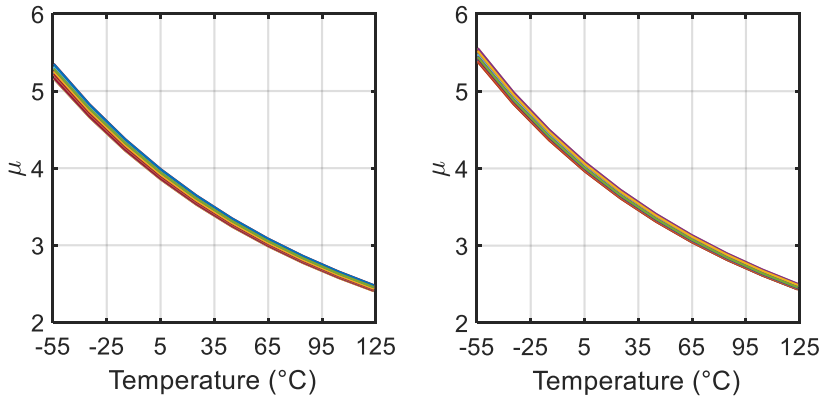
Figure 4.40: Die micrograph of the fabricated chip.

4.6.4.1 Calibration and inaccuracy

After ceramic DIL packaging, 20 samples from one wafer (i.e., 40 sensors of each WhB type) were characterized in a temperature-controlled oven from −55°C to 125°C. To suppress the effects of oven drift, they were mounted in good thermal contact with a large metal block.

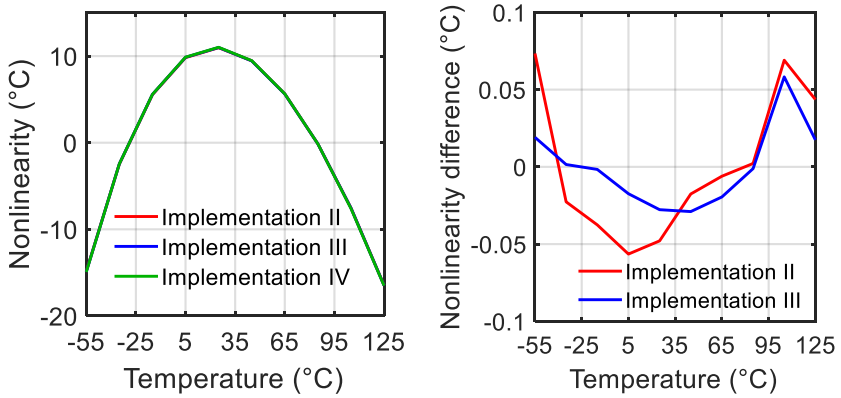
The measured performance of the sensors is shown in Figure 4.40. With the same 3-bit coarse trimming code (011), their spread is about ±3% full scale at RT, or ~7°C peak-to-peak error. This means that the trimming code can be simply set by measurements on a single sensor. As expected, the s-diffusion WhB has a higher (~6%) sensitivity than the s-poly WhB.

After an individual linear fit to compensate for process spread, the sensors exhibit a systematic non-linearity. Compared to the second and third Wheatstone bridge implementations, which used the same type of resistors and had the same operating range, the systematic nonlinearity varies by less than 0.1°C from batch to batch (Figure 4.41), indicating good repeatability.



(a) (b)

Figure 4.41: Bitstream average over temperature of (a) s-poly WhB sensors and (b) s-diffusion WhB sensors before trimming.

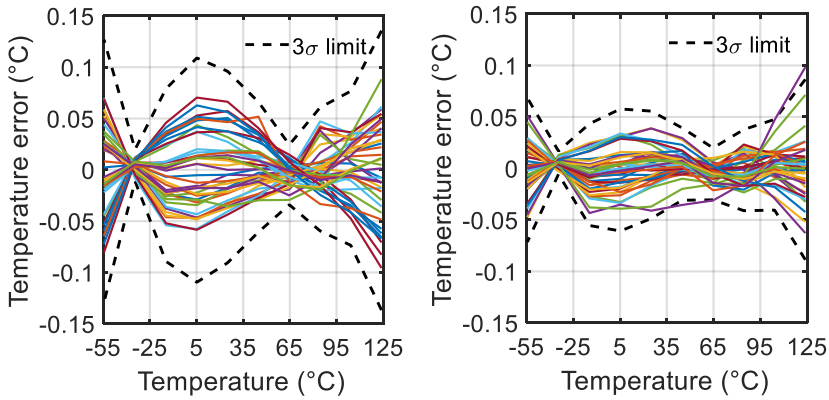


(a) (b)

Figure 4.42: (a) Measured systematic non-linearity of different WhB sensor implementations. (b) Difference compared to that of implementation IV.

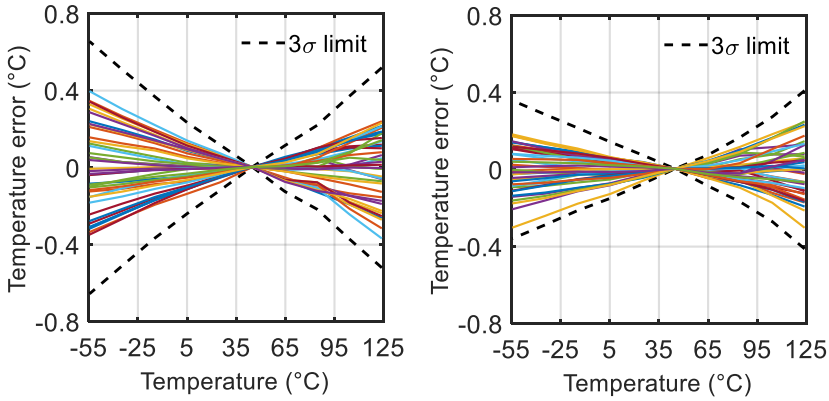
As in previous designs, the systematic non-linearity is removed by a fixed 5th order polynomial. This results in a 3σ spread of 0.15°C for the s-poly bridge, and only 0.1°C for the s-diffusion bridge (Figure 4.43). Similar results were achieved when the individual linear fit is replaced by a simpler 2-point calibration at −35°C and 85°C.

As discussed in section 4.6.1.2, the bitstream average μ is proportional to R_{DAC}/R_p, so that a 1-point gain trim is enough to correct for the spread in their nominal resistances. As shown in Figure 4.44, doing this results in a residual 3σ spread of 0.65°C for the s-poly WhB, and 0.4°C for the s-diffusion WhB.



(a) (b)

Figure 4.43: Residual temperature error of (a) s-poly WhB sensors and (b) s-diffusion WhB sensors after individual 1st-order fit and systematic nonlinearity removal.



(a) (b)

Figure 4.44: Temperature error of (a) s-poly WhB sensors and (b) s-diffusion WhB sensors after 1-point trim and systematic error removal.

Alternatively, a correlation-based 1-point trim, like that introduced in Chapter 3, section 3.3.2.2, can be used to exploit the correlation between the sensor's gain error and offset error. Compared to the simple individual gain trim presented here, correlation-based trimming achieves only slightly (~10%) better accuracy, at the expense of the batch calibration needed to determine the correlation coefficients.

4.6.4.2 Resolution and FoM

Bitstream spectra (20s interval, Hanning window, 10× averaging) of the ΔΣ-ADC's bitstream output are shown in Figure 4.45, where 0dB corresponds to an amplitude of 1 in the bitstream average μ (ranges from 2 to 6). Configuring the 1st stage OTA as a PD OTA results in a 3-dB increase in the modulator's noise floor, which agrees with the simulation results shown in Figure 4.38. As in previous designs, the residual 1/*f* noise is mainly due to the non-silicided resistors.

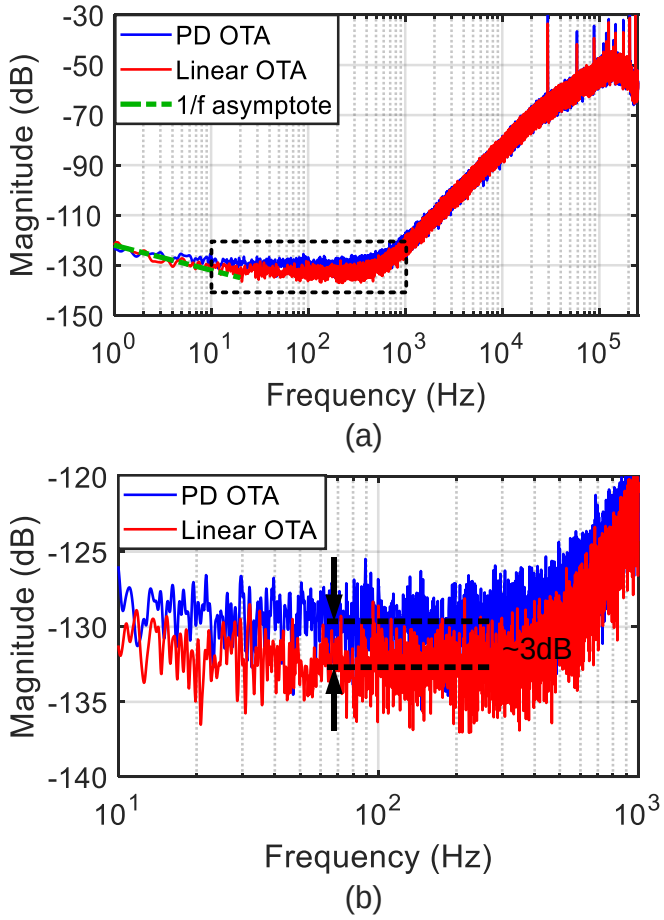


Figure 4.45: (a) Bitstream spectra of the sensor with different OTA configurations (10M samples, Hanning window, 10× averaging) and (b) a zoomed-in plot from 10Hz to 1kHz.

The sensor's resolution is derived via differential measurements, i.e., from the standard deviation of the difference in the output of two identical sensors on the same die. As shown in Figure 4.46, with standard deviations computed from

bitstream data acquired in a 1s interval, the s-poly WhB sensor's resolution is estimated to be 160μK_{rms} in an 8ms conversion time (T_{conv}). Due to its slightly higher sensitivity, the s-diffusion WhB sensor achieves 150μK_{rms} in the same T_{conv}. With a 55μW sensor power, the derived resolution FoMs of s-poly and s-diffusion WhBs are 11fJ·K^2 and 10fJ·K^2, respectively.

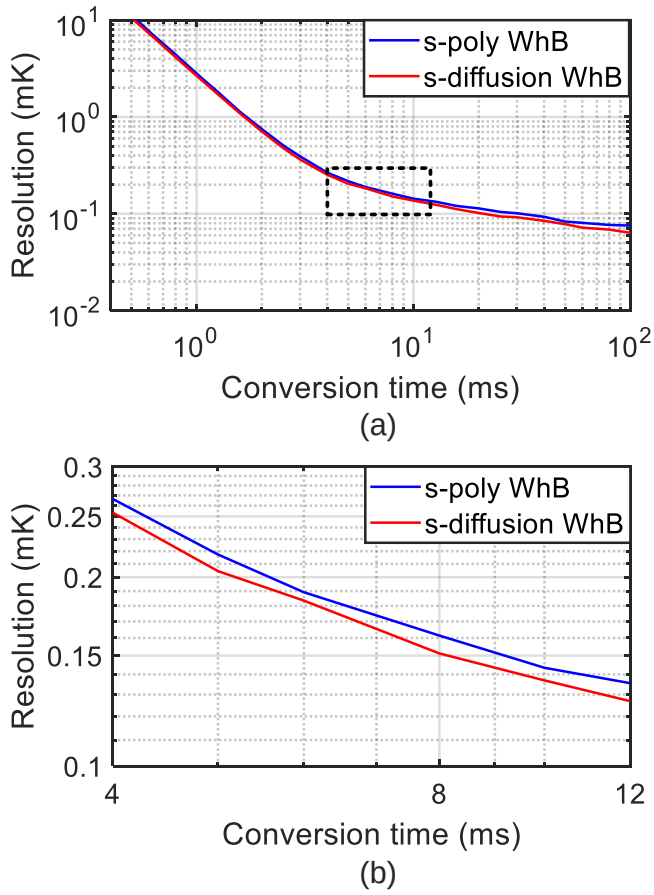


Figure 4.46: (a) Sensor resolution based on bitstream data acquired over a 1s interval and (b) a zoomed-in plot from 4ms to 12ms.

4.6.4.3 Comparison to implementation III

Compared to the third prototype, the fourth implementation achieves a 30% better inaccuracy despite occupying less chip area. It also achieves a 2× better energy efficiency, and its resolution FoM (10fJ·K^2) is close to the practical FoM limit of ~7fJ·K^2.

4.7 Comparison and concluding remarks

In this chapter, four Wheatstone-bridge-based temperature sensor prototypes were demonstrated, as summarized in Table 4.1. All the sensors use a 2nd-order CTΔΣ-ADC to directly digitize the temperature-dependent current output of a Wheatstone bridge. By systematically improving each design, their energy efficiency is dramatically enhanced, as can be seen from their FoM: ranging from 65fJ·K^2 (implementation I) to 10fJ·K^2 (implementation IV). At the end of this research (2020), implementation IV achieves the best energy-efficiency and relative inaccuracy among all Wheatstone bridge (dual-R) temperature sensors.

Table 4.1: Performance summary of the Wheatstone bridge implementations and comparison with the prior art.

	JSSC'15 [4.5]	Implementation I	Implementation II	Implementation III	Implementation IV
Sensor type	Resistor WhB	Resistor WhB	Resistor WhB	Resistor WhB	Resistor WhB
Technology	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm
Area [mm^2]	0.43	0.72	0.25	0.12	0.11
Temp. Range [°C]	−40─125	−40─85	−55─125	−55─125	−55─125
3σ Inaccuracy [°C] (trimming points)	0.4[a] (2[b])	0.1 (2[c])	0.12 (2[c])	0.14 (2[c])	0.1 (2[c])
Relative inaccuracy	0.48%	0.16%	0.13%	0.16%	0.11%
Power [μW]	65	180	94	79	55
Conv. time [ms]	0.1	10	5	10	8
Resolution [mK]	10	0.19	0.29	0.16	0.15
Res. FoM [fJ·K^2]	650	64	40	20	10

[a] Min/Max. [b] 1-point trim + 1st-order fit. [c] 1st-order fit

4.8 References

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[4.19] B. Gönen et al., " A continuous-time zoom ADC for low-power audio applications," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 1023-1031, April 2020.

[4.20] R. Sehgal et al., "A 13-mW 64-dB SNDR 280-MS/s pipelined ADC using linearized integrating amplifiers," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1878-1888, July 2018.

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Chapter 5

Application-driven designs

5.1 Introduction

In Chapters 3 and 4, WB- and WhB-based temperature sensors intended for the temperature compensation of MEMS/crystal frequency references were presented. However, this is only one of the many possible applications of resistor-based temperature sensors. In this chapter, two sensors intended for other applications are presented: one intended for biomedical applications, and the other intended for use as a building block in a RC frequency reference.

5.2 A low-power sensor for biomedical applications[1]

5.2.1 Background introduction

In wearable/implantable biomedical applications, body temperature (~37.5°C) must often be measured accurately, e.g. with errors less than 0.1°C from 39.0°C to 41.0°C, and less than 0.2°C from 35.8°C to 41.0°C [5.1]. This requires temperature sensors with sufficient resolution (< 40mK) in a short conversion time (< 100ms) to facilitate rapid, and thus low cost, calibration. Furthermore, since biomedical devices are typically powered by small thin-film batteries, their sensors should also have high energy efficiency and low power dissipation. Last but not the least, such sensors should be robust to supply and clock reference variations, as a stable supply/clock is not always available in biomedical environments.

BJT- or MOS-based temperature sensors are often used in biomedical applications due to their low power dissipation (< 2μW) and high resolution [5.2]- [5.4]. Although Wheatstone bridge sensors achieve state-of-the-art energy efficiency (Chapter 4), they typically dissipate more power (> 50μW) and are quite non-linear, requiring a complex digital backend to perform polynomial linearization. Some resistor-based

[1] S. Pan and K. A. A. Makinwa, "A 6.6μW Wheatstone-bridge temperature sensor for biomedical applications," in *IEEE Solid-State Circuits L.*, vol. 3, pp. 334-337, 2020.

sensors [5.5][5.6] dissipate much less power (< 0.1μW), however, they are much less energy-efficient, and their limited resolution (> 300mK) makes them unsuitable for biomedical applications.

This sub-section describes a low-power Wheatstone bridge sensor that meets biomedical requirements, while maintaining high energy efficiency. After a PWM-based 1-point trim, it achieves an inaccuracy of +0.2°C/−0.1°C (3σ) over a ±10°C range centered on 37.5°C. The use of PWM-based trimming obviates the need for a complex digital backend that implements a high-order linearizing polynomial and a correlated gain/offset trim. It is also quite energy efficient, achieving 200μK resolution in a 40ms conversion time while dissipating 6.6μW, which corresponds to a state-of-the-art resolution FoM of 11fJ·K^2. A power-down mode allows its average power to be significantly reduced, by duty-cycling, to ~700nW at 10 conversions/s.

5.2.2 Circuit implementation

5.2.2.1 Wheatstone bridge and series DAC

To maximize its sensitivity, as in Chapter 4, the Wheatstone bridge (WhB) sensor employs resistors with opposite temperature coefficients (TCs): silicided poly resistors (R_p) and n-poly resistors (R_n). Since the bridge dominates both the sensor's area and power dissipation, there is a trade-off between these two important parameters. With $R_n \approx R_p \approx 600k\Omega$, i.e. ~6× more than that in third/fourth WhB sensor implementation in Chapter 4. The bridge consumes ~4.3μW from a 1.6V supply, and occupies 0.06mm^2.

In all the designs presented in Chapter 4, the WhB sensor outputs are digitized by a continuous-time delta-sigma modulator (CTΔΣM) that uses a parallel n-poly DAC (R_{nDAC}) to dynamically balance the bridge (Figure 5.1 (a)). In steady-state, the CTΔΣM's bitstream average μ can be expressed as:

$$\mu = R_{nDAC}/R_n - R_{nDAC}/R_p. \quad (5.1)$$

Since R_{nDAC} and R_n are both n-poly resistors, the first term is a consant. However, since the absolute TC of R_p (0.29%/°C) is larger than that of R_n (−0.15%/°C), the second term is proportional to $1/T$ and is thus rather non-linear. Together with the resistors' higher-order TCs, this results in a non-linearity of ~0.3°C over the desired range (±10°C range around 37.5°C), which would then necessitate the use of polynomial non-linearity correction (Chapter 4).

This non-linearity can be mitigated by realizing the DAC with R_p resistors (Figure 5.1 (b)), in which case, μ can be expressed as:

$$\mu = R_{pDAC}/R_n - R_{pDAC}/R_p \tag{5.2}$$

This reduces the non-linearity to ~0.1°C over the same temperature range, thus obviating the need for digital linearization.

Since the desired temperature range is small (20°C), the resistance change in the Rn branch will also be small, and a large parallel resistor ($R_{pDAC} \approx 18 \cdot R_p$) is required to balance the bridge. To save area, a series DAC is used [5.7], which requires a much smaller ($R_{pDAC} \approx R_p/18$) resistor (Figure 5.1 (b), middle).

In this case, μ can be expressed as:

$$\mu = (2k+1) - (2k+2) \cdot R_p/R_n. \tag{5.3}$$

where $k = R_p/R_{pDAC}$. As in (5.2), its non-linearity is also determined by the R_{pDAC}/R_n and so remains the same.

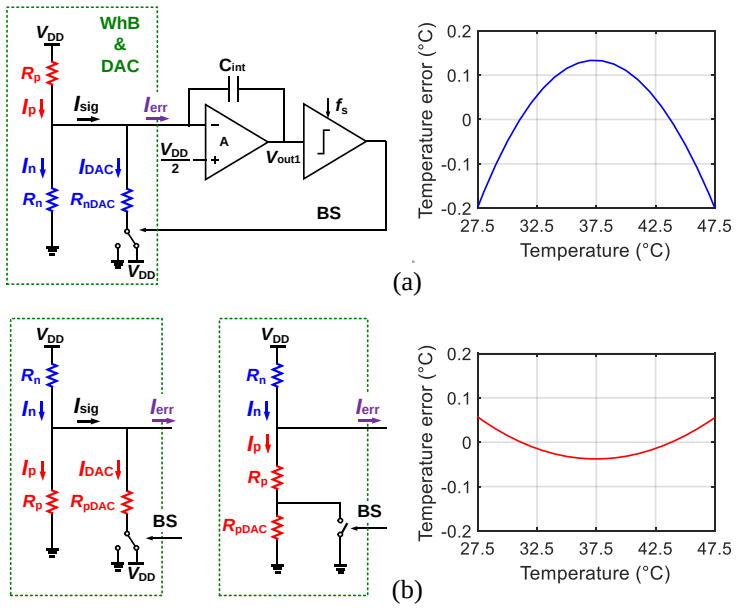


Figure 5.1: Simulated non-linearity of a Wheatstone bridge (WhB) sensor with (a) a parallel R_n DAC, and (b) with a parallel/series R_p DAC.

5.2.2.2 PWM-assisted trim

To compensate for process spread, the R_p/R_n ratio can be adjusted by trimming the R_n branch. However, compensating for the worst-case process spread (±40%) and achieving sufficient trimming resolution (< 0.05°C) requires a 12-bit trim DAC. To save area, this is implemented by combining a 5-bit resistor DAC (~15kΩ/step) with

a 7-bit PWM DAC. The former ensures efficient use of the modulator's dynamic range, while the latter provides sufficient resolution. As shown in Fig. 2, the resistor DAC is implemented with 31 series resistors, and the PWM trim is implemented by duty-cycling an extra series resistor at $F_{PWM} = F_S/128$, where F_S (=32kHz) is the sampling frequency of the modulator. To ensure a constant switch on-resistance, a dummy switch controlled by the inverse of the PWM signal (!PWM) is added in series with the duty-cycled resistor. Although quite area-efficient, the PWM trim adds a small AC component to the output current of the bridge I_{err}, which uses up ~20% of the modulator's input dynamic range.

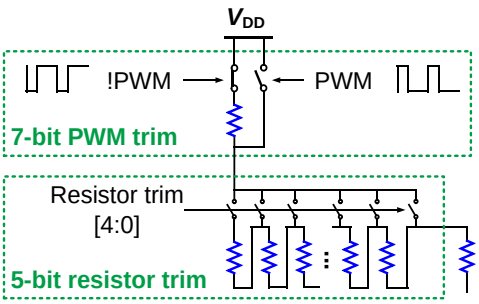


Figure 5.2: Hybrid R_n trim based on resistor segmentation and PWM.

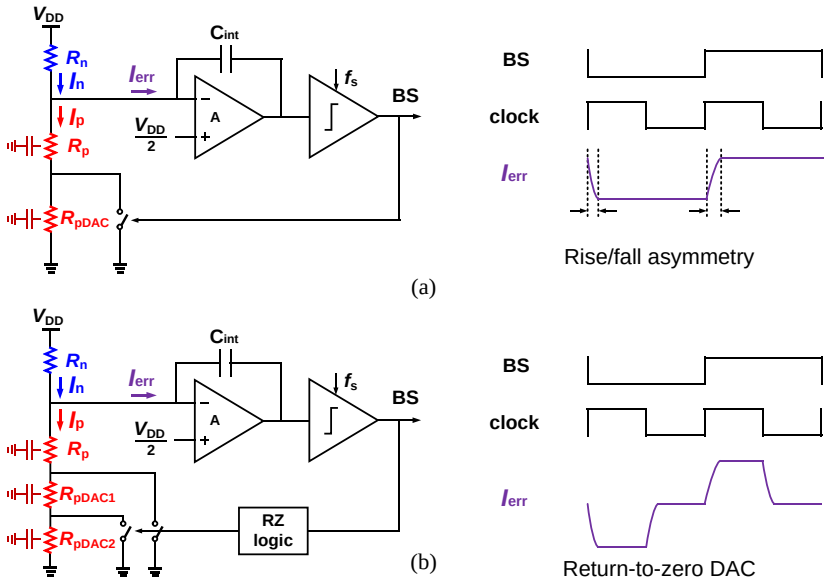


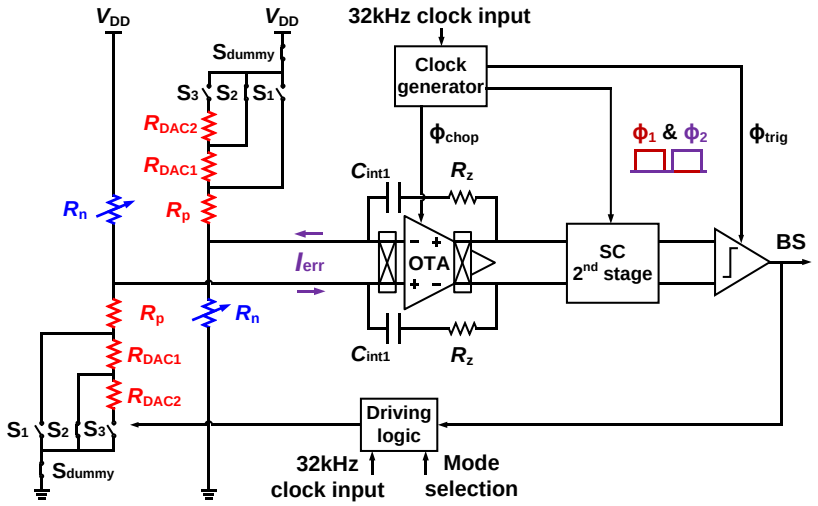
Figure 5.3: (a) Rise/fall asymmetry when using a non-return-to-zero DAC. (b) Return-to-zero (RZ) DAC achieved by splitting R_{pDAC}.

5.2.2.3 Return-to-zero DAC and DSM readout

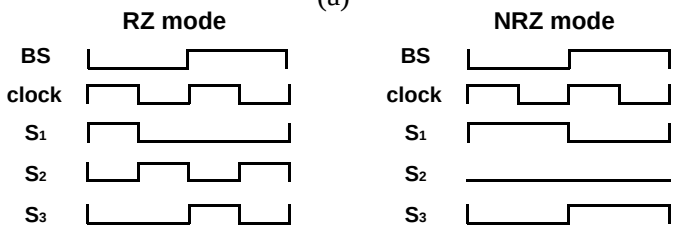
One drawback of a series R_p DAC is that it modulates the resistance of the R_p branches. Due to their parasitic capacitances, the resulting rise/fall times of I_{err} (~0.5µs) are quite significant when compared to the clock period (31.25µs). Using non-return-to-zero (NRZ) DAC pulses will then cause inter-symbol-interference (ISI), and degrade the modulator's noise floor. To mitigate this, a return-to-zero (RZ) DAC is implemented by splitting R_{pDAC} in two and returning to the resulting middle level after a half clock period, as shown in Figure 5.3 (b).

To improve the sensor's supply sensitivity, dummy switches (S_{dummy}) are also inserted in series with the DAC switches (S_1-S_3), so that there are always two series switches in both WhB branches, which cancels the effect of the voltage dependency of switch on-resistance.

The sensor's system block diagram is shown in Figure 5.4 (a). To achieve high resolution, the bridge is read out by a 2nd-order DSM. As in the 2nd Wheatstone bridge implementation (Chapter 4, section 4.4), the 1st stage is built around a current-reuse



(a)



(b)

Figure 5.4: (a) Simplified sensor block diagram. (b) DAC switching scheme under RZ or NRZ mode.

OTA, which employs high threshold voltage (high-V_T) input transistors to maximize its output range, and chopping to suppress its 1/f noise. The 2nd stage employs another current-reuse OTA and an area-efficient switched-capacitor filter.

Two extra operating modes have also been implemented. First, to test the effectiveness of the RZ DAC, a NRZ DAC can be implemented by modifying the timing of the signals that drive S_1-S_3, as shown in Figure 5.4 (b). Second, to implement a power-down mode, the WhB is disconnected from the supply by turning S_{dummy} off. The amplifiers are also switched off by shorting the gates of their PMOS/NMOS tail-current sources to V_{DD}/Gnd. For fast start-up, capacitors pre-charged to Gnd/V_{DD} can be used to restore their gate voltages within one clock cycle [5.6].

5.2.3 Measurement results

As shown in Figure 5.5, two sensors are fabricated on the same die in a standard 0.18µm CMOS process, allowing ambient temperature drift to be cancelled by differential measurements. They share the same clock/PWM generation circuit (0.003mm^2), and for flexibility, their decimation filters (sinc^2) are off-chip. The large 1st stage integration capacitors C_{int1} (MIM, 40pF) are located above the WhB (0.072mm^2), while the trimming circuits occupy 0.007mm^2. At F_S = 32kHz, each sensor consumes 6.6µW (4.2µW bridge, 2.1µW analog and 0.3µW digital) from a 1.6V supply, and occupies 0.12mm^2.

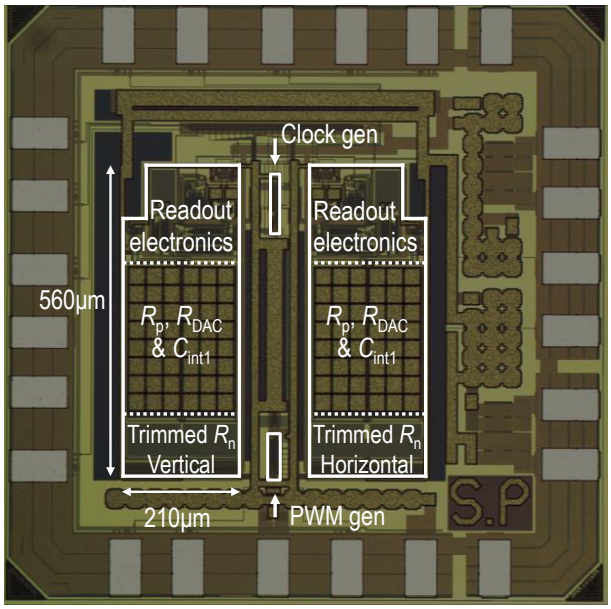


Figure 5.5: Die photo of the fabricated chip.

5.2.3.1 Calibration and inaccuracy

The sensors (21 ceramic-packaged samples from one wafer) were characterized from 27.5°C to 47.5°C in a temperature-controlled oven. Without trimming, the sensor's inaccuracy is about 10°C. After a 5-bit resistor trim at 37.5°C, the residual spread relative to a linear master curve is about ±2.5°C (Figure 5.6 (a)). This can be reduced to ±0.25°C (3σ) by applying a digital offset trim (Figure 5.6 (b)).

As indicated by (5.3), some of the remaining spread is caused by the residual error in the ratio R_p/R_n, which causes sensitivity variations that cannot be eliminated by the aforementioned offset trim. By trimming R_p/R_n (5-bit resistor trim + 7-bit PWM trim), this error is greatly suppressed, as shown in Figure 5.6 (c). Despite the residual trimming error at 37.5°C, the residual spread is then below +0.2°C/−0.1°C (3σ) without any additional post-processing (Figure 5.6 (d)).

To investigate the effects of packaging stress, 14 plastic-packaged chips from the same wafer were also characterized. This causes a systematic sensitivity error and increased spread. Using the linear master curve obtained from the ceramic-packaged chips results in +0.25/−0.1°C (3σ), as shown in Figure 5.7.

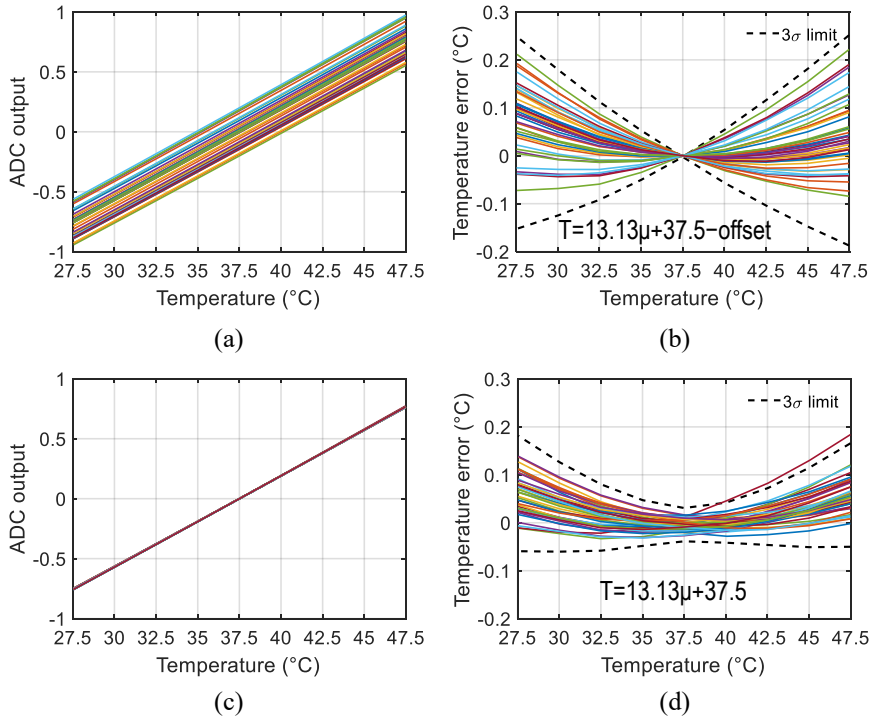
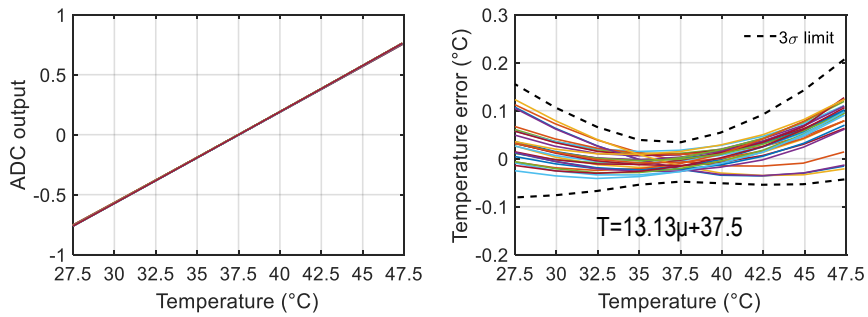
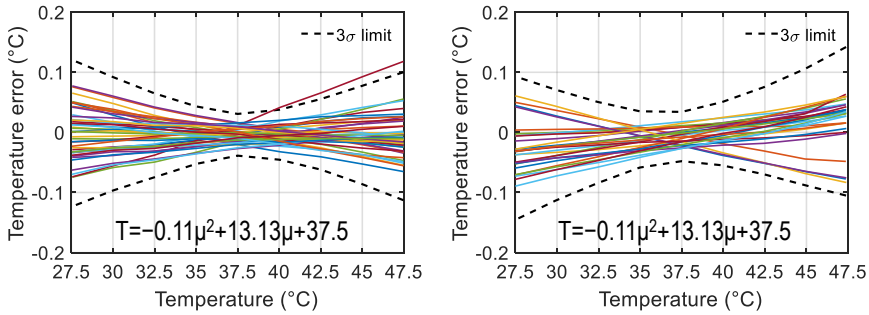


Figure 5.6: (a) Measured output of the ceramic-packaged sensors after resistor trim. (b) Inaccuracy after digital offset trim. (c) Measured output after PWM trim. (d) Inaccuracy after PWM trim without post-processing.



(a) (b)

Figure 5.7: (a) Measured output of plastic-packaged sensors after PWM trim. (b) Inaccuracy after PWM trim.



(a) (b)

Figure 5.8: Temperature inaccuracy with a quadratic master curve of (a) ceramic-packaged sensors (b) plastic-packaged sensors.

Even better accuracy can be achieved by using a quadratic master curve at the expense of a more complex digital backend. This results in a residual spread of below ±0.15°C (3σ) for both ceramic- and plastic-packaged sensors, as shown in Figure 5.8.

5.2.3.2 Resolution and FoM

FFTs of the sensor's bitstream (BS) outputs are shown in Figure 5.9. As expected, the use of an NRZ DAC instead of a RZ DAC significantly degrades the modulator's noise floor (by 9dB). Although PWM trimming does not impact the sensor's noise floor, it does introduce strong high-frequency tones. By limiting the conversion time (T_{conv}) to multiples of 8ms, these tones can be completely filtered out by the notches of the sinc^2 decimation filter. For T_{conv} = 8ms/40ms, the sensor achieves 1.1mK/200μK (rms) resolution (Figure 5.10), corresponding to resolution FoMs of 65fJ·K^2/11fJ·K^2.

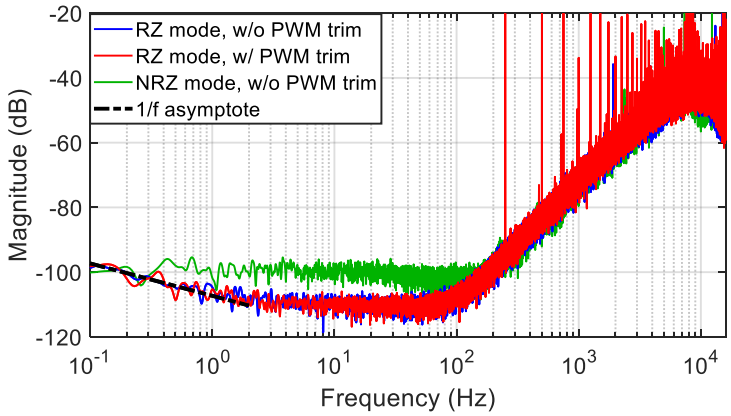


Figure 5.9: Measured bitstream (BS) spectra with different settings.

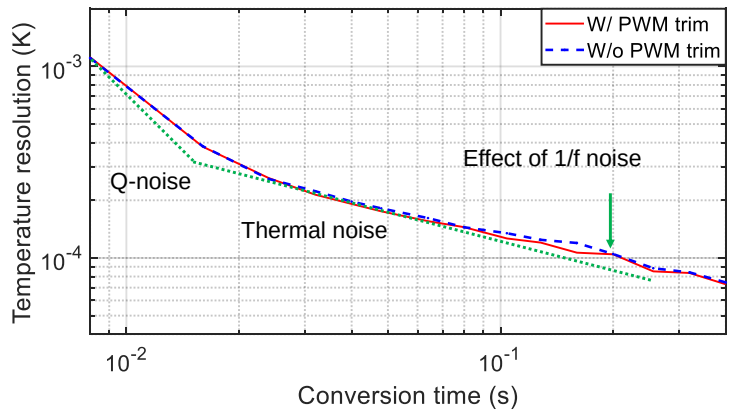
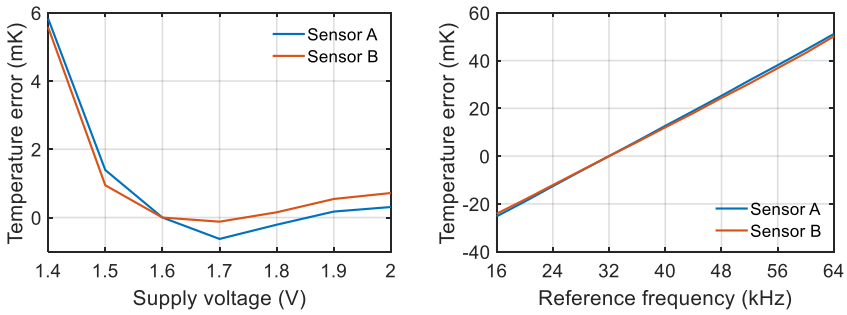


Figure 5.10: Measured bitstream (BS) spectra with different settings.

5.2.3.3 Supply and clock sensitivity

As shown in Figure 5.11 (a), the sensor achieves a power-supply sensitivity of only 4mK/V from 1.5V to 2V at 37.5°C (box method), which is the lowest ever reported for a temperature sensor. Its output is also robust to both input clock inaccuracy (1.6mK/kHz) and clock jitter (< 10% worse resolution with 2.2ns cycle-to-cycle jitter), as shown in Figure 5.11 (b). This makes the sensor well suited for use in wearable/implantable devices which often lack stable power supplies or well-defined clocks.



(a) (b)

Figure 5.11: (a) Supply sensitivity and (b) clock frequency sensitivity of two sensors on the same chip.

5.2.3.4 Power-down mode

In power-down mode, the sensor only draws 125nA at 37.5°C. As shown in Figure 5.12, the sensor starts up within 2 clock cycles (62.5µs) of the rising edge of the power-on signal, thus facilitating efficient duty-cycling. At 10 conversions/s and T_{conv} = 8ms, it dissipates an average power of only ~700nW.

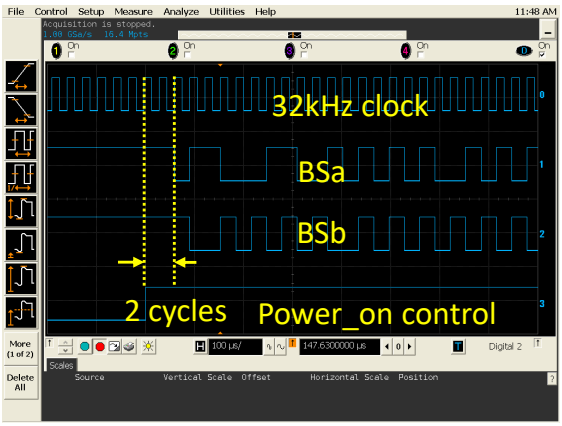


Figure 5.12: Measured BS outputs of a chip around the rising edge of power-on control.

5.2.3.5 Comparison to previous work

Table 5.1 summarizes the performance of the proposed temperature sensor and compares it with the prior-art. Compared to previous low power designs [5.2]-[5.6], it achieves much higher resolution and a state-of-the-art resolution FoM. Moreover, the use of on-chip trimming means that, apart from a decimation filter, no further

Table 5.1: Performance summary of the proposed sensor and comparison with the prior art.

	[5.2]	[5.3]	[5.4]	[5.5]	[5.6]	**This work**	
Sensor type	BJT	MOS	DTMOS	Resistor	Resistor	**Resistor**	
CMOS Technology [nm]	180	350	160	180	65	**180**	
Area [mm^2]	0.198	0.084	0.085	0.09	0.084	**0.12**	
Temperature range	25°C to 45°C	35°C to 45°C	-40°C to 125°C	-0°C to 100°C	-10°C to 120°C	**27.5°C to 47.5°C**	
3σ inaccuracy [°C] (trimming points)	±0.2 (1)	±0.1 [a] (2)	±0.4 (1)	+1.5/-1.4 [a] (2)	+0.34/-0.29 [a] (2)	**+0.2/-0.1 (1)**	
Number of samples	20	3	16	18	10	**42**	
On-chip trim	No	No	No	No	No	**Yes**	
Supply voltage (V)	1.0 & 1.8	1.4 & 2.1	0.85	1.2	0.6 & 1	**1.6**	
Supply sensitivity (°C/V)	N.A.	0.3	0.45	14	1.0	**0.004**	
Power consumption [µW]	1.1	0.11	0.6	0.071	0.000346	**6.6**	
Conversion time [ms]	500	100	6	30	1000	**8**	**40**
Resolution [mK]	10	35	63	300	380	**1.1**	**0.20**
Resolution FoM [$pJ \cdot K^2$]	55	13	14.1	190	50	**0.064**	**0.011**

[a] Min or max

digital hardware, e.g. for polynomial linearization or correlated trimming, is required. In contrast, after an offset trim, the measured inaccuracy of the sensor presented in Chapter 4, section 4.6 is limited by nonlinearity and sensitivity variations, and is about −0.6°C/+0.2°C (3σ) over the same temperature range.

5.2.4 Summary

A compact low-power resistor-based temperature sensor for biomedical purposes has been implemented in a standard 0.18µm technology. It is built around a high resistance (600kΩ) Wheatstone bridge that is read out in a self-balanced manner by a continuous-time delta-sigma modulator. An appropriately designed 1-bit series DAC improves both sensor nonlinearity and chip area, while a PWM-based trim reduces sensor spread and greatly simplifies its digital backend. The sensor occupies $0.12mm^2$ and consumes only 6.6µW from a 1.6V supply. Additionally, it achieves a resolution FoM of $11fJ \cdot K^2$ and an inaccuracy of +0.2°C/−0.1°C (3σ) in a ±10°C range around body temperature. These results demonstrate that the proposed sensor can serve as an energy-efficient replacement for BJT- or MOS- based temperature sensors in biomedical applications.

5.3 A Wheatstone bridge sensor embedded in a RC frequency reference[2]

5.3.1 Background introduction

In order to reduce the volume and cost of generating a system clock, MEMS/BAW based frequency references are widely used. An even better alternative would be the use of fully integrated CMOS-compatible frequency references. Depending on the time constant choices, these can be roughly categorized into three groups: LC oscillators [5.9][5.10], thermal-diffusivity-based oscillators [5.11][5.12], and RC oscillators [5.13][5.14].

LC oscillators, since they are based on lithographically defined components, can achieve sub-100-ppm inaccuracy over the industrial temperature range from −40°C to 85°C [5.9][5.10]. However, due to the frequency-dependent Q-factor of their on-chip inductors, such oscillators typically operate at GHz frequencies, and thus require mWs of power. Thermal-diffusivity-based oscillators can achieve an inaccuracy of ~300ppm after proper compensation [5.11], and can operate at a much lower frequency (~10MHz). However, they require on-chip heaters to generate thermal signals, which also consumes several mWs.

RC-based oscillators dissipate much less power. Due to the large TCs of on-chip resistors (usually >100ppm/°C), well-designed compensation is required to suppress the frequency error. In conventional designs, a rough 1st-order TC compensation can be achieved by combining resistors of positive/negative TCs in the analog domain [5.13][5.14]. However, the high-order TCs will remain, which limits the achievable frequency inaccuracy.

Alternatively, the compensation can be achieved by digital temperature compensation after digitizing the RC time constant. Thus, an on-chip temperature sensor is required to provide a compensating polynomial. The minimum frequency error is then partially limited by the temperature sensor's inaccuracy.

This sub-section describes a Wheatstone bridge temperature sensor embedded in such an RC frequency reference. To save chip area and power, a single ADC is multiplexed between the readout of RC filter and that of a Wheatstone sensor. Furthermore, the non-silicided poly resistors in the RC filter and the Wheatstone bridge are shared, resulting in better accuracy since the spread of these resistors will then be correlated and so will partially cancel each other out. The frequency reference

[2] H. Jiang, S. Pan, Ç. Gürleyük and K. A. A. Makinwa, "A 0.14mm^2 16MHz CMOS RC frequency reference with a 1-point trimmed inaccuracy of ±400ppm from −45°C to 85°C," in *IEEE ISSCC Dig. Tech. Papers*., Feb. 2021, pp. 436-437.

is realized in a standard 0.18µm technology, and occupies only 0.142mm^2. After a single-point trim, the 16MHz frequency reference achieves an inaccuracy of ±400ppm from −45°C to 85°C.

5.3.2 Circuit implementation

5.3.2.1 Circuit principle

The basic principle of the digitally compensated RC frequency reference is shown in Figure 5.13 [5.15]. It consists of a frequency-locked loop (FLL), which locks the frequency f_{DCO} of a digitally controlled oscillator (DCO) to the phase shift of an RC filter. The temperature dependence of the RC filter is digitally compensated by the information provided by a temperature sensor. To relax its accuracy requirements, the temperature coefficient (TC) of the RC filter should be minimized. In this work, it is implemented with non-silicided p-poly resistors (TC~−240ppm/°C) and MIM capacitors (TC~−30ppm/°C).

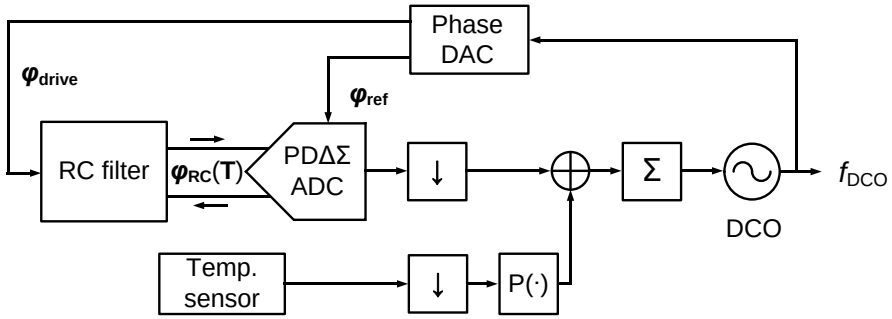


Figure 5.13: Block diagram of a digitally compensated RC frequency reference.

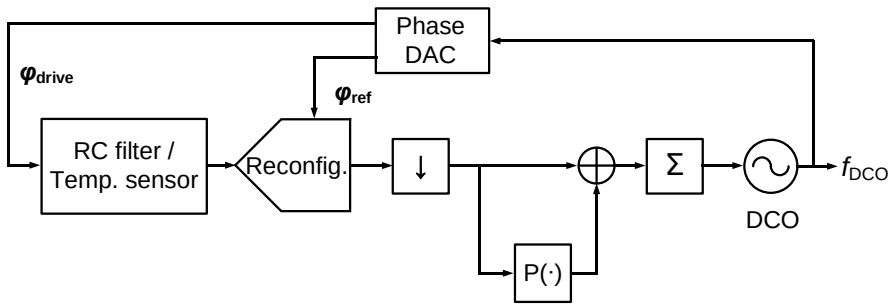


Figure 5.14: Block diagram of the proposed RC frequency reference.

To minimize the impact of resistor/capacitor spread on frequency error, as well as to save circuit area, the temperature sensor is merged with the RC filter. Furthermore, a single reconfigurable ΔΣ-ADC is reused to readout both of them, as shown in Figure 5.14.

5.3.2.2 Reconfigurable RC network and ADC

Figure 5.15 shows the simplified schematic diagram of the reconfigurable RC network and the ADC. It employs a WhB temperature sensor made up of p-poly resistors (R_n, 128kΩ, TC~−240ppm/°C) and silicided-diffusion resistors (R_p, 92kΩ, TC~3000ppm/°C). To reduce area and minimize the number of components that contribute to spread, the RC filter is realized by combining a single MIM capacitor (C_0) with the R_n branches of the WhB. The result is a low-pass filter (LPF) whose phase shift is determined by a single RC time constant. Compared to WBs, whose phase response is determined by the interaction of two different time constants, the use of a LPF is a promising way to achieve better inaccuracy after a 1-point trim. As in [5.15], the output of the WhB sensor and the phase-shift of the LPF exhibit similar non-linearity over the target temperature range (−45°C to 85°C), so that good accuracy can be achieved with a 4th order nonlinearity-correction polynomial. Furthermore, due to the shared p-poly resistors, the effect of their TC spread on the LPF and the WhB is correlated, resulting in a significant reduction in the spread of the temperature-compensated phase-shift of the LPF.

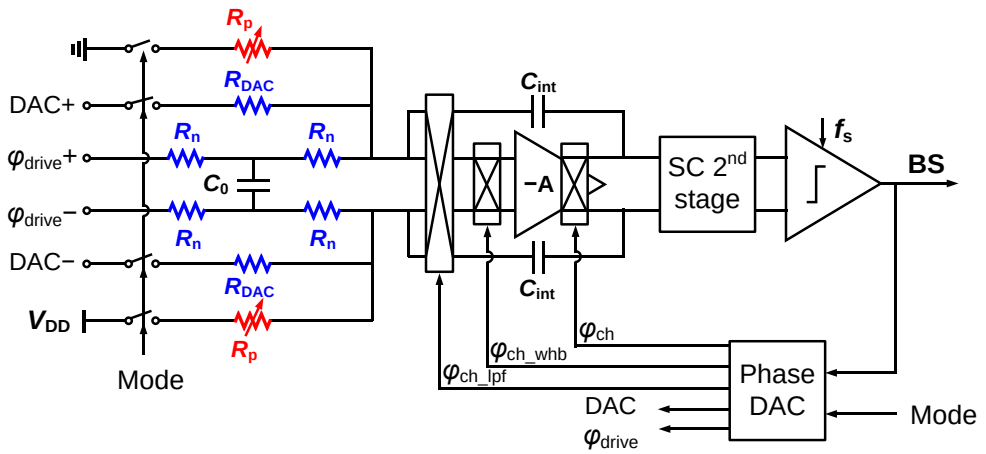
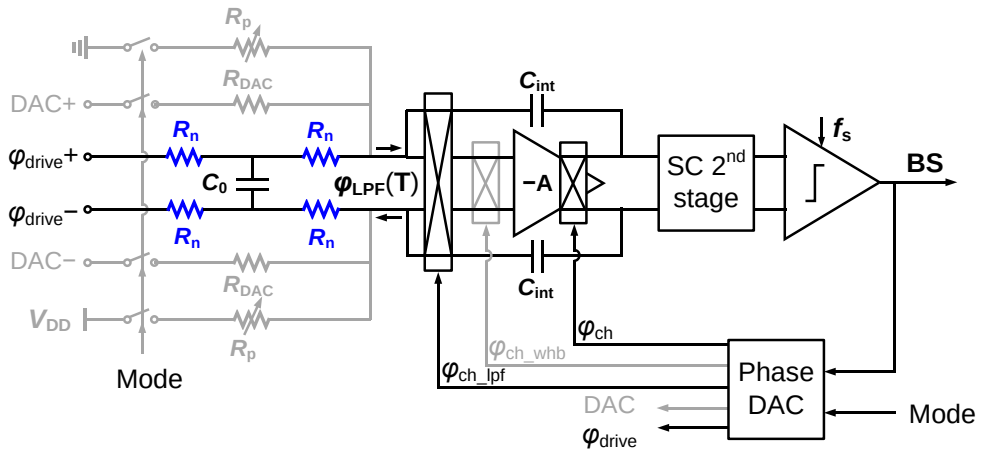


Figure 5.15: Simplified circuits diagram of the LPF/WhB readout circuit.

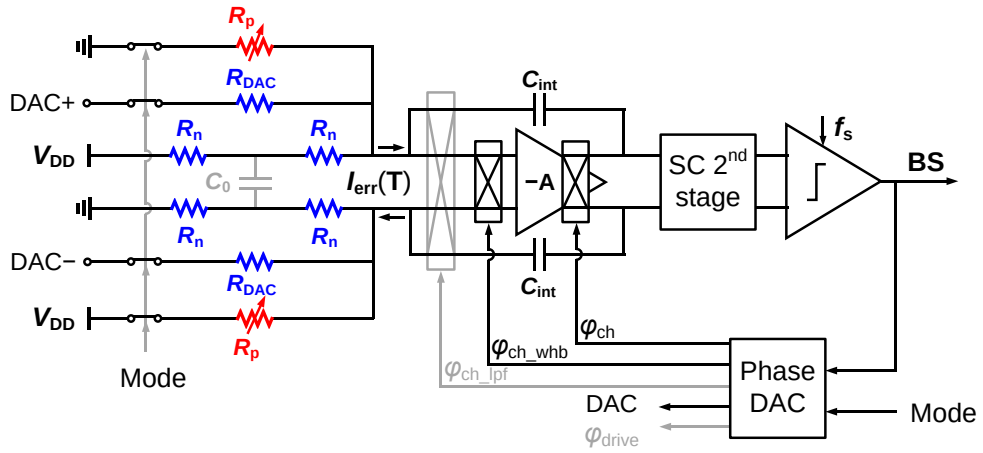
Both the LPF and the WhB are digitized by a feedforward 2nd-order CTΔΣ-ADC, with the 1st stage amplifier chopped at its sampling frequency (f_s). In the LPF mode, both R_p and R_{DAC} are disconnected from the supply, and the LPF is driven by a square wave at $f_{drive} = f_s = 500$kHz, which, after calibration, will be eventually provided by the DCO. By enabling the LPF chopper at the input of the 1st stage amplifier (φ_{ch_lpf})

while disabling that of the WhB (φ_{ch_whb}), the CTΔΣ-ADC is configured to demodulate the phase output of the LPF (Figure 5.16 (a)), like that presented in Chapter 3. To maximize phase sensitivity of the LPF, the phase references for demodulation (φ_{ch} and φ_{ch_lpf}) is set to −45°±5.625° w.r.t φ_{drive}, i.e., nearly orthogonal to the LPF's center frequency.

In the WhB mode (Figure 5.16 (b)), φ_{ch_whb} and φ_{drive} are disabled. The BS output toggles the RDAC switches the same way as introduced Chapter 4. To avoid the extra supply current coming from DAC resistors, the DAC resistors are switched between supply rails and V_{CM} (Chapter 4, section 4.6). Due to the DC operation in the WhB mode, the LPF capacitor (C_0) will not contribute any error.



(a)



(b)

Figure 5.16: Simplified schematic diagram under (a) the LPF mode and (b) the WhB mode.

All the circuit blocks of the reconfigurable ΔΣ-ADC, including the 1st stage amplifier and the switched-capacitor 2nd stage, are reused from the 2nd WB sensor implementation (Chapter 3, section 3.4). The current of the 1st stage amplifier (~8μA) is scaled to efficiently process the maximum current of the resistive front-end. The design of other blocks (polynomial engine and DCO) is beyond the scope of this thesis.

5.3.3 Measurement results

The prototype was fabricated in a standard 0.18μm CMOS process and packaged in ceramic DIL (Figure 5.17). It occupies 0.142mm^2, including ΔΣ-ADC with WhB & LPF, and DCO, while the former takes 88% (0.125 mm^2). However. as the silicided diffusion resistors in the WhB sensor operate at DC, it can be comfortably placed below the 1st stage integrator capacitor of the ΔΣ-ADC and avoid occupying extra area. Also, the p-poly resistors in the WhB is reused by the LPF. As a result, the additional area required by the WhB sensor is negligible. The circuit draws 88μA from a 1.8V voltage supply in the normal operation mode, or 41μA in the WhB readout mode. For flexibility, the digital backend was implemented in an external FPGA.

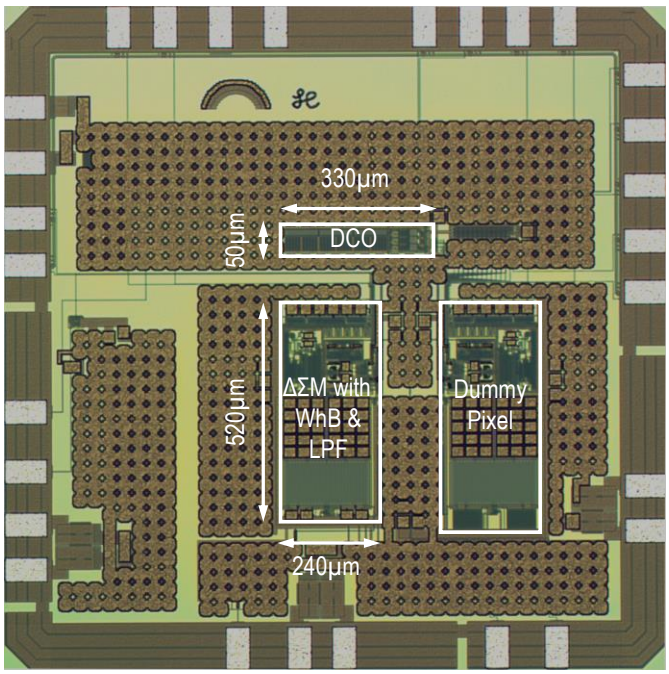
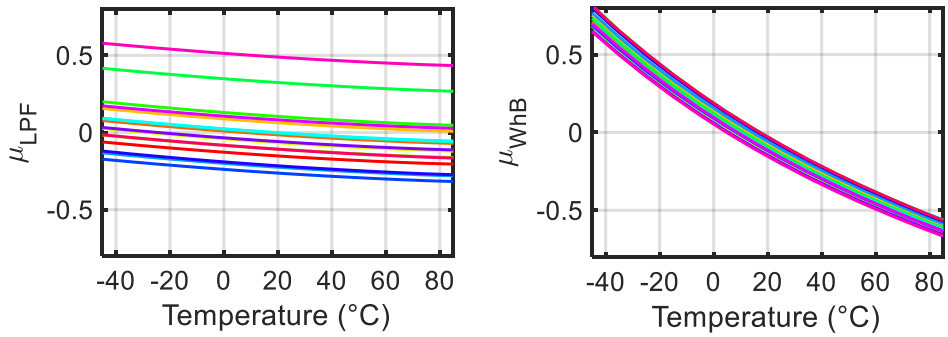


Figure 5.17: Die photo of the fabricated chip.

5.3.3.1 Calibration and inaccuracy

Fifteen devices were characterized in a temperature-controlled oven from −45°C to 85°C (Figure 5.18). Without trimming, the WhB sensor's peak-to-peak inaccuracy is ~14°C. After an offset trim and a fixed 4th order polynomial correction, the WhB sensor achieves a 3σ inaccuracy of 4.2°C. This can be improved to 0.46°C with a correlated 1-point calibration, as shown in Figure 5.19.



(a) (b)

Figure 5.18: Measured bitstream averages of (a) LPFs and (b)WhB sensors using an external 16MHz frequency reference.

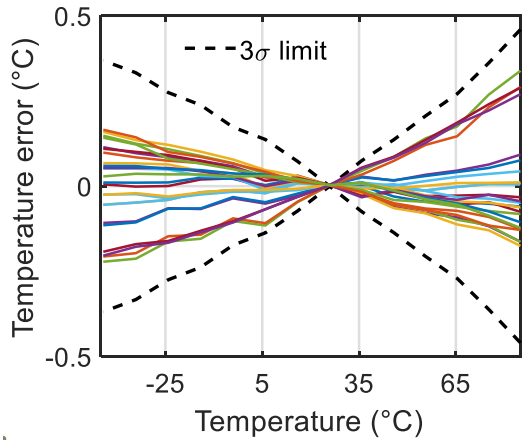


Figure 5.19: WhB sensor inaccuracy after correlation-based 1-point trim.

5.3.3.2 Resolution and FoM

The bitstream spectra of the WhB sensor is shown in Figure 5.20. The observed 1/*f* corner is ~10Hz, which is mainly from the non-silicided poly resistors. Due to the lack of an identical sensor on the same chip, the sensor's resolution is determined by

calculating the standard deviation of data from a single sensor after drift compensation. Within a 1s interval, the calculated resolution using sinc^2 filters is shown in Figure 5.21. With a conversion time of 10ms, its 200μK$_{rms}$ resolution corresponds to a resolution FoM of 30fJ·K^2.

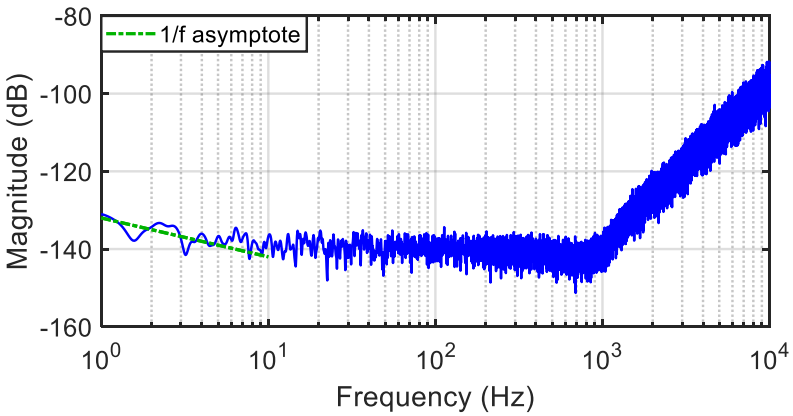


Figure 5.20: Power spectral density of the bitstream output.

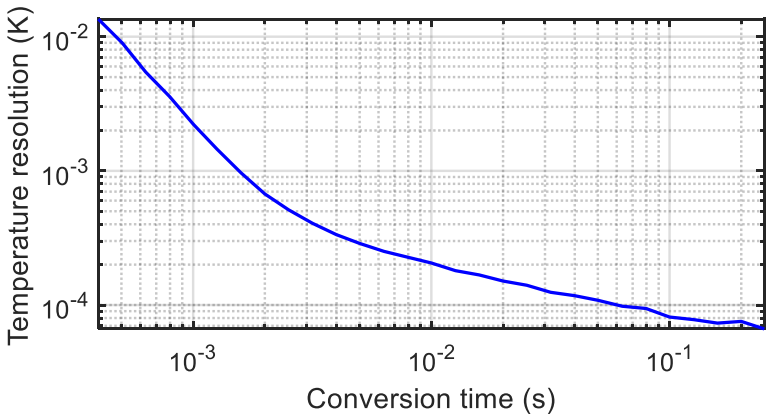
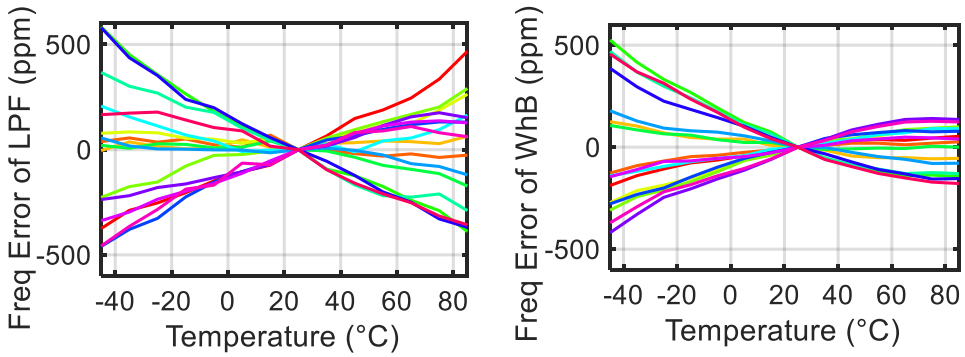


Figure 5.21: Temperature resolution vs. conversion time.

5.3.3.3 Frequency reference

After closing the loop of the frequency reference chip, the samples were characterized from −45°C to 85°C. As expected, the temperature dependence of the LPF output is quite low (−240ppm/°C). Compared to WB sensors presented in Chapter 3, the reduced ±5.625° phase DAC range introduces much smaller nonlinearity. From simulations, it contributes to less than 100ppm error after a simple offset trim, and the complicated μ to RC mapping can be skipped. Since the LPF non-linearity is similar to that of the WhB output (Figure 5.18), most of the frequency error

can be removed by applying a 1-point offset trim to the outputs of both the WhB and LPF at room temperature. As the WhB and the LPF are implemented on the same die, this trim is quite robust to ambient temperature variations [5.15]. After trimming, open-loop measurements show that the estimated frequency error due to the LPF alone is about ±520ppm, while the error due to the WhB alone is about ±470ppm, as shown in Figure 5.22. Due to the shared p-poly resistors, these errors are somewhat correlated, resulting in lower frequency error when the loop is closed. After an individual 1-point trim and a fixed 4th order polynomial nonlinearity correction, the proposed frequency reference achieves better than ±400ppm inaccuracy (Figure 5.23), which corresponds to a residual TC of 6.2ppm/°C (box method). The closed-loop period jitter is 10.2ps$_{rms}$. With a fixed digital input, the Allan Deviation of the DCO alone is around 40ppm, which drops to 0.4ppm in the closed-loop configuration.



(a) (b)

Figure 5.22: Estimated residue frequency error due to (a) LPF and (b)WhB.

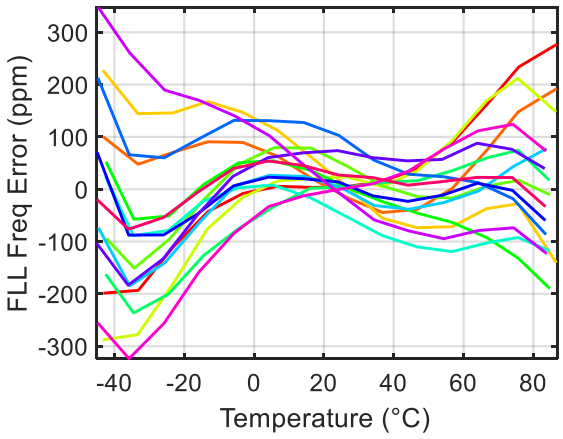


Figure 5.23: Measured frequency error after a 1-point trim and 4th order systematic non-linearity correction.

Table 5.2: Performance summary of the WhB sensor and comparison with those presented in Chapter 4.

	JSSC'15 [5.16]	Implementation III	Implementation IV		**This work**
Sensor type	Resistor WhB	Resistor WhB	Resistor WhB		**Resistor WhB**
Technology	0.18µm	0.18µm	0.18µm		**0.18µm**
Area [mm^2]	0.43	0.12	0.11		**0.125** [a]
Temp. Range [°C]	−40─125	−55─125	−55─125		**−45─85**
3σ Inaccuracy [°C] (trimming points)	0.4[b] (2[c])	0.14 (2[d])	0.1 (2[d])	0.4 (1)	**0.46 (1)**
Relative inaccuracy	0.48%	0.16%	0.11%	0.44%	**0.7%**
Power [µW]	65	79	55		**74**
Conv. time [ms]	0.1	10	8		**10**
Resolution [mK]	10	0.16	0.15		**0.20**
Res. FoM [fJ·K^2]	650	20	10		**30**

[a] Mostly reused area. [b] Min/Max. [c] 1-point trim + 1st-order fit. [d] 1st-order fit.

5.3.3.4 Comparision to previous work

Table 5.2 summarizes the performance of the proposed WhB sensor and compares it with sensors presented in Chapter 4. Due to the use of a single-bit DAC, the ΔΣ-ADC's 1st stage is not optimized for noise. Also, the WhB sensitivity is smaller due to the use of a low-TC poly resistor. Consequently, the sensor's energy-efficiency is worse than that of previous WhB sensors. Also, its 1-point trim accuracy is slightly worse. However, this sensor is well suited for the RC frequency reference compensation application, as it requires almost no additional chip area, while the accuracy/resolution performance is good enough.

The performance summary of the frequency reference is summarized in Table 5.3 and compared to other high-accuracy designs that achieve <10ppm/°C residual TC. Compared to [5.15], the proposed frequency reference achieves comparable accuracy after a 1-point trim at room temperature, as well as better energy and area-efficiency. This makes it highly compatible with IoT and wireline applications that require good accuracy and a high level of integration.

Table 5.3: Performance summary of the RC frequency reference and comparison with state-of-the-art.

	ISSCC'20 [5.15]		ISSCC'20 [5.17]	JSSC'18 [5.18]	JSSC'18 [5.19]	**This Work**
Technology	0.18µm		65nm	0.18µm	0.18µm	**0.18µm**
Area [mm^2]	0.3		0.18	1.65	0.17	**0.14**
Frequency [MHz]	16		32	7	24	**16**
Norm. Inaccuracy [ppm]	±400	±100	±530	±170	±215	**±400**
Trimming Points	2	2+Batch (6th order)	2	2+Batch (4th order)	3	**1+Batch (4th order)**
Temperature Range [˚C]	-45 to 85		-45 to 85	-45 to 85	-40 to 150	**-45 to 85**
Supply Range [V]	1.6 to 2.0		1.1 to 3.3	1.7 to 2.0	1.8 to 5.0	**1.6 to 2.0**
Supply Sensitivity [%/V]	0.12		0.008[a]	0.18	0.01	**0.2**
Number of Samples	20		6	8	1	**12**
Allan Deviation [ppm]	0.32		2.5	0.33	-	**0.4**
Power [µW]	400		34	750	200	**158.4**

[a] with on-chip LDO.

5.3.4 Summary

A Wheatstone bridge resistor-based temperature sensor has been implemented in a standard 0.18µm technology for the temperature drift compensation of an RC-based frequency reference. By reusing the existing readout circuit of the RC filter and doing careful layout, the sensor requires almost no additional chip area. After a 1-point trim, the frequency reference achieves an inaccuracy of better than ±400ppm from −45°C to 85°C. Compared to the fourth implementation shown in Chapter 4, the degraded 1-point trim inaccuracy is possibly due to a worse fabrication quality: the no-trim inaccuracy of this sensor is about 2× worse, and so is the error after a 1-point trim.

5.4 Concluding remarks

In this chapter, two resistor-based temperature sensor prototypes are presented to demonstrate their feasibility in different applications: biomedical temperature sensing and temperature compensation of RC frequency references. There are many other applications of resistor-based temperature sensors, such as thermal monitoring of microprocessors/DRAMs and wireless sensor nodes. These can be investigated in future work.

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Chapter 6

Conclusions and outlook

In this thesis, the development of resistor-based temperature sensors for the compensation of MEMS frequency references and other applications has been described. The main findings are presented in this chapter. Furthermore, the performance of resistor-based temperature sensors is summarized and compared to that of other types of CMOS temperature sensors, and some future research directions are proposed.

6.1 Main findings

The main findings of this thesis are:

- Of the various types of resistors available in CMOS processes, the silicided resistor is the best-suited for temperature sensing due to its large temperature coefficient (TC) and good stability (Chapter 1).
- Due to the relatively large TC of on-chip resistors, the theoretical energy efficiency of resistor-based temperature sensors is over an order of magnitude larger than that of conventional BJT-based ones (Chapter 1).
- Depending on the choice of the impedance reference, resistor-based temperature sensors have different characteristics. RC-based sensors, due to the use of temperature-insensitive capacitors, can achieve high accuracy, while dual-R-based sensors can achieve high energy-efficiency, especially by employing resistors with TCs of opposite polarity (Chapter 2).
- Wien-bridge (WB) and Wheatstone bridge (WhB) sensors are the preferred implementations of RC- and dual-R-based sensors, respectively. (Chapter 2).
- Despite exhibiting large untrimmed errors (>10°C), Wien-bridge sensors can achieve an inaccuracy of around 0.03°C over a 180°C temperature range with only two trimming points (Chapter 3).
- Compared to other types of poly resistors, silicided poly resistors have a much lower 1/*f* noise level. Also, they have lower stress-dependency: after a 2-point trim, the error introduced from plastic packaging is less than 0.2°C over a 220°C temperature range (Chapter 3).

- State-of-the-art energy-efficiency can be obtained by optimizing both the front-end and the readout circuit of a Wheatstone bridge sensor. A 10fJ·K^2 FoM has been achieved, which is only 6× larger than the theoretical limit imposed by the thermal noise of the Wheatstone bridge (Chapter 4).
- Although Wheatstone bridge sensors have a large nonlinearity (>15°C over a 180°C temperature range) and thus require high-order polynomial correction, this nonlinearity is quite stable: varying by <0.1°C over 3 batches (Chapter 4).
- By simply inserting tail resistors in a pseudo-differential OTA, the non-linearity of its transconductance can be reduced by >10× over corners without degrading its noise performance (Chapter 4).
- The use of a tail-resistor linearized OTA greatly improves the efficiency of multi-bit CTΔΣ-ADCs. The improved linearity leads to a significant reduction in quantization-noise folding, allowing the tail current of the OTA to be optimized for thermal noise (Chapter 4).
- Apart from the frequency compensation of MEMS/crystal oscillators, resistor-based temperature sensors can be advantageously used in other applications, e.g. in biomedical systems and RC-based frequency references (Chapter 5).

6.2 Temperature sensor comparison

To demonstrate the place of the presented resistor-based sensors in the temperature sensor universe, the best specifications of different types of sensors are summarized in Table 6.1. As the numbers were picked from different publications, design trade-offs (e.g., area vs. no-trim inaccuracy) are not reflected in this table.

As shown in Table 6.1, the WB/WhB sensors presented in this thesis can achieve state-of-the-art performance in terms of temperature range, relative inaccuracy, supply sensitivity, resolution, and resolution FoM. The designs were not particularly optimized for area and supply voltage, so this can still be improved. Compared to all CMOS temperature sensors published to date (2020), the Wien-bridge sensor presented in Section 3.5 achieves the best inaccuracy after a 2-point trim, the Wheatstone bridge sensor shown in Section 4.6 achieves the best resolution FoM, while the Wheatstone bridge sensor described in Section 5.2 achieves the lowest supply sensitivity.

The energy-efficiency of various types of CMOS temperature sensors is compared in Figure 6.1. Compared to Figure 1.2, solid star/square symbols have been added to indicate sensors presented in this thesis, as well as those published by others between 2017 and 2020. Prior to the start of this research, the best-reported resolution FoM for a CMOS temperature sensor was 650fJ·K^2 [6.2], as denoted by the dashed line. By

Table 6.1: State-of-the-art specifications of different types of CMOS temperature sensors by 2020 [6.1]. The shaded blocks indicate results presented in this thesis, while the numbers in bold are the best reported by any type of CMOS sensor.

	BJT	MOS	RES			TD	Best reported
			WB	WhB	Overall		
Area [mm²]	0.0025	**0.001**	0.007	0.044	0.006	0.0017	MOS [6.4]
Temp. Range [°C]	255	200	220	180	220	**270**	TD [6.5]
Relative inaccuracy (no trim)	0.3%	-	-	-	-	**0.2%**	TD [6.6]
Relative inaccuracy (1-pt trim)	**0.06%**	0.44%	0.32%	0.44%	0.32%	-	BJT [6.7]
Relative inaccuracy (2-pt trim)	-	0.11%	0.03%	0.11%	**0.03%**	-	RES (WB, Chap.3)
Supply voltage [V]	0.5 [a]	**0.4**	1.8	0.7	0.6	1	MOS [6.8]
Supply sensitivity [°C/V]	0.008	0.27	0.17	0.004	**0.004**	-	RES (WhB, Chap.5)
Power [µW]	0.7	0.00013	31	0.00005	**0.00005**	1300	RES [6.9]
Conversion time [ms]	0.01	**0.002**	5	0.01	0.0025	1	MOS [6.10]
Resolution [mK]	0.65	10	0.45	0.15	**0.1**	20	RES [6.11]
Res. FoM [pJ·K²]	0.19	1.4	0.11	0.01	**0.01**	140000	RES (WhB, Chap.4)

[a] With a charge-pump.

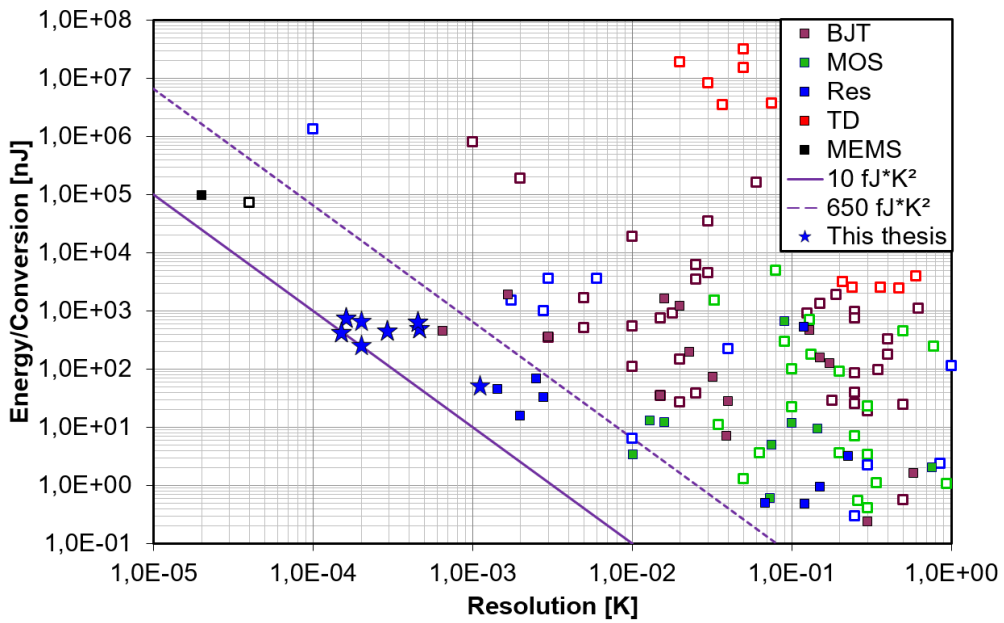


Figure 6.1: Energy per conversion vs. resolution of temperature sensors [6.1]. The stars represent the sensors presented in this thesis, while the solid/hollow squares indicate other sensors realized during/before this research, which started in 2016.

systematic circuit optimization, this has been improved by 65×, as represented by the solid line (10fJ·K^2). This FoM is even 4× better than that of MEMS-based sensors [6.3], which are not CMOS-compatible.

Roughly half of the specification records listed in Table 6.1 still belong to other types of sensors. Of these, inaccuracy is limited by the inherent properties of resistors, and will be hard to improve. Of the other specifications, however, there are no fundamental limitations to the further improvement of resistor-based sensors. For example, being a passive element, the maximum operating temperature range of resistors can be expected to be larger than that of BJTs or MOSFETs, while the minimum supply voltage should be smaller.

6.3 Systematic design approaches for accuracy

This thesis provides detailed design guidelines for improving the energy-efficiency of resistor-based sensors. However, a similar approach to improving the accuracy of such sensors would also be useful. Apart from facilitating the design of sensors with better accuracy, this knowledge would also help when designing compact sensors with relaxed inaccuracy requirements.

6.3.1 Cadence modeling

For BJT-based temperature sensors, one major source of inaccuracy is the effect of lithographic tolerances on the BJT's base width and the emitter area. This can be suppressed by using larger sensing BJTs [6.12]. Due to the existence of accurate process and mismatch models, the inaccuracy of BJT-based sensors can be well-predicted via simulations.

Unlike BJTs, the temperature characteristics of on-chip resistors are not as well-modeled. All the sensors presented in this thesis were implemented in the same standard 0.18μm CMOS technology. According to its documentation, all resistor variations (process and mismatch) are modeled as changes in the sheet resistance. In practice, however, both the sheet resistance and TC will spread, and there could be even some correlation between them [6.13].

To test the effectiveness of the process models, Monte-Carlo simulations (device mismatch) have been done on the Wien-bridge sensor presented in Section 3.5 and the Wheatstone bridge sensor presented in Section 4.6, as shown in Figure 6.2. For simplicity, the readout circuits are assumed to be ideal. The untrimmed inaccuracies of both sensors are less than 1°C, which is over 10× smaller than the measurement results. With process spread simulations, the untrimmed temperature errors become

larger than 100°C. However, as these simulations assume perfectly matched resistors and capacitors, the residual error will become zero after a single-point trim.

After applying the same 1-point/1st-order trimming methods used in Chapter 3/4 on Figure 6.2, the simulated sensor inaccuracies are on average an order of magnitude smaller than the measurement results, as shown in Figure 6.3/6.4. The almost-zero residual error shown in Figure 6.4(b) also confirms the theory presented in Chapter 4, section 4.2.2, that, without TC variations of resistors, a Wheatstone bridge sensor can be perfectly calibrated with two trimming points.

There are two possible reasons for the large discrepancy between simulation and measurement. The first reason is that the readout circuits presented in this thesis may be significant sources of inaccuracy. The second, and more likely, reason is that the simplified resistor model results in over-optimistic simulation results.

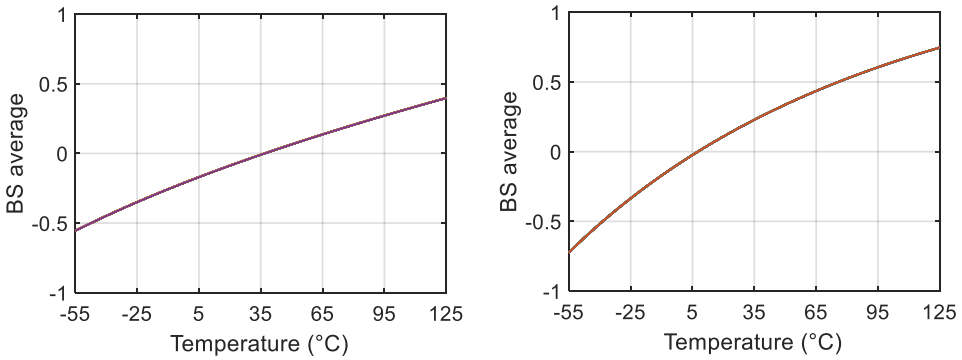


Figure 6.2: Simulated output of (a) WB sensor and (b) WhB sensor with ideal readout electronics.

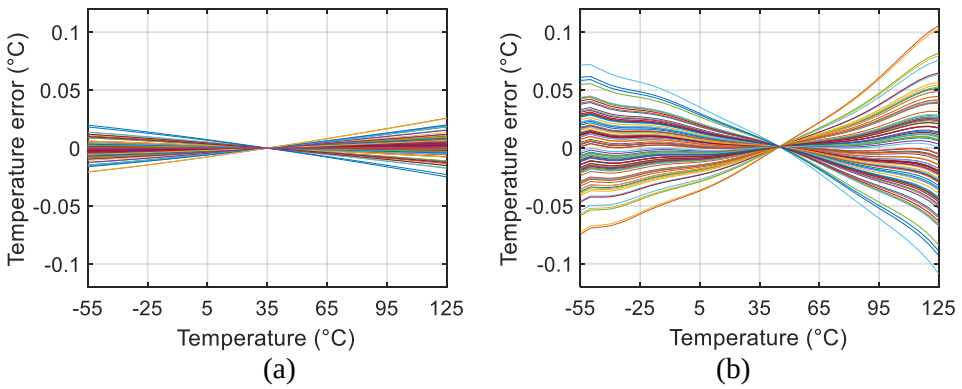


Figure 6.3: Simulated inaccuracy of (a) WB sensor and (b) WhB sensor after a 1-point trim and systematic error removal.

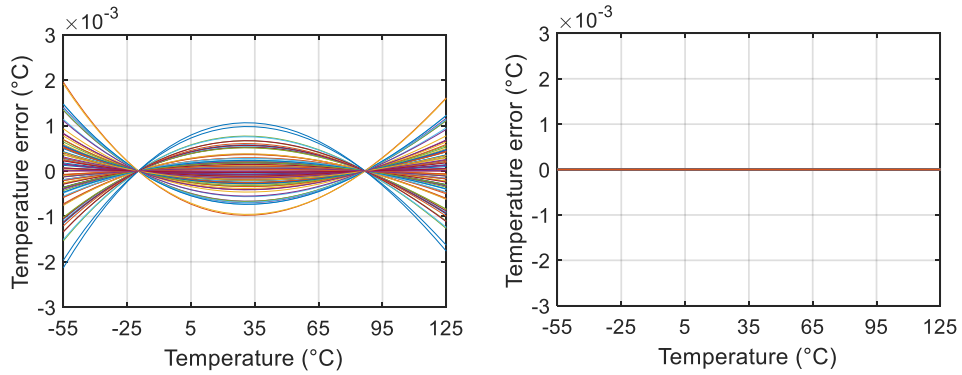


Figure 6.4: Simulated inaccuracy of (a) WB sensor and (b) WhB sensor after 1st-order fit and systematic error removal.

6.3.2 Data analysis

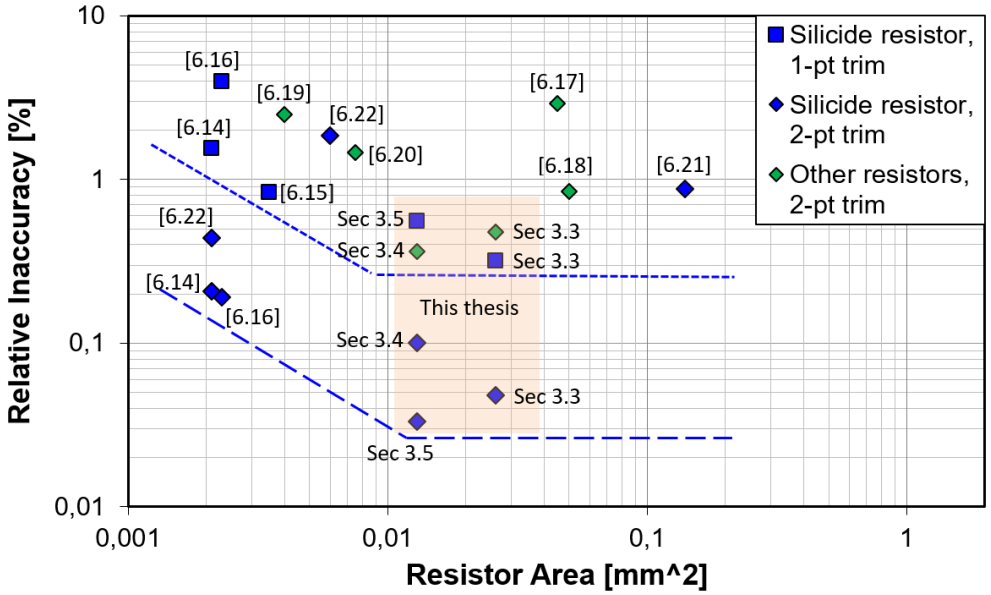
Another way to predict the achievable sensor inaccuracy is by analyzing all reported results. Figure 6.5 shows the inaccuracy vs. resistor area of different sensors. To enlarge the data set, WB/WhB sensors are regarded as special cases of RC/dual-R sensors, respectively. In general, sensors that use silicide resistors are more accurate than those that use other resistors.

As can be seen from the rough envelope curves in Figure 6.5 (a), the inaccuracy of RC sensors improves as the resistor area increases[6.14]. However, the trend stops when the resistor area reaches ~0.1mm^2. This can be explained as a combined effect of inherent inaccuracy of resistors (nominal value and TC spread) and the device mismatch. The former dominates the inaccuracy with a large resistor area, while the latter is the major inaccuracy contributor for compact sensors.

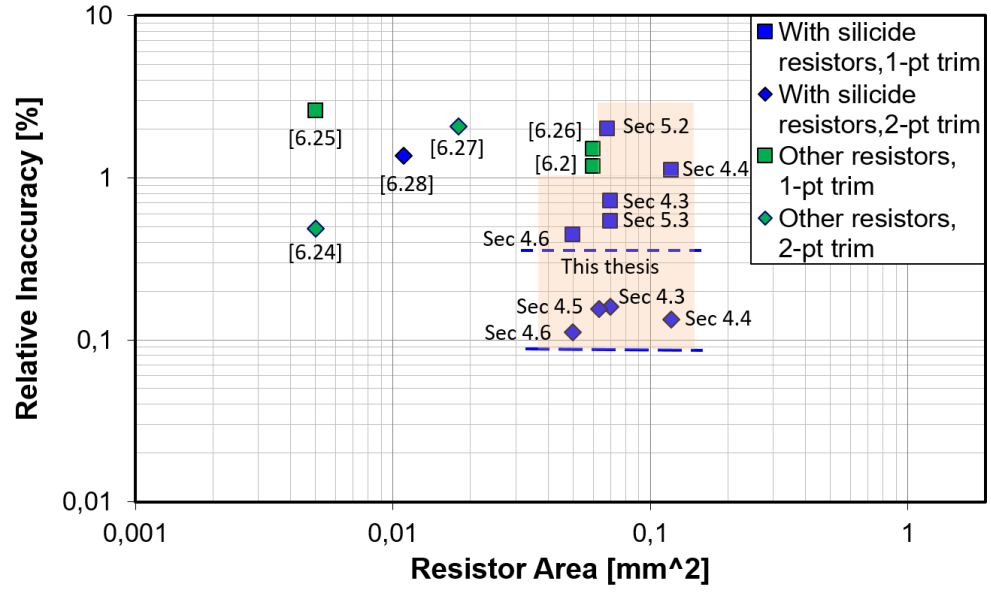
As of 2020, very small silicide resistors have not been used in dual-R sensors. As a result, envelope curves in the inaccuracy vs. area plot (Figure 6.5 (b)) cannot be drawn. It has been shown in [6.24] that small Wheatstone bridge sensors made from non-silicided resistors can also achieve decent inaccuracy after a two-point trim. With carefully designed readout circuits, similar sensors with silicide resistors should be even more accurate.

6.3.3 Experimental verification

The direct way to investigate the achievable inaccuracy of resistor-based sensors is to build an array of different types of stand-alone resistors and characterize them carefully. Although a bit tedious, this approach will rule out the effect of imperfect readout circuits.



(a)



(b)

Figure 6.5: Relative inaccuracy vs. resistor area of (a) RC and (b) dual-R sensors. The resistor areas were estimated from the published chip photos.

6.4 More future research directions

Apart from the aforementioned issue of the relationship between resistor area and sensor inaccuracy, many other directions related to this thesis are also worth investigating. Here is an incomplete list.

6.4.1 Area- and power-efficient digital backend

For simplicity, the digital backends of all the sensors presented in this thesis are implemented off-chip. However, commercial chips should have all the digital integrated, so that they can use standard protocols, like SPI or I^2C, for data communication.

Designing such a digital back-end is a non-trivial task especially under the constraint that its area and power should not dominate that of the analog front-end. Take a Wien-bridge sensor, for example, two high-order polynomials and a 2-point trim are required to remove its process spread and nonlinearity, and all the steps require high resolution. If not designed carefully, the digital calibration circuit alone would consume more area and power than the analog front-end.

6.4.2 Background calibration of Wheatstone bridge sensors

As presented in Chapter 2, WhB sensors with unsilicided poly resistors are vulnerable to long-term drift. When used for the compensation of MEMS frequency references, this drift might reduce the long-term stability of such references to tens of ppm. To overcome this issue, the WhB sensor can be periodically calibrated by a more stable temperature sensor, e.g. a BJT-based temperature sensor. As a result, the energy efficiency of the resulting hybrid sensor will still be determined by the WhB sensor, while the long-term stability will be limited by that of the BJT sensor, which can be less than 6mK over one year [6.29]. To reduce chip area, and thus fabrication cost, the readout circuit should preferably be shared by the two sensors.

6.4.3 Long-term stability of Wien bridge sensors

Compared to WhB sensors, WB sensors are made from stable silicided poly resistors and metal-insulator-metal (MIM) capacitors, and should be much more stable. If the silicided layer, due to its metal-like properties, is assumed to be perfectly stable, then the dominant source of drift will be due to the underlying poly layer (Figure 2.3), which is about 30× more resistive. As the drift of non-silicided poly resistors is between 0.2% to 0.8% (Chapter 2), the drift of silicided resistors should be 30× smaller, or no more than 300ppm. This corresponds to an estimated WB temperature

sensor drift of ~0.1°C over its lifetime and thus a freuquency error of below 3ppm for temperature-compensated MEMS oscillators. This hypothesis still needs to be verified by measurement results.

6.4.4 Energy-efficient Wheatstone bridge temperature sensors with scaled energy/conversion

Although the WhB sensors presented in Chapter 4 can achieve state-of-the-art energy-efficiency, their energy/conversion (~400nJ/conv) is higher than most BJT-based sensors, while their sub-mK resolution is an overkill in most applications. For example, a battery-powered RFID sensor only requires a resolution of some tens of milli-Kelvin [6.30]. To extend battery life it would be desirable to trade resolution for energy/conversion along the $10fJ{\cdot}K^2$ constant-FoM line (Figure 6.1), for instance by achieving a thermal-noise-limited resolution of 10mK while consuming 0.1nJ/conversion (~4000× smaller). Lower energy/conversion can be achieved by reducing power consumption or shortening conversion time. Tuning the design parameters (e.g., resistor value, supply voltage, sampling frequency, ΔΣ-ADC order) could possibly achieve a 10× reduction. However, new architectures are required to obtain another 400× reduction.

To reduce the average power of the WhB front-end, heavy duty-cycling can be applied, and the WhB output voltage can be stored on a hold capacitor [6.31]. As for the readout circuit, it should provide sufficient resolution at a low oversampling ratio. This can be achieved by using an oversampled SAR ADC [6.32]. However, combining the two techniques could be challenging, as the hold capacitor in [6.31] cannot provide the low-impedance voltage input required by [6.32].

Another drawback of resistor-based sensors is the need for costly temperature calibrations. One way to simplify the calibration process is by integrating an inherently accurate temperature sensor, e.g., a sensor based on an electro-thermal filter (ETF) on the same chip [6.6]. As a result, the sensor can be self-calibrated. Although the ETF will dissipate milli-watts of power, it can be disabled during normal operation, thus maintaining the sensor's energy-efficiency. As mentioned in section 6.4.2, integrating the two sensors with a (partially) shared readout circuit is necessary to reduce chip area and thus fabrication cost.

6.4.5 Applications of the tail-resistor linearized OTA

As shown in Chapter 4, section 4.6, the nonlinearity of OTAs can be greatly improved by using the proposed tail-resistor linearization technique. As a result, the readout circuit of the Wheatstone bridge sensor can be scaled for thermal noise, which optimizes its efficiency.

The same principle can be applied to general-purpose CTΔΣ-ADCs, and Figure 6.6 shows a simple translation while keeping the same readout electronics. By choosing the input resistor $R_{in} = R_p//(R_{DAC}/2) = 67k\Omega$ and switching the 4 DAC resistors (370kΩ each) between supply rails, both the equivalent impedance and thus noise of the two topologies are the same. However, the DAC resistors in Figure 6.6 (b) consume less power than the Wheatstone bridge in Figure 6.6 (a), and the estimated ADC power will be ~42µW instead of 55µW. Besides, the ADC will have a small stable input range, which is ~910mV under a 1.8V supply. Considering only its thermal noise, the ADC's expected Schreier FoM, which is DR+10·log(BW/power), should be ~183dB. This is similar to the state-of-the-art CTΔΣ-ADC [6.33], and could be further improved by optimizing its input range, i.e., the ratio between its input and DAC resistors.

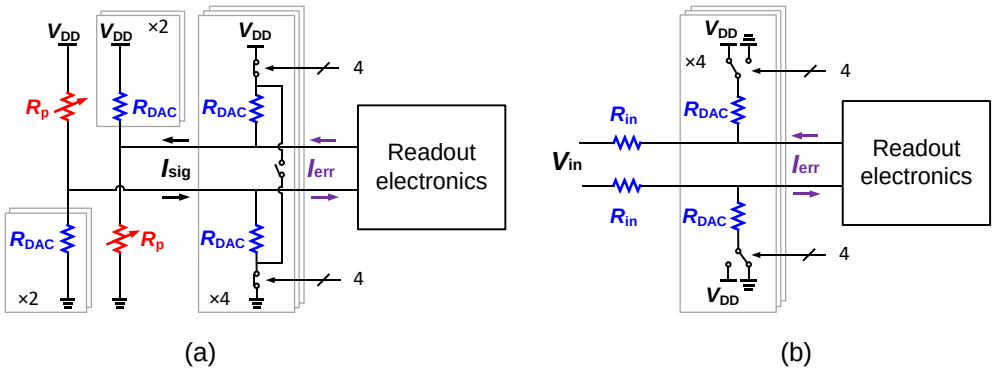


Figure 6.6: (a) Wheatstone bridge front end shown in section 4.6. (b) Input and DAC resistors of a CTΔΣ-ADC with equivalent input impedance and noise.

Another attractive application of the linearized OTA is processing small biomedical signals of ~10mV amplitude, e.g., electromyography (EMG) signals. Because of its high linearity, the signal can be amplified with almost no distortion. Moreover, the OTA is capacitively coupled, so that it has a large input impedance and a large common-mode rejection ratio at DC, which are both advantageous in biomedical electronics.

6.5 Concluding remarks

This thesis has discussed the development of energy-efficient resistor-based temperature sensors as well as their readout circuits. With this research, the energy-efficiency of CMOS temperature sensors is improved by 65×, and is approaching the theoretical FoM limit set by the thermal noise of the sensor front-end (6×). Also, accuracy- and application-driven sensors have been developed.

However, there are still many directions left unexplored about resistor-based temperature sensors, and further improvements are required before commercializing the prototype sensors. Moreover, this thesis has also presented some general analog design techniques, e.g., tail-resistor-based OTA linearization, which can potentially improve the performance of other circuits.

6.6 References

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A

Appendix

A.1 Measurement setup

In this thesis, all the fabricated temperature sensors are characterized by a Pt-100 reference. The key of accurate characterization is creating a thermal equilibrium condition, so that the temperature error between the Pt-100 reference and the sensors can be minimized.

To achieve this, the chips were kept in a large aluminum box, with a customized lid to prevent airflow and thus temperature fluctuations, as shown in Figure A.1. It also acted as a low-pass thermal filter with a low cut-of-frequency, making the sensor's temperature stable during measurements. For better thermal conductivity, the sensors were mounted inside the cavity of the aluminum box using thermal paste (Figure A.2). The Pt-100 temperature reference was inserted into a hole in the metal block near the chips.

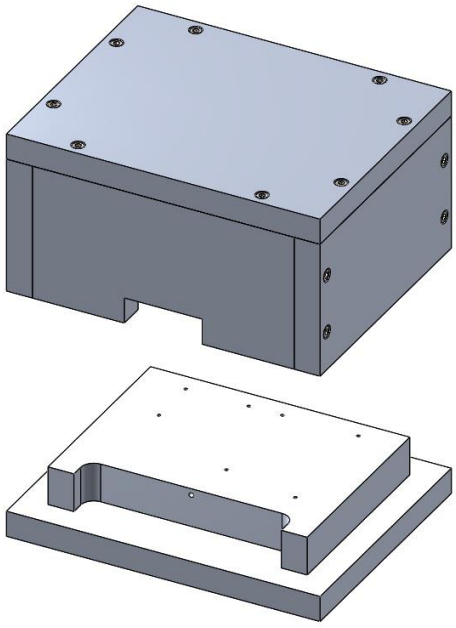

Figure A.1: Customized metal box: base and lid.

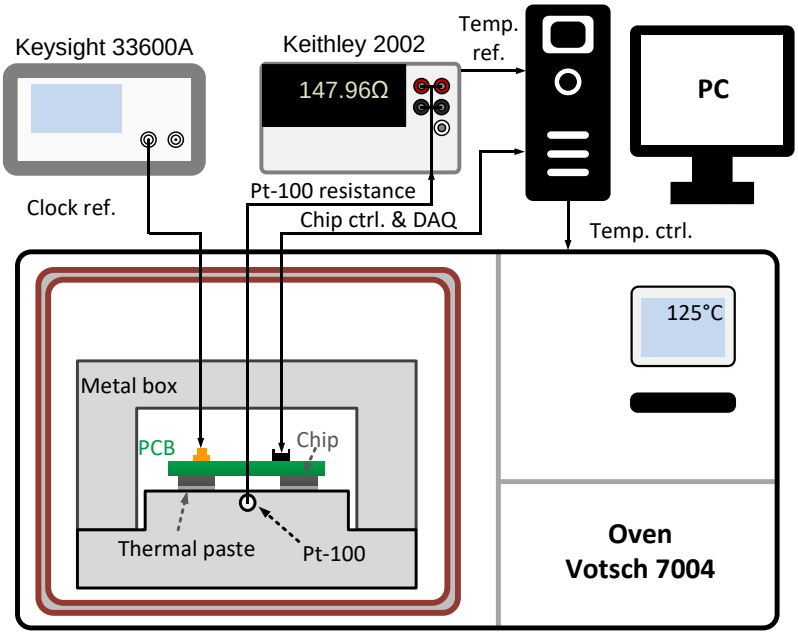

Figure A.2: Test setup for temperature sensor characterization.

As shown in Figure A.2, the Pt-100 is readout by an 8.5-digit Keithley 2002 multimeter. During temperature characterization, the bitstream capture would start only when the difference of two successive readouts of the Pt-100 temperature reference (about 20s per readout) was less than 3mK, held for about 400 successive readouts without any exception. Then the Pt-100 and the sensors could be considered in thermal equilibrium. With this setup, the oven settling time is about 4 hours for a single temperature point.

Moisture also plays an important role. As shown in Chapter 3, section 3.4, it affects the stress profile of the plastic package and thus the value of the sensing resistor via the piezoresistive effect. Although this effect is much weaker with ceramic packages, it should be still avoided in order to achieve the best sensor inaccuracy. This can be done with dehumidifier, or simply by selecting the correct temperature ramping direction. As shown in Figure A.3, when the test setup temperature is ramping down, the surface of the box is always cooler compared its cavity. Consequently, water droplets are generated on the surface of the metal box, but not the surface of packaged chips.

Last but not least, the noise of the clock reference should be minimized, especially for WB sensors. For the 1st WB sensor prototype (Chapter 3, section 3.3), the reference clock was generated by a low-jitter (<1ps) MEMS oscillator. For the rest experiments, it was generated by a function generator (Keysight 33600A) with a similar jitter performance.

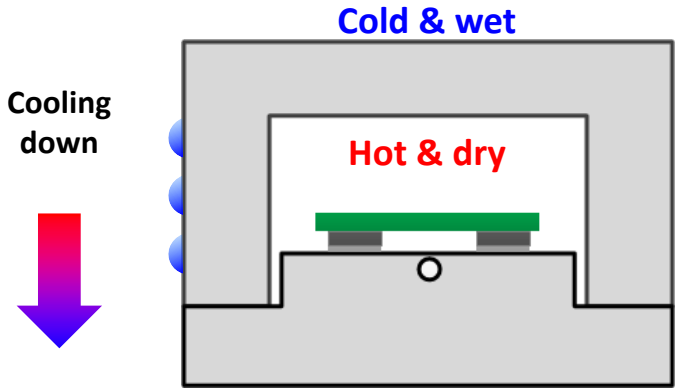

Figure A.3: Moisture effect inside the metal box avoided by ramping down the oven temperature.

A.2 OTA with tail-resistor linearization: condition of the 3rd-order nonlinearity cancellation

In this appendix, the optimum tail resistor value for the 3rd-order OTA nonlinearity suppression is derived, assuming that the transistors are operating in deep weak inversion.

For a single transistor in weak inversion region, its V-I characteristic is roughly exponential. After ignoring the effect of a finite output impedance and the back-gate effect, the output current I_d can be expressed as,

$$I_d = I_s \cdot e^{\frac{V_{gs}-V_T}{nU_T}}, \tag{A.1}$$

where V_T is the threshold voltage, I_s is the current at $V_{gs}=V_T$, n is a process-dependent slope factor, and $U_T=kT/q$ is the thermal voltage.

After applying a differential voltage $\pm\Delta V_g$ on the OTA with a tail resistor, the voltage drop on the tail resistor R_{tail} will increase due to the enlarged total current. Denoting the difference as ΔV_{tail}, the OTA's differential current output ΔI_o can be expressed as:

$$\Delta I_o = I_s \cdot e^{\frac{V_{gso}-V_T+\Delta V_g-\Delta V_{tail}}{nU_T}} - I_s \cdot e^{\frac{V_{gso}-V_T-\Delta V_g-\Delta V_{tail}}{nU_T}}. \tag{A.2}$$

Writing its Taylor series up to the 3rd order term, there is

$$\Delta I_o = I_s \cdot e^{\frac{V_{gs0}-V_T}{nU_T}} \left(\frac{2\Delta V_g}{nU_T} - \frac{4\Delta V_g \Delta V_{tail}}{2(nU_T)^2} + \frac{2\Delta V_g{}^3 + 6\Delta V_g \Delta V_{tail}{}^2}{6(nU_T)^3} \right) \quad \text{(A.3)}$$

In order to cancel the 3rd-order nonlinearity, there must be

$$-\frac{4\Delta V_g \Delta V_{tail}}{2(nU_T)^2} + \frac{2\Delta V_g{}^3}{6(nU_T)^3} = 0. \quad \text{(A.4)}$$

Thus, the relationship between ΔV_{g} and ΔV_{tail} becomes

$$\Delta V_{tail} = \frac{\Delta V_g{}^2}{6nU_T}. \quad \text{(A.5)}$$

Alternatively, ΔV_{tail} can be calculated as $\Delta I_{\text{tail}} \cdot R_{\text{tail}}$, i.e.,

$$\Delta V_{tail} = R_{tail} \cdot I_s e^{\frac{V_{gs0}-V_T}{nU_T}} \left(e^{\frac{\Delta V_g - \Delta V_s}{nU_T}} + e^{\frac{-\Delta V_g - \Delta V_s}{nU_T}} - 2 \right). \quad \text{(A.6)}$$

Writing its Tylor series up to the 2nd order term, there is

$$\Delta V_{tail} = R_{tail} \cdot I_s e^{\frac{V_{gs0}-V_T}{nU_T}} \left(\frac{-2\Delta V_{tail}}{nU_T} + \frac{2\Delta V_g{}^2 + 2\Delta V_{tail}{}^2}{2(nU_T)^2} \right). \quad \text{(A.7)}$$

With $\Delta V_{tail} = \frac{\Delta V_g{}^2}{6nU_T}$, and neglecting the term with $\Delta V_{tail}{}^2$, equation (A.7) can be rewritten as:

$$\frac{\Delta V_g{}^2}{6nU_T} = R_{tail} \cdot I_s \cdot e^{\frac{V_{gs0}-V_T}{nU_T}} \cdot \frac{2\Delta V_g{}^2}{3(nU_T)^2}. \quad \text{(A.8)}$$

Thus, the term $\Delta V_g{}^2$ can be cancelled on both sides, leaving

$$R_{tail} = \frac{nU_T}{4I_s \cdot e^{\frac{V_{gs0}-V_T}{nU_T}}} = \frac{nU_T}{2I_{tail}}, \quad \text{(A.9)}$$

where I_{tail} is the tail current of the differential pair given a zero differential input.

Summary

This thesis describes the design and implementation of integrated temperature sensors based on the temperature dependency of CMOS resistors.

Chapter 1 is an introduction to the thesis. It first discusses some general aspects of integrated temperature sensors, including their applications and specifications. Temperature compensation of MEMS/crystal frequency references is a demanding application: high temperature sensing resolution is needed to prevent the sensor's noise from increasing the frequency reference's jitter, while high energy efficiency is required to minimize the sensor's contribution to the reference's total energy budget. Moreover, high stability is required to suppress the reference's error under various conditions. After comparing various temperature sensing elements available in CMOS technology, resistor-based temperature sensors are chosen, which, compared to traditional BJT-based sensors, are in theory over 5× more energy-efficient.

Chapter 2 discusses some general concerns involved in the design of resistor-based temperature sensors. After comparing the characteristics of the different sensing resistors available in standard CMOS technology, silicided resistors are chosen due to their large temperature sensitivity and high stability. Apart from the sensing resistor, a reference impedance is required to convert resistance changes into digital information. Two possible sensor structures are dual-R (with a resistor reference) and RC (with a capacitor reference). The former is more energy-efficient, while the latter is more accurate. Among popular front-end topologies, Wien-bridge (RC) and Wheatstone bridge (dual-R) are preferred. To achieve high-resolution, they should be digitized by Delta-Sigma ADCs (ΔΣ-ADCs).

Chapter 3 presents the design of Wien-bridge sensors focusing on accuracy. To improve its noise and efficiency, the phase demodulator of the continuous time (CT) ΔΣ-ADC is achieved by multiplexers made from switches. Due to the use of square-wave inputs and phase references, the ADC output (μ) has a strong nonlinearity, which cannot be eliminated after a two-point trim. To suppress this effect, a μ-to-RC nonlinearity correction should be applied before trimming. Three Wien-bridge sensor prototypes have been implemented. After trimming, the first prototype achieves a 3σ inaccuracy of 0.03°C over an industrial temperature range from −40°C to 85°C, but occupies 0.72mm^2. With improved readout circuits, the third prototype achieves a similar inaccuracy over a wider military temperature range from −55°C to 125°C, while the area is only 0.12mm^2.

Chapter 4 discusses the design of Wheatstone bridge sensors focusing on energy efficiency. Compared to traditional Wheatstone bridge readout circuits using instrumentation amplifiers, sensors presented in this chapter are directly readout by

DAC resistors and CTΔΣ-ADCs. The first prototype uses a single-bit CTΔΣ-ADC and achieves a resolution figure-of-merit (FoM) of 65fJ·K^2. By systematically improving the design, the FoM of the fourth design reaches 10fJ·K^2, which is only 6× worse compared to the theoretical value defined by the thermal noise of the Wheatstone bridge. This is enabled by design techniques including multi-bit DAC, return-to-CM switching, linearized OTA, etc. It is worth mentioning that the OTA linearization is achieved by simply replacing the current source of its differential pair with a resistor, and the linearity of its transconductance is improved by at least an order of magnitude.

Chapter 5 presents two designs to broaden the application of resistor-based temperature sensors. The first is aimed for biomedical applications. With power scaling and properly-designed parallel DAC resistors, this sensor consumes only 6.6μW, and achieves a 0.2°C inaccuracy from 27.5°C to 47.5°C after an on-chip trimming, which greatly simplifies its digital backend. The second design is a sensor embedded in an RC-based frequency reference. By extensive circuit reusing, the additional area required by the Wheatstone bridge temperature sensor is negligible. Also, as the RC filter nonlinearity is similar to that of the Wheatstone bridge sensor output, the RC frequency reference error can be mostly removed by simple offset trims to the outputs of both the RC filter and the temperature sensor. Its remaining error is less than ±400ppm from −45°C to 85°C.

In Chapter 6, the main findings of this thesis are summarized. Resistor-based temperature sensors are especially competitive in applications that require both high resolution and high energy-efficiency. Compared to the-state-of-the art in 2016, the work presented in this thesis improves the energy-efficiency of CMOS temperature sensors is by 65×. This chapter also contains some suggestions for future directions, including a systematic design approach based on sensor accuracy, area- and power-efficient digital backend, background calibration, long-term-stability measurement, application of the tail-resistor-linearized OTA, etc.

Samenvatting

Dit proefschrift omschrijft het ontwerp en de implementatie van een geïntegreerde temperatuursensor gebaseerd op de temperatuursafhankelijkheid van CMOS weerstanden.

Hoofdstuk 1 dient als inleiding tot dit proefschrift. Het begint met een discussie van algemene aspecten van geïntegreerde temperatuursensoren inclusief hun toepassingen en specificaties. Temperatuurcompensatie van MEMS/kristal frequentie referenties is een veeleisende toepassing: goede resolutie is nodig om te voorkomen dat de sensor's ruis bijdraagt aan de frequentie-referentie's jitter, terwijl hoge energie-efficiëntie noodzakelijk is om de sensor's bijdrage aan het totale powerbudget te minimaliseren. Bovendien, goede stabiliteit is noodzakelijk om de referentie's afwijking onder de verschillende omstandigheden te verminderen. Na een vergelijking tussen verschillende CMOS compatibele temperatuur transducers, zijn op weerstand gebaseerde temperatuursensoren gekozen, die, in vergelijking met BJT-gebaseerde sensoren, in theorie meer dan 5× energie-efficiënter zijn.

Hoofdstuk 2 omschrijft verscheidene algemene aspecten die betrokken zijn bij het ontwerpen van weerstands-gebaseerde temperatuursensoren. Na een vergelijking van de karakteristieken van de verscheidene weerstanden die beschikbaar zijn in standaard CMOS technologie, zijn silicided weerstanden gekozen vanwege hun grote temperatuur gevoeligheid en hoge stabiliteit. Naast de meetweerstand is ook een referentie impedantie nodig om veranderingen in weerstand om te kunnen zetten in digitale informatie. Twee mogelijke sensor strategieën zijn: een duaal-R (met een referentie weerstand) en een RC (met een referentie capaciteit). De voormalige is meer energie-efficiënt, terwijl de laatste meer accuraat is. Tussen populaire front-end topologieën hebben de Wien-Brug (RC) en de Wheatstone-brug de voorkeur. Om goede resolutie, moeten deze gedigitaliseerd worden door Delta-Sigma ADC's (ΔΣ-ADC's).

Hoofdstuk 3 presenteert het ontwerp van een Wien-Brug sensor die gefocust is op accuraatheid. Om zijn ruis-efficiëntie te verbeteren is de fase demodulator van de continue-tijd (CT) ΔΣ-ADC geïmplementeerd door multiplexers die gemaakt zijn van schakelaars. Vanwege het gebruik van blok-golf input- en referentie-fase signalen heeft de ADC uitgang (μ) een sterke niet-lineariteit die niet weg getrimd kan worden door een twee-punt trim. Om dit effect te onderdrukken wordt een μ-naar-RC niet-lineariteit correctie toegepast voor het trimmen. Drie verschillende Wien-Brug sensor prototypen zijn geïmplementeerd. Na trimmen behaalt het eerste prototype een 3σ onnauwkeurigheid van 0.03°C over het industriële temperatuur bereik (van −40°C tot 85°C), maar vereist een oppervlak van 0.72mm². Met verbeterde uitlees schakelingen

behaalt het derde prototype een vergelijkbare onnauwkeurigheid over het bredere militaire temperatuurbereik (−55°C tot 125°C), terwijl zijn oppervlak maar 0.12mm² inneemt.

Hoofdstuk 4 bediscussieert het ontwerp van Wheatstone brug sensoren die op energie-efficiëntie gericht zijn. Vergeleken met traditionele Wheatstone brug uitlees schakelingen die gebruik maken van instrumentatieversterkers worden de sensoren die dit hoofdstuk presenteert direct uitgelezen door DAC-weerstanden en CTΔΣ-ADC's. Het eerste prototype maakt gebruik van een enkele-bit CTΣΔ-ADC en behaalt een resolutie maat-van-verdienste (Engels: FoM) van 65fJ·K². Door systematische verbetering van het ontwerp behaalt het vierde prototype een FoM van 10fJ·K², wat maar 6× slechter is vergeleken met de theoretische waarde gedefinieerd door de thermische ruis van de Wheatstone brug. Dit wordt mogelijk gemaakt door technieken zoals multi-bit ADC, terug-naar-CM schakelen, een gelineariseerde OTA, etc. Het is het waard om te zeggen dat de OTA-linearisatie behaald is door simpelweg de stroombron van het differentiële-paar te vervangen met een weerstand, waardoor de lineariteit van zijn transconductantie verbeterd is bij tenminste één orde-grootte.

Hoofdstuk 5 presenteert twee ontwerpen dat het aantal toepassingen van weestand-gebaseerde temperatuur sensoren verbreedt. De eerste is gericht op biomedische toepassingen. Doormiddel van het schalen van het vermogen en correct ontworpen parallel DAC-weerstanden behaalt deze sensor een vermogen van 6.6µW met een nauwkeurigheid van 0.2°C van 27.5°C tot 47.5°C na een in-chip trim, die de digitale backend enorm versimpelt. Het tweede ontwerp is een sensor dat onderdeel uitmaakt van een RC-gebaseerde frequentie referentie. Door extensief hergebruik van de circuits is het extra oppervlak dat nodig is voor de Wheatstone brug temperatuur sensor verwaarloosbaar. Daarbij, omdat de RC-filter niet-lineariteit vergelijkbaar is met die van de Wheatstone brug sensor, kan de RC frequentie-referentie afwijking verwijderd worden door een simpele offset trim aan de RC-filter en de temperatuur sensor. De resulterende afwijking is kleiner dan ±400ppm van −45°C tot 85°C.

In hoofdstuk 6 worden de hoofdvindingen van dit proefschrift samengevat. Op weerstand-gebaseerde temperatuur sensoren zijn voornamelijk erg competitief in toepassingen dat goede resolutie in combinatie met goede energie-efficiency nodig heeft. In vergelijking met de stand van zaken van 2016 verbetert het werk van dit proefschrift de energie-efficiëntie van CMOS temperatuur sensoren met 65×. Dit hoofdstuk bevat ook suggesties voor toekomstige onderzoek directies, e.g., een systematische ontwerp strategie gebaseerd op sensor nauwkeurigheid, een oppervlak en vermogens-efficiënt digitale backend, achtergrond kalibratie, lange-termijn stabiliteit metingen, toepassingen voor de staart-weerstand gelineariseerde OTA, etc.

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Sining Pan

Dec. 2020, Delft

List of publications

Top journal papers (JSSC)

1. **S. Pan**, J. A. Angevare and K. A. A. Makinwa, "A hybrid thermal-diffusivity/ resistor-based temperature sensor with a self-calibrated inaccuracy of 0.25°C (3σ) from −55°C to 125°C," invited for publication in *IEEE J. Solid-State Circuits* special issue on ISSCC 2021.
2. **S. Pan** and K. A. A. Makinwa, "A 10fJ·K^2 Wheatstone bridge temperature sensor with a tail-resistor-linearized OTA," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 501-510, Feb. 2021.
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6. **S. Pan**, J. A. Angevare and K. A. A. Makinwa, "A hybrid thermal-diffusivity/ resistor-based temperature sensor with a self-calibrated inaccuracy of 0.25°C (3σ) from −55°C to 125°C," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2021, pp. 78-79.
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14. **S. Pan** and K. A. A. Makinwa, " A 6.6-μW Wheatstone-bridge temperature sensor for biomedical applications," *IEEE Solid-State Circuits L.*, vol. 3, pp. 334-337, 2020.
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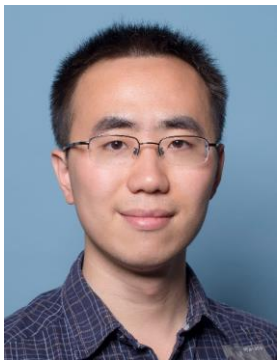
About the author



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