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Modeling, Experimental Validation, and Application of VARC HVDC Circuit Breakers

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Abstract—**This paper deals with the modeling, hardware results and model validation by measurements of a VSC assisted resonant current (VARC) dc circuit breaker (CB) and the application within a future network by simulation. The newly emerging VARC dc CB can be used as a solution for the protection of offshore multi-terminal HVDC (MTDC) grids. In this paper, the proposed VARC dc CB is modeled in detail in a PSCAD environment, by taking into account dielectric strength of the vacuum gap, high-frequency current quenching ability and parasitic components. The PSCAD-model is then verified by data from the testing of a 27 kV VARC dc CB prototype with maximum current interruption capability of 10 kA. Additionally, the initial transient interruption voltage and current slope at zero-crossing during the interruption are analyzed. With respect to scaling to a higher voltage level, three types of series connected modules are presented and the performances are compared. The performance of the series connected modules is simulated in a model of a 4-terminal HVDC grid. The obtained results validate the VARC dc CB as a promising solution for the dc fault isolation in MTDC grids.**

Index Terms—**HVDC circuit breaker, VARC, PSCAD, circuit breaker performance, HVDC grid, transient analysis.**

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I. INTRODUCTION

THE integration of sustainable and renewable technologies is changing the existing transmission system [1]. Significant progress has been made toward the development of Voltage Source Converters (VSCs) in the last few years, which enable meshed HVDC grid to provide a promising technological solution for the connection of offshore wind farms [2]. The meshed HVDC grids are urgently needed to utilize the potential of offshore energy resources, which provide sustainable and renewable energy [3]. However, several major technical barriers need to be conquered before the MTDC grids are realized [4], [5]. Among them, reliable, fast, low-loss and cost-effective HVDC CBs are key components needed to realize the MTDC grid [6].

Due to the absence of current-zeros in a dc system, the development of dc CBs is more difficult than that of ac CBs [7]. HVDC CBs are used to clear dc fault currents and isolate the faults from the HVDC converters, typically the half-bridge based modular multilevel converters (MMC) [8], [9]. The dc faults also need to be cleared in a very short time to prevent the blocking of full bridge MMCs [10]. Furthermore, the fast transients and high short-circuit currents make the dc fault interruption more difficult [11]. The energy stored in the inductance in the HVDC lines needs to be dissipated by the dc CB in order to interrupt the dc fault current [12]. Hence, the dc CB comprises an "energy absorbing branch" containing surge arresters (SAs), connected in parallel with the mechanical switch, and during interruption, the line current is forced to commutate to this branch. The clamping voltage of the SA therefore determines the transient interruption voltage (TIV) that occurs across the interrupting switch during current suppression. The requirements for the energy absorber are large absorption capability, voltage limitation and fast dissipation capability.

Substantial research on HVDC CBs has been done so far and different topologies and concepts have been proposed to protect the multi-terminal HVDC grids [13]–[15]. These HVDC CBs can be sorted into two categories: mechanical circuit breakers and hybrid circuit breakers. In both cases the line current is carried by mechanical contacts during normal operation in a "main branch" while, at switching events, it is temporarily transferred to a parallel branch. In the hybrid breaker, this branch comprises a string of series-connected semiconductor devices having turn-off capability (e.g., IGBTs) which extinguishes the

line current. Mechanical circuit breakers, on the other hand, utilize a parallel branch called "current injection branch", which injects an additional current component through the arc between the contacts of the breaker, while they are parting at opening. The injected current causes a zero-crossing of the total current passing through the mechanical switch, quenching the arc and stopping further current conduction. Once the current in the main branch has been eliminated the voltage across the temporary branch increases until it reaches the clamping voltage of the SA causing the line current to move into the latter.

Therefore, some similarities exist with regards to the basic operation principle of HVDC CBs in the sense that the line current is consecutively moved between the three branches, ending up in the energy absorption branch.

An advantage of mechanical dc CBs is the low conduction losses. However, the long operation delay of traditional spring-based driving mechanisms cannot meet the requirements of fast interruption in dc grids. Recently, the development of ultra-fast actuators based on electromagnetic repulsion mechanisms makes it possible for mechanical dc CBs to clear faults within a few milliseconds [16]–[18]. The hybrid dc CBs, comprising both semiconductors and mechanical interrupter components, combines the advantages of both fast interruption and low on-state losses. Various hybrid dc CB topologies have been proposed in [19]–[21]. During the fault current interruption, the series-connected semiconductor devices need to withstand the very high TIV, resulting in relatively high component costs for hybrid dc CBs.

A newly emerging dc CB concept, the voltage-source-converter resonant current (VARC) dc CB, has been proposed in [22]. The VARC CB utilizes a voltage source converter (VSC) and a series-resonant circuit to effectuate the commutation. The VSC generates a high frequency oscillation current, the amplitude of which gradually increases every half cycle until a zero-crossing is created in the arc current. In [23], the VARC main circuit design aspects are described and the single module prototype test results are demonstrated. For an HVDC application, several VARC modules need to be connected in series in order to reach a sufficient voltage level for the full-scale circuit breaker. For the implementation of VARC CB in an MTDC grid, a detailed model is essential for the transient studies and performance investigations.

The main contribution of this paper is a VARC dc CB model, comparison with existing experimental results, and the comparison of different topologies for series-connection of breaker modules.

The paper is organized as follows. In Section II, detailed modelling of the VARC HVDC CB is presented, including its operation principle and timing sequence. The performance of the model compared to existing experimental test results is presented in Section III, including an analysis of the initial transient interruption voltage (ITIV). In Section IV, a high voltage breaker consisting of VARC dc CB modules is modelled. Three topologies for series connection of VARC modules are demonstrated and analyzed in a 4-terminal HVDC grid. Finally, conclusions based on the results of the study are presented in Section V.
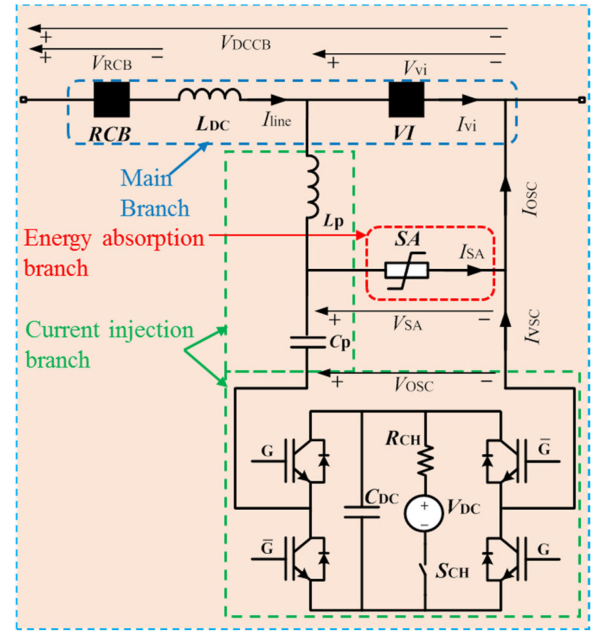

Fig. 1.   Configuration of VARC circuit breaker.

II. DC CIRCUIT BREAKER MODELING

A. Structure of the VARC DC Circuit Breakers

Fig. 1 illustrates the structure of the VARC dc CB. The VARC dc CB consists of three principal branches, which are the main branch, the current injection branch and the energy absorption branch. The main branch comprises a vacuum interrupter (VI), a fault current limiting reactor (L_{DC}), and a residual circuit breaker (RCB). The VI is actuated by an ultra-fast Thomson-coil mechanism to achieve a sufficient contact gap distance in a short time, ensuring adequate dielectric strength for the VI to be able to withstand the TIV during interruption. The fault current limiting reactor effectively prevents the increase of the fault current from rising too fast and limits its amplitude at the interruption instant. The residual circuit breaker is used to separate the main circuit of the breaker from the grid after an interruption. The current injection branch consists of two parts: the first part is an oscillation circuit composed of a capacitor (C_p) and an inductor (L_p); the second part is a VSC, energy storage capacitor (C_{DC}) and a charging circuit (V_{DC}, R_{CH} and S_{CH}) for the energy storage capacitor. The VSC can be controlled to rapidly increase the amplitude of the oscillating current by keeping its output voltage in the same direction as the oscillating current. The current injection branch capacitor (C_p) in the VARC CB is not pre-charged. Instead, the VSC energy storage capacitor (C_{DC}) is pre-charged, at relatively low voltage level, before the operation of the VARC CB.

B. Operating Principles and Timing Sequence

Fig. 2 illustrates the current and voltage waveforms during a typical interruption, where I_{line} is the current through the VARC dc CB, I_{OSC} is the oscillation current in the current injection branch, V_{OSC} is the voltage across the VSC, I_{vi} is the current
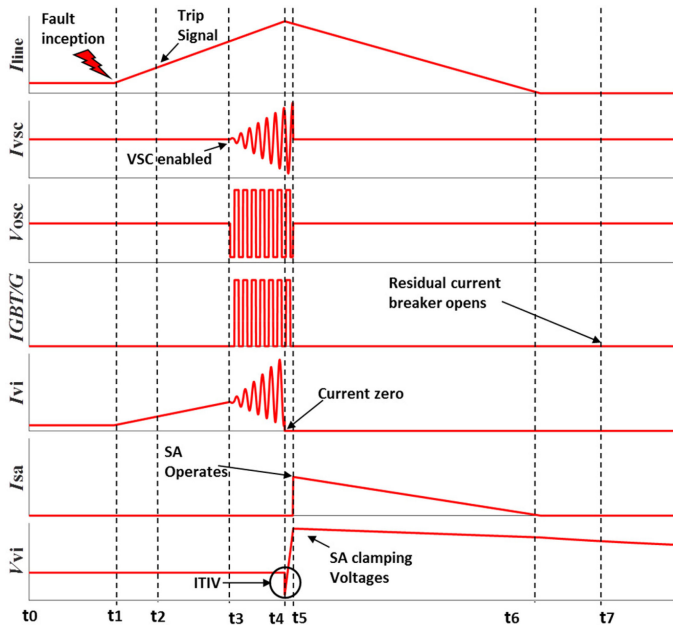
Fig. 2. Relevant voltage and current waveforms of the VARC dc CB.

through the VI, I_{SA} is the current through the SA and V_{vi} is the voltage across the VI. The detailed operation sequence is explained as follows:

1) $t_0 - t_1$: Before the operation of the CB, the VSC energy storage capacitor (C_{DC}) is pre-charged by the charging circuit.

2) $t_1 - t_2$: A fault occurs at instant t_1. As a result, the line current begins to rise, and the rate-of-rise of the line current is limited by the fault current limiting reactor (L_{DC}). At instant t_2, a trip signal is sent to the VARC dc CB.

3) $t_2 - t_3$: The VARC dc CB receives the trip signal at t_2 and the ultra-fast actuator starts to drive the separation of contacts. The contacts in the VI reach a sufficient gap distance to withstand the TIV at t_3.

4) $t_3 - t_4$: Shortly before the VI reaches sufficient contact separation at t_3, the VSC is activated. The oscillating current is generated, and its amplitude gradually increases every half cycle until a zero-crossing is created in the arc current.

5) $t_4 - t_5$: The VI stops to conduct at t_4. As the VI is connected in parallel to the oscillation branch, the initial transient interruption voltage (ITIV) across VI equals the remaining voltage of the current injection branch capacitor. At the same time, the line current is commutated to the current injection branch. During $t_4 - t_5$, the system keeps charging the current injection branch capacitor, until its voltage reaches the clamping voltage of SA at t_5.

6) $t_5 - t_6$: The SA starts to conduct at t_5, and the line current is commutated into the energy absorption branch. The SA current then decreases until it drops to zero at t_6.

7) $t_6 - t_7$: After the fault current interruption, some leakage current may exist in the system, as well as a low frequency interaction between the capacitor in the circuit breaker and the inductance connected in series with the breaker.

The residual circuit breaker is opened at t_7 to clear the leakage current and separate the breaker main circuit from the grid.

The VSC oscillation is enabled at t_3, so that the VARC dc CB can interrupt both the load current and the fault current successfully. If the VSC is enabled too early, the current-zero in the VI might be created too early for the contact gap to withstand the TIV. The choice of components for the resonant circuit depends primarily on the desired TIV and the maximum breaking current. The characteristic impedance of the resonant circuit is chosen close to the ratio between the TIV and the maximum breaking current, whereas the resonant frequency is chosen to provide good conditions for the VI. The current withstand capability of all the components in the current injection branch should also match the maximum breaking current. Details about how to design and choose the parameters of the resonant circuit and other components of the VARC dc CB are presented in [23].

The maximum fault current is determined by the L_{DC} in the DC system and the fault current rise time, which consists of the protection relay tripping time and the dc CB operating time. More explanation about these time instants can be found in [24]. The IGBTs used in the VSC are not required to turn off high currents, since the VSC always switches very close to the current zero crossings. This means that voltage stresses on the converter are minor, however, the peak currents in the converter are as high as the peak fault current. Due to the short time that the converter needs to conduct these currents, it does not present any particular challenges for common off-the shelf components.

C. Oscillation Current and Current Slope at Zero-Crossing

The excitation of the resonant branch current using the VSC is enabled at instant t_3. In the current injection branch, the C_{DC} is in series with the C_p, thus the equivalent capacitance in the oscillation circuit (C_{OSC}) can be obtained by (1). The voltage across C_{OSC} equals the pre-charging voltage (V_{DC}). Hence, the amplitude of the oscillation current in the first half cycle (I_{1p}) is given by (2), and the oscillation angular frequency (ω) is expressed by (3). In the next half cycle, the voltage of the VSC (V_{OSC}) is reversely connected to the oscillation circuit. The V_{OSC} is changed from $-V_{DC}$ to $+V_{DC}$. Subsequently, a $-2V_{DC}$ voltage step is added to the oscillation circuit, which causes the oscillation current amplitude to increase by $2I_{1p}$ every half cycle. Thus, I_{Np} is the current amplitude of the Nth half cycle (4), and N can be calculated by (5). Therefore, the oscillation current in time ($I_{VSC}(t)$) can be determined by (6). When the fault current (I_f) is interrupted at t_I, then zero-crossing is generated at t_I (7). Equation (8) gives the current slope at zero-crossing.

It should be noted that the stray resistance in the oscillation branch is neglected. In practice, the oscillation current is slightly lower due to the damping by stray resistance [23].

$$C_{OSC} = \frac{C_p C_{DC}}{C_p + C_{DC}} \tag{1}$$
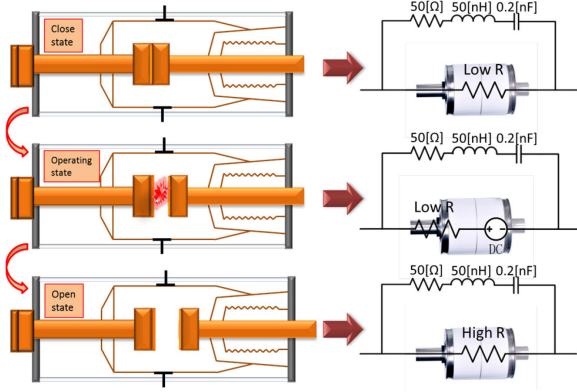
$$I_{1_p} = V_{DC} \sqrt{\frac{C_{OSC}}{L_p}} \tag{2}$$

Fig. 3.   VI state transitions.

$$\omega = \frac{1}{\sqrt{C_{\mathrm{OSC}} L_{\mathrm{p}}}} \tag{3}$$

$$I_{N_{\mathrm{p}}} = (2N - 1) V_{\mathrm{DC}} \sqrt{\frac{C_{\mathrm{OSC}}}{L_{\mathrm{p}}}} \tag{4}$$

$$N = \omega t / \pi \tag{5}$$

$$I_{\mathrm{VSC}}(t) = I_{N_p} \sin(\omega t) \tag{6}$$

$$I_f - I_{\mathrm{VSC}}(t_I) = 0 \tag{7}$$

$$\mathrm{d}i/\mathrm{d}t = I'_{\mathrm{VSC}}(t_I) \tag{8}$$

The oscillating circuit is designed based on the maximum fault current needs to be interrupted. The dimensioning of C_{p}, C_{DC} and L_{p} parameters is a trade-off between the sizing of the components, the high frequency current quenching capability and the peak value of oscillation current. Based on the equations (1)–(5), the oscillation current ($I\mathrm{osc}$) should be higher than fault current to generate current-zero. And the current slop at current zero should be lower than the maximum current quenching capability of VIs. The current quenching capability of a VI varies with several factors such as $\mathrm{d}i/\mathrm{d}t$ prior to current zero, the frequency of injected current and peak current prior to current zero. Since there has been no measured data available, the data published in [25] are used, in which the maximum value range of interruptible $\mathrm{d}i/\mathrm{d}t$ is 150–1000 A/μs. These values have been obtained for 50 Hz ac CBs, and they are used as an estimate of the quenching capability at higher frequency.

The upper and lower limits of oscillating frequency, according to [26] is usually 3 kHz to 10 kHz. The oscillating frequency determines the current slope at current zero and the choice of C_{p} and L_{p} parameters.

D. VI Electrical Model

The VI is modelled as an ideal resistive switch with parasitic components in parallel. The state of the VI can be divided into three categories, namely the closed state, the operating state and the open state, as shown in Fig. 3.

The closed state is modelled as a low resistance with the value of 80 μΩ [27]. The operating state represents the scenarios of re-ignition, restrike and arcing. According to [28], the arc voltage

in VIs is in the order of 20 V to 80 V, which depends on the characteristics of the VIs. The model takes into account the arc characteristic by utilizing a voltage source with a value of 50 V, which represents the arc voltage during current oscillation. As a result, the operating state is modelled as a low resistance in series with a dc voltage source as shown in Fig. 3. The dc voltage source direction is the same as the oscillation current direction. The open state is modelled as a high resistance with the value of 1 TΩ [27].

The parasitic components of the VI are explained in [29] and [26], which are used for system transient studies. In [26], the parasitic capacitance, the inductance and the resistance are connected in series, which are with the value of 0.2 nF, 50 nH and 50 Ω, respectively.

The dielectric strength of the VI is a very important parameter for the analysis of switching transients [29]. When the TIV absolute value exceeds the insulation strength during the interruption process, the VI might not withstand the TIV and a re-ignition could occur. The insulation strength (U_{b}) of the VI depends on the gap distance (s) when $s \geq 5$ mm [30]; f and α are parameters depending on the geometry of the coplanar profile, as (9) where f is 30 kV and α is 0.45. The dynamic gap distance (s) can be obtained as (10) from [22].

The dc CB operates as soon as it receives the trip signal. The actuator operating delay (t_{s}) is 1 ms. During the first millisecond of the actuator opening operation, the actuator experiences pre-tightening force and the gap distance remains zero during this period. Afterwards, the contact separates very quickly with a velocity of 3 m/s, and the gap distance increases linearly until the moving contact hits the damper.

$$U_b(s) = f s^{\alpha} \tag{9}$$

$$s = C(t - t_s) \tag{10}$$

The dynamic gap distance is modelled by making use of the dielectric strength. Once the TIV exceeds the dynamic dielectric strength, the VI cannot withstand the TIV and a re-ignition occurs. If the TIV does not exceed the dielectric strength during the interruption, the VI will remain in open state.

The vacuum arc is not stable when conducting low current. The chopping current represents the current through the interrupter required for an arc to be sustained. The chopping current of the VI mainly depends on the contact material. The chopping current of Cu/Cr contacts varies from 3–8 A [31], [32]. In this paper, a reasonable chopping current is chosen with the value of 5 A. Above this current, the interrupter switch model remains in the closed state. If the VI current drops below the chopping level, the VI is assumed to chop immediately and switch to the open state.

III. MODEL COMPARISON WITH EXPERIMENTAL RESULTS

A. Experimental Data

A VARC dc CB module prototype with a designed current interruption capability of 10 kA and TIV of 40 kV, see Table I,

TABLE I
PARAMETER OF THE TESTED VARC CB MODULE PROTOTYPE

| VARC CB Parameters	Label	Unit	Value
SA clamping voltage	V_{clamp}	kV	40
Oscillation inductance	L_p	μH	19
Oscillation capacitance	C_p	μF	2.5
Energy storage capacitance	C_{DC}	mF	3.75
Parasitic Parameters			
Capacitance across SA	C_x1	nF	5.2
Capacitance from module terminal to ground	C_x2	pF	15
Capacitance across vacuum gap	C_x3	nF	0.2
Resistance across vacuum gap	R_x3	Ω	50
Inductance across vacuum gap	L_x3	nH	50
Stray resistance	R	Ω	0.05
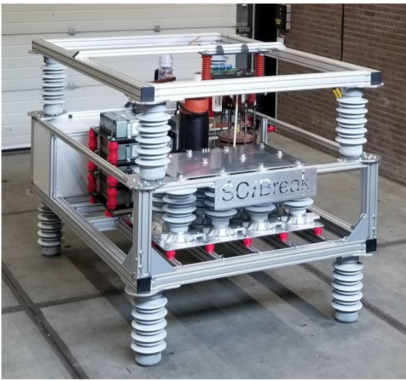
Fig. 4. Prototype of VARC dc CB.
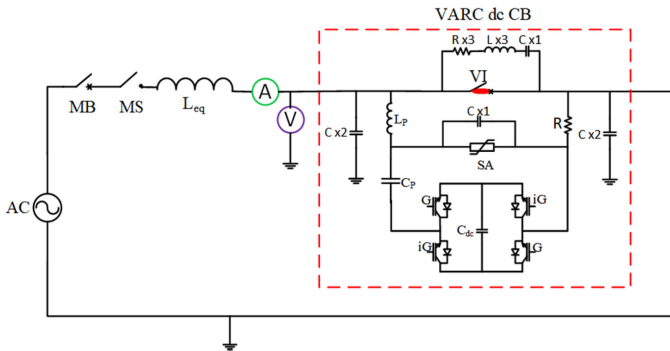
Fig. 5. a) Equivalent circuit for dc CB tests b) VARC CB with parasitic parameters.

was constructed by SCiBreak for testing within the PROMO-TioN EU-project. The prototype of the tested module is shown in Fig. 4 [23].

A series of tests were carried out in 2018 at DNV GL KEMA laboratories in Arnhem, including short-circuit interruption tests in both current directions and a nominal current interruption test.

The dc CB test circuit was supplied by ac short-circuit generators operated at low power frequency, 16.7 Hz. A simplified equivalent circuit is shown in Fig. 5a) [33]. The test circuit was energized by the 16.7 Hz ac voltage source in series with

TABLE II
TEST CIRCUIT PARAMETERS

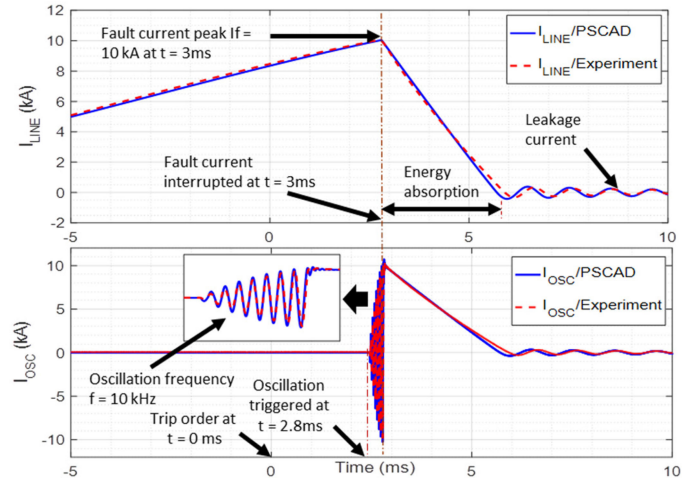| Parameters	Value
AC source voltage	6.76 kV
Series reactor	9.83 mH
θ	13°

Fig. 6. Line currents and oscillation currents; comparison of simulated and experimental results.

a making switch (MS) and an equivalent inductor (L_{eq}). A master breaker is employed to ensure the supply half a cycle current needed for the test. A short-circuit is applied at making angle θ on the source voltage waveform to ensure quasi-dc voltage during the entire current interruption process. After a short-circuit current starts to flow, a trip signal was sent to the VARC dc CB to start the current interruption process. The test circuit parameters for the tests at 10.6 kA are shown in Table II.

B. Model Verification

Comparisons of the results from the earlier experiments and a simulation is shown in Fig. 6 and Fig. 7. In this particular test case, the trip signal is sent to the VARC dc CB at $t = 0$ ms, and the ultra-fast actuator starts to drive the separation of VI. At $t = 2.8$ ms, the gap reaches a sufficient length to withstand the TIV, and the VSC is activated.

Consequently, the oscillation current in the current injection branch starts to oscillate, and the amplitude increases gradually until a current-zero is created in the VI, and the arc is extinguished. The initial V_{DC} is 1.6 kV, and it decreases gradually with the oscillation. As soon as the fault current is interrupted in the VI, the voltage V_{VI} rises sharply and the peak of the V_{vi} is approximately 47 kV. The high frequency oscillation is due to the stray impedance of VI. The high frequency oscillation superimposed on the voltage across the SA, which is limited by the clamping voltage of the SA. The clamping voltage of the SA is 40 kV. The current is commutated into the SA at $t = 3$ ms. Thereafter, the energy is absorbed by the SA and the current gradually decreases towards zero. It can be seen that there are differences between the measured and simulated
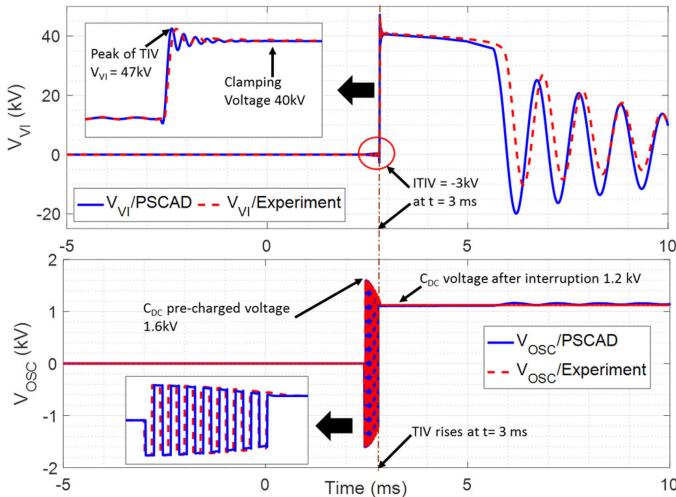
Fig. 7. VI voltages and oscillating voltages; comparison of simulated and experimental results.
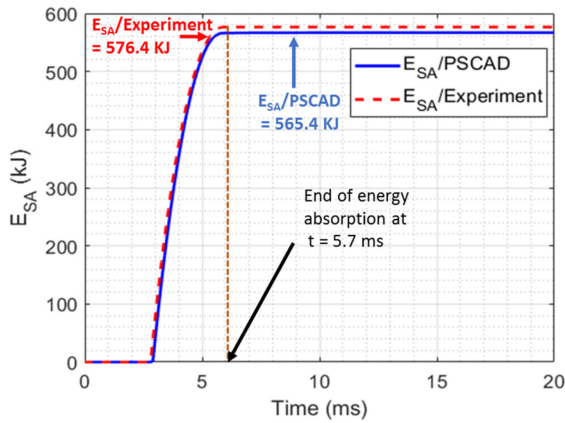

Fig. 8. Energy absorption of the SA; comparison of simulation results and experimental results.

Fig. 9. The relationship between fault currents and ITIV.

voltage after current interruption. This difference stems primarily from differences in I/V characteristics of the default surge arrester model of PSCAD, and the physical devices used in the experiments. The motivation for retaining this model is to not introduce custom components into the modelling. By making use of measured current and voltages across the SA, the energy absorption of the tested module is determined and verified by simulated results as shown in Fig. 8. The slight difference in the energy absorption of around 2% again results from differences in the characteristics of the SA model of PSCAD and that of the physical SA. Consequently, the difference in SA characteristics also leads to the difference in V_{VI} after fault interruption.

The results of the simulations are in good agreement with the values measured during the interruption.

C. Initial Transient Interruption Voltage (ITIV)

The ITIV across the VI at the instant of current-zero is of some interest, since it may impact the current interruption capability of the VI. Before the dc CB operates, the VSC energy storage
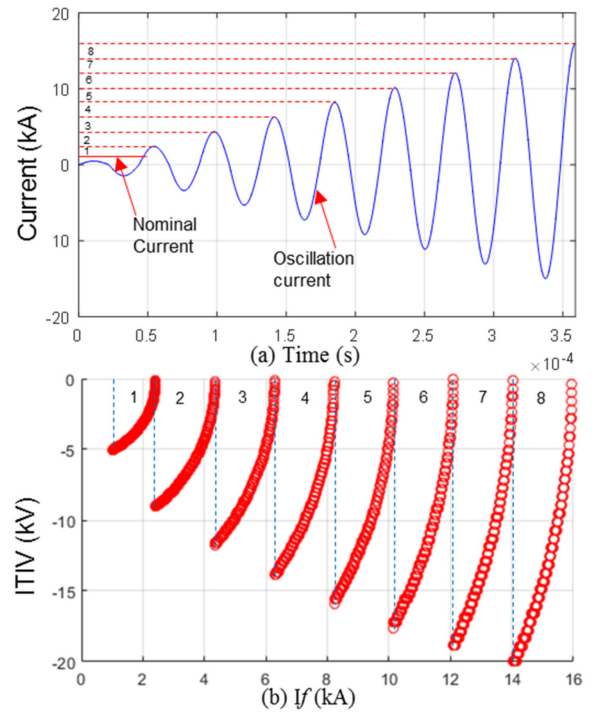
capacitor is pre-charged to V_{DC}. By changing the direction of the output voltage of the VSC at each current-zero of the current injection branch current, a voltage step of size $2V_{\mathrm{DC}}$, and alternating polarity, is superimposed on the resonant circuit. The voltage across the current injection branch capacitor, and the peak voltage across it during the Nth half cycle can be calculated using (12) and (11) respectively. As the VI is connected in parallel with the oscillation circuit, the VI voltage at $t = t_I$ (V_{vi_I}) is (14).

$$V_{n_p} = (2N - 1)\, V_{\mathrm{DC}} \tag{11}$$

$$V_{\mathrm{SA}}(t) = (-1)^N V_{\mathrm{DC}} + (-1)^{N+1} V_{n_p} \cos(\omega t - N\pi) \tag{12}$$

$$t_I = \sin^{-1}\left(I_f / I_{\mathrm{OSC}}(t_I)\right) \tag{13}$$

$$V_{\mathrm{vi}_I} = V_{\mathrm{SA}}(t_I) \tag{14}$$

The ITIV is determined by the fault current I_f, the energy storage capacitor voltage, V_{DC}, and interruption instant, t_I. ITIVs corresponding to interruption of different levels of fault current, with the same type of breaker main circuit, are shown in Fig. 9. After several half-cycles of oscillation, the oscillating current in the current injection branch is sufficient to generate a current zero-crossing in the VI. When the fault current increases from 1 kA to 2.3 kA, the ITIV across the VI changes from -5 kV to approximately 0 kV. In each interval from 1–8, the ITIV decreases from a maximum value to zero when a fault current increase. The VI can withstand -20 kV easily. When the current through the VI reaches zero crossing, the ITIV across VI increases promptly as a step voltage. This is a challenge for the VI in the VARC dc CB. For now, no results have been published regarding the rising rate of the ITIV. However, it should be

pointed out that the negative spike of ITIV should be kept as low as possible.

This peak value of ITIV not only depends on the fault current but it also depends on the L_p and C_p which define the oscillation current frequency. The difference of V_{OSC} between the simulated results and the experimental results are due to the measurement in the experiments. The voltage across VSC in the experiment is measured after the dc CB is triggered. While the voltage across VSC in the simulation is measured throughout the time of the interruption process.

IV. VARC DC CB Using Series Connected Modules

In order to use the VARC dc CB in multi-terminal dc grid, the voltage rating of the design should be scaled to the system level of the network. At the present time, no commercial single-break VIs are available for more than 126 kV. Therefore, several dc CB modules need to be connected in series to construct a breaker for high voltage. Due to the voltage clamping property of the SAs inside the CB modules, n CB modules can be connected in series to achieve the same TIV as one single module (15) with an imagined UHV VI. The distance s_1 in the equation is the gap distance in one single equivalent module, and s_n is the gap in n modules. As we can see from (16), the sum of gap distance in n modules, for the same dielectric withstand capability, is shorter than that in a single VI. The insulation strength (U_b) of the VI is a function of the gap distance (s) [30]; f and α are parameters depending on the geometry of the coplanar profile, as (15) where f is 30 kV and α is 0.45.

$$f s_1^\alpha = n f s_n^\alpha \tag{15}$$

$$\frac{n s_n}{s_1} = \left(\frac{1}{n}\right)^{\frac{1-\alpha}{\alpha}} < 1 \tag{16}$$

The total opening velocity for equivalent dielectric withstand capability in n modules, v_n, can be calculated by the same principle (17), (18). v_1 is the opening velocity in a single VI.

$$v_1 = s_1/t \tag{17}$$

$$v_n = \frac{s_1}{n \cdot t} \cdot \left(\frac{1}{n}\right)^{\frac{1-\alpha}{\alpha}} = \left(\frac{1}{n}\right)^{\frac{1}{\alpha}} \cdot v_1 < v_1 \tag{18}$$

According to (18), in order to achieve the same dielectric strength, the series connection separating velocity v_n is lower than that of one module v_1. Therefore, with the same ultra-fast driving mechanism of the dc CB, the series connection can achieve higher dielectric strength within a shorter time.

A. Structure of Series Connection

Three types of series-connection topologies are shown in Fig. 10a)-c). During steady state, the performance of these three topologies is the same. The difference between these structures is mainly the connection of SAs. The series connection topologies are designed to withstand the maximum system operation voltage, and the SA clamping voltage is selected to be 1.5 times the rated system voltage.
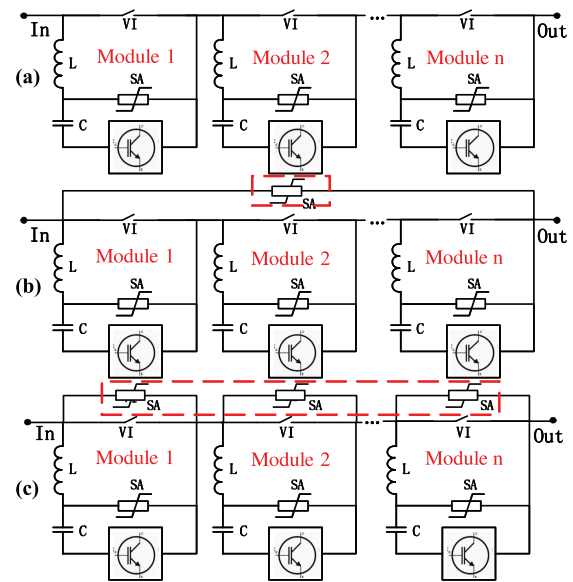

Fig. 10. Series connection topologies of VARC CB modules.

A benefit of the modularized construction of the dc CB is that the SA energy rating can be selected in such a way that n-1 modules successfully can operate as a full circuit breaker, making redundancy inherent in the concept. In the configuration shown in Fig. 10a), n modules are simply connected in series. For the MTDC grid, the fault current amplitude at each terminal is different, which depends on the MTDC structure, cable length and power flow. Therefore, the required dc CB rating depends on its application and location. Meanwhile, for the future MTDC grid more terminals will be connected to the existing grid, which results in the change of fault range. As shown in the configuration Fig. 10b) and c), an additional external SA is connected in parallel with the series modules. The prospective clamping voltage external SA is 1.5 times the rated system voltage, and the SAs inside the VARC modules are higher than 1.5 times the rated system voltage. In this way, the majority of the energy resulting from the interruption is absorbed by the external SA, and the module design is not affected by the energy rating required by the internal SA. For example, the possible effect from varying SA stray capacitance inside the breaker module can be disregarded.

B. Performance With Different Internal SAs Clamping Voltages

Fig. 11 and Fig. 12 shows the fault current interruption performance for different internal SA clamping voltages and associated energy absorption by the external SA for the topologies b) and c), respectively. It should be pointed out that when all the modules operate at the same time, topology b) and topology c) have the same performance. Hence, topology b) results have been chosen for the illustration of the effects of varying internal clamping voltage.

Described topologies in Fig. 10 consists of four 80 kV modules connected in series. The clamping voltages of the internal SAs in each module are 120 kV, 140 kV and 160 kV, respectively. The clamping voltage of the external SA is 1.5×320 kV =
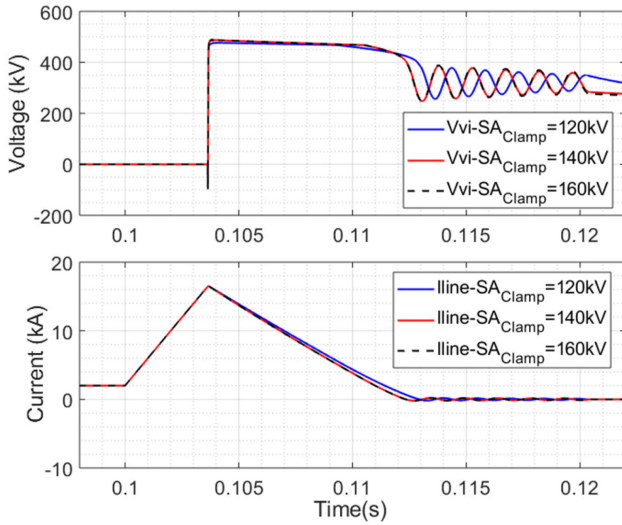
Fig. 11. Comparison of VI voltages and line currents for different clamping voltages for topology b) as shown in Fig. 10.
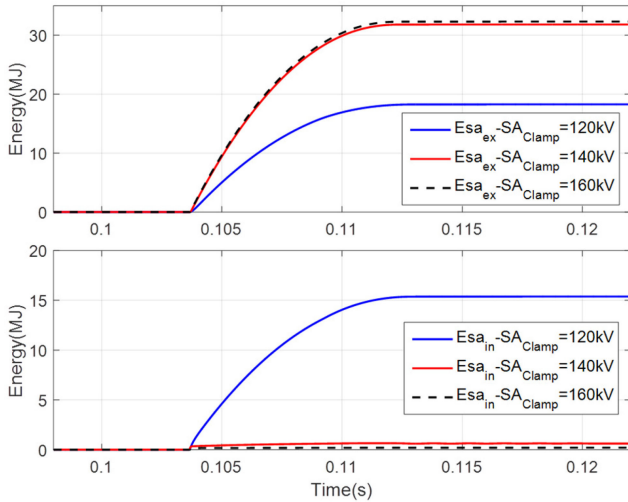

Fig. 12. Comparison of external SA energy absorption for different clamping voltages for topology b) as shown in Fig. 10.
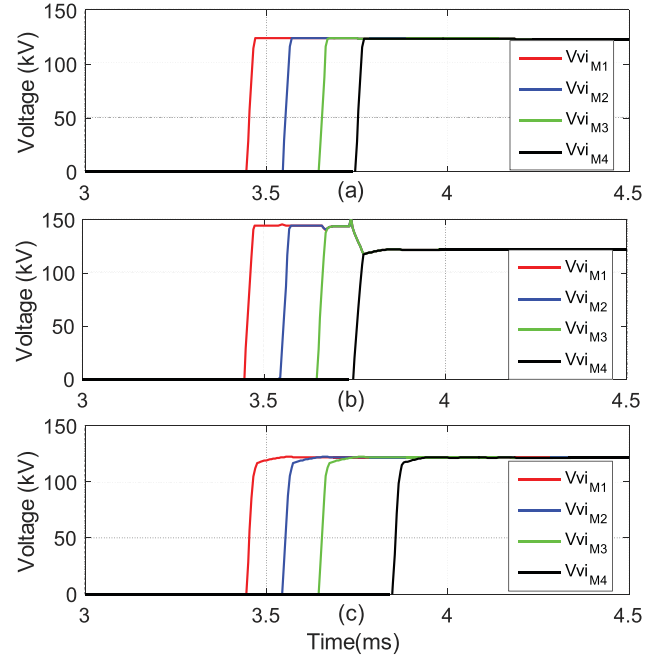

Fig. 13. VI voltages of four modules for different operation delay; upper graph – type (a) topology; middle graph – type (b) topology; lower graph – type (c) topology.

480 kV. In case when the internal clamping voltage of each module is 120 kV, the internal SAs absorbs 15.4 MJ, whilst the absorption of the external SA is 18.3 MJ. For clamping voltages of 140 kV and 160 kV, the external SA absorbs almost all the energy whilst the energy absorption by the internal SAs is negligible. By increasing the clamping voltage from 120 kV to 140 kV, the current interruption time decreases and the absorbed energy decreases to 32.6 MJ. Furthermore, when the clamping voltage is 160 kV, the interruption time remain the same. And the energy absorption in this case is 32.5 MJ.

C. Performance With Different Operation Delay

This example demonstrates the module performance for different operation delays for type a), b) and c) topology. In this case, the VSC oscillation is enabled around 3 ms. Exact operation times are slightly different from each other, which

are 2.8 ms, 2.9 ms, 3 ms and 3.1 ms for module 1,2,3 and 4, respectively.

Fig. 13 shows the voltages across the VIs during the fault current interruption by the four modules. The time of initial voltage rise corresponds to the instant when the current zero is reached. The oscillation currents in module 1 and 2 are injected earlier than expected, whilst for module 4 the injection is delayed. For type b) and c), the internal SAs clamping voltage in each module is set to 140 kV. Fig. 14 shows the energy absorption of each topology. Type a) has only internal SAs whilst type b) and c) have also an external SA which is denoted by an subscript "$_{EX}$".

It can be seen that for type a), the voltages across four modules are limited by the internal SAs to a value of 120 kV and the instant of energy absorption for all four modules is in line with the instant when clamping voltage is reached as shown in Fig. 13(a). The energy absorption is not equally divided among the SAs of the modules. For type b), the voltages across module 1, 2, 3 reaches 140 kV, which are limited by the internal SAs. After the current is interrupted, the voltage across all four modules are limited by the external SA with the value of 480 kV (Esa$_{EX}$), which is four times 120 kV as shown in Fig. 13. Thereafter, the voltage is distributed equally among the modules and great amount of the energy is absorbed by the external SA as shown in Fig. 14(b).

For type c), energy absorption begins at the time when the clamping voltage of the first module is reached. It is then shared equally among the modules even during different operation delays. For this topology, each module makes use of an external SA, which in this example has a clamping voltage of 120 kV. As the values of the clamping voltages of the internal SAs are
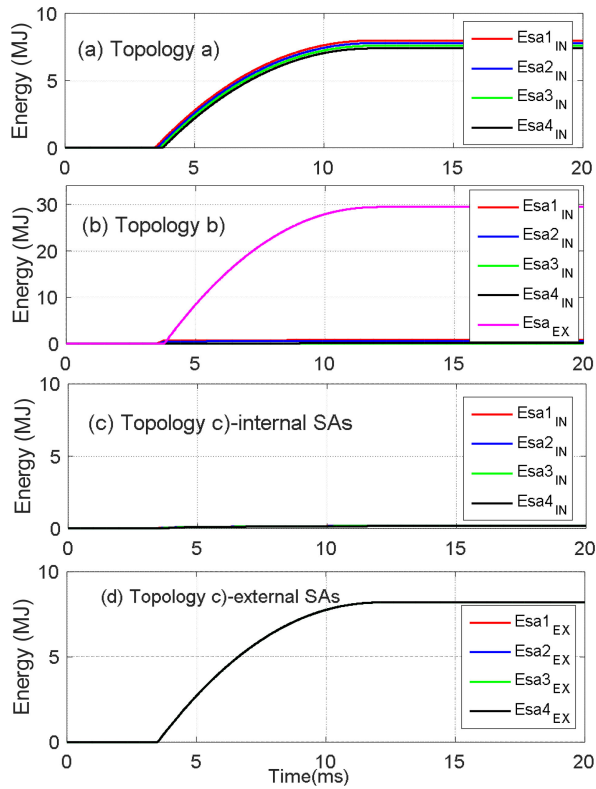
Fig. 14. Energy absorption of the SAs; (a) topology a); (b) topology b); (c) topology c) – internal SAs; (d) topology c) external SAs.
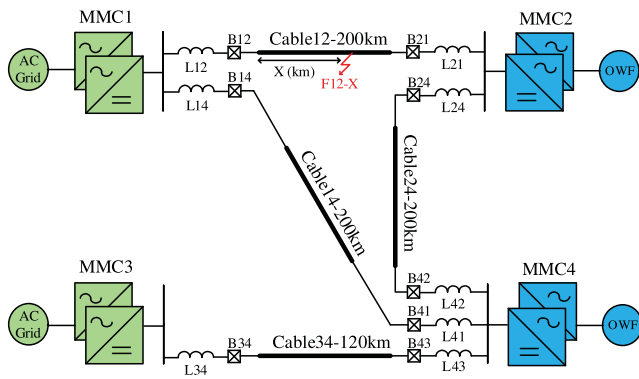

Fig. 15. Configuration of demonstration system.

140 kV, all the energy will be absorbed by the external SAs. This is clearly demonstrated in Fig. 14c) and d).

D. Interruption Performance of Series Connected Modules

The performance of a dc CB consisting of series connected modules is demonstrated in a 4-terminal MTDC system. A feasible MTDC network is developed for future offshore windfarms and some of the data about the components of the demonstration system are taken from [34]. The converters are half-bridge bipolar MMCs. The configuration of the studied 4-terminal MTDC system is shown in Fig. 15. Converters MMC2 and MMC4 connect the offshore wind power plant, and MMC1 and MMC3 connect the onshore ac grid. The MMC1, MMC2 and MMC4

TABLE III
DATA OF DEMONSTRATION 4-TERMINAL MTDC SYSTEM

| Parameter	Converters			
	MMCs 1	MMC 2	MMC 3	MMC 4
Active power	1200 MW	1000 MW	800 MW	1000 MW
Control mode	PVdc	PQ	PVdc	PQ
Reactive power	0 MVAR	0 MVAR	0 MVAR	0 MVAR
DC link Voltage	±320 kV			
Rated power	1200 MW			
Number of SMs per arm	400			
Arm capacitance C_{arm}	22 μF			
Arm reactor L_{arm}	42 mH			
Arm resistance R_{arm}	0.08 Ω			
AC converter voltage	166 kV			
Transformer leakage reactance	0.18 p.u			
AC grids and windfarms				
AC grids voltage	400 kV			
Windfarm output voltage	66 kV			
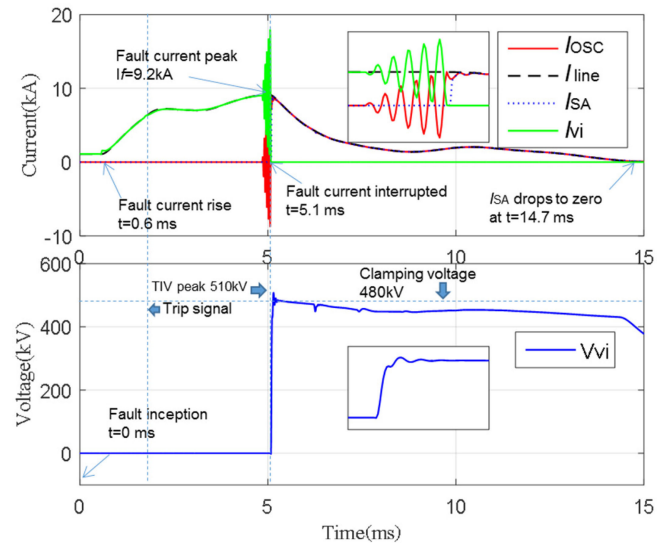
Fig. 16. Performance of short-circuit fault current interruption by B21.

are connected to each other by a 200 km cable, and MMC4 is connected to MMC3 by cable with a length of 120 km. The data of the 4-terminal MTDC system is shown in Table III, and it is modelled in a PSCAD environment.

The VARC dc CBs and the current limiting inductors are implemented at each bus terminal. In each of these VARC dc CBs, 12 modules are connected in series with the configuration shown in Fig. 10c). Two representative fault current interruptions are demonstrated in the 4-terminal MTDC system, which are short-circuit fault current interruption and reverse current interruption, respectively. It is noticeable that the fault current amplitudes are influenced by the fault location and the fault resistance. The fault is assumed to be detected instantly, and the trip signal is sent to the dc CB at the same time. The demonstration results are shown as follows:

1) Short-Circuit Fault Current Interruption: Fig. 16 shows a successful fault current interruption by the VARC dc CB located at B21 positive pole. The pole-to-pole fault occurs at 100 km of Cable12, with a fault resistance $R_f = 0.1$ Ω. The fault occurs at
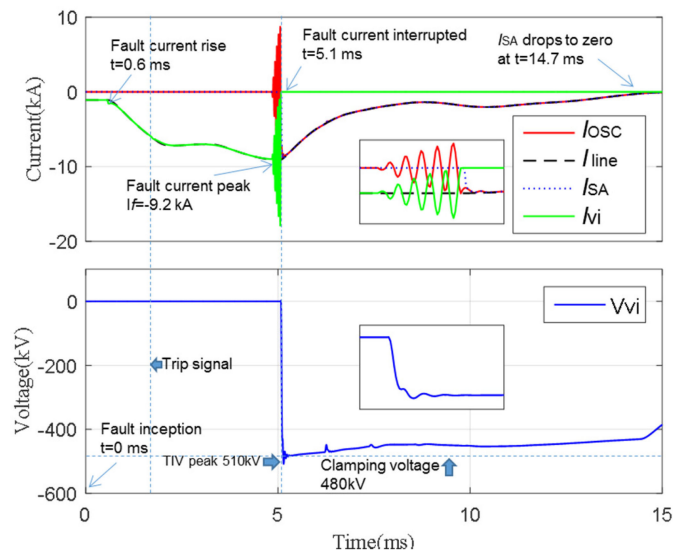
Fig. 17. Performance during reverse direction fault current interruption by breaker B21.

t = 0 ms, and the line current starts to rise consequently. The fault current at dc CB B21 starts to rise at t = 0.6 ms.

The fault current rate-of- rise is limited due to the inductance in the system. The trip signal is sent to the dc CB at t = 2 ms, and as soon as dc CB receives the trip signal, the ultra-fast actuator starts opening the VI contacts. At t = 5 ms, the gap reaches a sufficient size to withstand the TIV, and the VSC oscillation is enabled. Hence, the oscillation current in the current injection branch starts to oscillate, and its amplitude increases gradually until the current-zero is reached. As soon as the fault current is interrupted in the VI, V_{DCCB} rises sharply and reaches a peak value of ∼510 kV, which is limited by the clamping voltage of the SA. High frequency oscillation voltage superimposes on the peak of V_{DCCB} due to the parasitic components existing in the circuit. The SA starts conducting at t = 5.1 ms when V_{DCCB} reaches the clamping voltage, and the current is commutated into the SA. Thereafter, the energy stored in the system is absorbed by the SA and the SA current gradually decreases towards zero. One may note that the ITIV for this case has a negligible value. As explained in III.C, the ITIV depends on the oscillating current during the interruption process. In the case when the fault current is close to the peak of the oscillating current, the ITIV may have low or negligible values.

2) Reverse Direction Current Interruption: The performance of the VARC dc CB located at B21 negative pole during reverse direction current interruption is demonstrated in Fig. 17. The dc CB experiences a pre-fault current of −1 kA. The VARC dc CB interrupts the fault current in the typical manner after receiving the trip signal. The VARC CB is capable of interrupting bidirectional fault current. Meanwhile, withstanding the TIV of the opposite polarity as well.

V. CONCLUSION

The VARC dc CB provides a dc interruption solution for multi-terminal HVDC grids. The implementation of ultra-fast actuator significantly improves the capability to clear the fault within 3 ms after receiving a trip signal.

When the oscillation current amplitude gradually increases every half cycle, until a zero-crossing occurs, the worst-case current slope at current-zero significantly is reduced for both the nominal current interruption and the short-circuit interruption. This improves the current interruption capability of the mechanical switch.

The developed model, however, cannot be used as a deterministic model for a risk assessment for the interruption in practice. The VARC dc CB model can, however, be used for overvoltage analysis, fast transient analysis and re-ignition performance analysis. These phenomena play a very important role during dc current interruption and as such it can be used to study the effect of current interruption in an actual network topology, and how different network parameters affect the dc CB. Meanwhile, the parasitic components existing in the circuit can be calculated by the model, which may have impacts on the transient performance during current interruption.

The developed VARC dc CB model is compared by measurements from the experimental results performed with the prototype design shown in Fig. 4. The current waveforms obtained from the simulation studies show good agreement with the experimental results. The small difference can be seen in the VI voltage due to the difference of the SA characteristic applied in the simulation and the actual one resulting from the SA installed in the dc CB. The ITIV is computed and analyzed. The measured values resulting from the experiments are slightly lower than the computed results because of the parasitic components. When an existing grid is connected to a future MTDC, the fault current ratings are expected to increase. Since the VARC dc CB operates on the principle of gradually increased oscillation current, the breaker is inherently suitable for a wide range of fault currents, up to the peak current injection branch current that can be carried without exceeding the maximum capability of components.

The VARC dc CB can be implemented for higher voltage levels by connecting breaker modules in series. Topology c) shows better performance as the voltage and energy absorption is equally distributed among the modules. The performance of short-circuit interruption and reverse current interruption are demonstrated in a 320 kV, 4-terminal HVDC grids. Based on the extensive study and achieved results, VARC dc CB is a promising topology that can be applied in MTDC grids applications. We also point out that in the future more work will be done in order to see the performance of the dc CB for different pre-fault currents, reclosing, different network topologies and different fault locations.

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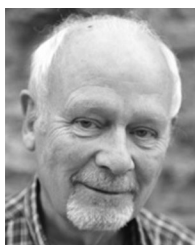
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