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A Transceiver ASIC for a Single-Cable 64-Element Intra-Vascular Ultrasound Probe

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***Abstract*— This article presents an application-specific integrated circuit (ASIC) designed for intra-vascular ultrasound imaging that interfaces 64 piezoelectric transducer elements to an imaging system using a single micro-coaxial cable. Thus, it allows a single-element transducer to be replaced by a transducer array to enable 3-D imaging. The 1.5-mm-diameter ASIC is intended to be mounted at the tip of a catheter, directly integrated with a 2-D array of piezoelectric transducer elements. For each of these elements, the ASIC contains a high-voltage (HV) switch, allowing the elements to transmit an acoustic wave in response to an HV pulse generated by the imaging system. A low-noise amplifier then amplifies the resulting echo signals and relays them as a signal current to the imaging system, while the same cable provides a 3-V supply. Element selection and other settings can be programmed by modulating configuration data on the supply, thus enabling full synthetic aperture imaging. An integrated element test mode measures the element capacitance to detect bad connections to the transducer elements. The ASIC has been fabricated in a 0.18-μm HV CMOS technology and consumes only 6 mW in receive. Electrical measurements show correct switching of 30-V transmit pulses and a receive amplification with a 71-dB dynamic range, including 12 dB of programmable gain over a 3-dB bandwidth of 21 MHz. The functionality of the ASIC has been successfully demonstrated in a 3-D imaging experiment.**

***Index Terms*— Element test mode, front-end application-specific integrated circuit (ASIC), intra-vascular ultrasound (IVUS), single cable, transceiver ASIC, ultrasound.**

I. Introduction

FORWARD-looking intra-vascular ultrasound (IVUS) can be a very useful tool in the treatment of chronic total occlusions (CTOs). A forward-looking IVUS probe can be used to locate a small hole in stenosis, to help opening the occlusion [1], [2]. Single-element probes with rotating or moving transducer elements have been proposed to implement probes with a small catheter diameter. It has also been shown that it is possible to reconstruct the 3-D images from data collected using a rotating single element with a lens [3]. However, the moving parts inside the catheter increase the complexity significantly and can also cause motion artifacts when imaging. Alternatively, array transducers can be used. Using an array, images can be created while having a stationary probe, reducing the mechanical complexity of the catheter. A major difficulty with arrays is that a large number of transducer elements have to be driven and read out. The size of the arteries limits the diameter of the catheter and thus the number of cables that can be used to transport signals from the tip to an imaging system. Prior work has shown that the number of cables can be reduced to a fraction of the number of elements [4]–[7], by using front-end application-specific integrated circuits (ASICs). Good quality images can be reconstructed using ASICs that are connected to the imaging system with four or more cables.

This work describes an ASIC that allows an array of transducer elements to be interfaced with an imaging system using only a single micro-coaxial cable, thus enabling 3-D imaging within the electrical and mechanical constraints of a single-element probe [8], [9]. The ASIC has been designed to interface with conventional pulse-echo imaging systems, which provide high-voltage (HV) pulses to a transducer to transmit an acoustic wave and then record the resulting echo signals. By means of programmable HV switches, the ASIC routes the pulse generated by the system to a selected subset of the elements. An on-chip low-noise amplifier (LNA) then amplifies the echo signals received by a selected transducer element and sends them to the imaging system. Thus, the ASIC allows the array to be treated as a digitally programmable single-element transducer and enables synthetic aperture imaging, in which an image is constructed by successively pulsing and receiving on the elements of the array. It also features an element test mode, intended to test whether all transducer elements are correctly connected to the circuitry. While the ASIC has been designed for an IVUS probe, the concepts can also be applied in other size-constrained ultrasound imaging applications.

In Section II, we describe the proposed system architecture. Section III discusses the details of the circuit implementation. Section IV presents the electrical and acoustical measurements. Section V and VI discuss the results and present the conclusions.

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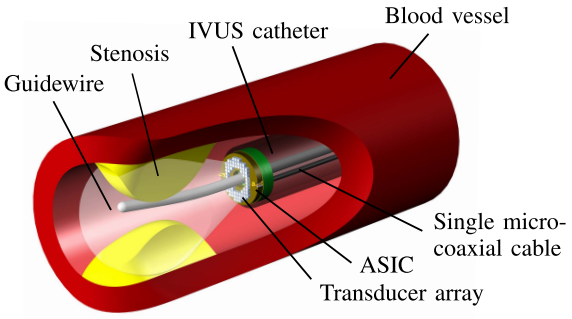


Fig. 1. Artist's impression of the ASIC mounted onto a catheter.

II. System Architecture

An ASIC has been designed to transmit and receive with an array of 64 piezoelectric transducer elements based on lead zirconate titanate (PZT), integrated directly on top of the ASIC, to create a forward-looking ultrasound probe. The transducers have a resonance frequency of 13 MHz, a resistance of 5 kΩ, and a capacitance of 0.7 pF at resonance. The element layout and acoustic design are similar to the work presented in [10], with the addition that all elements can be used to transmit and receive. The ASIC is connected using a single micro-coaxial cable and features a circular layout with a central hole to allow a guidewire to protrude, as shown in the artist's impression in Fig. 1.

To allow the ASIC to be connected to a conventional imaging system, an additional circuit on the system side is used to drive, configure, and read out the ASIC. The ASIC cycles through three modes. First, configuration data are sent to select the elements that will be active in the upcoming transmit–receive cycle. Second, an HV transmit (TX) pulse is applied to the selected transducer elements. Such a pulse could be generated on-chip using an HV pulser, but this limits the TX waveforms that can be generated to simple square-wave pulses [7]. Instead, to keep flexibility in choosing the TX waveform and its duration, the pulse is generated by the imaging system and routed by the ASIC to the selected subset of elements. Finally, after the transmit pulse, the ASIC switches to receive mode, amplifying the signal current generated by the selected receive element in response to the incoming acoustic echoes. The amplified current is sent over the cable, while the ASIC is supplied with a 3-V supply.

A block diagram of the ASIC is shown in Fig. 2. Programmable switches S_{tx} are used to connect the transducer elements to the cable for transmission. In receive, multiplexer S_{rx} is used to connect one of the transducer elements to an LNA. The LNA is required because a direct connection of the cable to the transducer, which has a very high impedance compared to the cable, would attenuate the signal significantly

The LNA is powered by a dc voltage of 3 V supplied over the cable. To be able to image using the transducer matrix, switches have to connect the individual transducer elements to the cable, the receive amplifier, or ground if not used (S_{gnd}). To configure those switches, self-clocking data are superimposed on the power supply. Pulsewidth modulation (PWM) was chosen, as only a simple circuit is required to recover the clock and data signal on the ASIC. Compared with other schemes, such as Manchester encoding, PWM-encoding has the benefit that all rising edges are spaced one clock period apart, resulting in easy clock recovery. Inside the ASIC, the data are recovered by an ac-coupled (via capacitor C_3) clock and data recovery (CDR) circuit and then used to program a configuration shift register. A low-dropout (LDO) regulator prevents the modulated supply from affecting the operation of the associated logic. After configuration, the data are latched and the LNA is switched OFF to reduce power consumption in the TX phase.

After configuration, a high-voltage transmit signal with a maximum peak amplitude of 30 V can be applied to the cable, which will drive the transducer elements selected for transmit to generate an acoustic pulse. Compared to using on-chip pulsers, this results in a lower power dissipation inside the ASIC and allows the pulse waveform to be defined on the system side. Transistors M_1 and M_3 clamp the high-voltage transmit signal to protect the low-voltage circuitry. A bias circuit (not shown) generates bias currents and the clamping voltage (V_{clamp}), which is stored on a capacitor during TX, when a stable supply voltage is absent.

The circuitry in the ASIC has to turn off the TX switches when it switches to RX mode; otherwise, the switch creates a short circuit between the output of the LNA and the transducer, rendering the LNA useless. To determine when the ASIC should switch to RX mode one could use a timing circuit, this, however, would limit the flexibility in duration of the transmit waveform. The start of the receive phase is therefore determined by a level detector circuit combined with a timer. When the signal on the cable, V_{cable}, is below 6 V for more than 200 ns, the ASIC switches to RX mode by turning off the TX switches and enabling the LNA and receive multiplexer. The 200-ns delay allows transmit waveforms to swing over the full voltage range and go below the 6-V threshold, provided that the frequency is high enough for the timer inside the level detector not to trigger.

The acoustic echoes, received by the element selected for receive, create a small-signal current that is amplified by the LNA. Because the transducers have a relatively high impedance, a topology with a low input impedance was used, in order to amplify the signal current. The LNA also functions as the cable driver. Commonly, voltage mode cable drivers are used [11]; they have to drive the full cable capacitance, requiring a power-hungry on-chip cable driver. In this work, we use current-mode signaling that is more power-efficient because the system spends the power to drive the cable voltage, while the on-chip cable driver only has to draw current from the cable. Since only a single cable is used, the supply current is also part of the signal, recognizable as a constant offset because the logic is quiet in the RX period. This offset can easily be filtered out on the system side by high-pass filtering of the signal.

III. Circuit Implementation

A. Transmit Switches

In transmit, HV pulses are required to actuate the piezo material and thus generate acoustic pulses that lead to echo

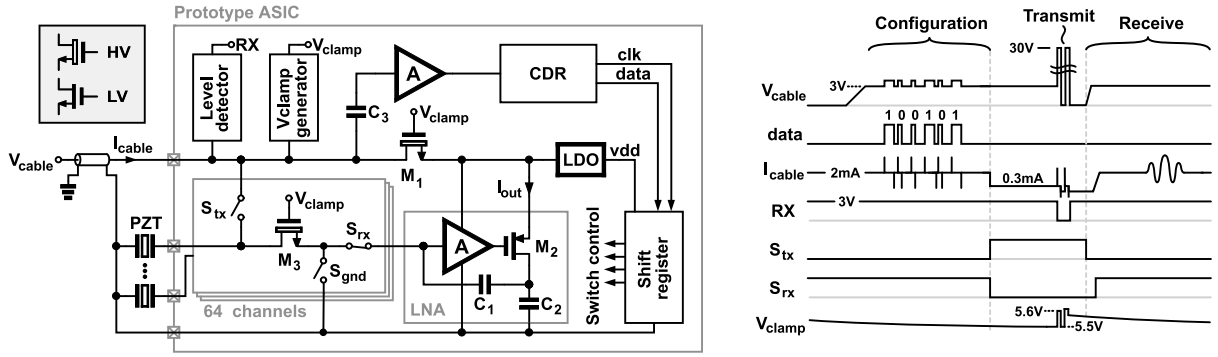


Fig. 2. Block diagram of the prototype ASIC and corresponding waveforms.

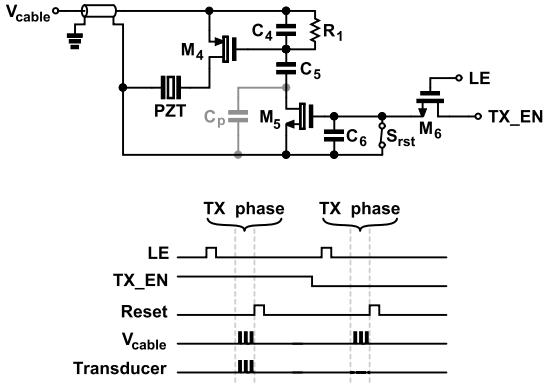


Fig. 3. Circuit implementation of latching transmit switch.

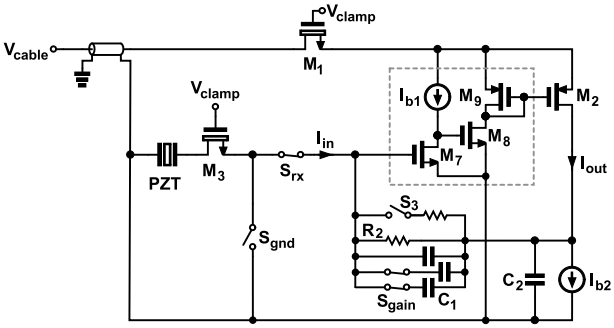


Fig. 4. Circuit implementation of the LNA.

signals with sufficient SNR. To allow transmit beamforming, switches are used that either pass or block an HV signal generated by the system. In prior work, driver circuits have been reported for HV switches using level shifters [12], [13] or a floating capacitor [14]. Those topologies, however, require an HV supply to be present and occupy a significant die area. As a small-area alternative, a switch driver based on a capacitive divider is used, similar to the switch demonstrated in [15].

Fig. 3 shows the circuit implementation of the transmit switches. During configuration, the data bit that controls the switch (TX_EN) is latched (using LE) on capacitor C_6, turning M_5 on or off. When M_5 is on, C_4 and C_5 form a capacitive divider, causing M_4 to turn on with a safe gate voltage when an HV pulse is applied. When M_5 is OFF, the parasitic capacitance of M_5, C_p, appears in series with C_5. Because C_4 and C_5 are much larger than this parasitic capacitance, the gate–source voltage on M_4 now remains small when an HV pulse is applied, ensuring that the TX switch stays OFF. When the ASIC switches back to receive mode, S_{rst} is used to turn off the switches until the next configuration phase. Pseudo-resistor R_1 defines the dc state of the TX switch. Because the switch structure does not require a supply voltage during TX and is substantially smaller (7300 μm^2) than conventional level-shifter-based switches, this topology allows 64 switches to be integrated on the ASIC.

B. Low-Noise Amplifier

The circuit implementation of the LNA and receive multiplexer is shown in Fig. 4. The multiplexer is controlled by the shift register and connects one of the 64 elements to the LNA. Unused elements are grounded by S_{gnd} to prevent capacitive feed-through and cross coupling between the receive channels.

The main purpose of the LNA is to buffer the receive signal such that it can drive the coaxial cable without significant attenuation. Since only the single cable is available, a topology is required that outputs the signal as a current. The LNA has a current gain I_{out}/I_{in} of $1 + C_2/C_1$ [16], where C_1 can be switched to program the gain in two 6-dB steps (50, 100, and 200). Reset switch S_3 brings the voltage on the transducer to the correct biasing voltage (800 mV) after TX. High-impedance resistor R_2 maintains the dc bias for long RX cycles and prevents drift due to leakage currents. Input transistor M_7 is biased at 600 μA to obtain an input noise level around 1 pA/$\sqrt{\text{Hz}}$. The second stage (M_8 and M_9) is needed to create the signal inversion required for negative feedback. The output stage (M_2) is biased at 800 μA to generate the desired signal-dependent supply current I_{out}.

C. Element Test Mode

With the delicate fabrication methods [17] required to make a miniature ultrasound probe, it can happen that elements are defective, shorted together, or not connected at all [18]. To detect such fabrication issues, a test mode has been integrated. It exploits the fact that the element capacitance

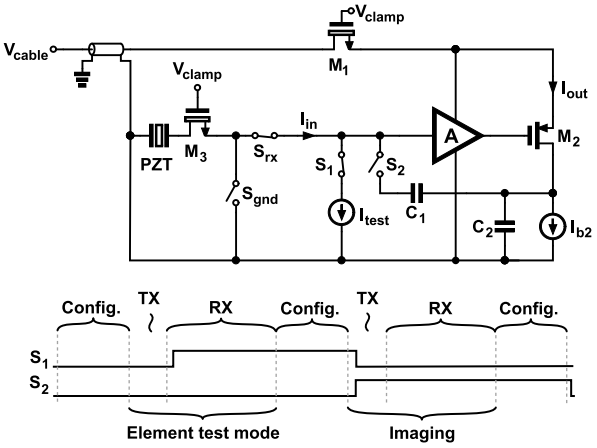


Fig. 5. LNA configured for element test mode.

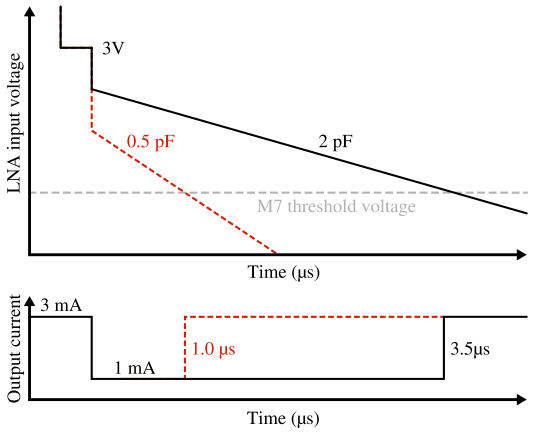


Fig. 6. Waveforms of the amplifier configured in test mode.

C_{PZT} holds the voltage applied by the system at the end of the TX phase, allowing it to be pre-charged to a known voltage. Fig. 5 shows how the LNA is reconfigured as a comparator to create the test mode circuit. A current source I_{test} is then used to discharge the element. The time required to do so is proportional to C_{PZT}. This time is measured by using the LNA as a comparator, by opening its feedback network with switch S_2, causing its output current to toggle when the voltage on the piezo material crosses the threshold of M_7. This results in a current pulse with a length proportional to C_{PZT}, which can be detected at the system side, thus enabling automatic testing of the transducer element connections.

Two reference capacitors (0.5 and 1.0 pF) were integrated on the ASIC to get an indication of the magnitude of the capacitance.

Fig. 6 shows with element capacitances of 0.5 and 2 pF how the element test mode works. After the TX phase, the voltage is purposely not returned to zero, leaving a voltage of 3 V on the input node of the LNA, limited by the clamp M_3. As soon as the ASIC switches to receive mode, the switch S_{rx} will close and the charge of the transducer element is shared with the input capacitance of the LNA, causing the voltage to step down. Subsequently, the current source I_{test} will

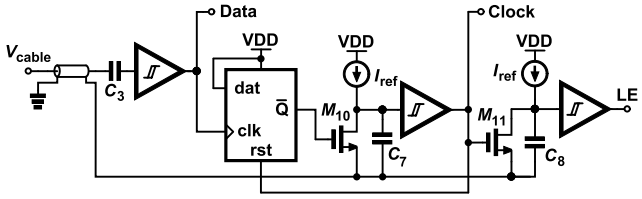


Fig. 7. Block diagram of data recovery circuit.

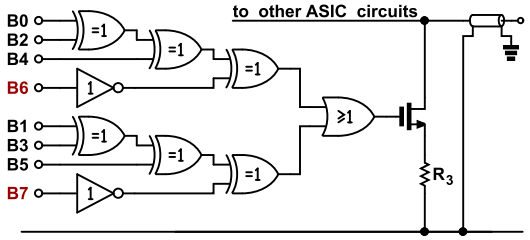


Fig. 8. Circuit used to return the CRC result to the system, where B0–B7 represent the data of one 8-bit shift register, and B6 and B7 are the CRC bits.

start discharging the capacitor, causing the output to toggle when the comparator reference voltage (threshold) is crossed. The consequence of the charge-sharing when switching to RX-mode is a minimum detectable capacitance, below which the comparator always toggles on the charge-sharing event. Since the feedback loop of the LNA is opened in element test mode, the normal receive mode is disabled until the next configuration phase.

D. Configuration

The transmit switches and receive multiplexer inside the ASIC have to be programmed prior to a transmit–receive cycle. PWM data are superimposed on the power supply to be able to send in total 88 bits of configuration data to the ASIC. Of the 88 bits, 64 bits are used for the TX switches, while the other bits are used for selecting the receive channel and configuring settings, such as the element test mode and LNA gain. The clock and data are recovered from the PWM signal by amplifying and thresholding the ac-coupled signal, as shown in Fig. 7. A current source charges capacitor C_7, which is reset by transistor M_{10} with every rising edge of the data signal. The time it takes for I_{ref} to charge C_7 determines the clock period. After the data have been read in, the absence of new clock cycles causes the voltage on C_8 to rise and toggle the Schmitt trigger, latching the new configuration settings.

A 2-bit cyclic redundancy check (CRC) is performed on the shift register data, using the circuit shown in Fig. 8, to confirm correct data transmission. In case of an incorrect transmission, a shunting resistor (R_3) is switched ON, increasing the power consumption. By monitoring the power consumption, erroneous data can be detected and the data retransmitted.

E. System Side Circuitry

On the system side, additional circuitry is used to interface the ASIC with a conventional imaging system. Fig. 9 shows

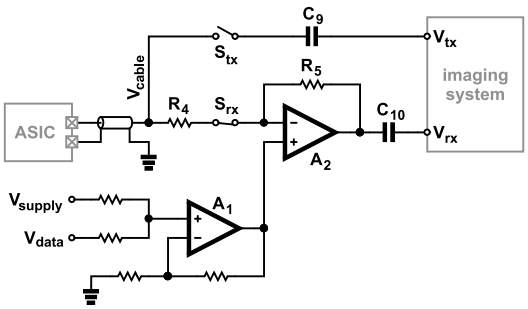


Fig. 9. Simplified diagram of the system-side circuit to interface the ASIC with a conventional imaging system.

a simplified diagram of this circuit, which was implemented using off-the-shelf components on a printed circuit board (PCB). In the RX phase, trans-impedance amplifier (TIA) A_2 is used to supply the ASIC with a fixed supply voltage (V_{supply}) while at the same time converting the amplified signal current containing the received echoes to a voltage V_{rx} with a trans-impedance gain set by R_5. Resistor R_4 is used to characteristically terminate the cable, whereas capacitor C_{10} rejects the dc component associated with the ASIC's supply current.

Voltage noise at the TIA's virtual ground leads to additional output noise, with a noise gain determined by the cable capacitance and, to a lesser extent, the ac power-supply rejection of the LNA. To ensure that the equivalent input-referred noise is well below the 1-pA/$\sqrt{\text{Hz}}$ noise floor of the LNA, the TIA's voltage noise should be kept below 14 nV/$\sqrt{\text{Hz}}$ in our design. V_{supply} can be adjusted to account for the voltage drop across the cable and resistor R_4 caused by the dc bias current of the ASIC. The signal current leads to a small-signal-dependent voltage drop across the cable and R_4, which in turn leads to a small gain error that is acceptable in our application.

To configure the ASIC, the PWM-encoded data V_{data} are added to the reference voltage at the non-inverting input of the TIA, using a summing amplifier. The negative feedback of A_2 causes the virtual ground to follow this signal, thus transmitting it over the coaxial cable to the ASIC. In TX, no supply is required and switch S_{rx} is opened to disconnect the TIA from the cable. S_{tx} connects the HV signal V_{tx} generated by the system that is ac-coupled to the cable.

F. Auxiliary Circuits

Part of the ASIC consists of low-voltage devices that cannot handle the large voltage levels of the TX phase. To protect them, clamps are used. Their gate voltage V_{clamp} is provided by a capacitor that is charged during the TX phase. The circuit that provides V_{clamp} is shown in Fig. 10. In the TX phase, storage capacitor C_{11} is charged to a voltage level set by the Zener diode D_1. Transistor M_{12} turns off when the voltage on the capacitor increases above 5.6 V. Diode D_2 is a protection diode to ensure that the voltage V_{clamp} does not increase beyond the maximum gate voltage of the used technology. Diode D_3 prevents that the charge on C_{11} is released via the drain–source diode of M_{12} when the signal V_{cable} is lower than the capacitor voltage.

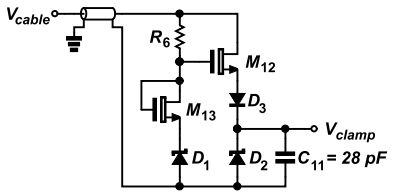


Fig. 10. Circuit to generate V_{clamp} with a storage capacitor C_{11} to keep the signal in absence of a supply voltage.

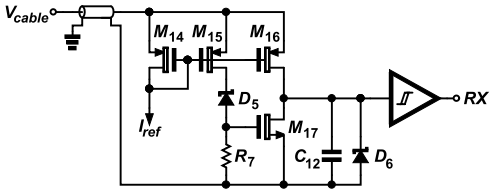


Fig. 11. RX phase detection circuit.

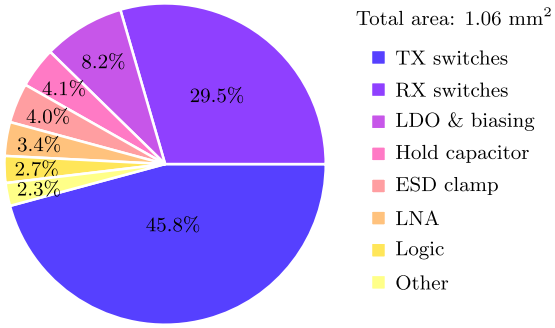


Fig. 12. Area breakdown of the fabricated ASIC.

Another important auxiliary circuit is the circuit that detects the RX phase, to enable the amplifier and disable the TX switches. This detection circuit is shown in Fig. 11. During transmit, M_{17} is turned on by the high voltage on the cable, as soon as the signal on the cable falls below about 6 V, M_{17} turns off, and the current mirror M_{14}–M_{16} starts to charge C_{12}. The current is set such that the Schmitt trigger toggles after about 200 ns when an RX supply voltage of 3 V is used.

IV. Experimental Results

A prototype ASIC has been fabricated in a 0.18-µm bipolar-CMOS-DMOS (BCD) process, of which the die micrograph is shown in Fig. 13(a). It has a 1.5-mm-diameter circular shape, with a central 0.5-mm circle left empty to accommodate a guidewire. The circuitry and pads are outside the circle are for test purposes and can be removed by laser cutting, as shown in Fig. 13(b). The two square bondpads (*sig* and *gnd*) connect to the coaxial cable. The die area is dominated by the HV devices used in the TX and RX switches, as shown in the area breakdown in Fig. 12.

A. Integration

Using the approach described in [17], an array of 64 piezoelectric transducer elements with a center frequency of 13 MHz and a 100-µm-pitch has been fabricated on top

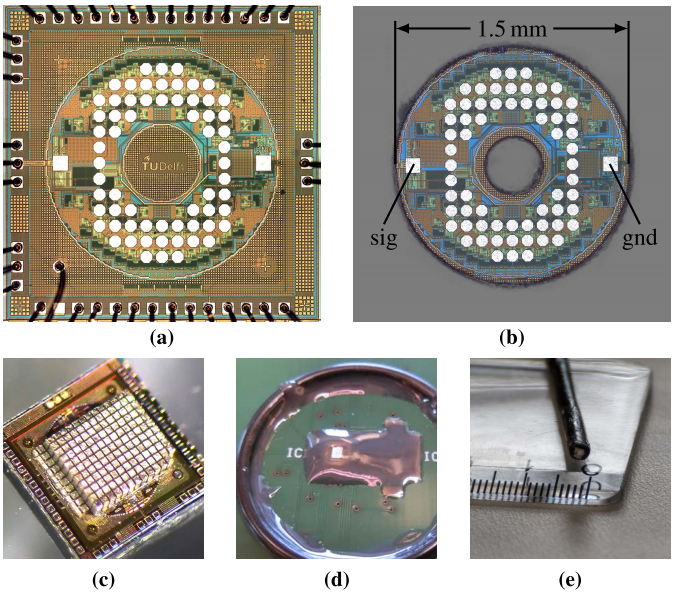


Fig. 13. (a) Die micrograph of the fabricated ASIC. (b) Laser-cut ASIC. (c) ASIC with piezo transducers (before placing the ground foil). (d) Ultrasound ASIC with transducer on a test PCB. (e) ASIC integrated in a prototype probe.

of the octagonal bond-pads, resulting in a 64-element 100-µm pitch array, as shown in Fig. 13(c). The common electrode of the transducer elements (ground foil) is realized by an aluminum foil on top of the transducer elements (not shown) and is connected to the gnd-pad using conductive glue. The central (dummy) elements are left on the ASIC here to ease the fabrication steps in the early prototypes. For electrical characterization, the die with transducer elements was bonded to a PCB, as shown in Fig. 13(d). In a later prototype, the ASIC was mounted on the tip of a cylindrical steel holder to create a prototype probe [see Fig. 13(e)].

B. Electrical Characterization

The ASIC has been characterized in combination with a 42-American wire gauge (AWG) coaxial cable of 1.5 m. Initially, the ASIC was characterized electrically without any piezo transducers.

In order to test whether the ASIC can be configured, configuration data were sent to it. Correct and incorrect data transmissions can be distinguished with the implemented CRC circuit. Fig. 14 shows a correct and an erroneous configuration of the ASIC, emulated by sending an incorrect CRC. The higher supply current, visible as an increased TIA output voltage after data transmission, indicates a mismatch between the data and CRC-bits and shows that it can effectively be used to detect incorrect transmissions of the configuration data.

The transfer function of the receive amplifier was measured by injecting a signal current into the LNA through a test input of the receive multiplexer and recording the output of the TIA on the system side. Fig. 15 shows the measured transfer function of the combination of the LNA in the ASIC and the TIA on the system side with the coaxial cable in between. The measurements show that the combination has a 3-dB

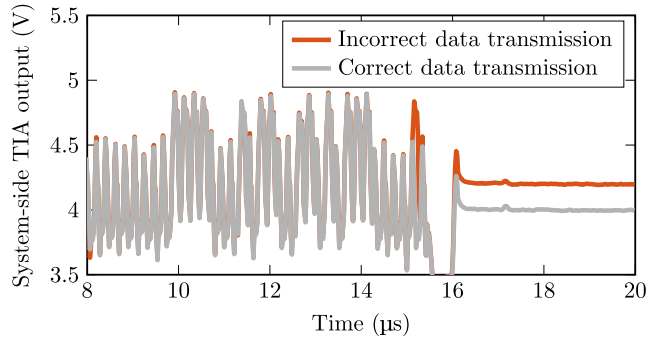


Fig. 14. TIA-output signal with a correct and an erroneous configuration data transfer.

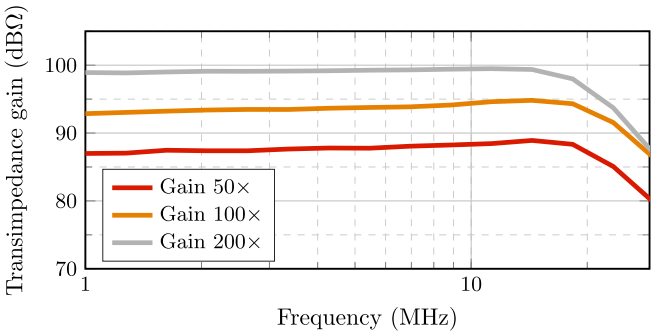


Fig. 15. Transfer function for the three gain settings.

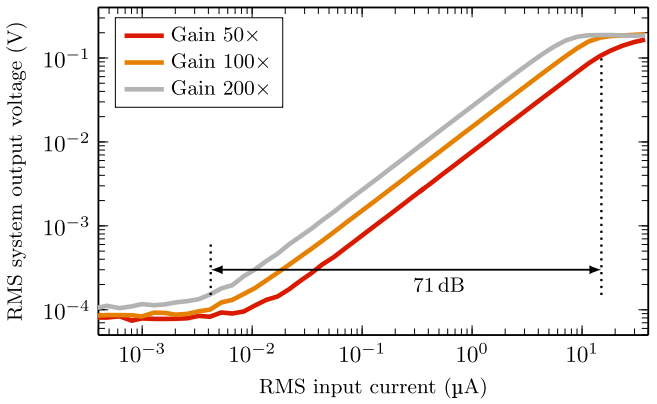


Fig. 16. Dynamic range measurement with electrical test input.

bandwidth of 20.5 MHz and the gain settings can correctly be configured. To determine the dynamic range of the amplifier, the input signal was increased until the output of the LNA started clipping. Fig. 16 shows the input current–output voltage relation of the circuit in receive mode. The input-referred rms noise current is about 4 nA, which is lower than the 4.4-nA in-band rms noise of the transducer. Signal compression increases to more than 1 dB for input signals larger than 15 µA in the lowest gain setting, making the total dynamic range of the circuit 71 dB including the programmable gain.

The transmit operation was evaluated by supplying a three-cycle square wave to the cable after configuration. The measured signal at the bondpad of one of the channels is shown in Fig. 17. As evident from the figure, the switch effectively passes or blocks the transmit waveform based on

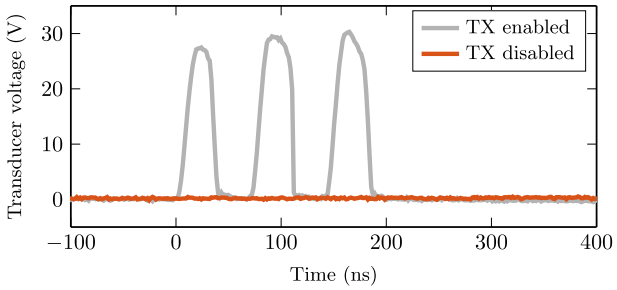


Fig. 17. Electrical measurement with TX enabled and TX disabled.

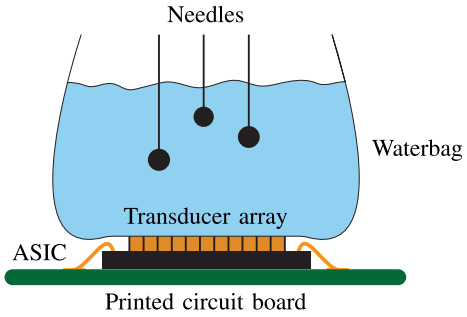


Fig. 18. Waterbag with needle phantom placed on top of the ASIC.

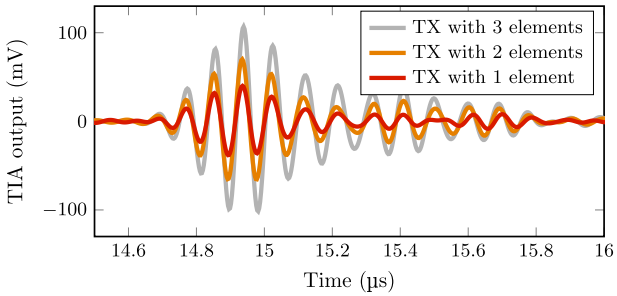


Fig. 19. Measured echo with one or multiple elements used for TX.

the configured setting. Also visible is the slightly smaller amplitude of the first pulse, which is caused by the capacitors in the electrostatic discharge (ESD)-protection circuit and the circuit that generates V_{clamp} that has to be charged in the first TX cycle.

C. Acoustic Measurements

For acoustic characterization, a small water bag was placed on top of the transducer array, as shown in Fig. 18. A pulse-echo experiment with a plate reflector shows that the amplitude of the echo received by one RX element, shown in Fig. 19, increases with the number of elements enabled for transmit, demonstrating effective switching of the applied 30-V pulses. In another experiment, two non-adjacent RX channels were read out while enabling the same transmitters. The corresponding waveforms are shown in Fig. 20 and show the expected arrival time difference.

Finally, an imaging phantom consisting of three needles was placed at a distance of 7–10 mm from the ASIC. A volumetric image was obtained with a full synthetic aperture acquisition scheme, by successively pulsing the 64 elements and

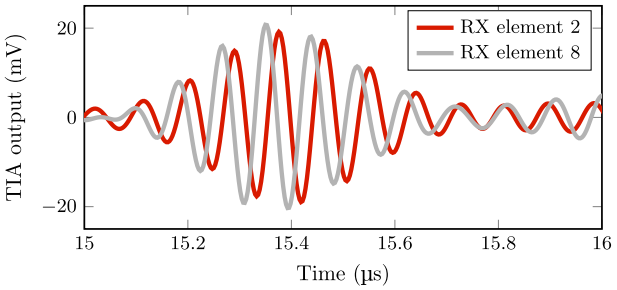


Fig. 20. Measured echo of two individual non-adjacent elements.

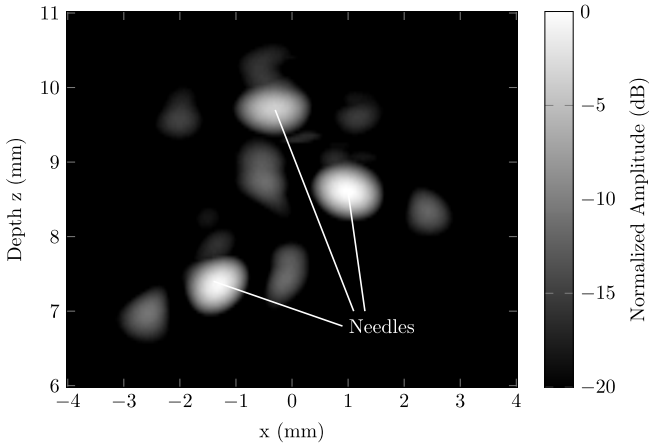


Fig. 21. Maximum projection of a 3-D image of the needle phantom, reconstructed using synthetic aperture beamforming.

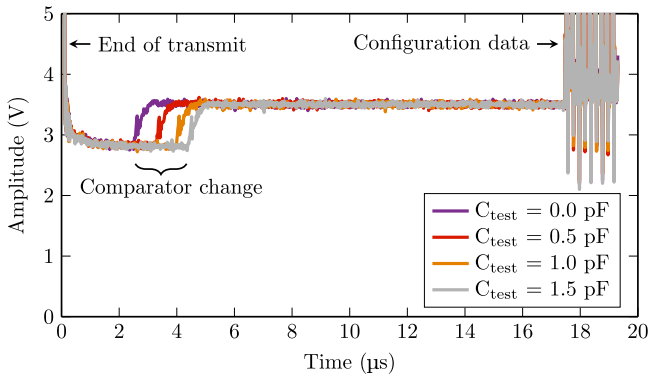


Fig. 22. RX waveforms at the output of amplifier A_2 with the element test mode enabled, for the different reference capacitor values (in parallel with a transducer element).

successively capturing the echoes received by all 64 elements and subsequently performing delay-and-sum beamforming. The maximum projection of the volumetric image (Fig. 21) clearly shows the three needles placed in front of the array. The artifacts visible in the image are due to the sidelobes and are common for the beamforming algorithm used.

D. Element Test Mode

The element test mode was evaluated by measuring all combinations of the two integrated test capacitors. In the measurements, shown in Fig. 22, the time at which the comparator

TABLE I
SYSTEM-LEVEL COMPARISON WITH PRIOR WORK

	This work	Gurun, 2014 [4]	Tekes, 2015 [5]	Tan, 2018 [6]	Chen, 2015 [11]	Lim, 2020 [7]
Number of interconnects*	1	13	13	4	1	4
TX, RX channels	64, 64	56, 48	64, 56	16, 64	0, 1	16, 16
Simultaneous RX channels	1	4	4	1	1	1
Chip dimensions	1.5 mm ⌀	1.4 mm ⌀	2.1 mm ⌀	1.5 mm ⌀	0.6×1 mm^2	1.23×2.45 mm^2
Transducer type	PZT	CMUT	CMUT	PZT	PVDF	CMUT
Center frequency	13 MHz	20 MHz	12 MHz	13 MHz	2.25 MHz	40 MHz
RX power	6 mW	20 mW	-	9.1 mW	13.2 mW	25.2 mW
RX bandwidth	20 MHz	40 MHz	-	16 MHz	20 MHz	37.5 MHz
RX dynamic range	71 dB	50 dB	-	53 dB	60 dB	-
TX voltage	30 V	25 V	12.5 V	30 V	N/A	44 V

* Number of interconnects excluding ground.

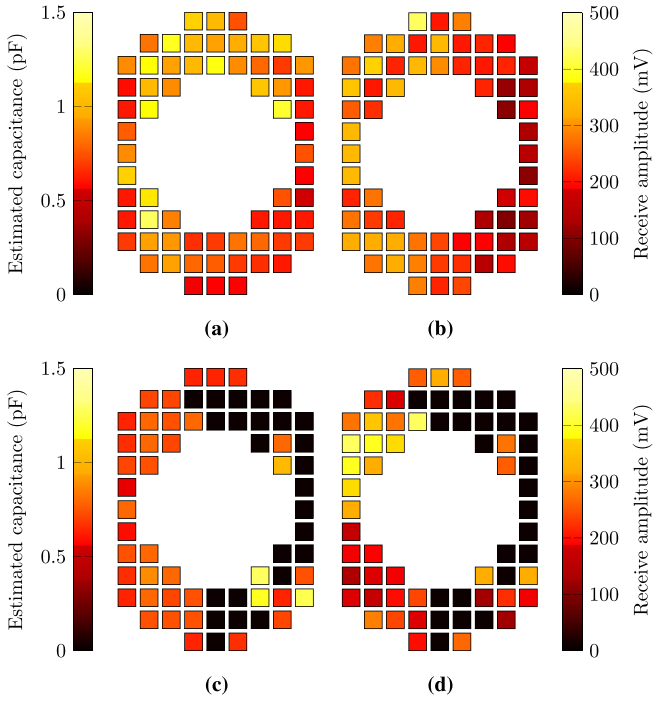


Fig. 23. Channel capacitance measured with the element test mode and corresponding channel receive amplitude. (a) and (b) Well working sample and (c) and (d) Sample with fabrication issues.

changes is clearly dependent on the channel capacitance. The test mode was then used to measure two fabricated samples, one of which fully works, and the other suffering from fabrication issues causing 40 % of the elements to be dead. Measurements on the fully working sample [Fig. 23(a)] show a variation in the channel capacitance between 0.5 and 1.3 pF. This variation is partly caused by the capacitance of routing parasitics on the ASIC. A receive measurement using an external ultrasound transmitter shows that all elements of this sample are working [see Fig. 23(b)]. The variation in amplitude can be attributed to element variations and difference in acoustic coupling to the liquid such as air bubbles. The other sample suffered from "fallen" elements, elements that were knocked over during the dicing step of the fabrication process due to bad adhesion of the conductive glue. In the capacitance plot [Fig. 23(c)], these elements are visible as a zero capacitance because their value is below the minimum detectable threshold. The elements without any receive signal in the acoustic measurement [Fig. 23(d)] correspond well with the elements with zero capacitance. This shows that the element test mode can be used successfully to detect fabrication issues.

V. DISCUSSION

The imaging frame rate of the ASIC highly depends on the implemented beamforming algorithm and imaging depth. When using full synthetic aperture imaging and an imaging depth of 12 mm, a volumetric frame rate of 5 Hz is possible with the current prototype. The imaging time of the prototype is dominated by the communication scheme, where each switch is programmed individually to make the prototype versatile for testing. The frame rate can be significantly improved by integrating logic that performs the channel selection automatically or by using more sophisticated imaging algorithms. The imaging depth is not limited by the circuit since the RX phase only ends when the system starts to send configuration data.

The capability to activate multiple elements in the transmit phase creates the possibility to increase the generated acoustic pressure and thus the penetration depth, which could be useful in specific applications where larger structures (e.g., thicker occlusions) have to be visualized. Transmitting on multiple elements simultaneously can also help to reduce the number of transmit events per frame, allowing a higher frame rate to be realized in trade for image quality.

In this work, the receive phase has been implemented with a single receive channel. When scaling to larger transducer arrays, it would be beneficial to receive with multiple channels at once. A possible implementation could be to use frequency multiplexing, which fits well with the relatively narrow bandwidth of the receive signals.

The ASIC can only handle unipolar transmit pulses due to circuit limitations. As an alternative to bipolar pulses, waveforms with an offset can be applied in transmit, making an acoustically similar transmission with half the amplitude.

The ASIC is compared with prior art in Table I. This work shows the first ASIC that combines transmit and receive functionality on multiple elements connected to an imaging system using a single coaxial cable while maintaining a comparable power consumption, bandwidth, and dimensions.

VI. Conclusion

This article has presented the first ASIC capable of interfacing an ultrasound transducer array via a single coaxial cable. The ASIC aims for 3-D forward-looking IVUS imaging and interfaces 64 transducer elements to an imaging system using a single coaxial cable. An LNA has been proposed that outputs a signal current to efficiently drive the micro-coaxial cable, which has a relatively high capacitance, while receiving a supply voltage through the same cable. A new HV switch has been proposed that occupies a substantially smaller die area than prior designs. A test mode has been integrated into the front end, to verify the integrity of the elements of the transducer array. In imaging experiments with a needle phantom, the successful operation of a prototype consisting of the ASIC and a transducer array integrated directly on top of the ASIC has been shown. Images with a quality suitable for forward-looking IVUS have been reconstructed, demonstrating the ASIC's potential to greatly simplify the realization of catheter-based miniature 3-D ultrasound imaging devices.

References

[1] B. K. Courtney *et al.*, "Innovations in imaging for chronic total occlusions: A glimpse into the future of angiography's blind-spot," *Eur. Heart J.*, vol. 29, no. 5, pp. 583–593, Mar. 2008.

[2] B.-K. Kim *et al.*, "Clinical impact of intravascular ultrasound–guided chronic total occlusion intervention with zotarolimus-eluting versus biolimus-eluting stent implantation: Randomized study," *Circulat., Cardiovascular Intervent.*, vol. 8, no. 7, Jul. 2015, Art. no. e002592.

[3] P. Kruizinga *et al.*, "Compressive 3D ultrasound imaging using a single sensor," *Sci. Adv.*, vol. 3, no. 12, Dec. 2017, Art. no. e1701423.

[4] G. Gurun *et al.*, "Single-chip CMUT-on-CMOS front-end system for real-time volumetric IVUS and ICE imaging," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 61, no. 2, pp. 239–250, Feb. 2014.

[5] C. Tekes *et al.*, "Real-time imaging system using a 12-MHz forward-looking catheter with single chip CMUT-on-CMOS array," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Oct. 2015, pp. 1–4.

[6] M. Tan *et al.*, "A front-end ASIC with high-voltage transmit switching and receive digitization for 3-D forward-looking intravascular ultrasound imaging," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2284–2297, Aug. 2018.

[7] J. Lim, C. Tekes, E. F. Arkan, A. Rezvanitabar, F. L. Degertekin, and M. Ghovanloo, "Highly integrated guidewire ultrasound imaging system-on-a-chip," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1310–1323, May 2020.

[8] D. Van Willigen *et al.*, "ASIC design for a single-cable 64-element ultrasound probe," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Oct. 2018, pp. 1–4.

[9] D. V. Willigen *et al.*, "Fabrication and characterization of a prototype forward-looking single-cable 64-element intra-vascular ultrasound probe," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Oct. 2019, pp. 978–980.

[10] J. Janjic *et al.*, "A 2-D ultrasound transducer with front-end ASIC and low cable count for 3-D forward-looking intravascular imaging: Performance and characterization," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 65, no. 10, pp. 1832–1844, Oct. 2018.

[11] C. Chen *et al.*, "A single-cable PVDF transducer readout IC for intravascular photoacoustic imaging," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Oct. 2015, pp. 1–4.

[12] A. Seidel, M. S. Costa, J. Joos, and B. Wicht, "Area efficient integrated gate drivers based on high-voltage charge storing," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1550–1559, Jul. 2015.

[13] Y. Igarashi *et al.*, "Single-chip 3072-element-channel transceiver/128-subarray-channel 2-D array IC with analog RX and all-digital TX beamformer for echocardiography," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2555–2567, Sep. 2019.

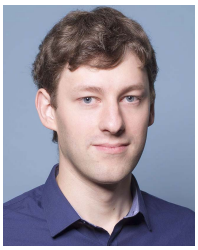
[14] M. Tan *et al.*, "A front-end ASIC with high-voltage transmit switching and receive digitization for forward-looking intravascular ultrasound," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2017, pp. 1–4.

[15] M. Tan *et al.*, "A 64-channel transmit beamformer with ±30-V bipolar high-voltage pulsers for catheter-based ultrasound probes," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1796–1806, Jul. 2020.

[16] B. Razavi, "A 622 Mb/s 4.5 pA/$\sqrt{\text{Hz}}$ CMOS transimpedance amplifier (for optical receiver front-end)," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2000, pp. 162–163.

[17] C. Chen *et al.*, "A prototype PZT matrix transducer with low-power integrated receive ASIC for 3-D transesophageal echocardiography," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 63, no. 1, pp. 47–59, Jan. 2016.

[18] K. Chen, B. C. Lee, K. E. Thomenius, B. T. Khuri-Yakub, H.-S. Lee, and C. G. Sodini, "A column-row-parallel ultrasound imaging architecture for 3-D plane-wave imaging and Tx second-order harmonic distortion reduction," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 65, no. 5, pp. 828–843, May 2018.



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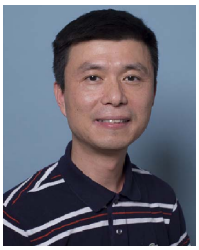

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