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An Output Bandwidth Optimized 200-Gb/s PAM-4 100-Gb/s NRZ Transmitter With 5-Tap FFE in 28-nm CMOS

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***Abstract*— This article presents a 200-Gb/s pulse amplitude-modulation four-level (PAM-4) and 100-Gb/s non-return-to-zero (NRZ) transmitter (TX) in 28-nm CMOS technology. To achieve the target data rate, the output bandwidth and swing of the proposed TX are optimized by minimizing the output capacitance of the 4:1 multiplexer (MUX) and driver stage with pull-up current sources and adopting a fully reconfigurable 5-tap feed-forward equalizer (FFE). The key circuit includes a segmented 8:4 MUX and 4:1 MUX/driver, a thermal encoder and retimer, and a flexible clock distribution network. Using the layout generated with Berkeley Analog Generator (BAG), the proposed TX achieves an eye opening with >52.9-mV eye height, 0.36 UI eye width, >98% RLM, and 4.63 pJ/b at 200-Gb/s PAM-4 signaling under >6-dB channel loss at 50 GHz, demonstrating the highest data rate achieved using a planar process.**

***Index Terms*— 28 nm, 4:1 multiplexer (MUX), Berkeley Analog Generator (BAG), clock distribution, four-level pulse-amplitude modulation (PAM-4), pulse generator, quarter-rate, SerDes, transmitter (TX), wireline.**

I. Introduction

THE ever-increasing demand for ultrahigh-speed interconnects has driven the development of wireline transmitters (TXs) operating at >100 Gb/s per lane [1]–[8]. For example, PCIe data rates [Fig. 1(a)] have doubled every three years, and the 2022 PCIe standard is aiming to achieve 128 Gb/s per pin and >256-Gb/s total bandwidth [9]. Fig. 1(b) also shows that per-lane Ethernet data rates [10] have doubled every 3.9 years, with standards targeting 200 Gb/s in 2026.

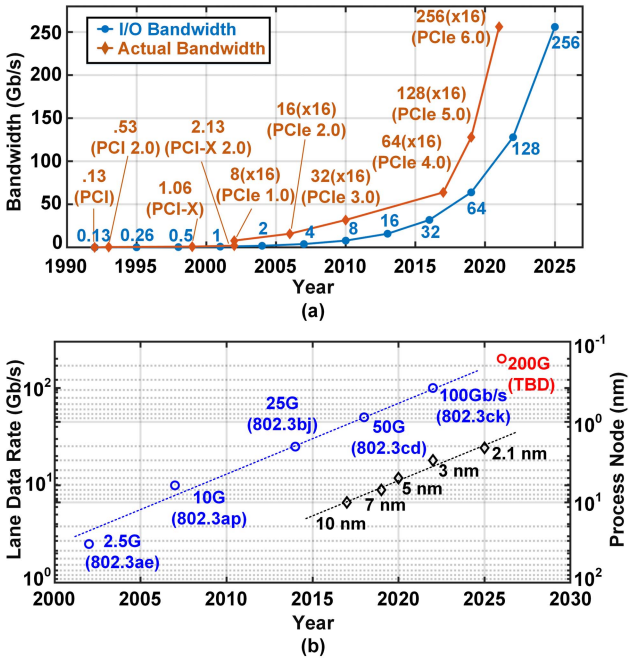

Fig. 1. (a) I/O bandwidth (data rate per lane) and actual bandwidth (data rate of link) of the PCIe standard versus year [9] and (b) summary forecast from the Ethernet Bandwidth Assessment [10].

In response to the demands of the latest interconnect standards, the data rates of SerDes TXs have been increasing by 2× approximately every 3–4 years, and the latest designs have reached >200 Gb/s [11], [12]. Meanwhile, as shown in Fig. 1(b), technology nodes have halved every 3.4 years [10]. FinFET technologies below 16 nm have been widely used in high-speed links, since the TXs used for system-on-chip (SoC) interfaces follow process technology scaling necessitated by "digital-first" architectures. Fortunately, the FinFET process is superior in providing a higher cut-off frequency and intrinsic gain compared to planar processes. This enables the TXs to meet the demands of ultrahigh-speed interconnects. Nevertheless, the mature planar processes are still preferable for the lower cost and higher yield.

Another recent SerDes trend is the application of four-level pulse-amplitude modulation (PAM-4) [1]–[7], [17]. Compared to non-return-to-zero (NRZ) signaling, PAM-4 signaling

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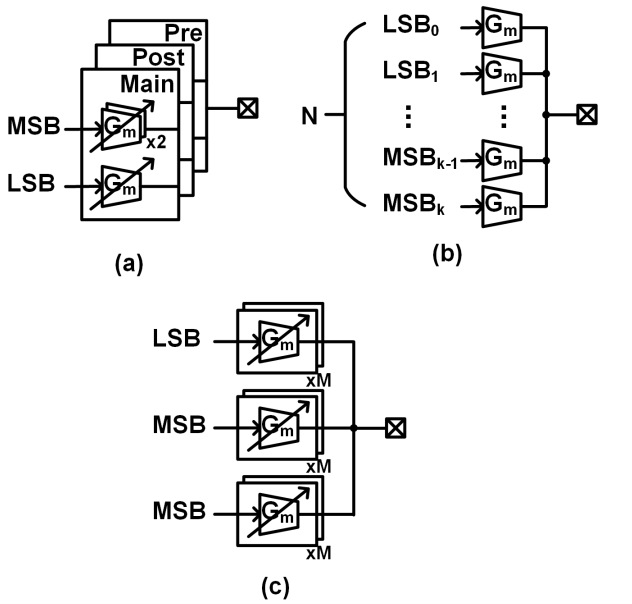


Fig. 2. FFE architectures. (a) Analog FFE, (b) DAC-based FFE, and (c) segmented FFE.

reduces the Nyquist frequency of transmitted data by half. Considering the exponential increase of loss versus frequency, for the same transmission speed, PAM-4 signaling provides better spectral efficiency. However, the vertical eye opening is only one-third of an NRZ data eye, which causes ∼9.5 dB worse signal-to-noise ratio (SNR). Since the PAM-4 eye is more sensitive to the inter-symbol interference (ISI) and linearity of the data path, the design of TXs with feed-forward equalizers (FFEs) becomes more challenging.

In this article, we present a 200 Gb/s PAM-4 and 100-Gb/s NRZ TX fabricated in a 28-nm CMOS technology. To achieve the target data rate with a planar process, several bandwidth extension techniques are introduced. First, the TX adopts a merged 4:1 multiplexer (MUX) and driver with pull-up current sources to extend the output bandwidth and output swing by minimizing the driver capacitance. Second, flexible clock timing control maximizes the timing margin between clock domains. Lastly, the TX adopts a data multiplexing architecture that supports a fully reconfigurable 5-tap FFE, while minimizing output capacitance. The proposed TX layout was generated using the Berkeley Analog Generator (BAG) [21] and thus can be quickly instantiated and ported to different processes.

This article is organized as follows. Section II describes the proposed TX architecture. Section III presents the design of critical blocks, including the 4:1 MUX and driver stage, coarse/fine FFE, 8:4 MUX, and the clock distribution. The BAG design flow and layout generation process is discussed in Section IV. Finally, Section V summarizes the measured results and Section VI draws the conclusion.

II. TX Architecture

When designing a high-speed SerDes TX, one must first choose the FFE structure. Fig. 2 shows three types of FFE architectures: analog FFE, digital-to-analog converter-based (DAC-based) FFE, and segmented FFE. The analog FFE implementation method has been widely used in applications requiring data rates <64 Gb/s [13], [14] for the high power efficiency, with tap coefficients adjusted in the analog domain. When this architecture is applied to a PAM-4 TX with N-tap FFE, the circuit is split into N sub-blocks, each containing LSB and MSB driver cells, as shown in Fig. 2(a). In this case, because the number of FFE taps (sub-blocks) is fixed, the equalization ability is insufficient for a high-loss channel. Moreover, for a low-loss channel, oversized taps used to cover various FFE configurations can degrade the output bandwidth.

The second option is the DAC-based FFE architecture [8], in which the G_m cells of the DAC are in the analog domain and the FFE is fully implemented in the digital domain [Fig. 2(b)]. The main advantage of this architecture is the ability to flexibly change the FFE settings to control the number of taps and tap coefficients. Because the G_m cells always remain active with different tap configurations, driving capability is fully utilized and maximized regardless of required equalization strength at different channel losses. However, for a realistic channel, a reasonable number of bits (usually 6–8 bits) for the DAC is required, which may increase the output parasitics of the G_m cells unless careful segmentation technique is taken [4] and degrade the output bandwidth, especially in 28 nm. Moreover, each fully designed G_m cell with a serializer, MUX, and driver increases the power overhead due to the added low-speed circuit blocks and capacitive load for the clock distribution.

The last option is the segmented FFE architecture [1], which is the combination of the analog FFE and DAC-based FFE architectures [Fig. 2(c)]. It provides coarse/fine tuning of the FFE taps by producing data with different delays that may then be selected. It guarantees the same flexibility in the number of FFE taps as the DAC-based FFE architecture. The segmented FFE architecture can further extend the output bandwidth by reducing the coarse FFE resolution. In addition, because the lower-speed serializers and MUX can be shared inside LSB or MSB cells, the power of the low-speed circuits and clock distribution can be reduced. As the fine FFE is still controlled in the analog domain, the overall FFE resolution can be sustained.

Another important decision is the serialization ratio and the clock frequency of the final MUX stage. As discussed in [1] and [2], compared with the half-rate architecture, the quad-rate architecture reduces the clock distribution power with a larger clock buffer fan-out, increases the timing margin of the final MUX, and removes the internal half-rate nodes. However, the quadrature clock spacing is critical and a high-speed 4:1 MUX is needed.

The proposed TX using a quarter-rate architecture and the segmented FFE structure with a configurable 5-tap FFE is shown in Fig. 3. The TX receives a differential 25-GHz clock followed by an injection-locked (IL) quadrature clock generator. Dedicated duty-cycle correction (DCC) and quadrature error correction (QEC) circuits are used to compensate duty-cycle distortion and quadrature errors. The data path receives the four-phase 25-GHz clocks ($C4_{I/Q}$) through a resonant clock buffer. The $C4_{I/Q}$ clocks are also divided to produce two pairs of four-phase 12.5-GHz clocks. Each pair of

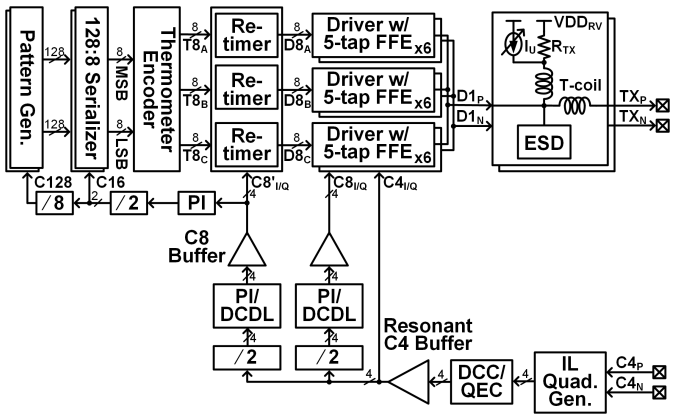


Fig. 3. Top-level schematic of the proposed TX.

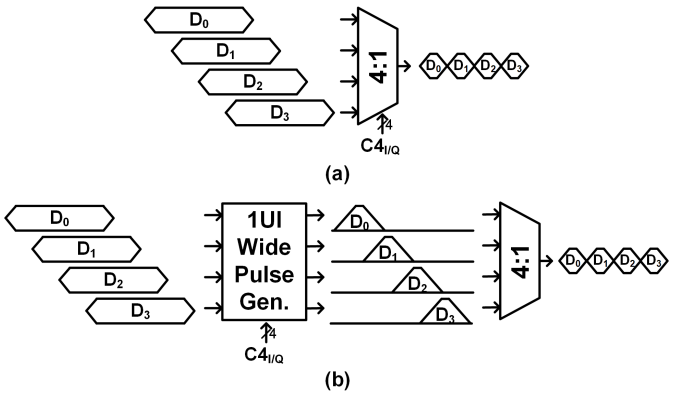


Fig. 4. Simplified block diagram of the 4:1 MUX structures. (a) Triple-stacked structure and (b) double-stacked structure with a 1-UI wide pulse generator.

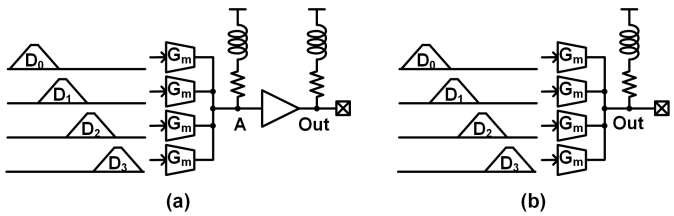


Fig. 5. Simplified block diagram of 4:1 multiplexing at the (a) pre-driver and (b) output node.

C8 clocks is distributed to the data path by C8 clock buffers through a phase interpolator (PI) and a digitally controlled delay line (DCDL), which serve as coarse/fine skew control to suppress the C8 quadrature errors and maximize the timing margins between clock domains.

The data path consists of pattern generators, 128:8 serializers, a thermometer encoder, retimers, and three FFE driver bundles which are equally weighted. In PAM-4 mode, the three retimers receive three thermometer-encoded signals ($T8_{A/B/C}$), while in NRZ mode, they receive three identical signals from the thermometer encoder. The retimer outputs ($D8_{A/B/C}$) are sent to the three driver bundles, each composed of six segments connected in parallel. The output currents from the segments are summed in a customized termination network with 90-Ω resistors, pull-up current sources, and electrostatic discharge (ESD) protection diodes. The T-coils inserted between the termination network and pads [3], [15], [16] are designed to minimize the worst-case ISI pattern.

III. Circuit Implementation

A. 4:1 MUX and Driver

The full-rate node and load capacitance from driver parasitics significantly affect the TX performance. Therefore, the 4:1 MUX and the driver stage are critical for the optimization of output bandwidth and TX power.

Fig. 4 shows triple-stacked and double-stacked 4:1 MUX structures. Although the circuitry of the triple-stacked structures [Fig. 4(a)] is simple, the resistance of the stacked transistors degrades the bandwidth of the 4:1 MUX, and the undriven internal nodes create data-dependent ISI [1]. On the other hand, the double-stacked 4:1 MUX with an 1-UI wide pulse generator [Fig. 4(b)] eliminates the undriven nodes of the stacked transistors, extending the output bandwidth, though this structure may consume more power unless proper fan-out is exercised since the function is split into two stages.

Fig. 5 shows two design options for the 4:1 MUX. Some state-of-the-art TXs adopt a 4:1 MUX in the pre-driver [1], [15] as shown in Fig. 5(a) to prevent the output network from loading the MUX directly. However, the MUX stage in the pre-driver introduces an internal full-rate node, which degrades the output bandwidth. To extend the bandwidth of this design, [15] adopts a passive inductor for shunt peaking. However, the segmented FFE architecture does not allow the addition of an inductor at the centralized internal node. An active inductor and load [1] can be added to each segment to extend the bandwidth, but the parasitic capacitance of the full-rate node neutralizes the effect of the active inductor in 28-nm CMOS technology; the size of the active inductor is insufficient to enable full-rate operation in this technology.

For this reason, we choose a merged 4:1 MUX and driver shown in Fig. 5(b), which was originally introduced in [2]. The driver has only one full-rate node at the output and thus we can implement a variety of bandwidth extension techniques without excessive area. For fine FFE tuning, the G_m cell in Fig. 5(b) needs at least one stacked device; it can change the output current of the driver by tuning its bias voltage. To enable this functionality and reduce the parasitic capacitance of the G_m cell, a tail-less current mode driver is preferred [1].

Fig. 6 shows the proposed 4:1 MUX/driver. To minimize the parasitic capacitance of the active devices (M1 and M2), the total widths of M1 and M2 are reduced while increasing their overdrive voltages. However, due to the large overdrive voltages, the transistors tend to stay in the linear region when the output voltage changes. The output resistance is

$$\begin{aligned} R_{\mathrm{OUT}} &= R_{\mathrm{OUTD}} || R_{\mathrm{OUTU}} \\ &= R_{\mathrm{OUTD}} || R_{\mathrm{OUTU,CS}} || R_{\mathrm{OUTU,RES}} \end{aligned} \tag{1}$$

where R_{OUTD}, $R_{\mathrm{OUTU,CS}}$, and $R_{\mathrm{OUTU,RES}}$ are associated with the pull-down active devices, the pull-up termination current sources and resistors, respectively. Therefore, when the

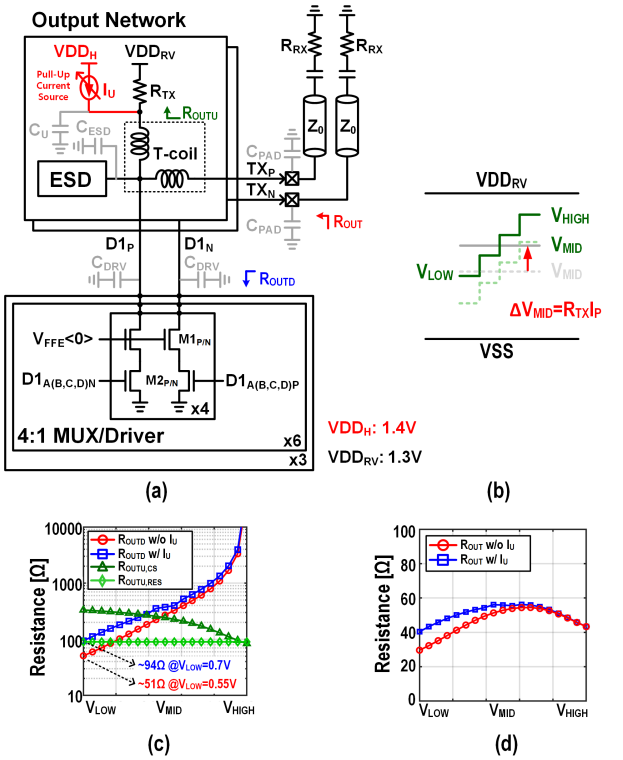


Fig. 6. Proposed merged 4:1 MUX/driver. (a) Schematic, (b) the output voltage level of the 4:1 MUX/driver, (c) post-layout simulation results of pull-down resistance without current sources (R_{OUTD} w/o I_U), pull-down resistance with current sources (R_{OUTD} w/ I_U), pull-up resistance of current sources ($R_{\mathrm{OUTU,CS}}$) and resistor ($R_{\mathrm{OUTU,RES}}$) versus output voltage levels, and (d) post-layout simulation results of the total TX output resistance without (R_{OUT} w/o I_U) and with (R_{OUT} w/I_U) pull-up current sources.

transistors M1 and M2 are in the linear region, the output resistance decreases, resulting in impedance mismatch. Fig. 6(c) shows the post-layout simulation results of the output resistances versus the output voltage levels. With an output swing of 1 V_{ppd}, R_{OUTD} from the active devices is only 51 Ω at the minimum voltage V_{LOW}. To satisfy the conditions for impedance matching, the pull-down transistor can be designed to operate in the saturation region by reducing the output swing. However, this reduces the SNR and tolerance to channel loss.

To address this issue, we need to leverage the common-mode voltage of the TX output. The simplest method of increasing the driver supply voltage, however, would cause reliability issue, as the two NMOS devices may experience larger V_{DS} and increase the driver power. In this design, we add a pull-up current source to increase the common-mode voltage (V_{MID}) level. By increasing V_{MID} up to 700 mV in the post-layout simulation, the corresponding resistance from the active devices increases to 94 Ω [Fig. 6(c)]. In addition, the pull-up current sources stabilize the overall output resistance (R_{OUT}) in combination with the driver output resistance ($R_{\mathrm{OUTD}}||R_{\mathrm{OUTU}}$). As a result, by adjusting the current at different PVT corners, the overall output impedance stays within 40–60 Ω across the whole output voltage range [Fig. 6(d)]. The capacitive loading from the pull-up current sources is minimal (∼7 % of the driver capacitance) and

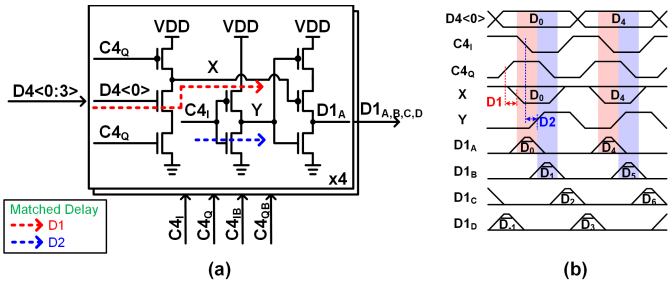


Fig. 7. 1-UI-wide pulse generator. (a) Schematic and (b) timing diagram.

isolated due to a T-coil. Therefore, it does not affect the output bandwidth. The T-coil extends the output bandwidth to approximately 33 GHz by compensating parasitic capacitance totaling 420 fF from the pull-up current source, termination resistors, driver, ESD protection diodes (supporting >1-kV human body model and 250-V charge device model levels), and pads.

Fig. 7 shows the proposed 1-UI pulse generator. The pulse generator based on two-stage dynamic logic eliminates the stack of three transistors and reduces the parasitic of internal nodes. While the first stage generates the data's rising edge using $C4_Q$, the second stage generates the falling edge using $C4_I$. In the first stage, when $C4_Q$ is 0, node X is reset to VDD, and when $C4_Q$ is 1, node X is evaluated using $D4\langle 0\rangle$. At the second stage, when node Y is 0, node X determines how the output node settles. When node Y is 1, the output node is reset to VSS. Since only one event happens at a time, when the $C4_Q$ and $C4_I$ edges arrive, data $D4\langle 0\rangle$ and node X have already settled. There are no unsettled nodes which usually create data-dependent ISI.

In addition, the first stage of the pulse generator and the clock $C4_I$ inverter are sized to have matched delays (D1 and D2 in Fig. 7), so the pulse generator output has 1-UI pulsewidth across different PVT conditions. By tuning relative clock delay between C4 and C8, the pulse window locates around the center of $D4$ data and with less than 2-UI variation. The rise and fall times at the output of the pulse generator are about 10 ps, as determined by the symmetric pull-up and pull-down strength of the second stage, which is fast enough to drive the 4:1 MUX/driver stage.

B. Coarse FFE and 8:4 MUX

Similar to article [17], the coarse FFE (Fig. 8) is configured by the D8 data selectors and C8 clock selectors. With proper segment assignment, the location and coefficient of the main tap can be adjusted from the first cursor to the fifth cursor. As an example, for the 3-tap configuration, the FFE could be chosen to have two taps of pre-cursor, two taps of post-cursor, or 1 tap each of pre-cursor and post-cursor. When using a constant coarse tap weight defined by the ratio of FFE tap segments to the total number of FFE segments, all segments are utilized either in the main tap or in equalization taps. This reduces the parasitic for a given peak amplitude or increases the output peak amplitude for a given set of output parasitic constraints. For example, considering an analog 3-

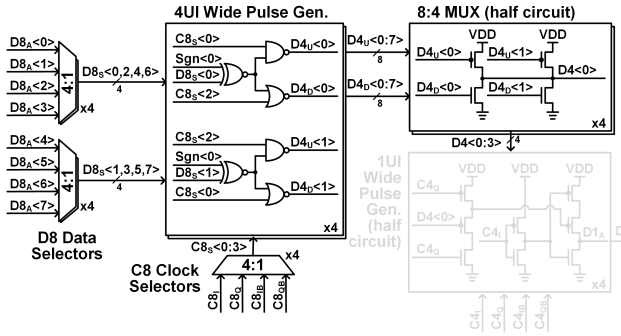


Fig. 8. Schematic of an 8:4 MUX with D8 data selectors and C8 clock selectors.

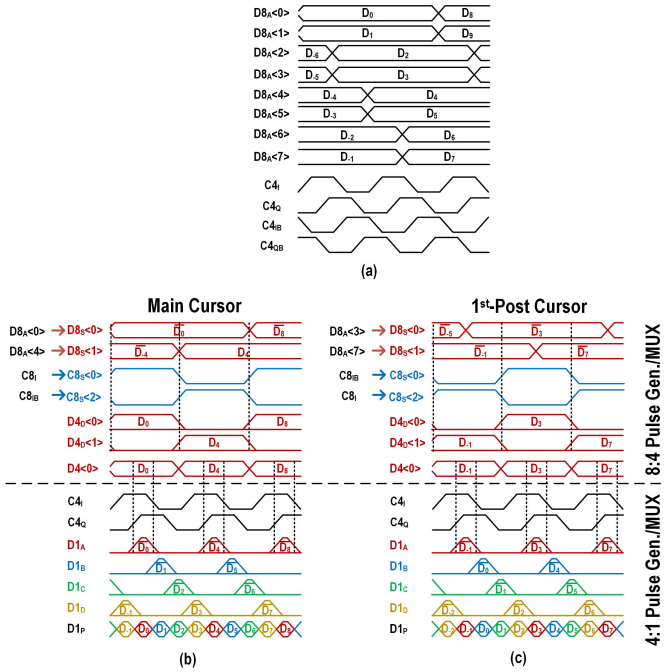


Fig. 9. Timing diagram of an example FFE configuration. (a) Input data and clocks, (b) main cursor, and (c) 1st post cursor configuration.

TABLE I

COARSE FFE SETTINGS FOR THE FIVE CURSORS

Cursor	0	1	2	3	4
$D8_S\langle 0\rangle$	$D8_A\langle 0\rangle$	$D8_A\langle 3\rangle$	$D8_A\langle 2\rangle$	$D8_A\langle 1\rangle$	$D8_A\langle 0\rangle$
$D8_S\langle 1\rangle$	$D8_A\langle 4\rangle$	$D8_A\langle 7\rangle$	$D8_A\langle 6\rangle$	$D8_A\langle 5\rangle$	$D8_A\langle 4\rangle$
$D8_S\langle 2\rangle$	$D8_A\langle 1\rangle$	$D8_A\langle 0\rangle$	$D8_A\langle 3\rangle$	$D8_A\langle 2\rangle$	$D8_A\langle 1\rangle$
$D8_S\langle 3\rangle$	$D8_A\langle 5\rangle$	$D8_A\langle 4\rangle$	$D8_A\langle 7\rangle$	$D8_A\langle 6\rangle$	$D8_A\langle 5\rangle$
$D8_S\langle 4\rangle$	$D8_A\langle 2\rangle$	$D8_A\langle 1\rangle$	$D8_A\langle 0\rangle$	$D8_A\langle 3\rangle$	$D8_A\langle 2\rangle$
$D8_S\langle 5\rangle$	$D8_A\langle 6\rangle$	$D8_A\langle 5\rangle$	$D8_A\langle 4\rangle$	$D8_A\langle 7\rangle$	$D8_A\langle 6\rangle$
$D8_S\langle 6\rangle$	$D8_A\langle 3\rangle$	$D8_A\langle 2\rangle$	$D8_A\langle 1\rangle$	$D8_A\langle 0\rangle$	$D8_A\langle 3\rangle$
$D8_S\langle 7\rangle$	$D8_A\langle 7\rangle$	$D8_A\langle 6\rangle$	$D8_A\langle 5\rangle$	$D8_A\langle 4\rangle$	$D8_A\langle 7\rangle$
$C8_S\langle 0\rangle$	$C4_I$	$C4_{IB}$	$C4_{IB}$	$C4_{IB}$	$C4_{IB}$
$C8_S\langle 1\rangle$	$C4_Q$	$C4_{QB}$	$C4_{QB}$	$C4_{QB}$	$C4_{QB}$
$C8_S\langle 2\rangle$	$C4_{IB}$	$C4_I$	$C4_I$	$C4_I$	$C4_I$
$C8_S\langle 3\rangle$	$C4_{QB}$	$C4_Q$	$C4_Q$	$C4_Q$	$C4_Q$

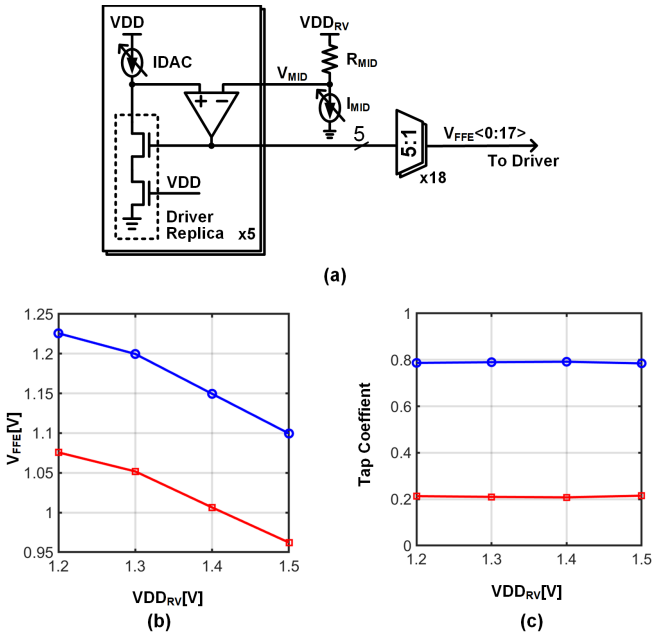


Fig. 10. Bias circuit for the fine FFE and simulations of FFE tolerance to supply voltage drift. (a) Schematic, (b) FFE bias voltage V_{FFE} versus driver voltage $\mathrm{VDD_{RV}}$, and (c) tap coefficients versus $\mathrm{VDD_{RV}}$, when coefficients set to 0.8 and 0.2.

tap FFE of Fig. 2(a) with the main tap, first pre-tap, and first post-tap ratios of 0.6, 0.2, and 0.2 respectively, the peak amplitude of the segmentation FFE is about 40% larger than that of a traditional FFE. The coarse FFE resolution is about 50 mV_{ppd} in the post-layout simulation.

The timing diagrams associated with the coarse FFE taps are shown in Fig. 9, for example, the main cursor and first post-cursor configurations. For the main cursor, $D8_A\langle 0\rangle$ is selected for $D8_S\langle 0\rangle$, while $D8_A\langle 4\rangle$ is selected for $D8_S\langle 1\rangle$. For the 4:1 clock MUXs, $C8_I$ and $C8_{\mathrm{IB}}$ are selected for $C8_S\langle 0\rangle$ and $C8_S\langle 2\rangle$, respectively. In this case, $D8_S\langle 0\rangle$ and $D8_S\langle 1\rangle$ are logically combined with $C8_S\langle 0\rangle$ ($C8_I$) and $C8_S\langle 2\rangle$ ($C8_{\mathrm{IB}}$) to generate pulses $D4_D\langle 0\rangle$ and $D4_D\langle 1\rangle$ and then further multiplexed to generate $D4\langle 0\rangle$. Lastly, $D4\langle 0\rangle$ is combined with $C4_I$ and $C4_Q$ to make D_0 at the final output $D1_P$.

Similarly, with the same 8:4 MUX, for the first post-cursor, $D8_A\langle 3\rangle$ is selected for $D8_S\langle 0\rangle$, while $D8_A\langle 7\rangle$ is selected for $D8_S\langle 1\rangle$. For the 4:1 clock MUXs, $C8_{\mathrm{IB}}$ and $C8_I$ are selected for $C8_S\langle 0\rangle$ and $C8_S\langle 2\rangle$, respectively. After being logically combined with $C8_S\langle 0\rangle$ ($C8_{\mathrm{IB}}$) and $C8_S\langle 2\rangle$ ($C8_B$), D_{-1} shows up at $D4\langle 0\rangle$, which will also be present at the final 4:1 MUX, delayed by 1-UI compared to the previously described configuration. Other five tap coarse FFE configurations are summarized in Table I.

C. Fine FFE

As mentioned in the top-level architecture description, the fine FFE is tuned by adjusting the bias voltage of the cascode device in the 4:1 MUX/driver. To support five FFE taps in our design, five different voltages are required for each segmentation of the driver, with each bias voltage generated from a replica drive and 7-bit current DAC. Fig. 10(a) shows the bias circuit used to generate the FFE bias voltages. I_{MID} and R_{MID} are used to generate the common-mode voltage V_{MID} at the TX output and track the driver supply voltage changes. When V_{MID} changes, the feedback loop—consisting of an op-amp and a replica circuit of the driver—changes the

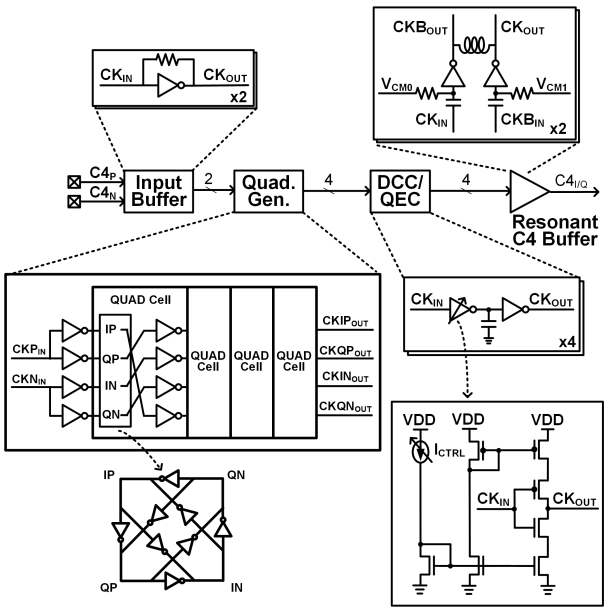


Fig. 11. Block diagram of the C4 clock path and circuit details.

gate voltage of the cascode device accordingly. Using 7-bit current DACs, the resolution of the fine FFE is 0.6 mV_{ppd}. A total range of approximately 76 mV_{ppd} is covered. In the fine FFE design, the five bias voltages generated from five copies of the current DAC, op-amp, and driver replica are connected to 18 segments through 18 5:1 MUXs. The bias circuit is simulated with $\pm 10\%$ driver supply voltage drift. As shown in Fig. 10(b) and (c), the errors of an example 2-tap FFE configuration remain $<2\%$.

D. Clock Path: C4 Clock Distribution

Fig. 11 shows the C4 clock distribution circuit. First, the external differential clock is received through a TIA-based clock RX to match the 50-Ω transmission line impedance and determine the output common-mode voltage. The quadrature clock is generated with an open-loop injection-locked quadrature clock generator, which consists of four stages of cascaded I/Q clock correlators [19]. The I/Q error is $<0.91\%$ at 30.37 mW. The phase noise is approximately -134.18 dBc/Hz at 1-MHz offset. The residual I/Q phase errors of the quadrature clock are corrected by a current-controlled delay line [18] driven by a 7-bit current DAC. From the post-layout simulation, we observe that the delay line provides a 1.4 ps tuning range at a maximum step size of 53 fs. This is enough to minimize the deterministic jitter at the 4:1 MUX introduced from clock distribution. Finally, two resonant clock buffers are adopted to drive the load capacitance of the 4:1 MUX along the data path. Inductors with $L = 142$ pH resonate with the total load capacitance, consisting of the input capacitance of the 4:1 MUX and routing parasitics at 25 GHz, to lower power consumption. The buffers in the final stage are ac-coupled, so the duty cycle errors of the output clock can be compensated by adjusting the input dc voltage. In the post-layout simulations, the resonant buffer consumes 49.14 mW, which is approximately 60% of the buffer power when inductors are not used. Fig. 12 shows the 25-GHz duty cycle of the output

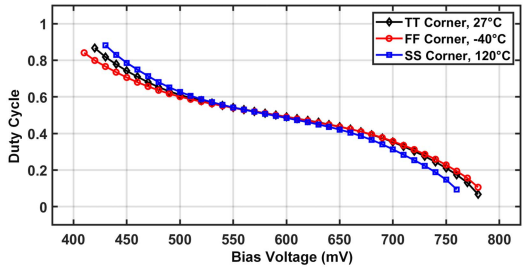


Fig. 12. Simulated C4 clock duty cycle versus input bias voltage under different corners and temperatures.

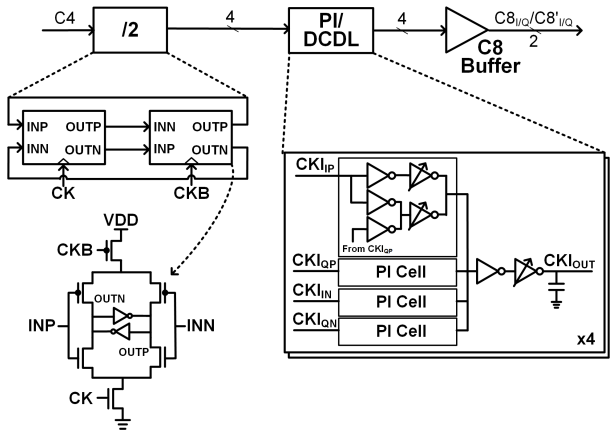


Fig. 13. Block diagram of the C8 clock path and circuit details.

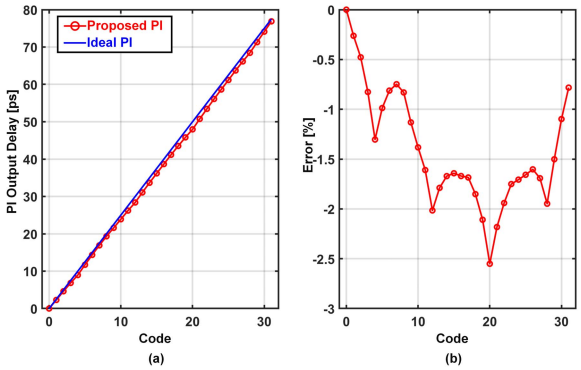


Fig. 14. (a) PI output delay versus ideal and (b) their percentage errors.

clock versus input bias voltage under different corners and temperatures in the post-layout simulation.

E. Clock Path: C8 Clock Distribution

To accommodate the delay across the 8:4 MUX, the 4:1 MUX, and the local clock buffer in the TX segments across PVT corners and to leave sufficient margin for the final 4:1 MUX, the C8 and C8' clock paths (Fig. 13) are designed with flexible delays. First, the C4 clocks go through a C^2MOS frequency divider, which can operate at 25 GHz across PVT corners and provide a large output swing to avoid the use of an extra CML-to-CMOS circuit. The divider consumes 8.93 mW of power in post-layout simulation. The divided clocks are then applied to an 5-bit inverter-based PI

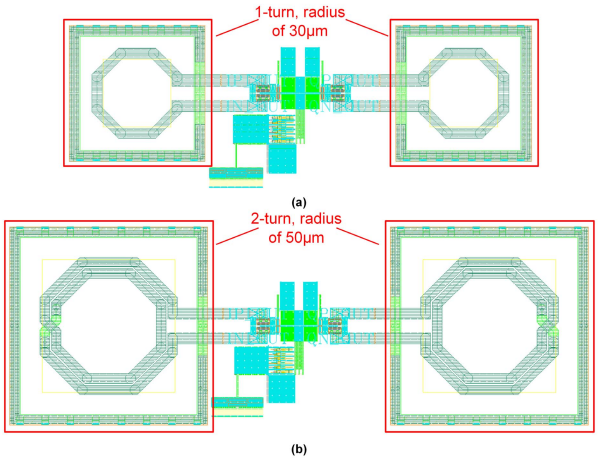


Fig. 15. C4 clock distribution layouts using (a) 1-turn inductor of radius 30-μm and (b) 2-turn inductor of radius 50-μm.

[20]. To improve the linearity, in the first stage, the 8-phase clocks are generated from the I/Q clocks and the interpolated clocks are subsequently generated in the second stage. As shown in Fig. 14, the two-stage PI increases linearity, with a maximum error of ∼2.5% observed in the post-layout simulation. To achieve a finer resolution and remove quadrature error, the current-controlled delay line, which has a resolution of 175 fs and a 4.6 ps tuning range, is used. ac-coupled buffers, similar to the ones used in the C4 clock distribution but excluding resonant inductors, are applied to drive the data path. Additionally, the duty cycle error can be adjusted via the input dc voltage, as in the case of the C4 buffer.

IV. Circuit Generation

Analog and mixed-signal (AMS) circuit designs have become increasingly complex and time-consuming in advanced technologies, with design rule explosion, progressively increased sensitivity to parasitics, and reliability issues. The Berkeley Analog Generator, an open-source hierarchical Python framework [21]–[23], was introduced to design AMS circuits quickly. BAG design scripts are written to automate design iteration loops, which involve circuit generation, extraction, simulation, and resizing. The design scripts drastically reduce the design and validation time. In addition, the layout and schematic python scripts are process-portable. Schematics and layouts can be generated in a new process simply by updating the low-level circuit-independent process scripts.

The proposed TX is primarily designed using BAG. Only top-level integration and the design of a handful of blocks, including ESD diodes and clock distribution wires, is done manually. First, Python-based layout generation scripts are written to describe circuit instance placement, routing, and/or power grid filling. These scripts extend the *XBase* layout engine [21] using different layout templates such as *TemplateBase*, *AnalogBase*, *DigitalBase*, and so on. The schematic generators are implemented with programmable device sizes. Utilizing process-specific input parameters associated with the grid, routing tracks, and device sizes, the layout and schematic generators produce DRC- and LVS-clean layouts.

In the generator design flow, the specifications and initial input parameters of the blocks and sub-blocks are derived from top to bottom. Then, the block-level designs are generated with BAG and extracted and verified manually to check whether specifications are satisfied. Iterations involving input parameter resizing, schematic and layout regeneration, and post-layout design simulation are performed until the design specifications are met. Finally, the generated block instances are combined to produce a top-level instance that satisfies all specifications. Because the time to regenerate a layout and schematic with modified sizes is less than 5 min, design iterations using this flow are only limited by simulation time. Fig. 15(a) and (b) shows two C4 clock distribution layouts with an 1-turn inductor of radius 30-μm and 2-turn inductor of radius 50-μm, respectively, demonstrating the flexibility and effectiveness of the layout generator.

Fig. 16 shows the hierarchy and flow of the TX design using the *XBase* layout engine. The schematic and layout generators fetch the design parameters and sizes to generate the schematic and layout for each block. For example, the 4:1 MUX schematic and layout are generated and extracted by running the BAG script. Post-layout simulations are performed, and the input parameters are adjusted until the bandwidth and rise/fall times meet requirements. Using a similar procedure, the high-level blocks are generated, such as the 128:8 serializer, 4:1 MUX and driver, T-coil, C4 and C8 clock distributions, current DAC, and voltage DAC. Finally, the customized blocks, digital design, and generated layouts are merged manually to produce the proposed top-level TX.

V. Measurement Results

The two prototype TXs (with and without ESD protection diodes) were fabricated in a 28-nm planar CMOS technology. The TX occupies an active area of 0.4323 mm^2 (Fig. 17). Fig. 18 shows the measurement setup. The output of the Keysight E8257D clock signal source is connected to a balun to generate the differential clock. This clock is fed to the chip via test probes. The chip's output data, also retrieved using test probes, is fed to the headers of the Keysight 86118A module through a dc block. The total channel loss through the probes, cables, dc blocks, and limited bandwidth of the sampling scope header is approximately 6 dB. The pulse response of the TX with the channel insertion loss is shown in Fig. 19. The insertion losses of the TXs with and without ESD protection were −13 and −15 dB, respectively.

Fig. 20 shows the data eye diagrams when applying PRBS7 patterns without and with ESD protection. Without ESD protection, the TX achieves a data rate up to 100 Gb/s using an NRZ pattern [Fig. 20(a)] and 200 Gb/s using a PAM-4 pattern [Fig. 20(c)]. Due to the ESD capacitance, the TX with ESD protection achieves a data rate up to 180 Gb/s using a PAM-4 pattern [Fig. 20(d)]. We also show that the data rate is 90 Gb/s when using the NRZ pattern [Fig. 20(b)]. The coarse and fine FFE coefficients for different scenarios are also indicated under the eye diagrams. The level mismatch ratios (RLM) of the PAM-4 eye diagrams are 98.4% and 98.2%, respectively, meeting the requirement of

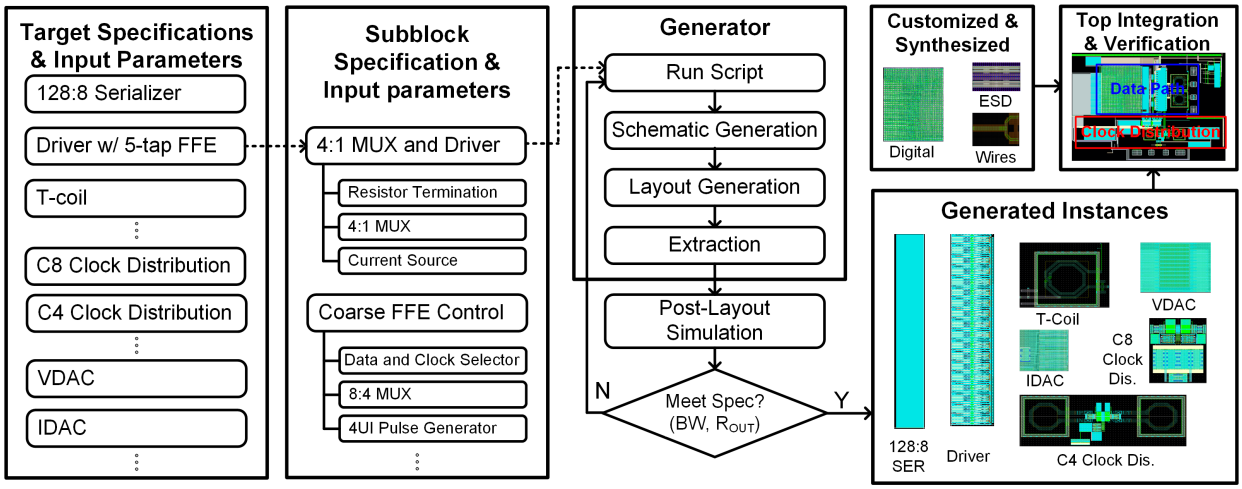
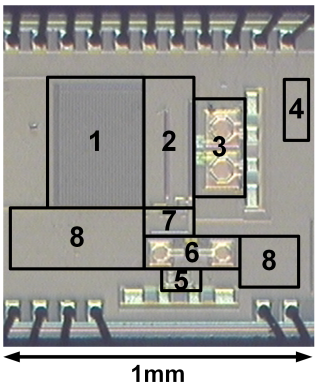


Fig. 16. Design flow of the proposed TX with BAG.



	Block	Layout
1	Pattern Gen+ Digital	Synthesized
2	TX Data Path	BAG
3	Output Network	BAG
4	FFE Bias Circuit	Custom + BAG
5	Clock Receiver	BAG
6	C4 Clock Dis.	BAG
7	C8 Clock Dis.	BAG
8	VDACs + IDACs	BAG
	Top	Custom

Fig. 17. Die photograph and layout details.

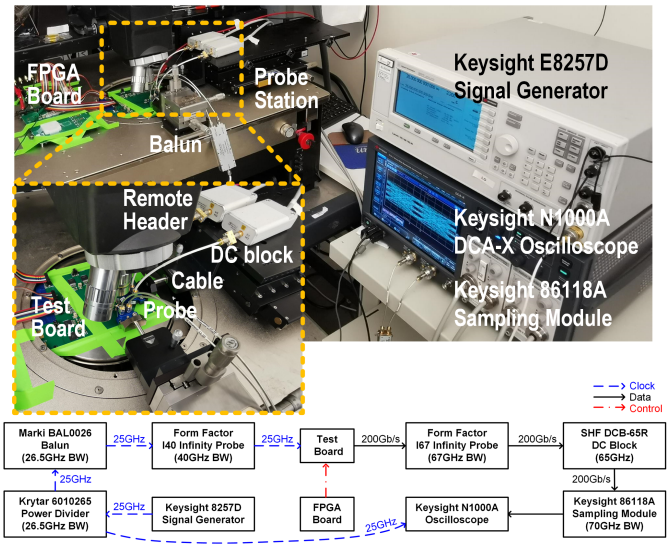


Fig. 18. Measurement setup.

>95% specified by relevant standards [24], [25]. As shown in the FFE coefficients of Fig. 20, under different scenarios, the reconfigurable FFE provides flexibility to change the FFE from having one main tap with one pre-tap and one post-tap to having one main tap and two post-taps. This allows the FFE

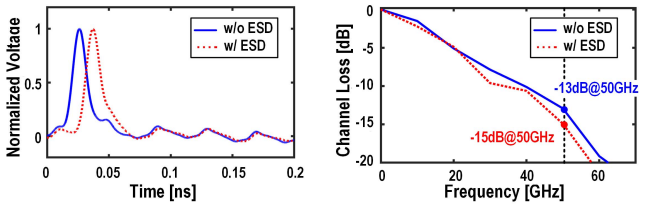


Fig. 19. 100-Gb/s pulse responses and insertion losses derived from measured pulse responses.

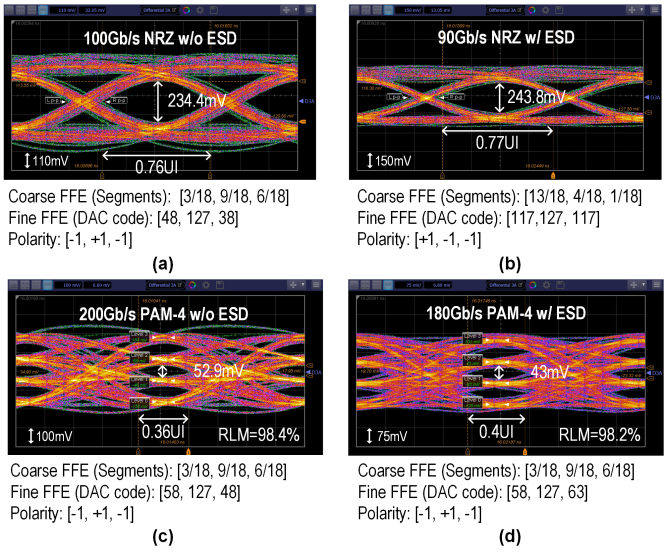


Fig. 20. Measured NRZ eye diagrams (a) without and (b) with ESD, and measured PAM-4 eye diagrams (c) without and (d) with ESD.

to accommodate different channels and data patterns, while maintaining the best performance.

To demonstrate the FFE capabilities, Fig. 21 compares the eye diagrams obtained when the FFE is on and off, while applying a 90 Gb/s NRZ pattern through a 16-in cable with 8-dB channel loss. Fig. 21(a) and (b) shows the pulse response and the derived insertion loss, respectively. Fig. 21(c) and (d) verifies the FFE function. Starting from a completely closed

TABLE II
TX PERFORMANCE COMPARISON

	[1]		[2]		[3]		[4]	[8]	[12]	This Work			
Technology	14nm		10nm		14nm		7nm	40nm	10nm	28nm			
Architecture	Quarter-rate		Quarter-rate		Quarter-rate		Quarter-rate	Quarter-rate	Quarter-rate	Quarter-rate			
Clock Source	External		On-chip		External		External	External	On-chip	External			
Output Swing w/o FFE (V_{ppd})	1		0.75		0.92		N/A	0.56	1.0	0.8			
FFE	3-tap		3-tap		8-tap		8-tap	8-tap	8-tap	5-tap			
ESD Protection	Yes		Yes		Yes		Yes	No	Yes	No		Yes	
Signaling	PAM-4	NRZ	PAM-4	NRZ	PAM-4	NRZ	PAM-4	NRZ	PAM-4	PAM-4	NRZ	PAM-4	NRZ
Data Rate (Gb/s)	128	64	112	56	112	56	112	100	224	200	100	180	90
Efficiency (pJ/bit)*	1.3	2.7	1.72	3.44	2.6	5.2	1.40	6.19	2.11	4.63	9.26	4.59	9.18
Eye Height (mV)	100**	240**	30	260	90**	170**	59	73	90	53	234	43	244
RLM	98.6%	N/A	98.5%	N/A	N/A	N/A	96.5%	N/A	99%	98.4%	N/A	98.2%	N/A
Active Area (mm^2)	0.048		0.0302		0.095		0.032	0.504	0.088	0.432			

*Excluding PLL and including DSP
**Estimated from eye-diagram

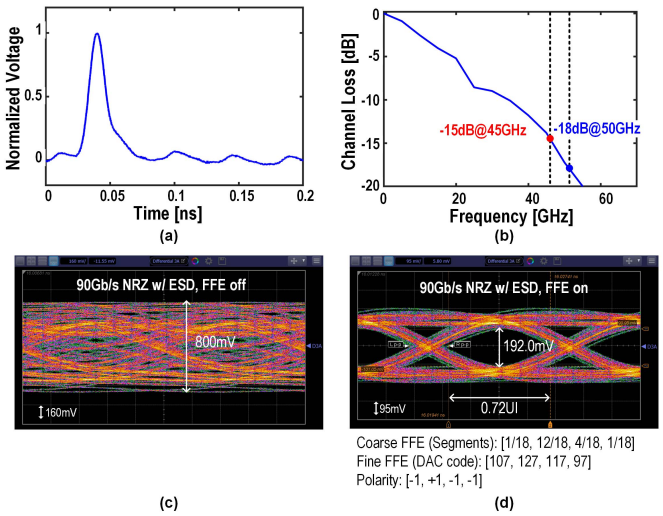


Fig. 21. (a) 16-in cable pulse response, (b) derived insertion loss, and the 90-Gb/s NRZ eye diagrams with (c) FFE off and (d) FFE on.

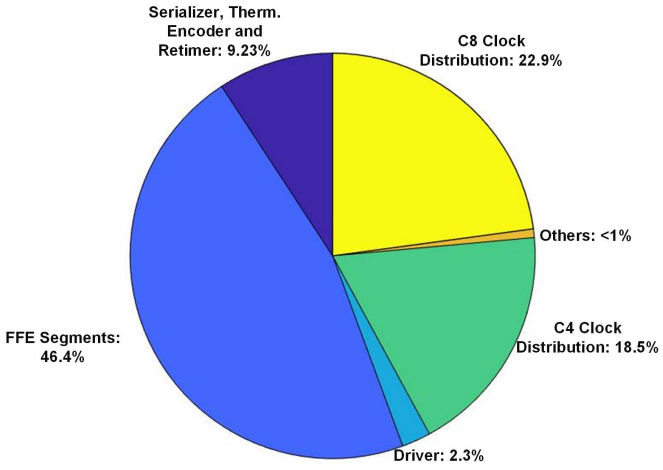


Fig. 22. Power breakdown based on post-layout extracted simulations.

eye, it is able to enlarge the data eye opening by compensating for ISI, leading to an eye height of 192 mV and eye width of 7.2 ps.

Fig. 22 shows the power breakdown of the chip based on the post-layout simulation, in which the FFE segments, C8 clock distribution, and C4 clock distribution consume approximately 46.4%, 22.9%, and 18.5% of the total power, respectively. Finally, Table II compares this article with the recently reported PAM-4 TXs operating above 100 Gb/s. With a planar CMOS technology, the proposed TX achieves the highest data rate with reasonable energy efficiency.

VI. CONCLUSION

A quarter-rate 100-Gb/s NRZ/200 Gb/s PAM-4 TX is proposed. The key techniques to reduce the output capacitance and optimize the output bandwidth/output swing are discussed, including the 4:1 MUX/driver with pull-up current sources, the reconfigurable 5-Tap FFE, and the flexible clock distribution network. This article demonstrates a SerDes TX design with the state-of-the-art data rate using a planar 28 nm process.

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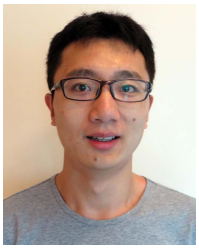

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