Power-Efficient Amplifiers for Data Converters

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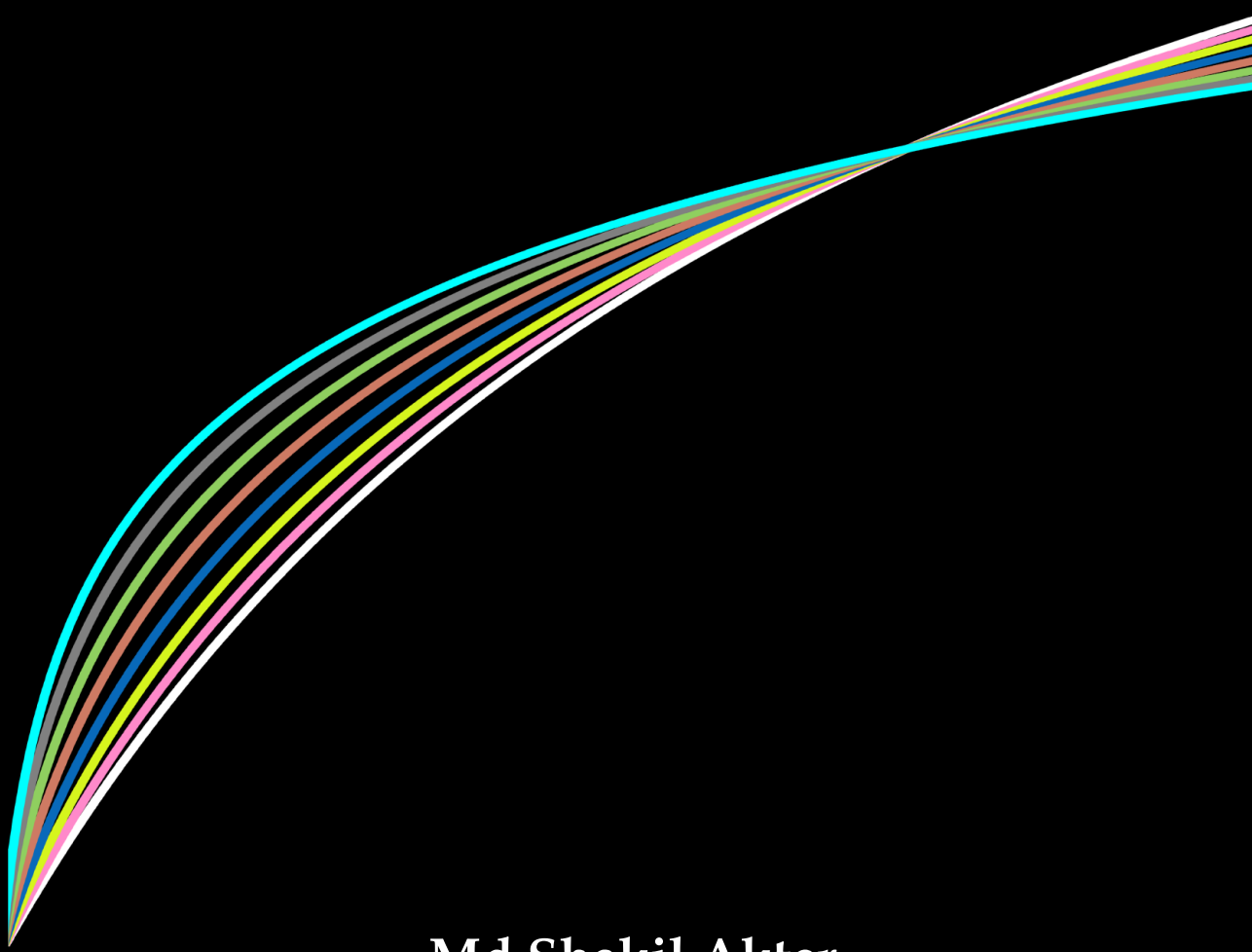

Md Shakil Akter

Power-Efficient Amplifiers for Data Converters

Power-Efficient Amplifiers for Data Converters

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology

by the authority of the Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen
Chair of the Board for Doctorates
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To my mother, Aklima

&

my wife, Kashmiena

Contents

1

Introduction

1.1 Motivation

Over the last few decades, the semiconductor industry has seen tremendous growth due to the continuous scaling of fine-line integrated circuit technology. Driven primarily by digital circuits such as microprocessors, memory and digital signal processing (DSP) units, the number of transistors per unit area has doubled every eighteen months [1]. Analog signal processing blocks have also benefited from this technology scaling, however, not to the same extent as digital circuits. As a result, they often limit the throughput of DSP-based systems [2].

In many systems, an analog-to-digital converter (ADC) is an essential analog signal processing block. Since real-life signals (speech, image) are analog by nature, they must first be digitized by an ADC before they can be used by a DSP unit. In order to do this without introducing extra noise or non-linearity, ADCs often consume a significant portion of system power. Hence, the design of power-efficient ADCs is an active research field, relevant to many applications requiring portability, high speed, and a wide dynamic range.

The use of software-defined radios [3], [4] in telecommunication systems is one such application. Driven by the trend towards more digital signal processing, their ADCs are located as close to the antenna as possible, so that channel selection, i.e. filtering and mixing, can be performed in the digital domain. The benefit of such systems are their flexibility and easy scalability to accommodate new communication standards. However, this requires a

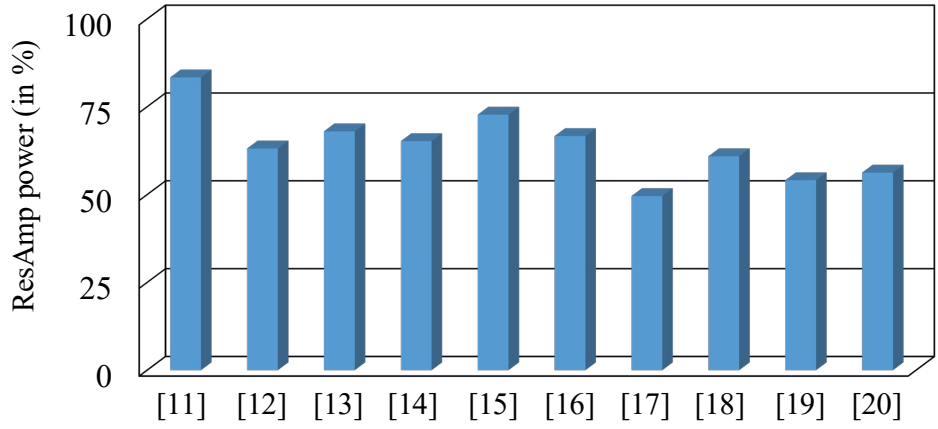

Figure 1.1: Percentage of the ADC power dissipated in residue amplifiers.

wideband ADC that can resolve weak signals in the presence of a strong interferer (or blocker) from an adjacent channel. Thus, the ADC must be linear (> 80dB) and support a wide dynamic range [5], [6]. Simultaneously, it needs to be power-efficient to compete with a traditional mixer-based approach.

Pipelined ADCs are often chosen for such wide-bandwidth and moderate-to-high resolution (> 10b) applications. Numerous studies [5]–[33] have been conducted at both the circuit and architectural level to improve the power efficiency of these ADCs. A crucial building block for such ADCs is a gain-stage that can suppress the noise from backend stages, thus improving the ADC's overall noise performance. It is often implemented as a switched-capacitor amplifier (known as a residue amplifier or ResAmp) that interfaces with the subsequent pipelined stages. However, since there is no gain-stage before the first amplifier, its noise directly appears at the ADC input. Hence, it dictates the overall noise and power efficiency of the ADC. Figure 1.1 shows a few examples from the literature [11]–[20] in which the percentage of power consumed by their ResAmps was determined. As expected, these amplifiers dissipate a significant portion of ADC power. With this in mind, the main goal of the research described in this thesis is the design of power-efficient amplifiers with optimal noise performance.

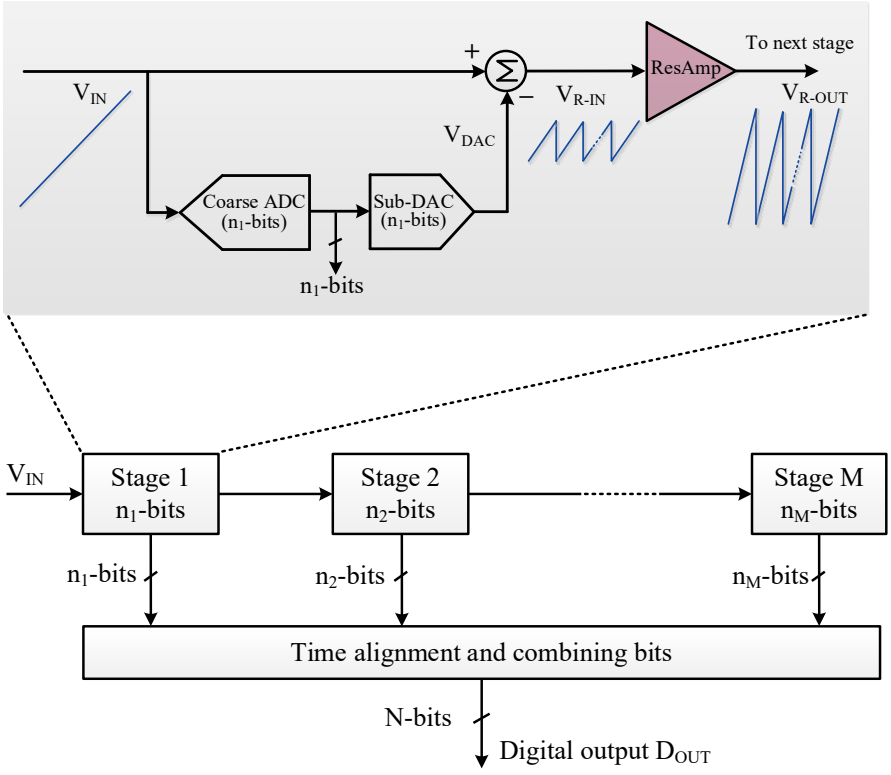

Figure 1.2: Simplified block diagram of a pipelined ADC.

1.2 Pipelined ADC: Brief Overview

A pipelined ADC architecture employs multiple sub-ranging stages to convert an analog input signal into a digital output. Figure 1.2 shows a simplified block diagram of a pipelined ADC. Each stage consists of a coarse ADC that quantizes the sampled input V_{IN} with a chosen number of bits. The sub-DAC uses these bits to form an estimated input signal V_{DAC}. The difference between V_{IN} and V_{DAC} represents the residue input $V_{R\text{-}IN}$, which needs to be processed by the following stages. As shown in Figure 1.2, the amplitude of the residue input $V_{R\text{-}IN}$ is usually less than the ADC's full-scale range. Hence, it is amplified by a residue amplifier before it is passed on to the next stage.

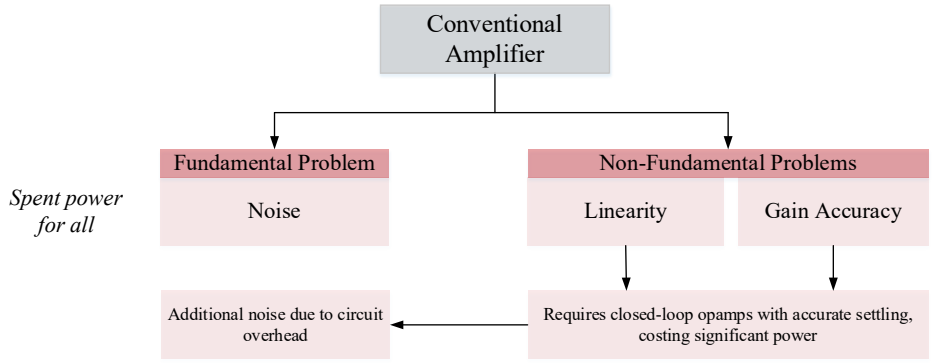

Figure 1.3: Design approach for a conventional residue amplifier.

The pipelined stages operate in complementary phases, i.e. while one stage amplifies the residue signal, the next stage samples it. As a result, the throughput of the ADC can be as fast as that of a single-stage while still allowing digitization of the analog signal with high resolution. Since different stages operate on an input sample at different times, their digital outputs should be time-aligned and combined to generate the final digital output D_{OUT}.

1.3 Residue Amplifier: Design Challenges

A residue amplifier (ResAmp) needs to transfer the discrete-time sub-ranged signals from one pipelined stage to the next. To maintain signal integrity during this transfer, it needs to adhere to specifications such as noise, linearity, and gain accuracy. Conventional ResAmp designs mostly address these challenges in a purely analog fashion (Figure 1.3) by employing a precision op-amp in a closed-loop configuration [10]–[17]. Consequently, static gain errors and nonlinearities are suppressed by the amplifier's high loop gain. However, due to the resulting circuit complexity, these amplifiers often exhibit sub-optimal noise performance. Moreover, they require a large bandwidth to reduce dynamic errors and achieve the desired gain accuracy. For example, if an ADC backend is to resolve 10-bits after a ResAmp, then it needs about 60dB or 6.9τ settling accuracy, where τ is the ResAmp's time constant. This demand for accurate settling requires a significant amount of power (more detail in Chapter 2), degrading the amplification efficiency.

Over the past few years, various amplifier topologies and circuit techniques have evolved [18]–[32] to improve power efficiency. Some examples include ring amplifiers [19], open-

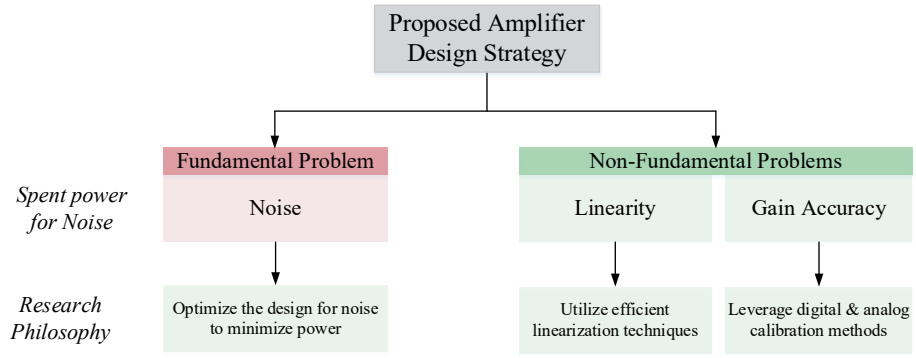

Figure 1.4: Amplifier design approach followed in this research.

loop or integrating amplifiers [21], class-AB amplifiers [22], zero-crossing detectors [23], capacitive charge pumps [24], pulsed bucket brigades [27], and time-based amplification [28]. Of the different amplifier topologies, open-loop or integrating amplifiers [21], [26], [29]–[32] inherently provide the lowest small-signal bandwidth and thus the lowest power dissipation for a given noise performance. However, they also exhibit more nonlinearity. Since this is deterministic in nature, it can often be mitigated with the help of digital calibration.

Although digital calibration is not a new concept, it is increasingly used to simplify ResAmp design and improve power-efficiency [9], [11], [15], [21], [24]–[35]. However, the amount of digital assistance used should be balanced against the power overhead entailed. Therefore, it is useful to identify which tasks can be delegated to the digital domain without costing much power. For example, error correction generally requires significantly more power than error detection because it requires faster logic (discussed in Chapter 2). Moreover, from literature it can be seen that while gain errors can be calibrated in a low-power manner [33], nonlinearity calibration requires more power [34]–[35].

1.4 Research Direction

Figure 1.4 depicts the design approach that will be followed in this work. It can be broken down into three main components as follows:

Developing New Circuit Techniques: Efficient analog techniques are developed to improve the ResAmp power efficiency. A significant part of this is the development of new

linearization techniques that allow open-loop/integrating amplifiers to achieve high linearity without affecting their excellent noise properties.

Developing Power-Efficient Switched-capacitor Amplifiers: The design philosophy is to dissipate power primarily to reduce noise, and then to resolve other circuit imperfections with minimal power overhead. Thus, push-pull inverter-like structures, and integrating amplifiers are investigated.

Combining Digital and Analog Calibration Techniques: Existing digital calibration techniques are leveraged to simplify the amplifier design. However, its power overhead is minimized by only doing digital error detection. The detected errors are subsequently corrected in the analog domain (i.e., at their source) using efficient analog techniques.

1.5 Organization

This dissertation consists of seven chapters and is organized as follows. Chapter 2 describes various circuit design choices that have been used to optimize the power efficiency of residue amplifiers. It also addresses the use of digital calibration. Chapter 3 reviews existing and proposes new linearization techniques to improve amplifier linearity. It is shown that the proposed techniques enable open-loop amplifiers to achieve excellent linearity while preserving their optimal noise performance. Utilizing the concepts in Chapters 2 and 3, three prototype amplifiers have been implemented. The first is presented in Chapter 4, which describes a class-AB residue amplifier in a pipelined split-ADC. Chapter 5 describes an open-loop amplifier that utilizes a resistive degeneration technique to achieve high linearity. Chapter 6 introduces a new integrating amplifier topology based on the concept of a floating supply. It employs a novel linearization technique, described in Chapter 3, to achieve excellent linearity. The effectiveness of this proof-of-concept amplifier, in 28nm CMOS, is validated with experimental results. Finally, Chapter 7 summarizes the thesis and concludes with possible future work.

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2

Digitally Assisted Residue Amplifier

As outlined in Chapter-1, this chapter describes the application of digital techniques to optimize the power efficiency of residue amplifier (ResAmps). Section 2.1 discusses the influence of different circuit parameters on amplifier power efficiency. This is elaborated by showing examples of amplifiers based on push-pull inverter topology in Section 2.2. Section 2.3 explains the concept of incomplete settling and how it can reduce the amplifier's power dissipation. Finally, Section 2.4 focuses on calibrating amplifier nonidealities with minimum power overhead.

2.1 Power Efficiency

There are numerous figures-of-merit (FoM) in the literature [1]–[3] that can be used to evaluate the power efficiency of a ResAmp. One such measure, known as the Schreier FoM [2], is given below:

$$\mathrm{FoM}_S = \mathrm{DR(dB)} + 10\log\left(\frac{\mathrm{BW}}{P_{amp}}\right) \tag{2.1}$$

Equation (2.1) suggests that the amplifier's power efficiency can be improved by lowering its power dissipation P_{amp} for a given bandwidth (BW) and dynamic range (DR).

While the above outcome is obvious, it is essential to understand what design choices can lead to a low-power amplification. To do this, the power efficiency metric F_{circuit}, given in [3], can be used. It is a dimensionless number that is dictated by circuit design choices. [3] provides a detailed overview of how circuit parameters can influence this F_{circuit}, and how it can be used to compare various amplifier topologies. The expression for F_{circuit} is given below:

$$F_{\text{circuit}} = \text{NEF}\, n_\tau \left((V_{GS} - V_{th})/V_{\text{DD}}\right) / \left(\eta_{\text{cur}}\eta_{\text{vol}}^2\right) \tag{2.2}$$

where,

$$\text{NEF} = \text{Noise excess factor} = \frac{\text{Total noise power}}{\text{Noise power } g_m \text{ transistor(s)}}$$

n_τ = Number of time-constant (τ) settling of the amplifier

$$\eta_{\text{cur}} = \text{Current efficiency of the amplifier} = \frac{\text{Required current for } g_m}{\text{Total current drawn from the supply}}$$

$$\eta_{\text{vol}} = \text{Voltage efficiency of the amplifier} = \frac{\text{Maximum peak-to-peak signal voltage}}{\text{The supply voltage } V_{\text{DD}}}$$

Note that a lower F_{circuit} represents a better power efficiency. Equation (2.2) indicates that an amplifier will achieve a high power efficiency or low F_{circuit} if

(i) Its NEF = 1 (note that NEF is always ≥ 1). This means that the total noise is contributed mainly by transistors that provide signal gain or g_m.

(ii) It settles within a smaller number of τ (more on this in Section 2.3).

(iii) A lower gate overdrive voltage (V_{GS}–V_{th}) is used, encouraging weak-inversion operation for MOSFETs.

(iv) It exhibits a high current efficiency η_{cur}, approaching 1. To realize this, extra current branches not necessary for attaining g_m should be avoided.

(v) Its voltage efficiency η_{vol} can be increased by using circuit topologies that allow large signal swings relative to the supply voltage V_{DD}.

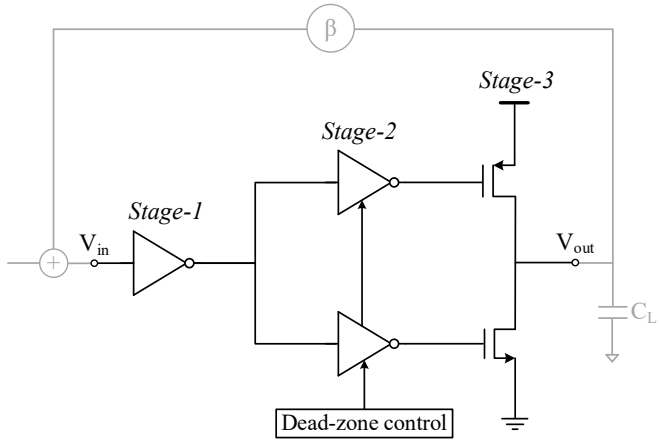

Figure 2.1: Simplified half-circuit of a ring amplifier.

2.2 Efficient Amplifier Topologies

In the last several years, various power-efficient amplifier topologies have been proposed [4]–[14]. A detailed overview and comparison of those can be found in [3]. In this section, two of these will be briefly discussed: the ring amplifier [4]–[5] and the push-pull inverter [7]–[9]. Both amplifiers are based on simple inverter circuits, hence offer power-efficient approaches to discrete-time amplification in nanoscale CMOS technologies.

2.2.1 Ring Amplifier

The ring amplifier [4]–[5] consists of three inverter stages in a closed-loop feedback configuration, as shown in Figure 2.1. However, unlike a conventional closed-loop amplifier, it does not make the internal-pole dominant (using techniques such as Miller or Ahuja compensation) to obtain stability. In fact, the amplifier is allowed to oscillate or ring at the start of amplification.

A stable response is achieved over the amplification time through a dynamic large-signal stabilization method. This is facilitated by introducing a “dead zone” in the transfer function of the output stage, within which both output devices are switched OFF, thus reducing the effective gain to zero. Hence, although the amplifier can ring at first, as soon as its output voltage gets close to the desired value, the output stage will enter its dead zone, realizing a

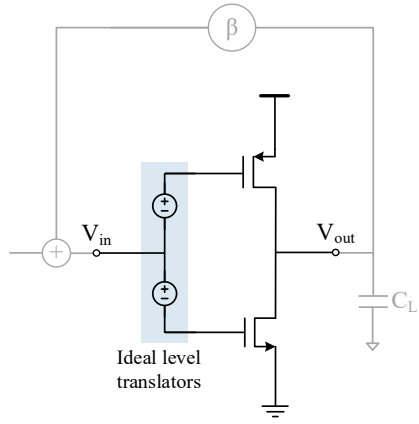

Figure 2.2: Simplified half-circuit of a single-stage inverter or class-AB amplifier.

high output impedance that pushes its output pole to low frequencies and thus stabilizes the amplifier. Since the stability directly depends on the dead zone's width, it should be carefully controlled with dedicated circuitry (Figure 2.1).

The ring amplifier has several benefits. It has fast internal nodes, resulting in a fast settling response and high power efficiency. It employs complementary input stages, thus boosting transconductance g_m by reusing bias currents. Moreover, it supports a large output signal swing. However, the drawback of this approach is that the input-referred noise, which is primarily determined by the input stage, requires a certain power overhead.

2.2.2 Inverter Amplifier

The push-pull inverter (or a class-AB amplifier) [7]–[9] is another power-efficient topology for discrete-time systems. It contains a single inverter stage, as shown in Figure 2.2, in contrast to the ring amplifier's three-stage design. Due to its single-stage topology, the amplifier is inherently stable and exhibits a fast transient response. It achieves nearly 2× larger g_m because the same quiescent current flows through both the NMOS and PMOS transistors. It can also support a large signal swing as there is no cascoding or tail current source in the output branch.

While the abovementioned benefits are shared by both the ring amplifier and the push-pull inverter, the latter offers two added benefits. First is the excellent noise performance with a NEF close to 1. This is because all the transistors that contribute noise also provide

signal gain (or g_m). Second, it exhibits a high current efficiency ($\eta_{cur} = 1$) [3] because the current drawn from the supply is efficiently used to create signal g_m. Due to these benefits, the focus of this work will be on the optimal design of push-pull inverters.

The circuit benefits and resulting high power efficiency of the push-pull inverter come with a few design challenges. First, this amplifier has inherently low DC gain, and hence its closed-loop gain varies across PVT, necessitating digital calibration (discussed in Section 2.4). Second, it requires level shifters to actively drive the NMOS and PMOS inputs (proposed in Section 4.2.1). Third, it exhibits low CM rejection, which can be mitigated by differential sampling (Section 4.3.2) or the "floating supply" technique (Section 6.2.2) presented in this thesis.

2.3 Incomplete Settling

A ResAmp relies on accurate settling to transfer the residue signal from one pipelined stage to the next in a typical closed-loop configuration. However, the amplifier's bandwidth needs to be sufficiently wide to achieve this within a specified amplification time. As a result, the amplifier's power dissipation is often increased. A viable option to reduce this power is to lower the settling accuracy (i.e. n_τ in (2.2)) of the amplifier [15], [16]. In this section, the effect of incomplete settling on the amplifier's gain, noise, and power dissipation is analyzed to show how it can assist in obtaining power-efficient amplification.

2.3.1 Transient Gain

Consider the closed-loop switched-capacitor amplifier shown in Figure 2.3, where C_S and C_F are the sampling and feedback capacitors, respectively. C_L denotes the load capacitor. During the amplification phase, the output voltage $V_{OUT}(t)$ is built up over time (t) in response to the applied input step V_{IN}. $V_{OUT}(t)$ can then be expressed as follows:

$$V_{OUT}(t) = V_{IN} \frac{C_S}{C_F} \frac{A\beta}{1+A\beta} \left(1 - exp^{-t/\tau}\right) \tag{2.3}$$

where, A denotes the open-loop gain, β is the feedback factor [$=C_F/(C_S+C_F)$], and τ represents the closed-loop time constant of the amplifier. τ is inversely proportional to the amplifier's closed-loop bandwidth f_{-3dB}. The expressions for τ and f_{-3dB} are shown below:

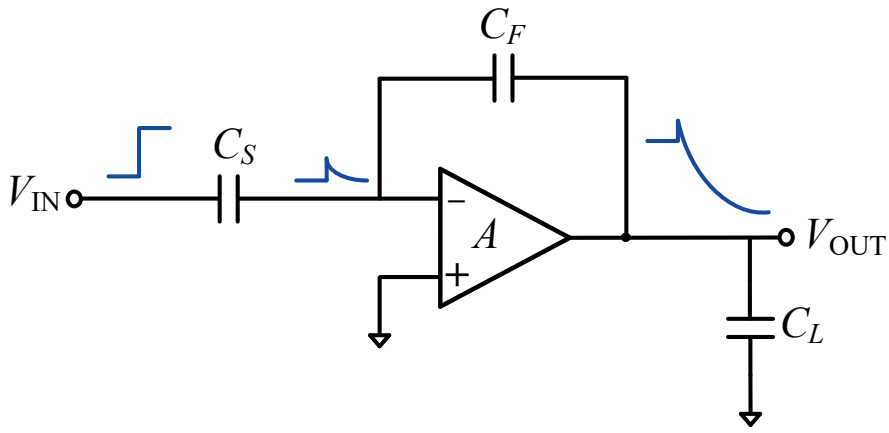

Figure 2.3: Switched-capacitor amplifier in a closed-loop configuration.

$$\tau = \frac{1}{2\pi f_{\text{-3dB}}} \tag{2.4}$$

$$f_{\text{-3dB}} = \frac{\beta g_m}{2\pi C_L} \tag{2.5}$$

It is evident that the large-signal transient gain $G(t)$ of the amplifier, defined as the ratio of the instantaneous amplitude of the output signal to the amplitude of the input step, increases with time. The transient gain can be derived from (2.3) as follows:

$$G(t) = \frac{V_{\text{OUT}}(t)}{V_{\text{IN}}} = \left(\frac{C_S}{C_F}\frac{A\beta}{1+A\beta}\right)\left(1 - exp^{-t/\tau}\right) \tag{2.6}$$

The exponential component in (2.6) represents the gain error $G_{\text{err}}(t)$ due to settling:

$$G_{\text{err}}(t) = exp^{-t/\tau} \tag{2.7}$$

When the settling error approaches zero, the amplifier reaches its steady-state gain (G_{SS}), which is given by the capacitor ratio and loop gain $A\beta$ as follows:

$$G_{\text{SS}} = \frac{A\beta}{1+A\beta}\frac{C_S}{C_F} \tag{2.8}$$

Figure 2.4 shows the settling behavior of the amplifier's gain $G(t)$ and its error $G_{\text{err}}(t)$. The x-axis represents the amplification time normalized to the time constant τ. It can be

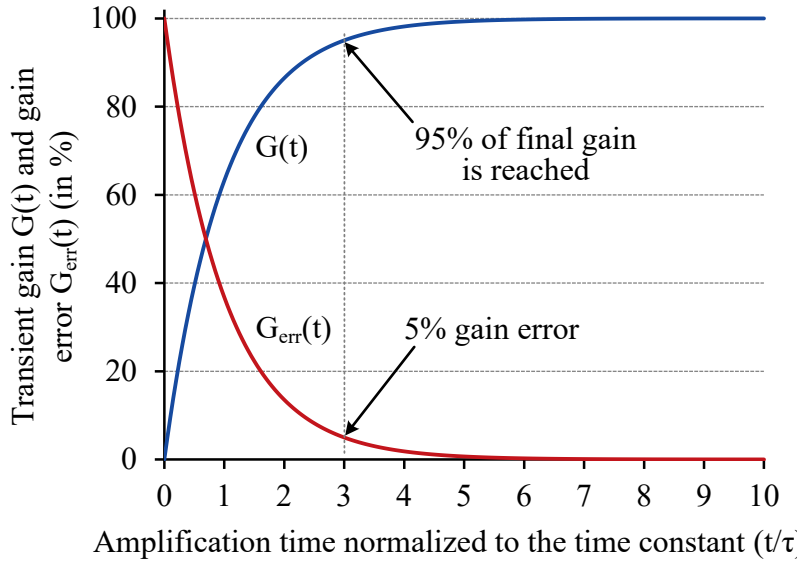

Figure 2.4: Transient gain and gain-error of the amplifier versus its degree of settling.

observed that the amplifier achieves most of its gain during the first few time-constants of settling. After 3τ settling, it reaches 95% of its steady-state gain and exhibits a 5% gain error. This can be further reduced by allowing more settling. However, since the power dissipated in the amplifier is equal for every time interval τ, this will require more power.

Usually, a ResAmp operates for a fixed amplification time t_A, specified by the ADC clock. Let us assume that the target gain of the amplifier after the time t_A is G_{eff}. By using the Equations (2.6) and (2.8), the gain G_{eff} at time $t = t_A$ can be written as follows:

$$G_{eff} = G(t = t_A) = G_{SS}(1 - exp^{-n_\tau}), \tag{2.9}$$

where, $n_\tau = t_A/\tau$ = the number of τ settling during the amplification phase (representing settling accuracy).

Equation (2.9) indicates that there can be various n_τ choices to achieve the target gain G_{eff} if the steady-state gain G_{SS} is appropriately adjusted. According to (2.8), G_{SS} can be tuned by simply changing the capacitor ratio (C_S/C_F). In closed-loop amplifiers, the steady-state gain G_{SS} is typically made equal to the required gain G_{eff}. However, selecting a $G_{SS} > G_{eff}$ allows for less settling (i.e. lower n_τ) to achieve G_{eff}. This is illustrated in Figure 2.5. As G_{SS}

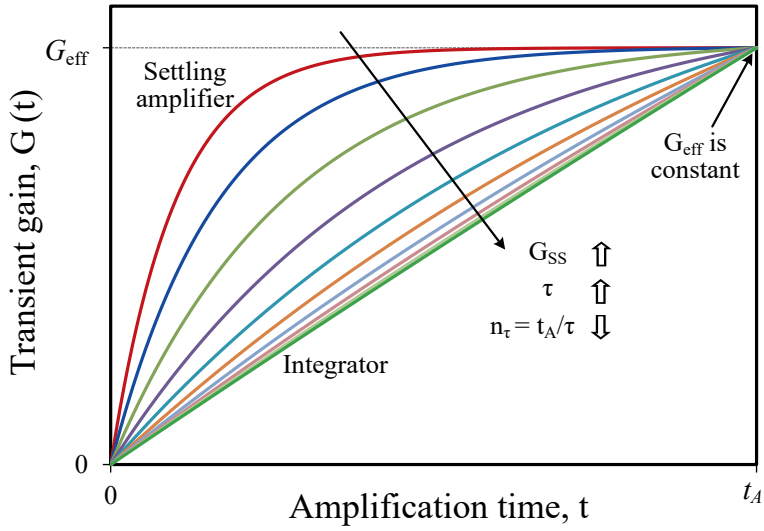

Figure 2.5: Transient gain of the amplifier for various steady-state gains (G_{SS}). It should be noted that the final gain of the amplifier at the end of the amplification phase (t = t_A) is constant for all the G_{SS} values.

is increased, n_τ is lowered to keep a constant gain G_{eff} by allowing a larger settling time constant τ. This means the amplifier requires less bandwidth ($f_{-3dB} \propto 1/\tau$), thus less power. Hence, it can be concluded from the above discussion that by correctly combining incomplete settling with a higher steady-state gain G_{SS}, an amplifier can achieve its desired amplification G_{eff} with significantly reduced power dissipation.

2.3.2 Power Dissipation and Noise

The discussion so far has indicated that incomplete settling enhances amplifier power efficiency. This section analyzes this benefit quantitatively by calculating the amplifier's power dissipation and noise-power as a function of settling n_τ. Note that the analysis shown here uses the derivations given in [15]–[18]. A sufficiently high loop gain is assumed to simplify the analysis.

First, we calculate the power dissipation (P_{amp}) of the amplifier in terms of its degree of settling (n_τ). It can be expressed as follows:

$$P_{amp} = \frac{V_{DD}}{2\eta_{cur}} V_{GT}\, g_m \qquad (2.10)$$

where, $V_{GT} = V_{GS} - V_{th}$ = the overdrive voltage of the input transistor. By combining expressions (2.4) and (2.5), transconductance g_m can be represented as follows:

$$g_m = \frac{C_L}{\tau}\left(\frac{1}{\beta}\right) = \frac{C_L}{t_A}\, n_\tau\,(1 + G_{SS}) \tag{2.11}$$

Substituting (2.11) into (2.10) and by using (2.9), the following expression can be derived:

$$P_{amp} = \frac{V_{DD} V_{GT} C_L}{2\eta_{cur} t_A}\left[n_\tau\left(1 + \frac{G_{eff}}{1 - exp^{-n_\tau}}\right)\right] \tag{2.12}$$

Equation (2.12) confirms the intuition that the amplifier's power dissipation P_{amp} decreases with reduced settling, i.e. with smaller n_τ. In the limit case, when n_τ approaches zero (for an ideal integrator), P_{amp} reaches its minimum value. To calculate this, part of (2.12) can be evaluated by applying the L'Hospital's rule[1] [19] as follows:

$$\lim_{n_\tau \to 0} \frac{n_\tau}{1 - exp^{-n_\tau}} = \lim_{n_\tau \to 0} \frac{\frac{\mathrm{d}}{\mathrm{d}n_\tau}(n_\tau)}{\frac{\mathrm{d}}{\mathrm{d}n_\tau}(1 - exp^{-n_\tau})} = \lim_{n_\tau \to 0} \frac{1}{exp^{-n_\tau}} = 1$$

Using the above calculation in (2.12) results in the amplification power as follows:

$$P_{amp}(n_\tau \to 0) = \frac{V_{DD} V_{GT} C_L}{2\eta_{cur} t_A}\; G_{eff} \tag{2.13}$$

Next, the amplifier's output noise power ($P_{n,out}$) is calculated as a function of its settling n_τ. As derived in [18], the output noise power $P_{n,out}$ can be expressed as follows, assuming that the load capacitor C_L limits the noise bandwidth of the amplifier:

$$P_{n,out} = \frac{\gamma kT}{C_L}\left(\frac{1}{\beta}\right)(1 - exp^{-2n_\tau}) + \frac{kT}{C_L} exp^{-2n_\tau}$$
$$= \frac{\gamma kT}{C_L}(1 + G_{SS})(1 - exp^{-2n_\tau}) + \frac{kT}{C_L} exp^{-2n_\tau}$$

Here, γ is the noise factor of the MOS transistor. Substituting the value of G_{SS} from (2.9) results in as follows:

[1] L'Hospital's rule: The limit of a quotient of functions is equal to the limit of the quotient of their derivatives

$$P_{n,\text{out}} = \frac{\gamma kT}{C_L}\left(1+\frac{G_{eff}}{1-exp^{-n_\tau}}\right)(1-exp^{-2n_\tau}) + \frac{kT}{C_L}exp^{-2n_\tau} \tag{2.14}$$

The last term in (2.14), i.e. $\frac{kT}{C_L}exp^{-2n_\tau}$, is a noise component associated with resetting the load capacitor C_L. If C_L is assumed to be perfectly reset before amplification, then kT/C_L noise is sampled across it. As the amplifier settles during amplification, it forces the output voltage on C_L to follow the input according to (2.3). Consequently, any initial sampled noise voltage on C_L is reduced exponentially over the amplification time [18].

To understand how noise $P_{n,\text{out}}$ changes with settling, two extreme scenarios can be considered. In the first case, the amplifier is assumed to have a near-complete settling (i.e. large n_τ). Consequently, the expression of (2.14) reduces to:

$$\begin{aligned} P_{n,\text{out}}(\text{large } n_\tau) &\approx \frac{\gamma kT}{C_L}\left(1+\frac{G_{eff}}{1-0}\right)(1-0) + \frac{kT}{C_L}\times 0 \\ &\approx \frac{\gamma kT}{C_L}\left(1+G_{eff}\right) \end{aligned} \tag{2.15}$$

Equation (2.15) indicates that if the amplifier has sufficient settling, the reset noise component due to C_L will disappear. For the second case, let us assume that the amplifier does not settle, with n_τ approaching zero. Thus, (2.14) can be approximated as follows:

$$P_{n,\text{out}}(n_\tau \to 0) \approx \frac{\gamma kT}{C_L}\left(2G_{eff}\right) + \frac{kT}{C_L} \tag{2.16}$$

Comparing (2.16) with (2.15) shows that the output noise power $P_{n,\text{out}}$ gradually increases with reduced settling n_τ. This is partly due to the reset noise of C_L but also because the amplifier's inherent noise contribution gets larger with smaller n_τ [16].

The above observations can be better visualized by plotting the amplifier's power dissipation P_{amp} and noise $P_{n,\text{out}}$ as a function of settling. As shown in (2.9), the target gain G_{eff} of the amplifier depends on its steady-state gain G_{SS} and settling accuracy n_τ. If we increase the steady-state gain G_{SS}, the amplifier can lower its settling accuracy n_τ to reach the same target gain G_{eff}. This relationship between n_τ and G_{SS} for a given G_{eff} can be derived by rearranging (2.9) as follows:

$$n_\tau = -ln\left(1-\frac{G_{eff}}{G_{\text{SS}}}\right) \tag{2.17}$$

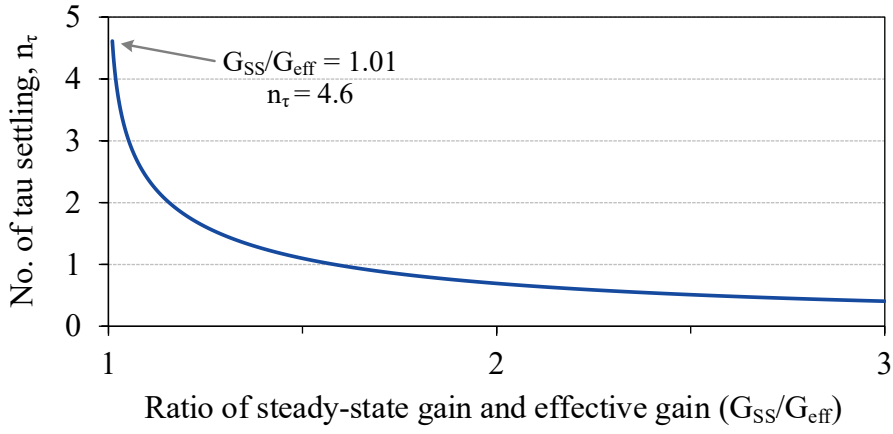

Figure 2.6: Required number of tau settling n_τ to achieve a constant gain G_{eff} as a function of G_{SS}/G_{eff} ratio.

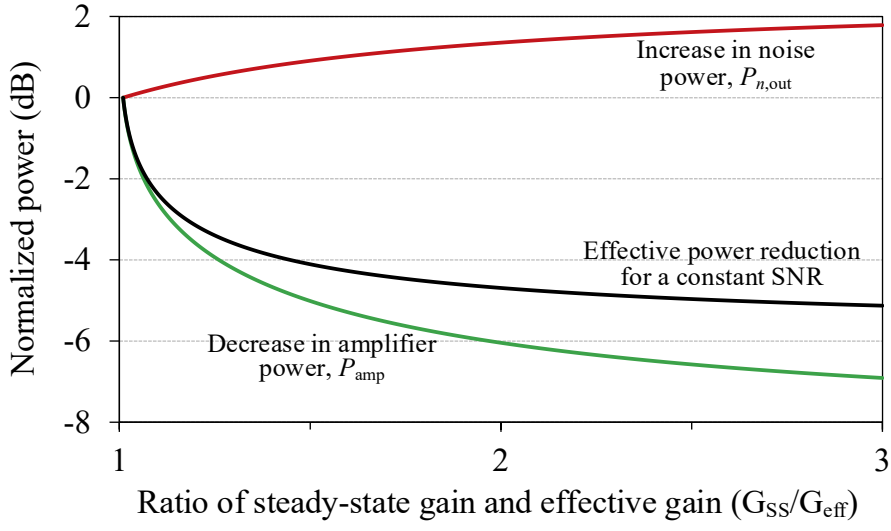

Figure 2.7: Normalized power dissipation and noise power of the amplifier as a function of G_{SS}/G_{eff} ratio. Note that the normalized powers are calculated with respect to their values at G_{SS}/G_{eff} = 1.01.

Figure 2.6 illustrates how the settling accuracy n_τ can be reduced for a constant effective gain G_{eff} when the gain factor (G_{SS}/G_{eff}) is increased. It can be observed from (2.17) that n_τ approaches infinity when G_{SS}/G_{eff} = 1. To avoid this boundary condition, an arbitrary starting point is chosen for G_{SS}/G_{eff}, which is 1.01 instead of 1.0, as can be seen from Figure 2.6.

We can use the n_τ from (2.17) in (2.12) and (2.14) to evaluate the power dissipation P_{amp} and noise $P_{n,out}$ of the amplifier, respectively. It is shown in Figure 2.7 for $G_{eff} = 2$. Both P_{amp} and $P_{n,out}$ are normalized relative to their values at the chosen starting point, i.e. when $G_{SS}/G_{eff} = 1.01$. It can be observed from Figure 2.7 that raising the steady-state gain, i.e. reducing n_τ, decreases the amplifier's power dissipation while increasing its output noise power. For example, when $G_{SS}/G_{eff} = 1.6$, the amplifier requires 1τ settling compared to 4.6τ for $G_{SS}/G_{eff} = 1.01$. Consequently, the power dissipation is decreased by 5.3 dB with a 1 dB increase in noise power. Since the decrease in power dissipation is significantly larger than the increase in noise power, the amplifier's overall power efficiency is improved. It can be further deduced from Figure 2.7 that the amplifier reaches optimum power efficiency when it does not settle and behaves like an integrator [10]–[14]. Hence, incomplete settling is used in this research to enhance amplification efficiency.

However, the use of incomplete settling in amplifiers comes with a few drawbacks. First, the amplifier is unable to build up enough loop gain and thus exhibits inaccurate steady-state gain G_{SS} even though β is accurate. Consequently, the effective gain G_{eff} is sensitive to the process, supply voltage, and temperature (PVT) variations. Gain calibration can be used to resolve this issue, as will be discussed in the next section. Second, due to the limited loop gain, linearity will not be significantly improved by negative-feedback. However, it can be improved by digital calibration (Section 2.4) or by using linearization techniques discussed in Chapter 3.

2.4 Calibration

In this section, the use of calibration in a residue amplifier is discussed. Calibrating analog errors in the digital domain is not a new idea [18], [20]–[23]. It is becoming increasingly attractive as technology scaling enables faster and more efficient digital signal processing. However, care should be taken when leveraging digital calibration to minimize its power and area overhead.

Calibrating an error involves two steps: (i) error detection and (ii) error correction. The detection circuit needs to track or detect the error over changing PVT conditions, which is a relatively slow process. Therefore, the detection logic can operate at a rate much lower than the ADC clock, dissipating negligible power. Unlike the detection circuit, the error correction logic must run at the ADC clock rate to correct each data sample. Hence, digital

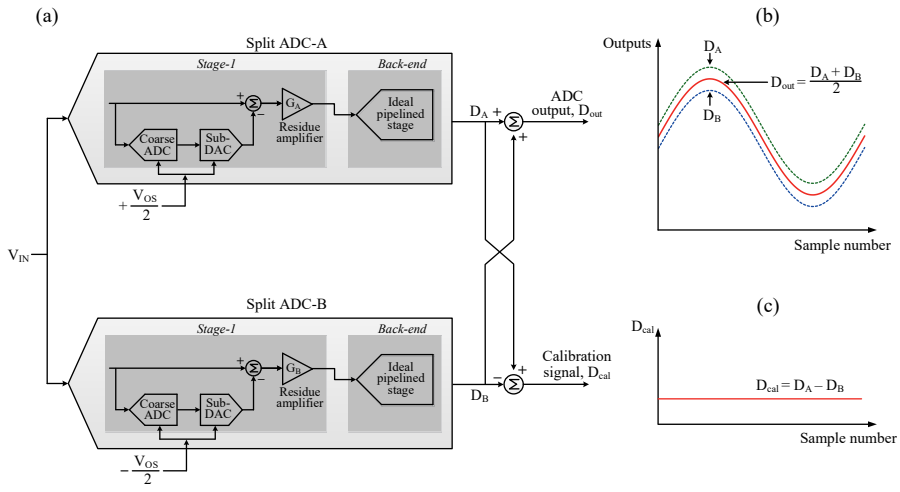

Figure 2.8: (a) Simplified diagram of a pipelined split-ADC architecture and its (b) digital output and (c) calibration signal for a sinusoid input.

error correction can often require considerable power dissipation. This section will elaborate further on these error detection and correction processes.

2.4.1 Error Detection

The first step of calibration is to detect the errors of the residue amplifier. Examples of errors include offset, inaccurate gain, and nonlinearity. An offset in a residue amplifier causes a shift in the ADC input-output transfer curve but does not cause INL/DNL errors. In contrast, gain error and nonlinearity affect signal integrity, thus needs to be calibrated. Various digital calibration techniques can be used to detect these errors. They can operate in the foreground [24] or background [20] and also can be deterministic [9] or stochastic [23] in nature.

In this design, the well-known split-ADC calibration [21], [25]–[27] technique is investigated to detect amplifier errors. It has been chosen because of its deterministic nature, thus requiring fewer clock cycles to converge than statistics-based approaches. Additionally, it can operate continuously in the background, unlike other deterministic methods such as queue-based [9], [22], foreground [24], [28], and skip-and-fill calibration [20], [29], which either interrupt the regular conversion cycle or sacrifice conversion speed.

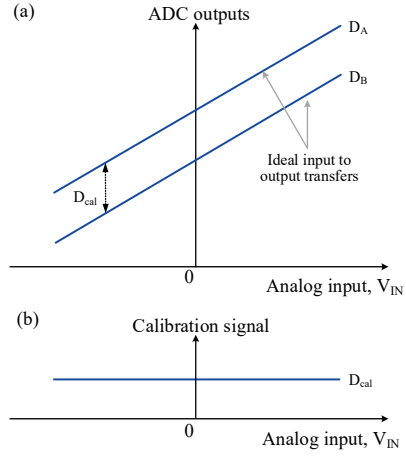

Figure 2.9: (a) Ideal ADC transfers and (b) calibration signal.

The concept of a pipelined split-ADC is shown in Figure 2.8 [18]. The entire ADC is split into two ADCs (Figure 2.8(a)) with digital outputs D_A and D_B. The overall ADC output (D_{out}), shown in Figure 2.8(b), is formed by averaging D_A and D_B as follows:

$$D_{\text{out}} = \frac{D_A + D_B}{2} \tag{2.18}$$

Since every circuit block is split in half, the power in each half-circuit is 2× lower, but the combined power and noise stays the same.

To simplify our discussion, each ADC is assumed to have a 1.5-bit first stage and an ideal backend stage. To enable error detection, an input offset voltage V_{OS} is applied between the two ADC channels, in their respective coarse-ADCs and sub-DACs. This offset voltage forces the two ADCs to follow different trajectories so that they exhibit non-identical errors for the same input signal. The difference between the two ADC outputs contains the error information of the ADCs and hence can be used for calibration. The difference (or calibration) signal D_{cal} (see Figure 2.8(c)) is given as follows:

$$D_{\text{cal}} = D_A - D_B \tag{2.19}$$

Ideally, this difference signal D_{cal} yields the digital representation of the offset voltage V_{OS} and should be constant without any signal content (Figure 2.8(c)). Since signal averaging is

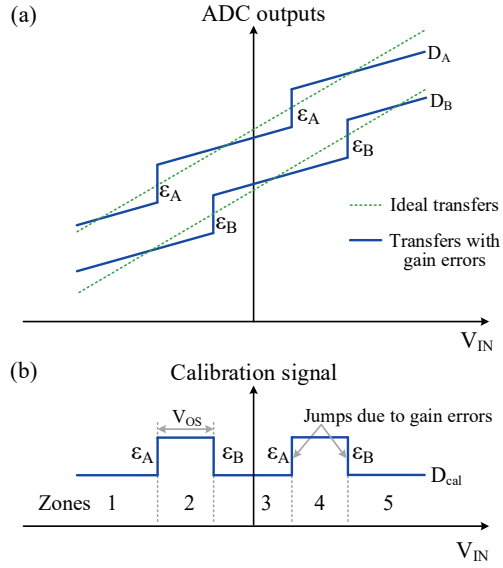

Figure 2.10: (a) ADC transfers and (b) calibration signal when the residue amplifier has gain error.

not required in principle to extract the errors (unlike stochastic methods [23]), calibration can converge faster.

2.4.1.1 Gain Error Detection

Figure 2.9(a) illustrates the input-output transfer of the split-ADC when no error are present. Since the two ADCs have straight lines as transfer curves, the resultant calibration signal D_{cal} is a flat line, as shown in Figure 2.9(b). If the stage-1 ResAmp has a gain error, the ADC transfer deviates from these ideal lines and exhibits discontinuities or jumps in the transfer curve, as shown in Figure 2.10(a). These jumps occur when the stage-1 input moves from one sub-range to the next. By applying an input offset V_{OS}, these subrange transitions of the two ADCs are shifted from one another. As a result, when one ADC exhibits a jump due to a gain error, the other ADC experiences no jump and can therefore be used as a reference to detect this error.

Figure 2.10(b) shows the resulted calibration signal when the ResAmp has gain errors. It also exhibits jumps similar to the transfer curve, thus deviating from a flat horizontal line. These jumps due to gain errors are represented by ε_A and ε_B in Figure 2.10. To detect the magnitude of ε_A and ε_B, the calibration signal can be divided into five zones based on the

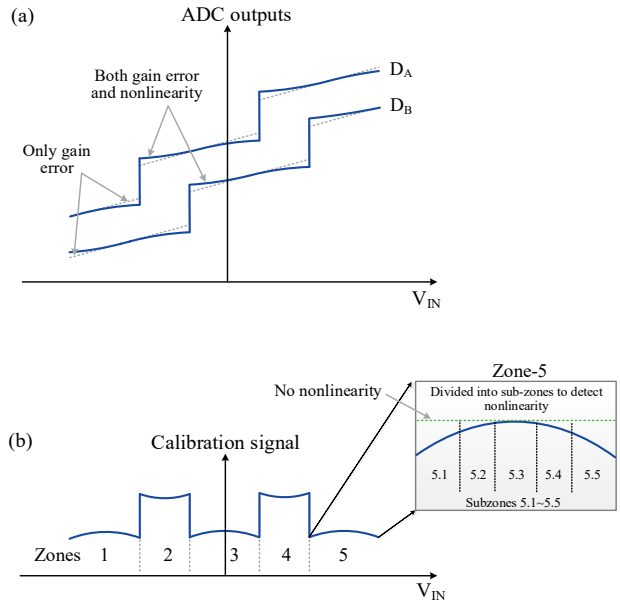

Figure 2.11: Use of the split-ADC calibration technique to detect the third-order nonlinearity of the residue amplifier.

outputs of stage-1 coarse-ADC. The data samples accumulated in each of these zones are averaged to reduce the effect of thermal noise so that a better estimation of the D_{cal} value can be obtained. The average D_{cal} values of these five zones can be used to calculate ε_A and ε_B as follows:

$$\varepsilon_A = (D_{\text{cal-2}} - D_{\text{cal-1}}), \quad \text{or, } \varepsilon_A = (D_{\text{cal-4}} - D_{\text{cal-3}}) \tag{2.20}$$

$$\varepsilon_B = (D_{\text{cal-3}} - D_{\text{cal-2}}), \quad \text{or, } \varepsilon_B = (D_{\text{cal-5}} - D_{\text{cal-4}}) \tag{2.21}$$

Note that $D_{\text{cal-i}}$ is the average digital value of zone-i, where i can be 1, 2, 3, 4, or 5.

2.4.1.2 Nonlinearity Detection

The split-ADC technique can also be used to detect the nonlinearity of the residue amplifier [18]. To simplify the discussion, only the detection of the third-order distortion component is considered, as this is usually the dominant nonlinearity. Figure 2.11(a) shows

the ADC's input-output transfer curve when its ResAmp exhibits both gain error and nonlinearity. Like gain errors, errors due to nonlinearity manifest themselves as a jump at the sub-range transitions. However, they also cause individual subranges to deviate from a straight line. Since the subranges of both split-ADCs exhibit third-order distortion, subtracting them results in a second-order term, as can be seen from the calibration signal D_{cal} in Figure 2.11(b).

As shown earlier for gain error detection, the average values of D_{cal} in consecutive zones are compared. However, for nonlinearity detection, we need to zoom into one of those zones, e.g., zone-5. The MSB bits of the backend stages can be used to divide this zone-5 into multiple sub-zones (e.g., five sub-zones called 5.1 to 5.5). The accumulated data samples in each of these sub-zones are then averaged out to lower the noise. Note that without any distortion, the average D_{cal} values in all these sub-zones would be the same (i.e. a flat line as shown in Figure 2.11(b)). Thus, by comparing the D_{cal} values in these sub-zones, the third-order nonlinearity coefficient of the residue amplifier can be estimated.

2.4.2 Error Correction

Once the errors are detected in the digital domain, they need to be corrected to recover the performance of the ADC. Error correction can be performed either in the digital or in the analog domain. Both approaches are discussed in the following sections, assuming the residue amplifiers only exhibit gain errors.

2.4.2.1 Digital Correction

Digital error correction [18], [20]–[23] compensates for analog inaccuracies by post-processing the ADC output in the digital domain. This process can be better understood by giving an example. Suppose the ADC encoder expects the ResAmp gain to be G_D. However, due to gain error, the ResAmp exhibits a lower gain G_A. This will create jumps in the ADC transfer, as discussed in Section 2.4.1.1. Digital error correction can eliminate this jump by adjusting the bit weight or digital gain (G_D) of the encoder, as shown in Figure 2.12(a). Although the ADC subranges are realigned due to this, the slope of the input-output transfer remains unchanged. It can be inferred that digital error correction cannot recover the noise degradation because of reduced analog gain. It also cannot recover the ADC resolution (or range) that is lost due to gain error (Figure 2.12(a)). Moreover, as mentioned earlier, unlike digital error *detection* that can be performed at a sub-sampling rate ($<< F_S$), digital error

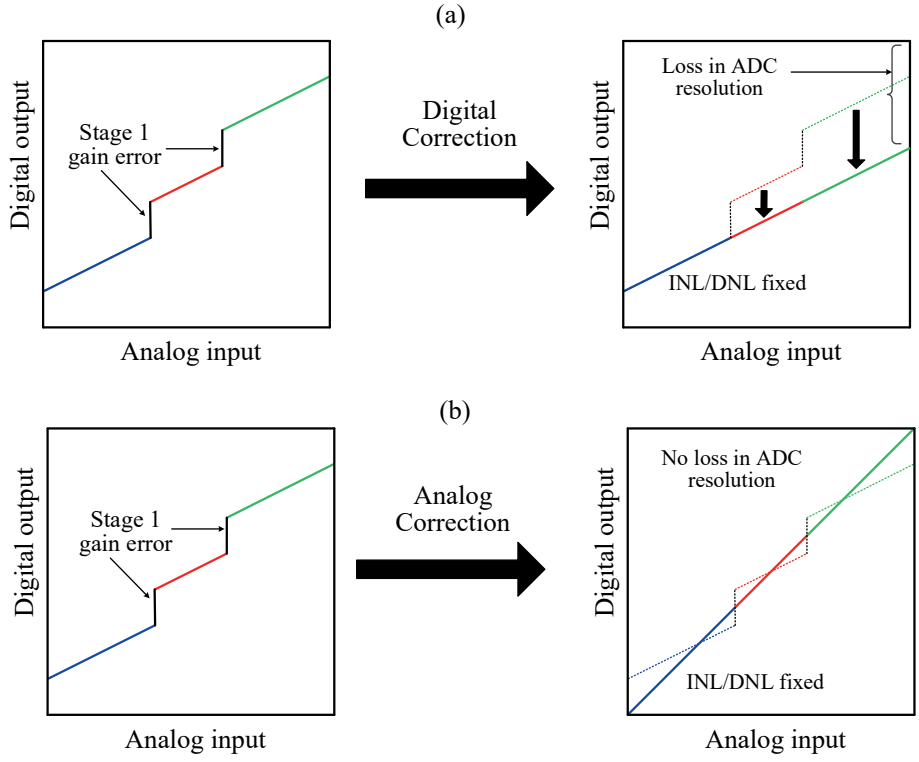

Figure 2.12: Comparison of (a) digital and (b) analog gain-correction. The solid and dashed lines represent before and after the correction, respectively.

correction must operate at the full clock rate F_S of the ADC. Consequently, it usually consumes considerable power [22], [23].

2.4.2.2 Analog Correction

Analog error correction [27], [30] is fundamentally different from digital error correction because the errors are mitigated at the source. Figure 2.12(b) shows the analog gain-error correction approach. For the above example, instead of modifying the digital encoder gain G_D, the actual ResAmp gain G_A is adjusted to ensure $G_D = G_A$. This not only realigns the ADC subranges but also eliminates the slope-error from the ADC transfer. As a result, both the resolution and the noise performance of the ADC are restored. Therefore, this work utilizes analog error *correction* in combination with digital error *detection* to calibrate ResAmp inaccuracies.

2.5 Summary

This chapter discusses the design of power-efficient residue amplifiers. First, their power efficiency is discussed as a function of various circuit parameters. Next, the effect of incomplete settling on the amplifier's gain, noise, and power dissipation is analyzed. It is concluded from this analysis that the amplifier becomes more power-efficient with reduced settling; however, its gain becomes susceptive to PVT variations. The last part of this chapter is, therefore, focused on calibration. The split-ADC calibration technique is discussed, along with how it can be used to detect amplifier errors. Finally, different error correction approaches are explained.

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3

Linearization Techniques

Residue amplifiers (ResAmps) typically employ closed-loop configurations [1]–[6] to reduce distortion. However, digital calibration techniques have made it possible to employ more efficient amplifier topologies that are not necessarily linear. For instance, open-loop amplifiers [7]–[11] exhibit high power efficiency but poor linearity. As shown in Chapter 2, however, their nonlinearity can be digitally detected [7], [10], [12]–[16] and then corrected by analog techniques.

This chapter discusses the use of analog linearization techniques for amplifiers. The objective is to review and propose techniques that improve the inherent linearity of amplifiers with minimal power overhead. Section 3.2 discusses linearization methods based on the strong-inversion operating region of MOSFETs. Subsequently, linearization techniques in the weak-inversion region are presented in Sections 3.3–3.5. Finally, Section 3.6 describes various design aspects related to these linearization methods.

3.1 Introduction

The transconductance of an amplifier $g_{m,\text{eff}}$ is a function of its voltage-to-current (V–I) characteristic. It is constant for a linear amplifier. Since ResAmps usually drive a passive load (i.e. signal-independent), linearizing this $g_{m,\text{eff}}$ often ensures a linear gain, ignoring output modulation effects like channel-length shortening, drain-induced barrier lowering (DIBL), or static feedback. Hence, the following sections discuss techniques to linearize $g_{m,\text{eff}}$.

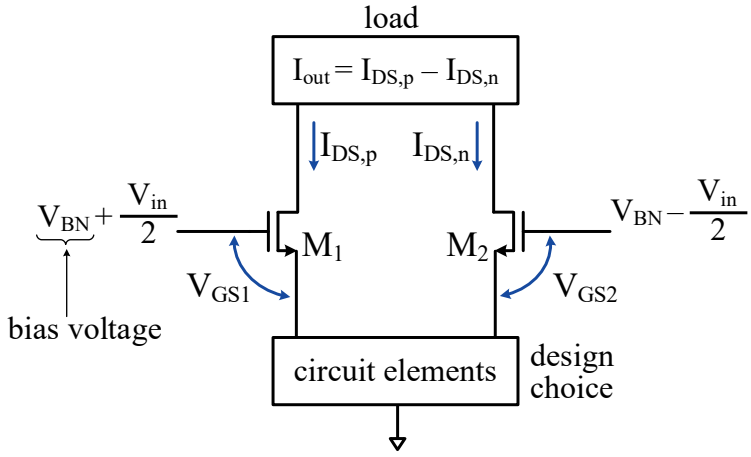


Figure 3.1: Conceptual diagram of an NMOS input pair with its basic circuit construction.

Figure 3.1 depicts a conceptual diagram of an NMOS differential pair. V_{in} and V_{BN} are the input and bias voltages, respectively. The drain-to-source currents flowing through the input transistors M_1 and M_2 are represented by $I_{DS,p}$ and $I_{DS,n}$. The differential output current I_{out} is defined as the difference between these two currents as follows:

$$I_{out} = I_{DS,p} - I_{DS,n}. \tag{3.1}$$

To linearize the amplifier, I_{out} must be proportional to V_{in} so that $g_{m,eff}$ is constant and signal independent. This can be accomplished in various ways depending on how the circuit at the source-side of the NMOS input pair is implemented, as will be discussed in the following sections.

3.2 Linearization in the Strong-Inversion Region

The strong-inversion region in MOSFETs is traditionally the most widely used operating region for designing amplifiers. Transistors in the strong-inversion region offer better speed than those in the weak-inversion region because they can be sized smaller with less parasitic capacitance. In this region, I_{DS} current varies quadratically with the gate-source voltage V_{GS}. It can be expressed as follows [17], [18] :

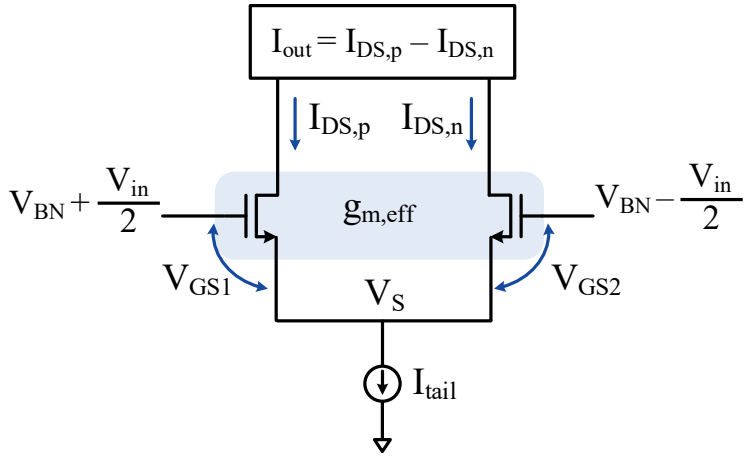


Figure 3.2: Simplified circuit topology of a differential pair with a fixed tail current source.

$$I_{DS} = \frac{\beta_n}{2}(V_{GS} - V_{th})^2, \tag{3.2}$$

where $\beta_n = \mu_n C_{ox}(W/L)$, and V_{th} is the threshold voltage of the transistor.

To analyze the nonlinearity, let us first consider a conventional differential pair with a fixed tail current source, as shown in Figure 3.2. By using Equation (3.2) in (3.1), I_{out} can be found as follows:

$$I_{out} = \frac{\beta_n}{2}[(V_{GS1} - V_{th})^2 - (V_{GS2} - V_{th})^2]. \tag{3.3}$$

Here, $(V_{GS1} - V_{th}) = V_{GT1}$ = the overdrive voltage of the input transistor M1, and $(V_{GS2} - V_{th}) = V_{GT2}$ = the overdrive voltage of M2. Thus, the expression in (3.3) can be rearranged as follows [18]–[20]:

$$\begin{aligned} I_{out} &= \frac{\beta_n}{2}[V_{GT1}^2 - V_{GT2}^2] \\ &= \frac{\beta_n}{2}(V_{GT1} + V_{GT2})(V_{GT1} - V_{GT2}) \\ &= \frac{\beta_n}{2}(V_{GT1} + V_{GT2})V_{in}\,. \end{aligned} \tag{3.4}$$

Note that ($V_{GT1} - V_{GT2}$) = V_{in} because the source nodes of the input devices are tied together. It can be deduced from Equation (3.4) that the output current I_{out} will only have a linear dependence on the input voltage V_{in} if the sum of the overdrive voltages ($V_{GT1} + V_{GT2}$) is constant [18]–[20].

For the circuit of Figure 3.2, an expression for the sum ($V_{GT1} + V_{GT2}$) can be derived as follows [18]:

$$\begin{aligned} & I_{tail} = I_{DS,p} + I_{DS,n} \\ \Rightarrow\ & I_{tail} = \frac{\beta_n}{2}\left[{V_{GT1}}^2 + {V_{GT2}}^2\right] \\ \Rightarrow\ & I_{tail} = \frac{\beta_n}{2}\left[\frac{(V_{GT1}+V_{GT2})^2}{2} + \frac{(V_{GT1}-V_{GT2})^2}{2}\right] \\ \Rightarrow\ & (V_{GT1}+V_{GT2}) = \sqrt{\frac{4I_{tail}}{\beta_n} - V_{in}^2} \end{aligned} \tag{3.5}$$

Substituting the expression for ($V_{GT1} + V_{GT2}$) from (3.5) into (3.4) results in the following differential output current [17]:

$$I_{out} = \frac{1}{2}\beta_n V_{in}\sqrt{\frac{4I_{tail}}{\beta_n} - V_{in}^2} \tag{3.6}$$

Figure 3.3(a) shows the sum ($V_{GT1} + V_{GT2}$) as a function of the input voltage V_{in}. Since the tail current I_{tail} is constant (Figure 3.2), the sum of overdrive voltages ($V_{GT1} + V_{GT2}$) varies nonlinearly with the input voltage V_{in}, according to (3.5). Consequently, the output current I_{out} given by (3.6) is also nonlinear with the input V_{in}, as shown in Figure 3.3(b). Note that the maximum signal current I_{out} in this circuit is limited by the fixed tail current I_{tail}. A maximum input signal $V_{in,max}$ can then be defined for the situation when I_{out} is equal to I_{tail} (further detail in [17]). If an input voltage larger than $V_{in,max}$ is applied, the output current will not change because it is limited to I_{tail}. Consequently, the effective transconductance $g_{m,eff}$ decreases, exhibiting a strong compressing nonlinearity.

Various circuit techniques [18]–[22] can be applied in the strong-inversion saturation region to ensure that the sum of the overdrive voltages ($V_{GT1} + V_{GT2}$) is a constant. For instance, the common-source node V_S of the differential pair can be connected to ground [18], [22] instead of to a tail current source, as shown in Figure 3.4. Since the source node

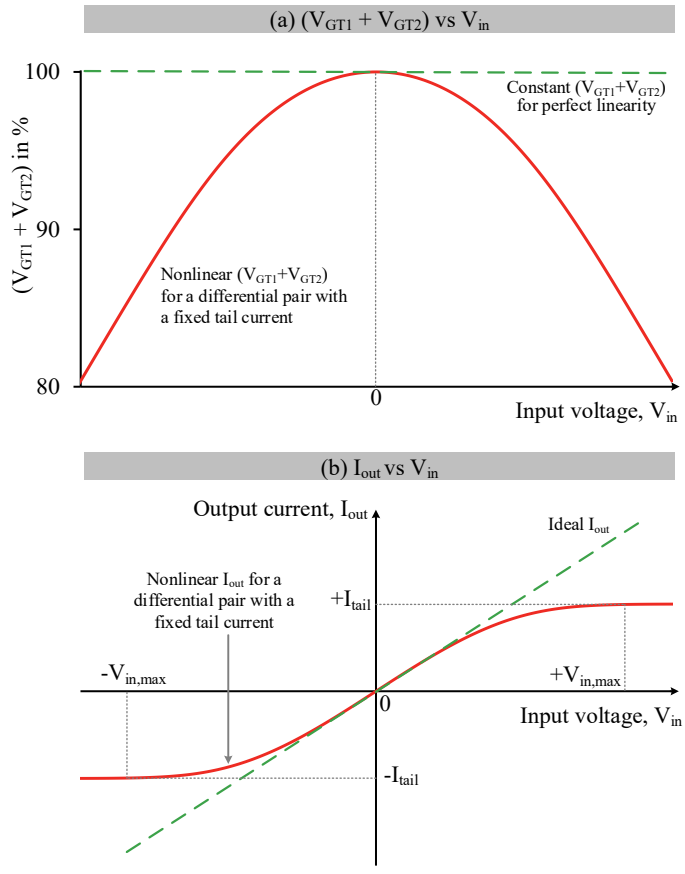


Figure 3.3: Simulated (a) overdrive voltage sum (V_{GT1}+V_{GT2}) and (b) differential output current I_{out} as a function of the input voltage V_{in}.

is grounded (V_S = 0), the sum of the overdrive voltages can be expressed as follows when the inputs are driven differentially:

$$\begin{aligned}(V_{GT1} + V_{GT2}) &= \left(V_{BN} + \frac{V_{in}}{2} - V_{th}\right) + \left(V_{BN} - \frac{V_{in}}{2} - V_{th}\right) \\ &= 2\,(V_{BN} - V_{th}) \end{aligned} \tag{3.7}$$

Expression (3.7) shows that the sum (V_{GT1} + V_{GT2}) is constant because both the bias and threshold voltages are signal-independent. Hence, the differential output current I_{out} in (3.4) is a linear function of the input signal V_{in} as follows:

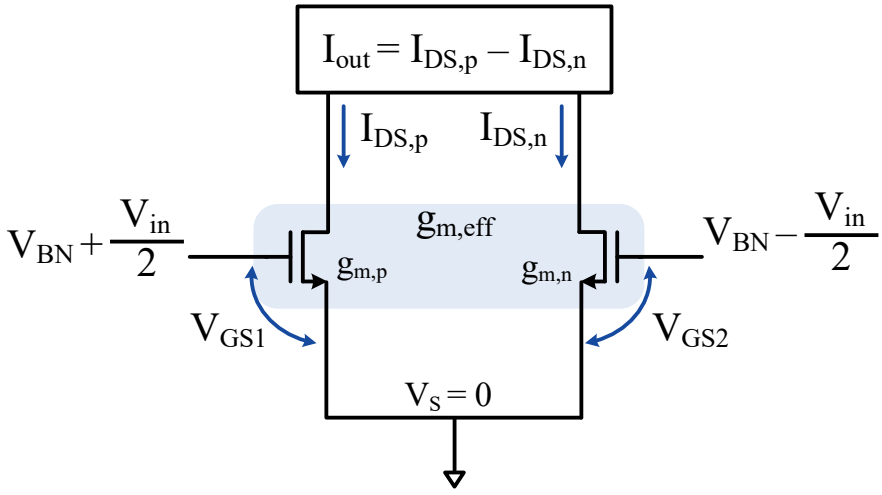


Figure 3.4: Simplified circuit topology of a differential pair with grounded source nodes.

$$I_{out} = \beta_n (V_{BN} - V_{th}) V_{in} \tag{3.8}$$

Consequently, the effective transconductance $g_{m,eff}$ becomes a constant as shown below:

$$g_{m,eff} = \frac{dI_{out}}{dV_{in}} = \beta_n (V_{BN} - V_{th}) \tag{3.9}$$

However, in reality, even when operated in the strong-inversion saturation region, real MOSFETs do not have perfectly quadratic characteristics due to non-idealities such as velocity saturation and mobility reduction [18]–[20]. Hence, equation (3.8) ultimately does not hold, causing the output current I_{out} to vary nonlinearly with the input signal V_{in}. The resulting transconductance $g_{m,eff}$ is nonlinear, exhibiting a compressing characteristic.

Although both the differential pairs in Figure 3.2 and Figure 3.4 exhibit compression, the grounded source pair demonstrates significantly better linearity than when a fixed tail current is used. Moreover, it supports a larger output current I_{out} because there is no fixed tail current to limit the maximum I_{out}. Figure 3.5 and Figure 3.6 show the differential output currents and transconductances of both circuits as a function of the input V_{in}, respectively. An equal bias current is considered for both amplifiers. The output current I_{out} of the grounded source pair deviates less from the ideal current compared to the differential pair

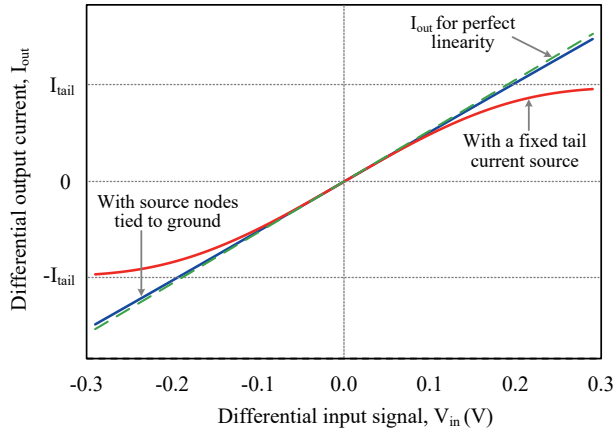


Figure 3.5: Simulated output currents of the differential pairs as a function of the input voltage.

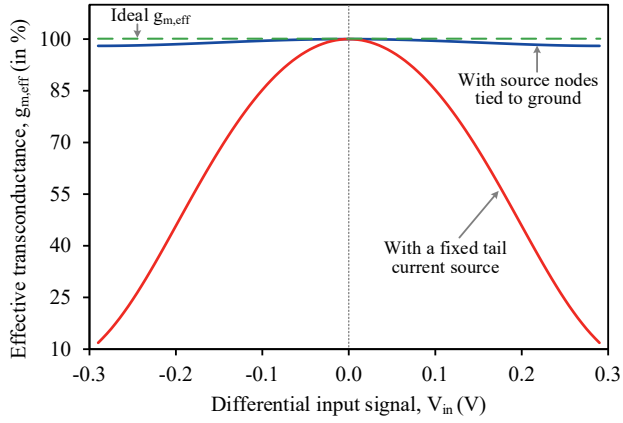


Figure 3.6: Simulated transconductances of the differential pairs as a function of the input voltage.

with a fixed tail current. Therefore, its transconductance $g_{m,\text{eff}}$ varies significantly less with V_{in}, exhibiting high linearity [18]. Hence, this technique is utilized in the ResAmp presented in Chapter 4.

An alternative method of linearizing a differential pair in strong-inversion is to build a signal-dependent tail current [18] instead of using a fixed current source. This tail current needs to be expanding with the input signal to compensate the amplifier's compressing nonlinearity. From (3.5) and (3.6) it can be seen that the tail-current need to expand quadratically with the input signal, like:

$$I_{\text{tail}} = I_{\text{tail-constant}} + \frac{\beta_n}{4} V_{\text{in}}{}^2 \ . \tag{3.10}$$

Equation (3.10) shows that the tail current I_{tail} requires a fixed part $I_{\text{tail-constant}}$ and a signal-dependent part. The implementation of such a current source can be found in [18], [20], [21].

Let us introduce a parameter α to the signal-dependent part as follows which can be useful to observe how the amplifier's nonlinearity profile changes with the signal-dependent portion of I_{tail}:

$$I_{\text{tail}} = I_{\text{tail-constant}} + \alpha \frac{\beta_n}{4} V_{\text{in}}{}^2 \tag{3.11}$$

Substituting the I_{tail} expression of (3.11) in (3.5) gives the following result for ($V_{\text{GT1}} + V_{\text{GT2}}$):

$$\begin{aligned} (V_{\text{GT1}} + V_{\text{GT2}}) &= \sqrt{\frac{4}{\beta_n}\left(I_{\text{tail-constant}} + \alpha \frac{\beta_n}{4} V_{\text{in}}{}^2\right) - V_{\text{in}}^2} \\ &= \sqrt{\frac{4}{\beta_n} I_{\text{tail-constant}} - (1-\alpha) V_{\text{in}}{}^2}. \end{aligned} \tag{3.12}$$

If $\alpha = 0$, then the tail current is constant, similar to a conventional differential pair shown in Figure 3.2. Hence, the amplifier exhibits a compressing nonlinearity. Note that the sign before the input term is negative in this case. As the parameter α increases, the value of $(1 - \alpha)$ decreases, reducing the compression. At $\alpha = 1$, the signal-dependent part in (3.12) is zero, which results in a constant ($V_{\text{GT1}} + V_{\text{GT2}}$). As a result, the amplifier exhibits perfect linearity. If α becomes higher than one, then the sign of the coefficient $(1-\alpha)$ flips and the amplifier starts to exhibit an expanding nonlinearity. Thus, by adjusting the parameter α, the nonlinear characteristics of the amplifier can be tuned so that high linearity is obtained.

3.3 Linearization in the Weak-Inversion Region

Consider the same circuit of Figure 3.4; however, the transistors are now biased in the weak-inversion saturation region. As shown in [23], the drain-source current I_{DS} of a

MOSFET in weak-inversion can be expressed as follows, assuming its body is tied to ground:

$$I_{\mathrm{DS}} \cong I_{D0}\, exp\left(\frac{V_G}{nU_T}\right) exp\left(\frac{-V_S}{U_T}\right)\left(1 - exp\left(\frac{-V_{\mathrm{DS}}}{U_T}\right)\right), \tag{3.13}$$

where V_G = gate voltage, V_S = source voltage, V_{DS} = drain-source voltage, I_{D0} is a process-dependent parameter, n is the weak-inversion slope factor (~1.4), and U_T is the thermal voltage (kT/q). By assuming that the drain-source voltage $V_{\mathrm{DS}} > 4U_T$ (arbitrary choice), the term $exp\left(\frac{-V_{\mathrm{DS}}}{U_T}\right)$ becomes almost zero, and the above equation can be simplified as follows:

$$I_{\mathrm{DS}} \cong I_{D0}\, exp\left(\frac{V_G}{nU_T}\right) exp\left(\frac{-V_S}{U_T}\right), \tag{3.14}$$

Substituting $V_{\mathrm{S}} = 0$ and $V_G = V_{\mathrm{BN}} + 0.5V_{\mathrm{in}}$ in (3.14), for the positive-half circuit of Figure 3.4, results in the following drain-source current:

$$\begin{aligned} I_{\mathrm{DS,p}} &= I_{D0}\, exp\left(\frac{V_{\mathrm{BN}} + \frac{V_{\mathrm{in}}}{2}}{nU_T}\right) \\ &= I_B\, exp\left(\frac{V_{\mathrm{in}}/2}{nU_T}\right) \end{aligned} \tag{3.15}$$

where $I_B = I_{D0}\, exp\left(\frac{V_{\mathrm{BN}}}{nU_T}\right)$ = the amplifier's bias current.

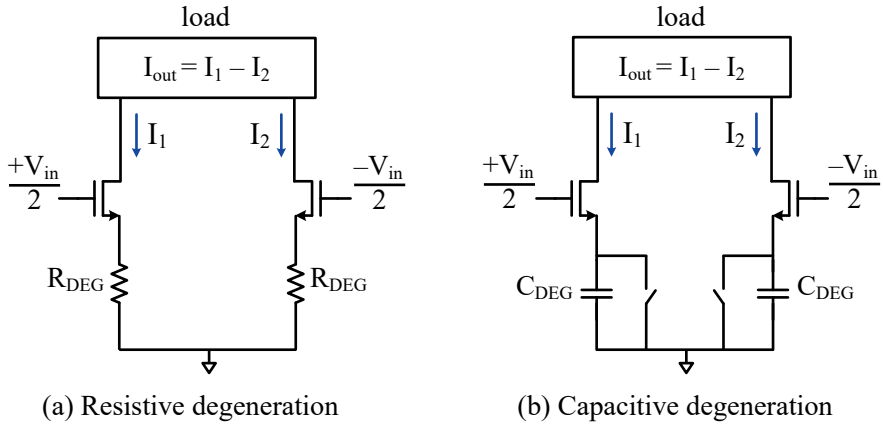
Since the drain current varies exponentially with the input, the transconductance $g_{m,\mathrm{p}}$ is also exponential, as can be seen from the following expressions:

$$g_{m,\mathrm{p}} = \frac{dI_{\mathrm{DS,p}}}{d(V_{\mathrm{in}}/2)}$$

$$= \frac{I_B}{nU_T}\, exp\left(\frac{V_{\mathrm{in}}/2}{nU_T}\right) \tag{3.16}$$

$$= \frac{I_{\mathrm{DS,p}}}{nU_T} \tag{3.17}$$

Similarly, for the negative half-circuit of the amplifier in Figure 3.4, the transconductance $g_{m,\mathrm{n}}$ can be written as follows:



(a) Resistive degeneration (b) Capacitive degeneration

Figure 3.7: Basic amplifier configurations for the presented linearization technique in the weak-inversion region, using (a) resistive and (b) capacitive degeneration.

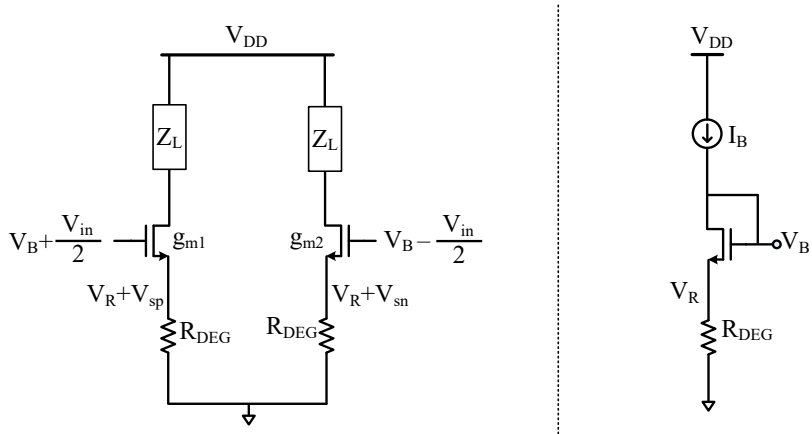
$$g_{m,\mathrm{n}} = \frac{I_B}{nU_T}\, exp\left(\frac{-V_{\mathrm{in}}/2}{nU_T}\right), \tag{3.18}$$

The amplifier's effective transconductance $g_{m,\mathrm{eff}}$ can be obtained by averaging $g_{m,\mathrm{p}}$ and $g_{m,\mathrm{n}}$ as follows:

$$g_{m,\mathrm{eff}} = \frac{g_{m,\mathrm{p}} + g_{m,\mathrm{n}}}{2} \tag{3.19}$$

Since the increase in $g_{m,\mathrm{p}}$ is stronger than the decrease in $g_{m,\mathrm{n}}$ with input signal V_{in}, the amplifier exhibits an expanding nonlinearity. To linearize the amplifier, we need to weaken this expanding g_m. This can be achieved by incorporating circuitry that compresses the g_m. It should be noted that this strategy is similar to that used in strong-inversion, where *additional expanding* circuitry is added to linearize the *compressing* g_m.

The following sections describe techniques to linearize the g_m of weak-inversion MOSFETs. These techniques use a weak-degree of degeneration to reduce and eventually linearize the expanding g_m of the transistor. This degeneration can be achieved either with resistors R_{DEG} (Figure 3.7(a)) or with switched-capacitors C_{DEG} (Figure 3.7(b)). In the next section, the linearization technique with resistive degeneration is discussed. The capacitive degeneration technique will be discussed in Section 3.5. Note that although the presented techniques are discussed for weak-inversion MOSFETs, they can also be applied to bipolar junction transistors.



(a) Resistively degenerated amplifier (b) Bias circuit

Figure 3.8: (a) Resistively degenerated amplifier with its (b) bias circuit.

3.4 Resistively Degenerated Linearization (RDL) Technique

This section explains the resistively degenerated linearization (RDL) technique, both intuitively and with mathematical analysis. The presented technique is based on [24]. Further details regarding the RDL technique and a prototype circuit implementation can be found in Chapter 5.

3.4.1 Intuitive Analysis

Figure 3.8(a) depicts a differential amplifier with two degeneration resistors R_{DEG} and output loads Z_L. The amplifier's bias circuit is shown in Figure 3.8(b), where I_B denotes the bias current. The transconductances of the amplifier's positive and negative half-circuit can be expressed as follows:

$$g_{m,\mathrm{p}} = \frac{g_{m1}}{1 + g_{m1} R_{\mathrm{DEG}}} \tag{3.20}$$

$$g_{m,\mathrm{n}} = \frac{g_{m2}}{1 + g_{m2} R_{\mathrm{DEG}}} \tag{3.21}$$

where g_{m1} and g_{m2} represent the transconductance of the input transistors.

The overall transconductance $g_{m,\mathrm{eff}}$ can be obtained by using (3.19). This $g_{m,\mathrm{eff}}$ varies nonlinearly with the input signal V_{in}. However, the characteristic of this nonlinearity,

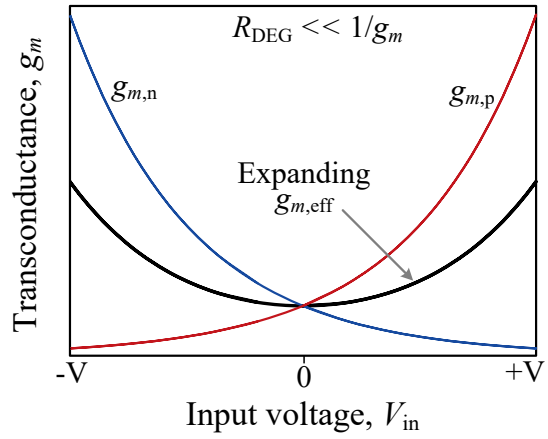


Figure 3.9: Transconductance of a resistively degenerated amplifier for $R_{DEG} << 1/g_m$.

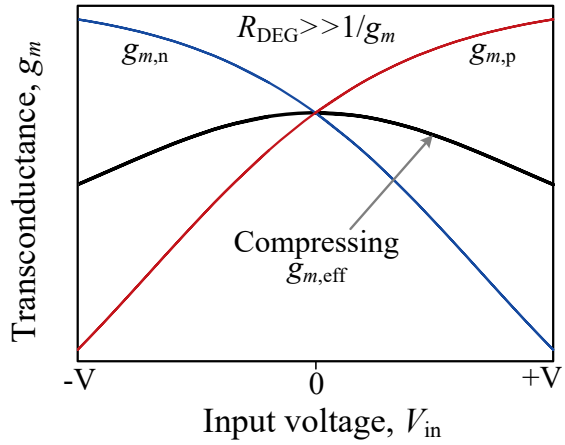


Figure 3.10: Transconductance of a resistively degenerated amplifier for $R_{DEG} >> 1/g_m$.

whether it is expanding or compressing, depends on the degree of degeneration ($1+g_mR_{DEG}$). This can be seen by considering two extreme circuit conditions and then analyzing how $g_{m,eff}$ varies with V_{in} in each case:

(i) when the degeneration resistance R_{DEG} is zero or small ($R_{DEG} << 1/g_m$).

(ii) when the degeneration resistance R_{DEG} is large ($R_{DEG} >> 1/g_m$).

In the first case, the R_{DEG} resistor is much smaller than the transistor's $1/g_m$, making the degeneration factor ($1+g_mR_{DEG}$) ≈ 1. Hence, the transistors are not degenerated, similar to

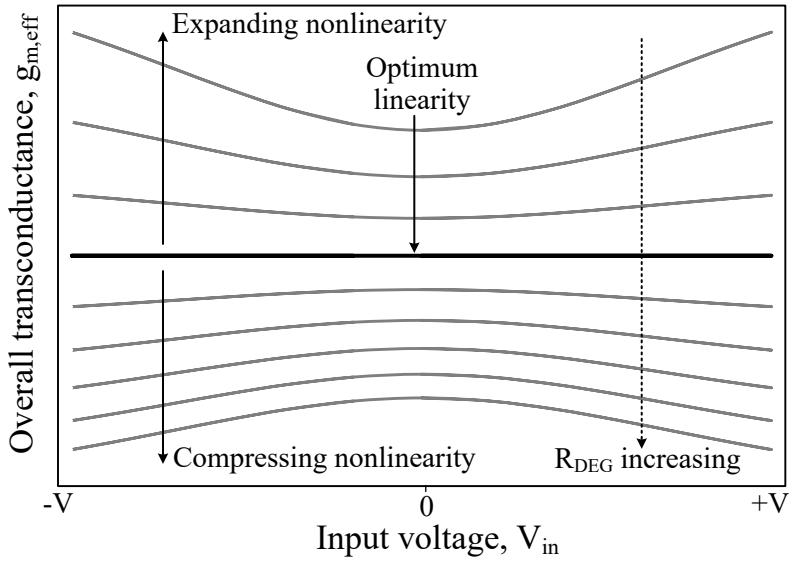


Figure 3.11: Transition from an expanding to a compressing nonlinearity as the degeneration resistance R_{DEG} increases.

the circuit of Figure 3.4. Consequently, the transconductances $g_{m,p}$ and $g_{m,n}$ vary exponentially with the input signal, causing an expanding $g_{m,eff}$ as discussed in Section 3.3. This is illustrated in Figure 3.9.

Now consider the second case in which a large degeneration resistor is used ($R_{DEG} >> 1/g_m$). Due to the large internal loop gain or degeneration factor ($1+g_m R_{DEG}$), the transistor's exponential *V–I* characteristic is strongly reduced, limiting the maximum transconductance. Hence, as the input voltage V_{in} increases, the transconductance $g_{m,p}$ does not grow much (Figure 3.10) and will eventually be limited to $1/R_{DEG}$. However, $g_{m,n}$ drops continuously according to (3.21) because the transconductance g_{m2} of the MOSFET decreases. Since $g_{m,n}$ decreases more than the corresponding increase in $g_{m,p}$, the overall transconductance $g_{m,eff}$ decreases as the input signal increases. Therefore, the nonlinear characteristic of the amplifier becomes compressing, as can be seen from Figure 3.10.

It can be concluded from the above discussion that the amplifier's nonlinearity can be modified from an expanding to a compressing characteristic by adjusting its degree of degeneration. Figure 3.11 illustrates this change in amplifier nonlinearity as the degeneration resistor R_{DEG} is gradually increased from zero. Since the degeneration

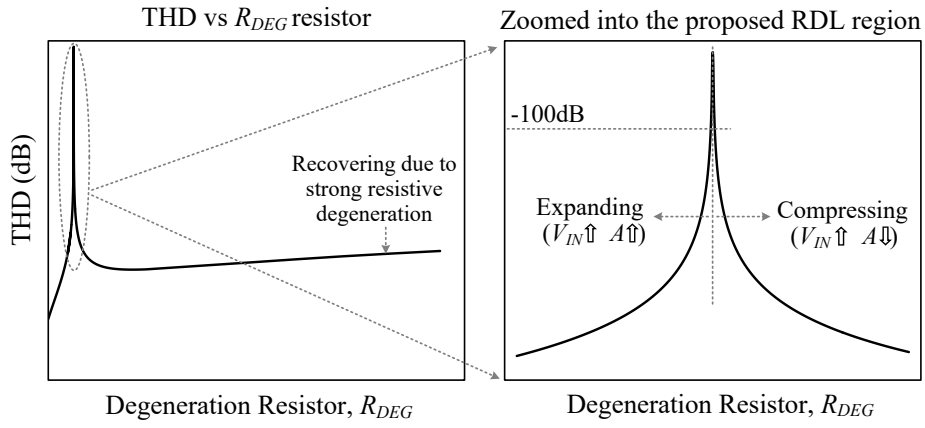


Figure 3.12: THD as a function of the degeneration resistor R_{DEG}.

increases with higher R_{DEG}, the overall transconductance $g_{m,\mathrm{eff}}$ becomes less and less expanding, eventually becoming compressing. During this transition from an expanding to a compressing nonlinearity, the amplifier's $g_{m,\mathrm{eff}}$ or gain becomes almost independent of the input signal. Hence, it exhibits optimum linearity.

Figure 3.12 shows the amplifier's total harmonic distortion (THD) as a function of the degeneration resistance R_{DEG}. Note that traditional degeneration methods [25]–[26] use a relatively large R_{DEG} resistance, which improves the linearity at the cost of reduced transconductance $g_{m,\mathrm{eff}}$. However, the proposed linearization technique uses a much smaller degeneration resistance R_{DEG} to optimize the linearity. Since the resulting degeneration factor $(1+g_mR_{DEG})$ is relatively small, the proposed method [24] is significantly more power-efficient than a traditional degeneration method.

3.4.2 Mathematical Analysis

In this section, the required degeneration to achieve the optimal linearity is calculated. Consider the resistively degenerated amplifier in Figure 3.8(a). For its positive-half circuit, $V_G = V_B + 0.5V_{\mathrm{in}}$ and $V_S = V_R + V_{\mathrm{sp}}$, where V_B and V_R are the bias voltages at the gate and source terminals, respectively. Substituting these values in (3.14) results in the following I_{DS} expression:

$$I_{\mathrm{DS}} = I_{D0}\, exp\left(\frac{V_B + 0.5V_{\mathrm{in}}}{nU_T}\right) exp\left(-\frac{V_R + V_{\mathrm{sp}}}{U_T}\right) \tag{3.22}$$

The bias voltage V_R and the bias current I_B (Figure 3.8(b)) can be expressed as follows:

$$V_R = I_B\, R_{\mathrm{DEG}} \tag{3.23}$$

$$I_B = I_{D0}\, exp\left(\frac{V_B}{nU_T}\right) exp\left(-\frac{V_R}{U_T}\right) \tag{3.24}$$

Using the bias current expression of (3.24) in (3.22) results in the following:

$$I_{\mathrm{DS}} = I_B\, exp\left(\frac{V_{\mathrm{in}}}{2nU_T}\right) exp\left(-\frac{V_{\mathrm{sp}}}{U_T}\right) \tag{3.25}$$

Since the drain-source current I_{DS} flows through the degeneration resistance R_{DEG}, the following equation can be written:

$$I_B\, exp\left(\frac{V_{\mathrm{in}}}{2nU_T}\right) exp\left(-\frac{V_{\mathrm{sp}}}{U_T}\right) = I_B + \frac{V_{\mathrm{sp}}}{R_{\mathrm{DEG}}}$$

$$\text{or,}\quad V_{\mathrm{sp}} = V_R\left[exp\left(\frac{V_{\mathrm{in}}}{2nU_T}\right) exp\left(-\frac{V_s}{U_T}\right) - 1\right] \tag{3.26}$$

Due to the iterative dependency between V_{sp} and V_{in}, a numerical expression of V_{sp} in terms of V_{in} cannot be derived. However, it can be expressed in terms of the Lambert W function [27], [28] as follows:

$$V_{\mathrm{sp}} = U_T\ LambertW\left(0,\ \left(\frac{V_R}{U_T}\right) exp\left(\frac{V_R}{U_T}\right) exp\left(\frac{V_{\mathrm{in}}}{2nU_T}\right)\right) - V_R \tag{3.27}$$

The Lambert W function, also known as the omega function, is a set of functions that can be used to solve the inverse relation of the function $z = f(W) = W\, exp(W)$.

Similarly, for the negative-half circuit, the source voltage V_{sn} can be expressed as:

$$V_{\mathrm{sn}} = U_T\ LambertW\left(0,\ \left(\frac{V_R}{U_T}\right) exp\left(\frac{V_R}{U_T}\right) exp\left(\frac{-V_{\mathrm{in}}}{2nU_T}\right)\right) - V_R \tag{3.28}$$

Calculating V_{sp}, V_{sn}, and the resulting amplifier gain (in MATLAB) reveal that the optimal

linearity occurs when $V_R/U_T \approx 1/2$. The same condition is derived in [24] under the assumption that the amplifier generates only up to third-order harmonics. It is also confirmed with transistor-level simulations that the amplifier's third-order harmonic distortion is significantly reduced when $V_R \approx U_T/2$. Hence, the condition for optimal linearity can be written as follows:

$$V_R = I_B R_{\mathrm{DEG}} \approx U_T/2 \tag{3.29}$$

In the quiescent situation (i.e. $V_{\mathrm{in}} = 0$), the transconductance at the optimal linearity condition $g_{m,\mathrm{opt}}$ can be derived by combining (3.16) and (3.29) as follows:

$$g_{m,\mathrm{opt}} = \frac{I_B}{nU_T} exp(0) = \frac{U_T/2R_{\mathrm{DEG}}}{nU_T} = \frac{1}{2nR_{\mathrm{DEG}}} \approx \frac{0.35}{R_{DEG}} \tag{3.30}$$

Equation (3.30) indicates that at the optimum linearity, the degeneration factor $(1+g_m R_{\mathrm{DEG}})$ is approximately 1.35. Thus, the amplifier's effective transconductance is reduced only by 1.35×. For BJTs, this optimal degeneration factor is 1.5 instead of 1.35 (for MOSFET) since their $n = 1$.

Note the above analysis assumes that the NMOS transistor's body is tied to the ground. If it is tied to the source node instead, then the expression of the I_{DS} current will change from (3.25) as follows:

$$I_{\mathrm{DS}} = I_B \, exp\left(\frac{V_{\mathrm{in}}}{2nU_T}\right) exp\left(-\frac{V_{\mathrm{sp}}}{nU_T}\right) \tag{3.31}$$

This will change the optimal V_R and $g_{m,\mathrm{opt}}$ expressions, which can be derived using the same method. The resulting expressions are shown below, in which the weak-inversion slope factor n appears in the V_R expression instead of in the $g_{m,\mathrm{opt}}$ expression:

$$V_R \approx nU_T/2 \tag{3.32}$$

$$g_{m,\mathrm{opt}} \approx \frac{1}{2R_{DEG}} \approx \frac{0.5}{R_{DEG}} \tag{3.33}$$

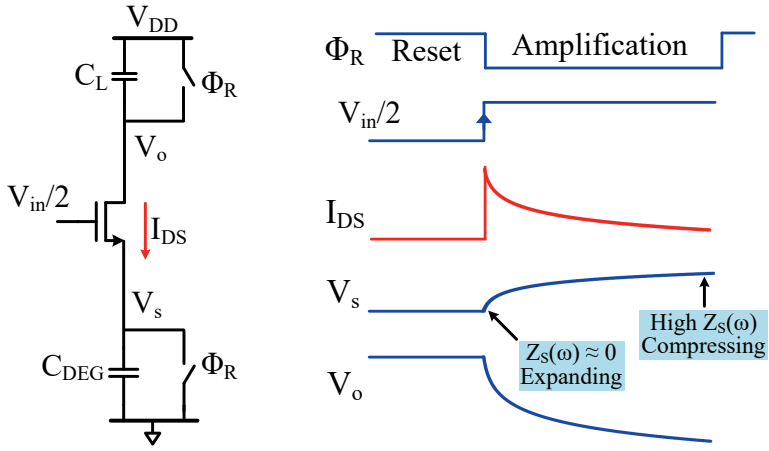


Figure 3.13: Time-domain analysis of a dynamic amplifier half-circuit during capacitive degeneration.

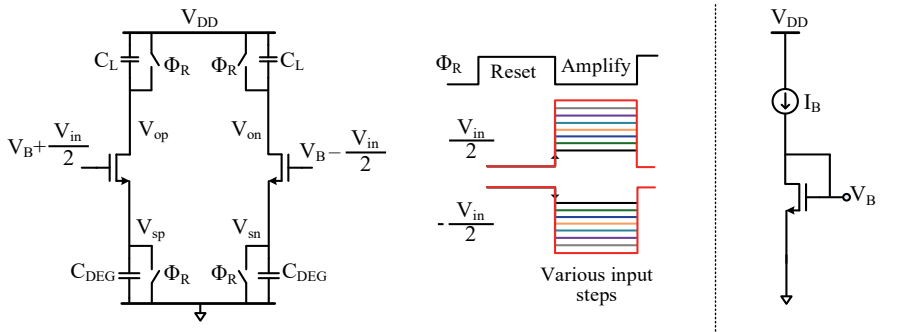
3.5 Capacitively Degenerated Linearization (CDL) Technique

Instead of using a resistor, a switched capacitor can also be used to degenerate an amplifier. However, this is only suitable for discrete-time applications such as in ADCs. This section explains this capacitively degenerated linearization (CDL) technique [29], both intuitively and mathematically. Chapter 6 describes the prototype amplifier implementation that employs this linearization technique.

3.5.1 Intuitive Analysis

Figure 3.13 shows a half-circuit of a dynamic amplifier that is degenerated by a switched capacitor C_{DEG}. A load capacitor C_L is added at the drain, which together with the source capacitor C_{DEG} defines the amplifier's steady-state gain (C_{DEG}/C_L). Since the amount of degeneration due to the C_{DEG} capacitor changes over time, it is more intuitive to analyze this circuit in the time domain.

The circuit operates in two phases: reset and amplification. During reset, C_{DEG} and C_L capacitors are pre-charged to the ground and supply voltages, respectively. At the start of the amplification phase, an input step ($V_{in}/2$) is applied to the half-circuit of the amplifier. As a result, a drain-source current I_{DS} flows through it, charging the capacitors. Since the load capacitor is chosen to be smaller than the degeneration capacitor ($C_L < C_{DEG}$), the drain



(a) Capacitively degenerated amplifier (b) Bias circuit

Figure 3.14: (a) Differential dynamic amplifier using capacitive degeneration and (b) its bias circuit.

voltage V_o changes faster than the source voltage V_s, providing amplification. For high-frequency components associated with the input step, the degeneration capacitor C_{DEG} acts like a low impedance ($Z_S(\omega) \approx 0$). Thus, at t = 0, the degeneration equals zero. The amplifier essentially behaves like a differential pair with grounded source nodes and exhibits expanding nonlinearity due to weak-inversion operation (explained in Section 3.4). However, as the amplification progresses, the impedance $Z_S(\omega)$ of the C_{DEG} capacitor gradually becomes higher. This higher impedance degenerates the amplifier more, eventually causing it to exhibit a compressing nonlinearity similar to a resistive degeneration with a large R_{DEG} (>> $1/g_m$).

Figure 3.14(a) shows a differential implementation of the CDL amplifier. Its bias circuit is shown in Figure 3.14(b). The transient large-signal gain $A(t)$ of this amplifier can be derived by taking a ratio of its differential output voltage to the differential input step V_{in} as follows:

$$A(t) = \frac{V_{op}(t) - V_{on}(t)}{V_{in}} \tag{3.34}$$

Figure 3.15 shows this large-signal gain over time for several values of the input step V_{in}. As can be observed, the transient gain $A(t)$ exhibits signal-dependent settling, indicating nonlinearity. Note that for a perfectly linear circuit, all curves in Figure 3.15 would fall on top of each other.

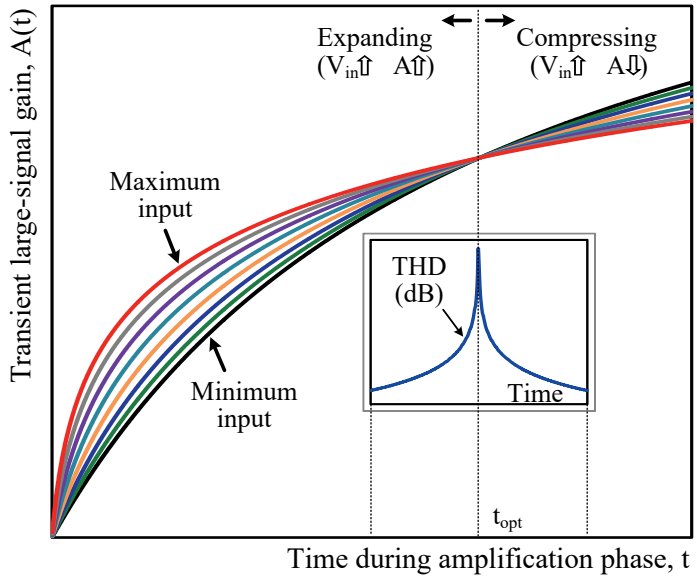


Figure 3.15: Transient large-signal gain versus amplification time for different input steps.

At the start of the amplification phase, the gain is higher for larger input signals V_{in}. Thus, the amplifier exhibits an expanding nonlinearity. As the amplification progresses, the gain becomes less expanding and eventually starts to display compressing behavior, i.e. it drops for larger inputs. During this cross-over moment t_{opt}, when the nonlinearity changes from an expanding into a compressing characteristic, the gain becomes independent of the input signal. Hence, the amplifier exhibits perfect linearity, as indicated by the peak in THD (Figure 3.15). The existence of this ideal linearity can be proven mathematically, as will be described in the following section.

3.5.2 Mathematical Analysis

In this section, the amplifier's transient gain is calculated to show that it is signal-independent at the cross-over moment t_{opt}. For this derivation, the differential amplifier is assumed to have no mismatch. Furthermore, the amplifier's harmonic components are derived, revealing that the proposed CDL technique can only eliminate odd-order distortions at t_{opt}. The even-order harmonics are eliminated due to the differential operation of the amplifier.

3.5.2.1 Derivation of the Differential Gain

The drain-source current I_{DS} for the positive-half circuit of a capacitively degenerated amplifier (Figure 3.14) can be expressed by (3.25). It is repeated here for convenience:

$$I_{DS} = I_B \, exp\left(\frac{V_{in}}{2nU_T}\right) exp\left(-\frac{V_{sp}}{U_T}\right). \tag{3.35}$$

Equation (3.35) assumes that the body of the NMOS transistor is tied to the ground. The bias current I_B can be expressed as follows:

$$I_B = I_{D0} \, exp\left(\frac{V_B}{nU_T}\right). \tag{3.36}$$

The voltage V_B denotes the bias voltage at the gate of the transistors (Figure 3.14). During the amplification phase, the drain-source current I_{DS} flows through the degeneration capacitor C_{DEG} to charge it. Therefore, the following equality holds for the positive half-circuit of the amplifier:

$$\begin{aligned} C_{DEG}\frac{dV_{sp}}{dt} &= I_B \, exp\left(\frac{V_{in}}{2nU_T}\right) exp\left(\frac{-V_{sp}}{U_T}\right) \\ \Rightarrow \; exp\left(\frac{V_{sp}}{U_T}\right)\frac{dV_{sp}}{dt} &= \frac{I_B}{C_{DEG}} exp\left(\frac{V_{in}}{2nU_T}\right) \end{aligned} \tag{3.37}$$

Integrating both sides of (3.37) results in as follows:

$$\begin{aligned} \int_0^{V_{sp}} exp\left(\frac{V_{sp}}{U_T}\right) dV_{sp} &= \int_0^t \frac{I_B}{C_{DEG}} exp\left(\frac{V_{in}}{2nU_T}\right) dt \\ \Rightarrow U_T \, exp\left(\frac{V_{sp}}{U_T}\right) &= \frac{I_B t}{C_{DEG}} exp\left(\frac{V_{in}}{2nU_T}\right) + c_1 \\ \Rightarrow V_{sp}(t) = U_T \, ln\left(\frac{I_B t}{C_{DEG}U_T} exp\left(\frac{V_{in}}{2nU_T}\right) + c_1 \frac{1}{U_T}\right), \end{aligned} \tag{3.38}$$

where c_1 is an integration constant, and t represents the duration of amplification. At the beginning of amplification, i.e. at time $t = 0$, the voltage at the source terminal of the transistor is also zero ($V_{sp} = 0$). This initial condition can be used in (3.38) to determine the integration constant c_1 as follows:

$$0 = U_T \, ln\left(0 + c_1 \frac{1}{U_T}\right)$$

$$\Rightarrow c_1 = U_T \tag{3.39}$$

Substituting the value of c_1 in (3.38) results in the following:

$$V_{sp}(t) = U_T \, ln\left(1 + \frac{I_B t}{C_{DEG} U_T} exp\left(\frac{V_{in}}{2nU_T}\right)\right) \tag{3.40}$$

$$\Rightarrow V_{sp}(t) = U_T \, ln\left(1 + \alpha(t) \, exp\left(\frac{V_{in}}{2nU_T}\right)\right) \tag{3.41}$$

where the factor $\alpha(t)$ is given by:

$$\alpha(t) = \frac{I_B t}{C_{DEG} U_T} \tag{3.42}$$

Similarly, for the negative half-circuit of the amplifier in Figure 3.14, the source voltage V_{sn} can be expressed as:

$$V_{sn}(t) = U_T \, ln\left(1 + \alpha(t) \, exp\left(\frac{-V_{in}}{2nU_T}\right)\right) \tag{3.43}$$

During the amplification period, the amplifier's output voltage increases with time due to the input step. The transient gain of the amplifier can be written using the expression in (3.34) as follows:

$$\begin{aligned} A(t) &= \frac{V_{op}(t) - V_{on}(t)}{V_{in}} \\ &= \frac{C_{DEG}}{C_L} \; \frac{V_{sp}(t) - V_{sn}(t)}{V_{in}}. \end{aligned} \tag{3.44}$$

By using the expressions of (3.41) and (3.43) in (3.44), the gain $A(t)$ can be expressed as:

$$A(t) = \frac{C_{DEG}}{2nC_L} + \frac{C_{DEG}}{C_L} \frac{U_T}{V_{in}} \ln\left(\frac{\alpha(t) + exp\left(-\frac{V_{in}}{2nU_T}\right)}{1 + \alpha(t) \, exp\left(-\frac{V_{in}}{2nU_T}\right)}\right) \tag{3.45}$$

If the factor $\alpha(t)$, given by (3.42), is equal to one, then the transient gain $A(t)$ becomes:

$$A(t)_{\alpha(t)=1} = \frac{C_{\mathrm{DEG}}}{2nC_L} + \frac{C_{\mathrm{DEG}}}{C_L}\frac{U_T}{V_{\mathrm{in}}}\ln\left(\frac{1+exp\left(-\frac{V_{\mathrm{in}}}{2nU_T}\right)}{1+exp\left(-\frac{V_{\mathrm{in}}}{2nU_T}\right)}\right)$$

$$\Rightarrow A(t)_{\alpha(t)=1} = \frac{C_{\mathrm{DEG}}}{2nC_L} + \frac{C_{\mathrm{DEG}}}{C_L}\frac{U_T}{V_{\mathrm{in}}}\ln(1)$$

$$\Rightarrow A(t)_{\alpha(t)=1} = \frac{C_{\mathrm{DEG}}}{2nC_L} \tag{3.46}$$

Equation (3.46) shows that the amplifier's transient gain is signal-independent when the factor $\alpha(t) = 1$, indicating perfect linearity. The optimal gain is approximately one-third ($1/2n \approx 0.35$) of the amplifier's steady-state gain (C_{DEG}/C_L). The amplifier, therefore, only needs to settle to less than half a time constant (τ) to achieve this gain. Hence, it effectively behaves like an integrator, which is favorable for noise performance [9], [30]. Moreover, the CDL technique degenerates the transconductance $g_{m,\mathrm{eff}}$ by only ~1.5× to achieve this optimal linearity, thus improving the power efficiency significantly compared to traditional degeneration.

The condition for optimal linearity is given by:

$$\alpha(t) = 1$$

$$\Rightarrow \frac{I_B t}{C_{\mathrm{DEG}} U_T} = 1 \tag{3.47}$$

Both the amplification period t and bias current I_B can be adjusted to achieve this optimal linearity. The optimal amplification time t_{opt} and bias current $I_{B,\mathrm{opt}}$ can be expressed as:

$$t_{\mathrm{opt}} = \frac{C_{\mathrm{DEG}} U_T}{I_B} \tag{3.48}$$

$$I_{B,\mathrm{opt}} = \frac{C_{\mathrm{DEG}} U_T}{t} \tag{3.49}$$

The source voltage V_{sp} of (3.41) at the optimal linearity condition becomes:

$$V_{\mathrm{sp}}(\alpha(t)=1) = U_T\, ln\left(1 + 1\times exp\left(\frac{V_{\mathrm{in}}}{2nU_T}\right)\right) \tag{3.50}$$

For the quiescent condition, i.e when no input voltage is applied ($V_{in} = 0$), the source voltage is given by:

$$V_{sp}(\alpha(t)=1)_{V_{in}=0} = U_T\, ln(2) \approx 0.7U_T \tag{3.51}$$

Equation (3.51) suggests that the quiescent source voltage at the optimal linearity is proportional to the thermal voltage U_T, similar to the resistive degeneration case (3.29). However, the proportionality constant is 0.7 for the CDL but 0.5 for the RDL technique.

It should be noted that if the body of the NMOS transistor is connected to its source node instead of the ground, then the drain-source current will vary according to (3.31). In that case, the optimal gain $A(t = t_{opt})$ and time t_{opt} can be calculated by following the same derivation method. The resultant expressions are shown below, in which the weak-inversion slope factor n appears in the optimal time but not in the optimal gain expression:

$$A(t = t_{opt}) = \frac{C_{DEG}}{2C_L} \tag{3.52}$$

$$t_{opt} = \frac{n\, C_{DEG} U_T}{I_B} \tag{3.53}$$

3.5.2.2 Derivation of Harmonic Components

It has been shown in the previous section that the amplifier's differential gain is linear at the optimal time t_{opt}. This is only valid when an ideal matching between left and right is assumed in the amplifier. Any mismatch between the differential circuits gives rise to even-order distortion, resulting in a nonlinear gain. However, the amplifier still does not contain any odd-order harmonics at t_{opt}, which can be proven by deriving its harmonic components. This means a single-ended implementation is sufficient to remove all odd-order distortions, as will be shown below.

For the optimal linearity condition, the source voltage V_{sp} from (3.50) can be written as follows, defining $p = 1/(2nU_T)$:

$$V_{sp}(\alpha(t)=1) = f(V_{in}) = U_T \, ln\left(1 + exp\left(pV_{in}\right)\right) \tag{3.54}$$

A Taylor series expansion can be applied to (3.54) as follows to evaluate the harmonic distortion components in V_{sp}:

$$f(V_{in}) = f(0) + V_{in} f'(0) + \frac{V_{in}^2}{2!} f''(0) + \frac{V_{in}^3}{3!} f'''(0) + \frac{V_{in}^4}{4!} f^{IV}(0) + \cdots \tag{3.55}$$

The derivative values such as $f'(V_{in})$, $f''(V_{in})$, $f'''(V_{in})$ can be calculated as follows:

$$f'(V_{in}) = \frac{d}{dV_{in}}(V_{in}) = \frac{pU_T \, exp(pV_{in})}{1 + exp(pV_{in})} \tag{3.56}$$

$$f''(V_{in}) = \frac{d}{dV_{in}} f'(V_{in}) = p f'(V_{in}) - \frac{(f'(V_{in}))^2}{U_T} \tag{3.57}$$

$$f'''(V_{in}) = \frac{d}{dV_{in}} f''(V_{in}) = p f''(V_{in}) - \frac{2 f'(V_{in}) f''(V_{in})}{U_T} \tag{3.58}$$

$$f^{IV}(V_{in}) = \frac{d}{dV_{in}} f'''(V_{in}) = p f'''(V_{in}) - \frac{2[f'(V_{in}) f'''(V_{in}) + (f''(V_{in}))^2]}{U_T} \tag{3.59}$$

$$\begin{aligned} f^{V}(V_{in}) &= \frac{d}{dV_{in}} f^{IV}(V_{in}) \\ &= p f^{IV}(V_{in}) - \frac{2[f'(V_{in}) f^{IV}(V_{in}) + 3 f''(V_{in}) f'''(V_{in})]}{U_T} \end{aligned} \tag{3.60}$$

Evaluating these derivatives, given by (3.56) to (3.60), at zero input ($V_{in} = 0$) results in the following:

$$f'(V_{in}=0) = \frac{pU_T}{2} \tag{3.61}$$

$$f''(V_{in}=0) = \frac{p^2 U_T}{4} \tag{3.62}$$

$$f'''(V_{in}=0) = 0 \tag{3.63}$$

$$f^{IV}(V_{in}=0) = \frac{-p^4 U_T}{8} \tag{3.64}$$

$$f^{V}(V_{in}=0) = 0 \tag{3.65}$$

Using these derivative values at $V_{in} = 0$ (given in (3.61) to (3.65)) in (3.55) results in the following expression:

$$V_{sp}(\alpha(t)=1) = f(V_{in}) = U_T \ln 2 + \frac{pU_T}{2} V_{in} + \frac{p^2 U_T}{8} V_{in}^2 - \frac{p^4 U_T}{192} V_{in}^4 + \cdots \tag{3.66}$$

Similarly, for the negative-half circuit of the amplifier, the source voltage V_{sn} at the optimal linearity condition can be calculated as follows (assuming no mismatch):

$$V_{sn}(\alpha(t)=1) = f(V_{in}) = U_T \ln 2 - \frac{pU_T}{2} V_{in} + \frac{p^2 U_T}{8} V_{in}^2 - \frac{p^4 U_T}{192} V_{in}^4 + \cdots \tag{3.67}$$

It can be concluded from (3.66) and (3.67) that each half-circuit of the amplifier does not exhibit any odd-order harmonics at the optimal linearity condition. The single-ended voltages (V_{sp} or V_{sn}) only contain an offset, a signal component, and all even-order harmonics. Both the offset and even-order harmonics are significantly reduced due to the differential operation ($V_{sp} - V_{sn}$) and will be nullified if an ideal matching is assumed.

3.6 Design Considerations

This section focuses on practical design considerations of the presented linearization techniques such as bias inaccuracy and circuit mismatch. Although the points are discussed for the CDL technique, they also apply to the RDL technique.

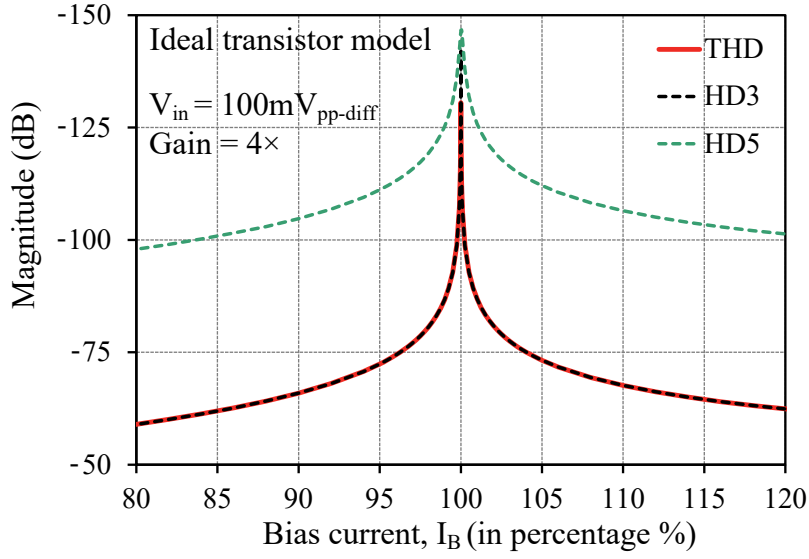


Figure 3.16: Simulated nonlinearity of a capacitively degenerated amplifier with variation in bias current. An ideal transistor model is assumed for this simulation.

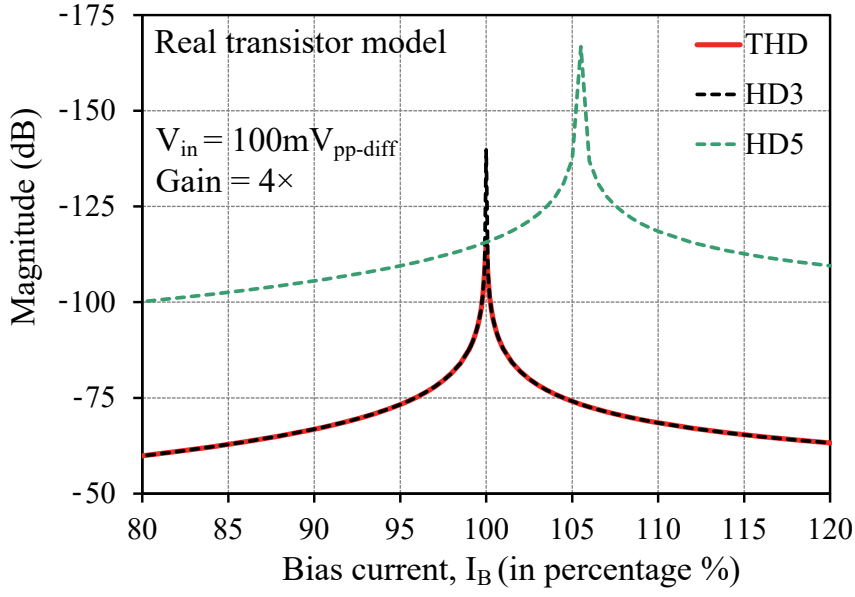


Figure 3.17: Simulated amplifier nonlinearity with bias current variation using the CDL technique.

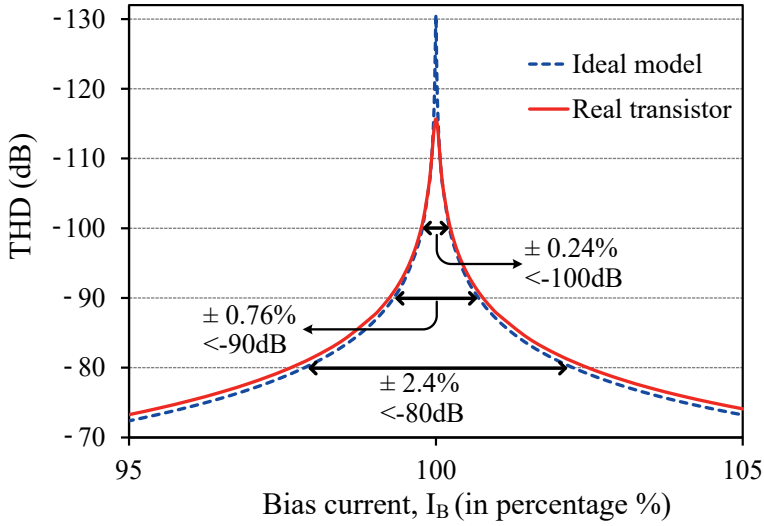


Figure 3.18: Simulated THD versus bias current for both ideal and real transistor models.

3.6.1 Bias Sweep

In a pipelined ADC, the allocated time for amplification is usually governed by the system clock and cannot be changed easily. In contrast, the bias current I_B of the amplifier can be easily made programmable. As shown in (3.49), the bias current for optimal linearity $I_{B,\text{opt}}$ has a specific relationship with the degeneration capacitance C_{DEG}, thermal voltage U_T, and allocated amplification time t. However, due to PVT variation, the bias current can deviate from the optimal value $I_{B,\text{opt}}$. Figure 3.16 shows how the amplifier's linearity is affected as the bias current varies from $I_{B,\text{opt}}$. This analysis assumes an ideal transistor model in weak-inversion and also no mismatch between the differential circuits. An input signal swing of $100\text{mV}_{\text{pp-diff}}$ and a gain of 4× are used for this nonlinearity simulation. As shown in Figure 3.16, the proposed CDL technique eliminates all odd-order harmonics at the optimal linearity condition (I_B = 100%). This is also expected from the mathematical analysis discussed in the previous section.

When a real transistor is used instead of an ideal model, the cancellation of HD3 and HD5 does not occur precisely at the same bias point, as shown in Figure 3.17. However, the impact of that is minimal because, with both ideal and real transistor models, the amplifier exhibits better than –100dB of total harmonic distortion (THD). Also, in both cases, THD is limited by HD3 for the majority of the bias sweep.

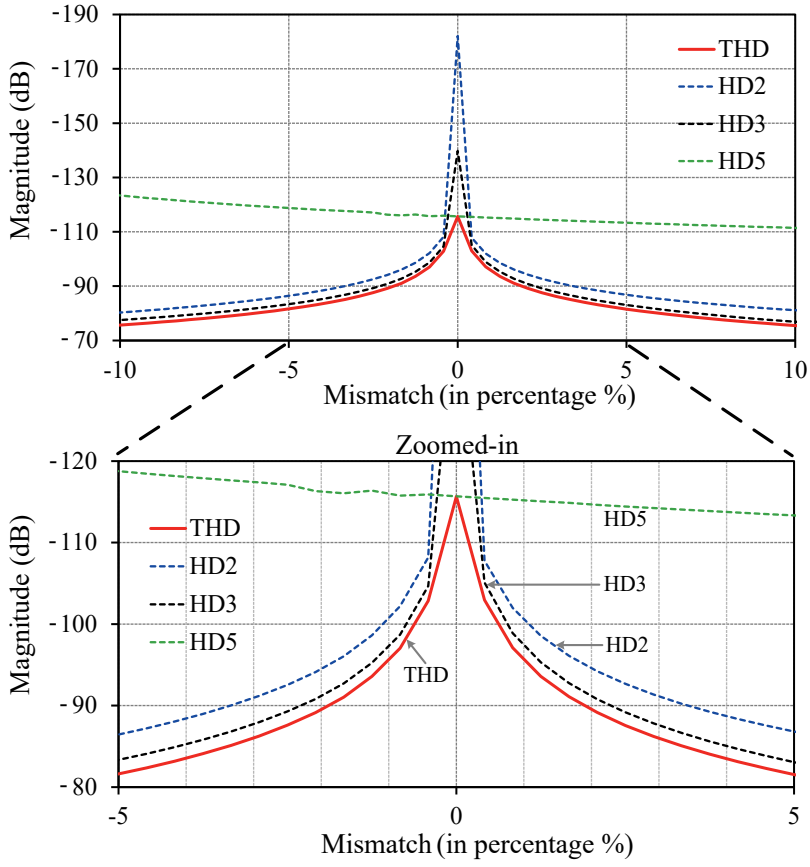


Figure 3.19: Simulation nonlinearity versus mismatch when the amplifier is calibrated once at zero mismatch. For this simulation, an input signal swing of $100mV_{pp\text{-}diff}$ is used with 4× gain.

Both with an ideal model and a real transistor, the amplifier's linearity degrades when the bias current deviates from the optimal value (Figure 3.18). Note the similarity between the THD results of the ideal and real transistors. As can be expected, the target linearity determines the acceptable range of bias current variation. If an application requires >100dB linearity, then the bias current can vary maximally ±0.24%. To ensure such accuracy over PVT, the CDL technique should be used in tandem with a digital error detection loop. However, as the required linearity decreases, a larger variation in bias current can be tolerated. For example, with ±5% bias current inaccuracy, the amplifier still exhibits better than 70dB linearity, which is sufficient for many applications. This wide linear range makes the CDL technique viable also for amplifiers that do not use digital nonlinearity calibration.

3.6.2 Effect of Mismatch

As discussed in the previous section, the proposed CDL technique helps minimize odd-order harmonic distortion. However, it cannot mitigate even-order harmonics, the cancellation of which depends on the symmetry of the differential circuit. Hence, any mismatch between the differential elements, e.g., the input transistors, will cause an imbalance in the symmetrical operation and give rise to even-order harmonics.

To analyze this effect, the amplifier's input transistors (Figure 3.14) are set to a different aspect ratio to introduce mismatch. Figure 3.19 shows the simulated nonlinearity due to this mismatch. During this test, the amplifier is optimized for linearity once at no mismatch condition. Consequently, as a mismatch is introduced in the circuit, both HD2 and HD3 degrade because we deviate from the optimal condition. With a ±5% and ±10% mismatch, the amplifier still exhibits better than –80dB and –70dB THD, respectively. However, note that in advanced CMOS process nodes, a matching accuracy of 1% can be readily achieved, which would result in a THD of better than –95dB.

The degradation of HD3 with mismatch can be mitigated if the amplifier is used in an ADC, where digital nonlinearity *detection* is used to optimize the bias current. This is because the calibration will take into account any systematic mismatch while optimizing the bias current for linearity. The resulting nonlinearity is depicted in Figure 3.20, which shows that the HD3 does not degrade anymore due to circuit mismatch. Although the overall THD improves because of this, it is eventually limited by the HD2 as the proposed CDL technique cannot mitigate it. If the system requires lower second-order distortion, then offset calibration [29], [31] can be implemented.

3.6.3 Impact of Biasing Region

The proposed linearization technique relies on an exponential *V–I* relationship and hence requires MOSFETs to operate in the weak-inversion saturation region. How far the amplifier should be biased in weak-inversion depends on the desired maximum input signal swing. However, suppose the amplifier (Figure 3.14) deviates from the weak-inversion (WI) operating region to the moderate-inversion and eventually to the strong-inversion (SI) operating region. In that case, the CDL technique will be less effective, causing a gradual degradation in linearity, as discussed below.

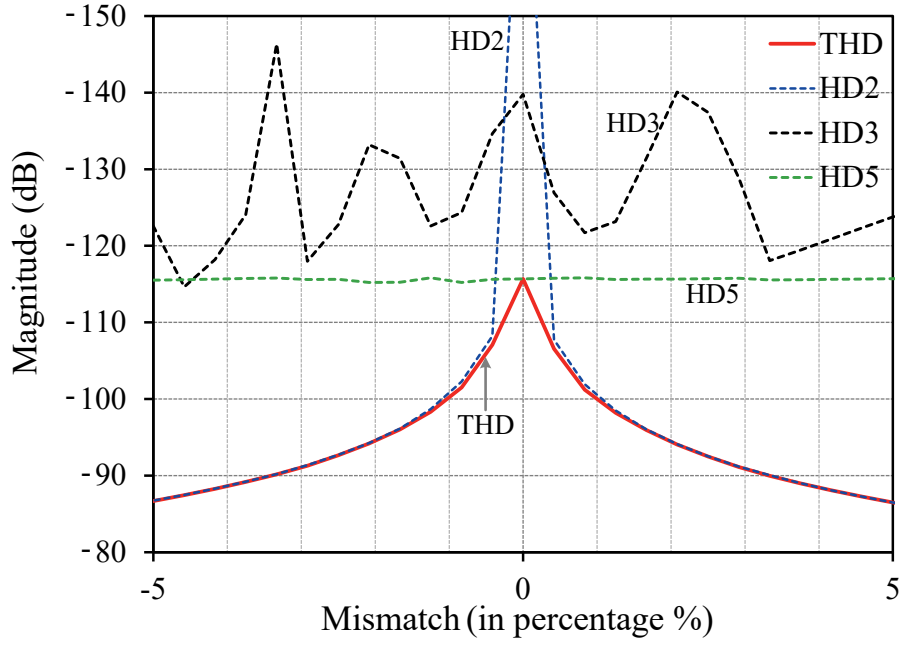


Figure 3.20: Simulation nonlinearity versus mismatch when the amplifier is calibrated for every mismatch value.

Figure 3.21 shows a simulation result that explains how changing the amplifier's bias region affects its linearity performance. The bias region is modified by scaling the aspect ratio (W/L) of transistors with a parameter n_f while keeping the bias current constant. For this simulation, an input signal swing of $100\text{mV}_{\text{pp-diff}}$ is used. In the default case, i.e. $n_f = 1$, the input transistors have an overdrive voltage ($V_{GT} = V_{GS} - V_{th}$) of about –115mV. As n_f is reduced, the W/L of the transistors become smaller, thus requiring a larger overdrive voltage V_{GT} to carry the same bias current. Consequently, the transistors are pushed towards the moderate- and eventually strong-inversion saturation region, where their V–I characteristics are no longer exponential. In that extreme scenario ($n_f = 1/32$ and $V_{GT} = 70\text{mV}$), the proposed CDL technique is not effective anymore, as can be expected. However, it should be noted from Figure 3.21 that even in moderate-inversion, where the overdrive voltage V_{GT} is around zero, the proposed linearization technique significantly improves the linearity of the amplifier.

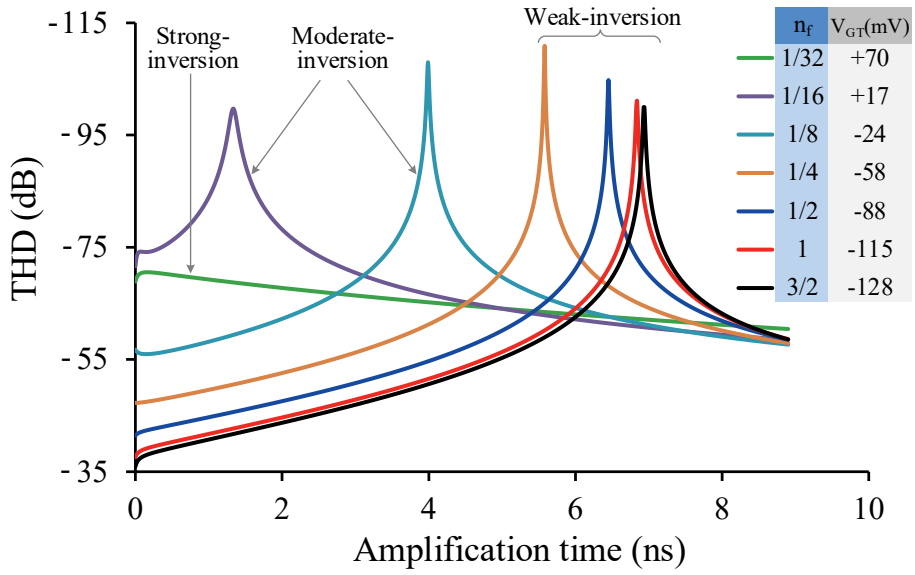
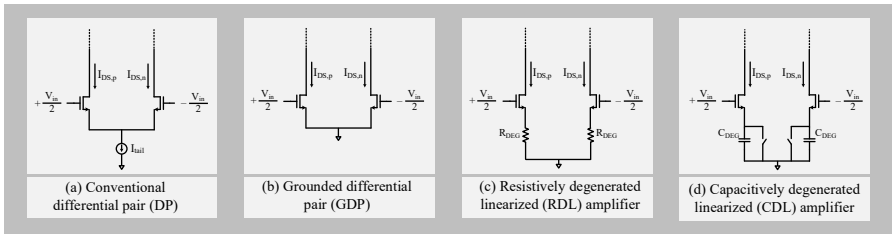


Figure 3.21: Simulated THD versus amplification time for several design sizes of the amplifier n_f. By reducing the n_f factor while keeping the bias current constant, the overdrive voltage V_{GT} of the amplifier is increased. This increased V_{GT} voltage pushes the amplifier from the weak-inversion into the strong-inversion saturation region.

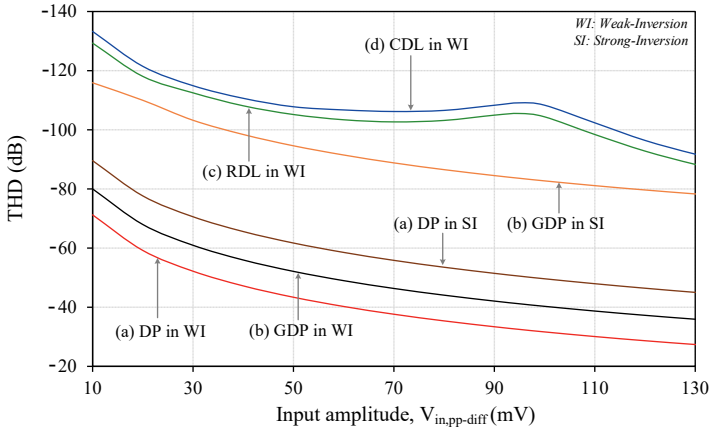
It can also be observed from Figure 3.21 that optimal linearity occurs earlier during the amplification phase when V_{GT} is higher. The reason for this is explained as follows. With an increase in V_{GT}, the V–I characteristic of the MOSFET becomes less exponential because it gradually moves away from the weak-inversion region. Hence, the amplification begins with less expanding behavior, which then requires less compression to reach the optimal linearity. As a result, the optimal gain of the amplifier decreases. This gain reduction can be compensated by increasing the capacitor ratio (C_{DEG}/C_L) of the amplifier.

3.7 Summary

This chapter focuses on the linearity of residue amplifiers built from differential pairs. It describes various linearization techniques to improve amplifier linearity in a power-efficient way. First, a few well-known techniques based on the strong-inversion (SI) operating region



(e) Nonlinearity Comparison of Various Amplifier Input Stages



Input Pairs	THD at 100mV$_{pp\text{-}diff}$
(a) DP in WI	32
(b) GDP in WI	40
(a) DP in SI	50
(b) GDP in SI	83
(c) RDL in WI	104
(d) CDL in WI	108

Figure 3.22: (a)–(d) Various well-known and proposed amplifier input-topologies and (e) a comparison of their simulated nonlinearities. The quiescent currents in all the amplifiers were kept the same for this comparison.

of MOSFET are described. Next, linearization techniques based on the weak-inversion (WI) operation are presented that employ resistive or capacitive degeneration. These techniques are explained both intuitively and mathematically, along with some of their practical design considerations. Figure 3.22 shows an overview of the simulated nonlinearities of various amplifier stages discussed in this chapter. It includes the conventional differential pair (Figure 3.22(a)) to the proposed capacitively degenerated amplifier (Figure 3.22(d)). Figure 3.22(e) shows a comparison of their simulated nonlinearities. Compared to the conventional differential pair, the other topologies such as the grounded differential pair in SI (Figure 3.22(b)), the resistively (Figure 3.22(c)), and capacitively degenerated amplifiers in WI exhibit significantly better linearity. Hence, these linearization techniques (Figure 3.22(b)–(d)) are used in the proposed residue amplifiers of Chapters 4–6, respectively.

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4

Implementation I – A Class-AB Residue Amplifier for a Pipelined Split-ADC

4.1 Introduction

This chapter presents a push-pull class-AB residue amplifier (ResAmp) for pipelined analog-to-digital converters (ADCs). It employs a novel level shifting technique to bias the amplifier's NMOS and PMOS gates. As shown in Section 4.2, this technique eliminates the need for any additional level-shifting capacitors, saving significant power dissipation and area. Furthermore, incomplete settling (discussed in Section 2.3) is used in the ResAmp to enhance its power efficiency. The amplifier is sufficiently linear by design, and thus only its gain error needs correction.

Gain error calibration is implemented by combining digital error detection and analog error correction to minimize power overhead. The errors are detected in the digital domain by using the split-ADC technique. After detection, the amplifier's gain error is corrected by adjusting its bias current. Since the error is corrected at its source, there is no loss of ADC

This chapter is based on the journal publication by the authors M. S. Akter, R. Sehgal, F. van der Goes, K. A. A. Makinwa and K. Bult, "A 66-dB SNDR Pipelined Split-ADC in 40-nm CMOS Using a Class-AB Residue Amplifier," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2939-2950, Oct. 2018.

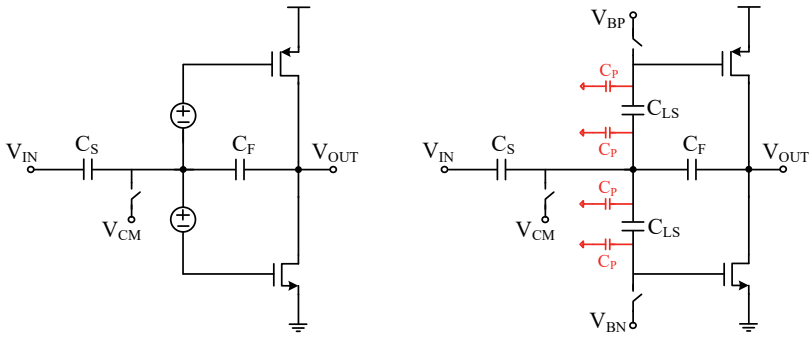

Figure 4.1: Class-AB amplifier half-circuit with (a) ideal voltage source level shifters and (b) capacitor level shifters.

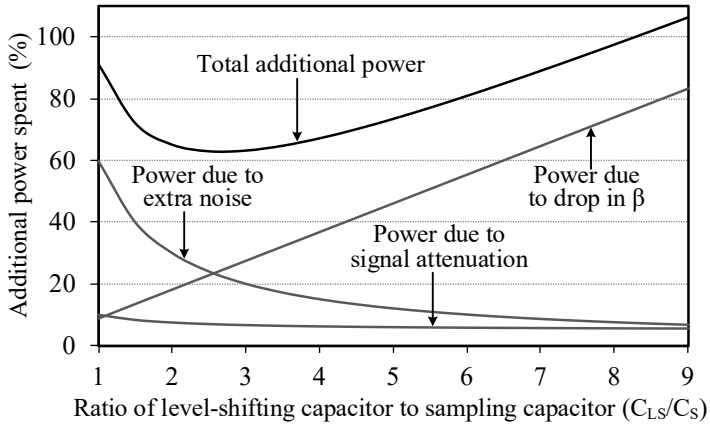

Figure 4.2: Calculated power penalty due to extra capacitor level shifters (C_{LS}) in a class-AB amplifier compared to that with ideal voltage source level shifters.

resolution, as explained in Section 2.4.2. Moreover, this error correction approach requires no additional power overhead.

The calibration of the pipelined split-ADC prototype in 40nm CMOS reaches convergence in only 12k clock cycles. With a near-Nyquist input, the ADC achieves a 66 dB SNDR and 77.3 dB SFDR at a 53 MS/s clock speed. The overall power dissipation is 9 mW, of which 0.83 mW is consumed in the residue amplifiers.

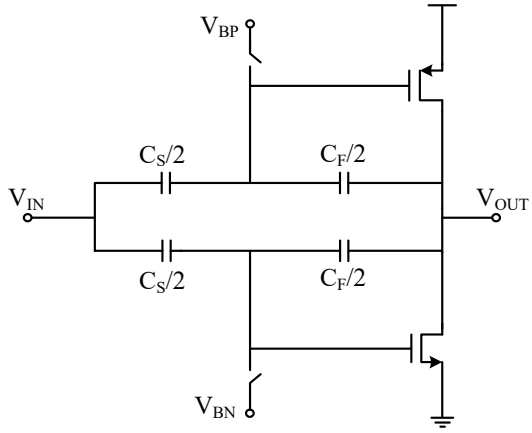

Figure 4.3: Half-circuit of the proposed class-AB residue amplifier using a split-capacitor level-shifting technique.

4.2 Class-AB Residue Amplifier Design

Over the years, several power-efficient residue amplifier topologies have been proposed [1]–[11]. One such topology is the push-pull inverter or class-AB residue amplifier [1], [3], [5] shown in Figure 2.2 (repeated in Figure 4.1(a) for convenience). As discussed in Section 2.2, it offers several benefits such as high current driving capability, improved g_m/I_d, and large output swing. This section will describe the design details of this class-AB residue amplifier.

4.2.1 Split-Capacitor Level Shifting Technique

One of the challenges of a class-AB amplifier design is the need to simultaneously drive the inputs of both its NMOS and PMOS devices. Since they are usually biased at different voltages, a level shifter is required between the two inputs, modeled as ideal voltage sources in Figure 4.1(a). These voltage sources can be implemented by switched-capacitor circuits [3], [5], as shown in Figure 4.1(b). However, the additional level-shifting capacitors C_{LS} increase chip area and significantly degrade the amplifier's power efficiency (more detail in Appendix A). First, these C_{LS} capacitors add kT/C noise. Second, they attenuate the input signal due to the voltage division between C_{LS} and C_{GS} (gate-source) capacitors. Therefore, the C_{LS} capacitors need to be quite large to mitigate both these effects. However, increasing C_{LS} increases the parasitic capacitance (C_P) at the virtual ground, reducing the amplifier's feedback factor β and bandwidth. Figure 4.2 shows this tradeoff under the assumption that

the parasitic capacitance C_P is 5% of the intended capacitance C_{LS}. Even at the optimum point, an amplifier with C_{LS} level shifters requires 63% more power than one with ideal level shifters (Figure 4.1(a)) for the same bandwidth and noise.

To eliminate the drawbacks of the C_{LS} capacitors, this work presents a "split-capacitor" biasing technique. As shown in Figure 4.3, it uses the already available sampling C_S and feedback C_F capacitors to perform the level-shifting operation. Both capacitors are split in half and used to store the level-shifting voltages, allowing the amplifier's NMOS and PMOS transistors to be biased independently. Hence, the C_{LS} capacitors, and their associated drawbacks, are eliminated.

Splitting the capacitors into two halves (Figure 4.3) does not affect the amplifier's noise performance. Although the sampled noise across each $C_S/2$ capacitor is doubled ($2kT/C_S$) compared to a single C_S capacitor, it transfers to the amplifier's output with a gain equal to the capacitor ratio $\frac{C_S/2}{C_F}$. Hence, each $C_S/2$ capacitor contributes an output noise power of $(2kT/C_S) \times (C_S/2C_F)^2 = (1/2) \times (kT/C_S) \times (C_S/C_F)^2$. The overall noise power, therefore, remains the same as in the case of a single C_S capacitor. Intuitively, this can be understood by realizing that the total sampling capacitance stays the same after the splitting, and so the associated noise power must also be the same. In fact, the proposed class-AB amplifier achieves the same performance as the amplifier with ideal level shifters (Figure 4.1(a)).

However, the split-capacitor approach does require two bottom plate switches and clock drivers, which leads to a minor increase in area and power compared to ideal level-shifters. The two bottom-plate sampling clocks should also be well synchronized to ensure that the signals sampled on the split-capacitors are as equal as possible.

4.2.2 Linearity

The residue amplifier in this design requires about 60dB linearity, which, as shown in Figure 3.22, can be achieved by proper design. The amplifier employs grounded differential pairs whose transistors are biased in the strong-inversion (SI) saturation region. As shown in Section 3.2 and Figure 3.22, the resulting class-AB amplifier is more linear [12] than a differential pair with a fixed tail current source. Although the choice of SI operation slightly degrades the amplifier's power efficiency (g_m/I_d), it is offset by the fact that digital nonlinearity calibration [13]–[16] is not required. A more serious drawback is that the

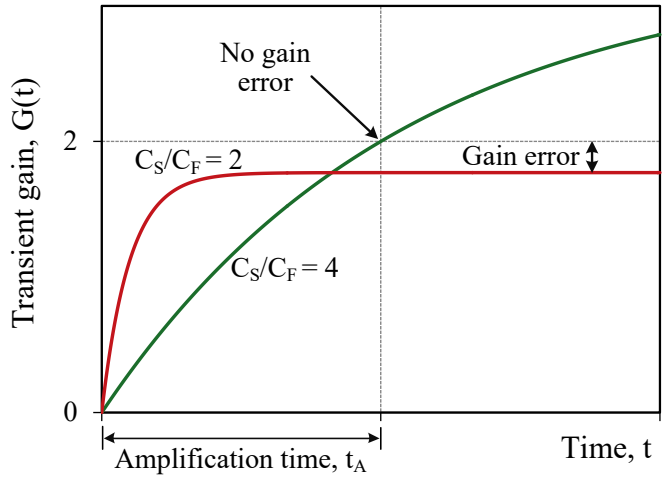

Figure 4.4: Gain settling of an amplifier for different capacitor ratios (C_S/C_F).

amplifier has no common-mode rejection capability. However, this can be addressed through circuit techniques, which will be discussed in Section 4.3.2.

4.2.3 Use of Incomplete Settling

Incomplete settling is used in the proposed residue amplifier to reduce its bandwidth and power dissipation substantially. Moreover, it helps to optimize the trade-off between the amplifier's noise performance and power dissipation [15], [16], as explained in Section 2.3. An amplifier gain $G_{eff} = 2$ is considered in the following discussions, since the ADC [16] employs a 1.5bit/stage MDAC (more on this in Section 4.3).

Gain enhancement techniques (such as cascoding or gain-boosting) are not used in the amplifier to keep it simple and allow higher output swings (Figure 4.3). Consequently, it exhibits a low DC gain (A). This reduces the amplifier's effective gain G_{eff} even after complete settling, causing a static gain error $\left(\frac{1}{1+A\beta}\right)$. Figure 4.4 illustrates this for the case in which the amplifier uses a capacitor ratio $C_S/C_F = 2$ to achieve $G_{eff} = 2$. The gain reduction can also be observed in (2.6), even with no settling error, i.e. when $exp^{-t_A/\tau} = 0$. Although the impact of this gain error on distortion can be mitigated with calibration, it would still affect the ADC's noise by increasing the input-referred noise from the subsequent pipelined stages.

Therefore, the proposed design combines a higher capacitor ratio, $C_S/C_F = 4$, with incomplete settling to avoid gain reduction. As a result, the desired gain can be obtained by merely adjusting the amplifier's time constant τ (Figure 4.4). Since τ is inversely proportional to the amplifier's bandwidth, it can be tuned by making the bias current programmable. This facilitates the implementation of an analog gain correction, as will be discussed in Section 4.4.2.

4.2.4 Jitter Induced Noise

This section describes the impact of jitter-induced noise when an amplifier uses incomplete settling. As will be shown, the impact is negligible because the jitter requirement is more stringent at the input sampler. In the case of complete settling, jitter in the sampling clock results in negligible noise because the amplifier's output does not change much at the sampling moments. However, this is not the case with incomplete settling, resulting in a jitter-induced noise voltage σ_v. As shown in [15], the jitter noise voltage σ_v (that occurs when output voltage = ADC full-scale) normalized to the LSB of the ADC back end is given by:

$$\sigma_{v,\mathrm{LSB}} = \frac{\sigma_v}{\mathrm{LSB}_{\mathrm{backend}}} = 2^{B_{\mathrm{backend}}} \cdot \frac{\sigma_t}{\tau} \cdot \frac{exp^{-t_A/\tau}}{1 - exp^{-t_A/\tau}}, \tag{4.1}$$

The symbol σ_t represents the standard deviation of the clock jitter, and B_{backend} is the resolution of the ADC back end. As expected, jitter affects the output noise voltage more when the amplifier's settling is reduced (i.e. smaller t_A/τ) or if the timing jitter (σ_t/τ) is high.

In the limit case, when $t_A/\tau \to 0$ (ideal integrator), the jitter-induced noise voltage is maximized. It can be derived by taking the limit of $t_A/\tau \to 0$ in (4.1), as given below:

$$\sigma_{v,\mathrm{LSB(worst)}} = 2^{B_{\mathrm{backend}}} \cdot \frac{\sigma_t}{t_A} = 2^{B_{\mathrm{backend}}} \cdot 2F_{\mathrm{S}}\sigma_t \tag{4.2}$$

Note that the amplification time $t_A \approx T_S/2 \approx 1/2F_S$, where T_S is the clock period and F_S is the clock frequency. The jitter-induced noise of (4.2) can be compared with that caused at the input sampler. For a full-scale signal at the input sampler, the jitter induced noise normalized to the LSB of the ADC is given as follows:

$$\sigma_{v\text{-samp,LSB}} = \frac{\sigma_{v\text{-}s}}{\mathrm{LSB}_{\mathrm{ADC}}} = 2^{(B_{\mathrm{stg1}}+B_{\mathrm{backend}})} \cdot 2\pi F_{\mathrm{IN}}\, \sigma_t \tag{4.3}$$

where, B_{stg1} is the resolution of the ADC first-stage in bits, and F_{IN} is the input signal frequency. The worst-case jitter noise at the input sampler occurs when F_{IN} is close to the Nyquist frequency $F_S/2$, as shown below:

$$\sigma_{v\text{-samp,LSB(worst)}} = 2^{(B_{stg1}+B_{\text{backend}})} \cdot \pi F_S \, \sigma_t \tag{4.4}$$

Dividing (4.4) by (4.2) gives:

$$\frac{\sigma_{v\text{-samp,LSB(worst)}}}{\sigma_{v,\text{LSB(worst)}}} = 2^{B_{stg1}} \cdot \frac{\pi}{2} \tag{4.5}$$

Equation (4.5) indicates that even when the first ADC-stage has a single-bit resolution, the worst-case jitter noise voltage at the input sampler is π times higher than that contributed by the amplifier. The design has to accommodate the jitter requirement at the input sampler by moderating the clock jitter σ_t. Hence, the jitter noise due to the amplifier settling has a minor effect on this design.

4.3 ADC Implementation Details

4.3.1 ADC Architecture

As a test vehicle for the proposed amplifier, the SHA-less 12-bit pipelined split-ADC [16] shown in Figure 4.5 was implemented. Each split-ADC comprises nine 1.5-bit MDAC stages using the proposed class-AB residue amplifier, followed by a 5-bit flash-ADC back end. The extra 2 bits in the back end are only used to improve the calibration accuracy. The digital outputs of the two split-ADCs are averaged to provide the overall ADC output and subtracted to generate a calibration signal D_{cal}.

An offset voltage (V_{OS}) is added between the split-ADC reference paths to enable gain error detection. The capacitors are scaled down by a factor of two per stage for stages 1 to 3 (C_S, $C_S/2$, $C_S/4$, $C_S/4$….), while the residue amplifiers are only scaled down twice (g_m, $g_m/2$, $g_m/2$…). Note that the ADC's power efficiency can be further improved by implementing more aggressive stage scaling, i.e. by resolving more bits per stage.

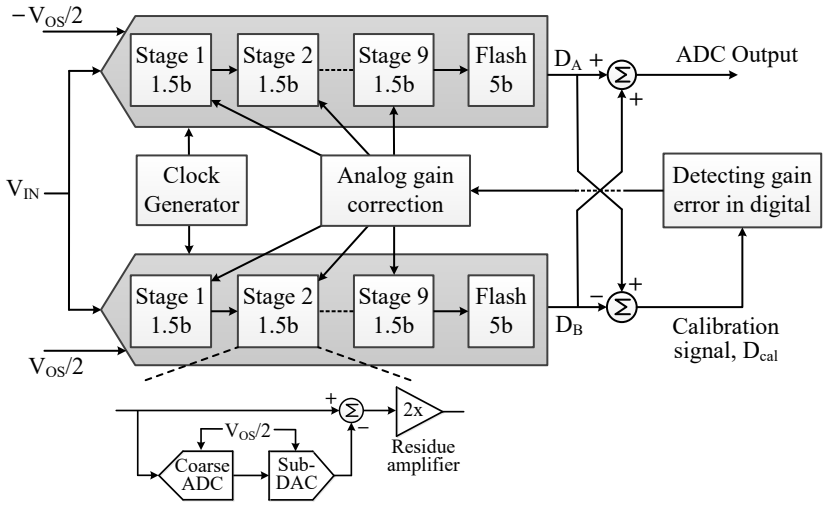

Figure 4.5: Implemented pipelined split-ADC structure.

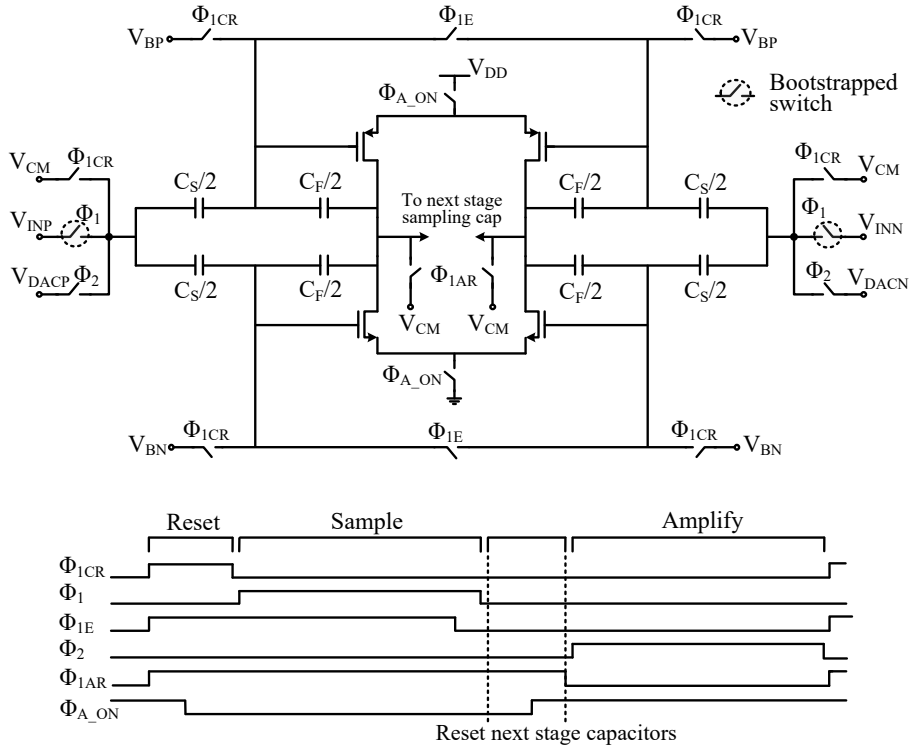

Figure 4.6: MDAC stage topology with timing diagram.

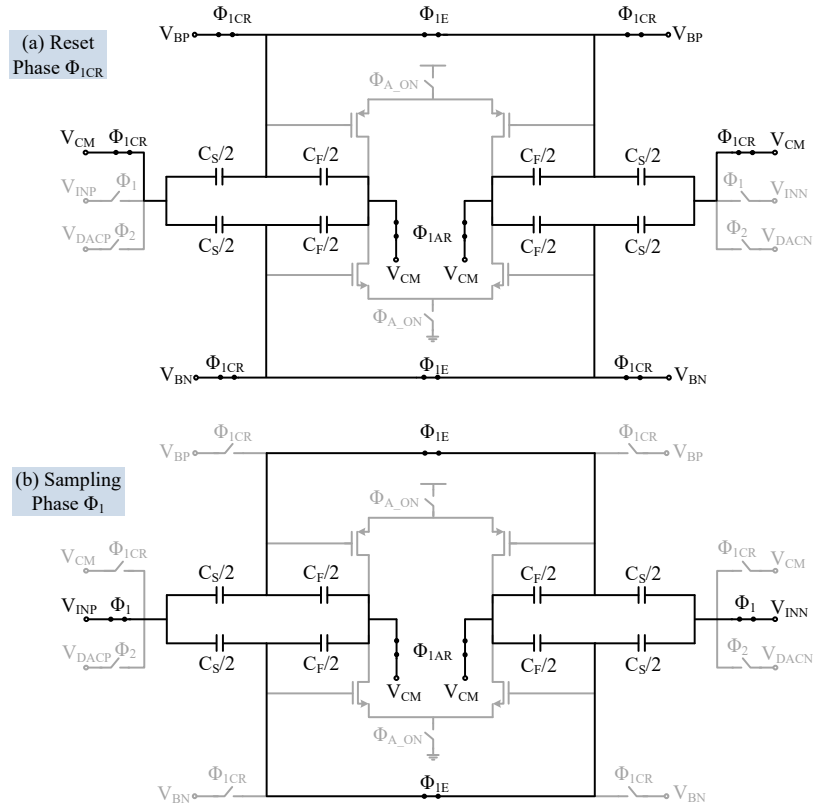

Figure 4.7: Circuit operation of the MDAC during the (a) reset Φ_{1CR} and (b) sampling Φ_1 phases.

4.3.2 MDAC Design

A 1.5-bit per stage MDAC is used in the first nine stages of the ADC, each effectively resolving 1 bit. The MDAC topology and its timing scheme are shown in Figure 4.6. Bootstrapped switches [17], [18] and bottom-plate sampling [19], [20] are used to ensure low sampling distortion. Although a "flip-around" MDAC usually achieves better speed and noise performance, a "non-flip-around" MDAC topology has been chosen in this design. This is because it simplifies the gain calibration [21], [22], as both the input signal (V_{IN}) and the sub-DAC reference (V_{DAC}) experience the same gain error.

When designing a residue amplifier, it is vital to ensure that its present output signal does not depend on the previous output samples. This is because ResAmps operate on subranged signals. Hence, any intersymbol interference (ISI) can degrade the ADC linearity. Since the proposed ResAmp uses incomplete settling, its output will experience ISI if there is no reset.

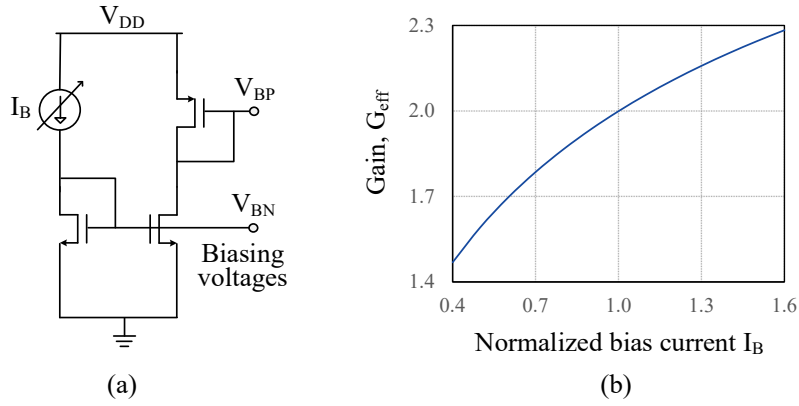

Figure 4.8: (a) Bias circuit of the residue amplifier, and (b) dependence of its gain on the bias current (I_B).

Therefore an additional reset phase (Φ_{1CR}) is introduced to remove ISI by resetting the MDAC capacitors, as shown in Figure 4.7(a). This phase is also used to establish the bias voltages of the ResAmp. To minimize its overhead, Φ_{1CR} is made 24 times shorter than the sampling (Φ_1) and amplification (Φ_2) phases.

The proposed ResAmp is pseudo-differential and hence exhibits an equal common-mode (CM) and differential-mode gain. As a result, CM signals will be amplified as they propagate through the stages, potentially overloading the ADC. To avoid this, a differential sampling technique [5] is used, where the CM impedance of the sampling network is raised by disconnecting the CM switches during the sampling phase Φ_1 (Figure 4.7(b)). Thus, only the differential signal is captured on the sampling capacitors, eliminating any CM signal propagation. When not in use, the residue amplifiers are switched off by the Φ_{A_ON} clock (Figure 4.6), which reduces their power dissipation by about half.

4.3.3 Bias Design

As mentioned in Section 4.2.3, the effective gain (G_{eff}) of the residue amplifier varies with its time-constant τ. Hence, G_{eff} can be adjusted by tuning the quiescent current I_B of the amplifier via a bias current DAC. The dependence of G_{eff} on I_B is shown in Figure 4.8, along with the amplifier's bias circuit. The DAC's LSB step is chosen to ensure that G_{eff} can be set to 10-bit accuracy, while its range is set to about ±25% to compensate for the variation in G_{eff} over PVT. Both requirements can be met with a 9-bit bias current DAC. Simulations show that even with the minimum bias current, the amplifier's transistors still operate in the

strong-inversion saturation region. Therefore, the amplifier maintains its linearity over the full DAC range.

In this design, a 3-bit current DAC sets the nominal current of the amplifier. In addition, 5-bit coarse and 5-bit fine binary current DACs are implemented to correct the gain errors. There is an overlap of about 1 bit between the coarse and fine DACs to prevent large DNL or missing current steps. The LSB current is 80nA, which can be increased or decreased by a factor of two. It should be noted that the extra programmability is not essential and is added for test purposes. Apart from some leakage current, there is no significant power penalty associated with this gain correction approach. However, there is an area penalty since the individual current DACs are sized for monotonicity. The entire bias block occupies 0.05 mm^2, which is around 7% of the ADC core area. The accuracy of the bias current and hence the bias block area can be relaxed by using a multi-bit/stage ADC architecture [10], which imposes less stringent requirements on ResAmp accuracy. For example, a two-stage 14-bit pipelined ADC is presented in [10], where the residue amplifier only needs to be 7-bit accurate (same as the backend) because the first stage already resolves 7-bits.

4.4 Gain Calibration

In this work, an efficient gain calibration scheme is proposed for the residue amplifier that significantly reduces calibration power. This section discusses the methods used for error detection and correction.

4.4.1 Error Detection in the Digital Domain

The split-ADC calibration technique [23]–[26] is used to detect the ResAmp gain error. Section 2.4 already describes the details of this split-ADC detection scheme. Before performing an error detection, the mismatch between the two ADCs is calibrated using the slope-mismatch averaging technique [25]. This removes any tilt or slope in the calibration signal D_{cal}, thus allowing accurate detection of a gain error.

The split-ADC detection method is chosen in this work due to its deterministic nature and consequent faster convergence speed. Unlike other calibration schemes [13], [27], [28], it operates continuously in the background and hence does not impact the ADC's conversion speed. However, it adds an area and power overhead because some of the blocks are not

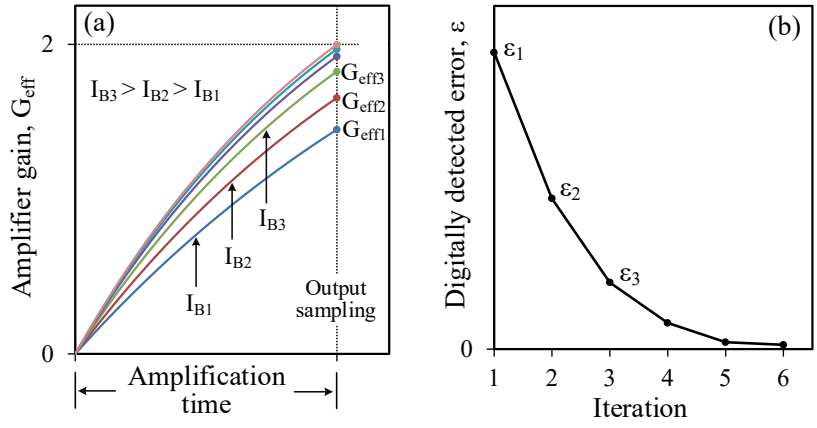

Figure 4.9: Convergence of a single-stage gain calibration: (a) the amplifier's gain for several bias current values and (b) the detected error due to this inaccurate gain over multiple iterations of calibration.

noise-limited and also cannot be split in half (e.g., comparators, flash-ADCs). The overall ADC power dissipation is therefore increased by about 10%.

4.4.2 Analog Gain Correction

Once the errors are detected in the digital domain, they need to be corrected either in the digital [10], [13]–[16] or in the analog domain [29], [30]. In this design, an analog gain-correction is used by programming the amplifier's bias current (Section 4.3.3). The calibration starts from the ADC back-end and progresses toward the first stage because the detected gain error is affected by errors in the back-end stages.

Figure 4.9 illustrates the convergence of a single-stage gain calibration. Consider an initial bias current I_{B1} that results in a gain of G_{eff1} (Figure 4.9(a)). Since the digital gain of the encoder is set to 2, this results in an error ε_1 (Figure 4.9(b)), which is digitally detected by the split-ADC technique. The polarity of ε_1 indicates whether the bias current needs to be increased or decreased. Since the gain is lower than 2 in this case, the bias current is increased to I_{B2}. Consequently, the amplifier's gain increases from G_{eff1} to G_{eff2}, resulting in a smaller gain error ε_2. By following similar steps for a couple of iterations and tuning the bias current appropriately, $G_{eff} = 2$ can be obtained. Since the bias current is only used to achieve the desired gain, there is no additional power penalty associated with this gain correction approach.

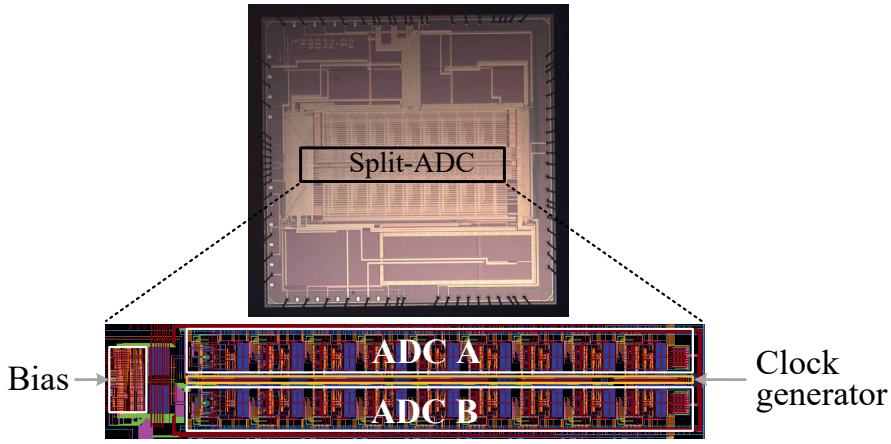

Figure 4.10: Die photograph.

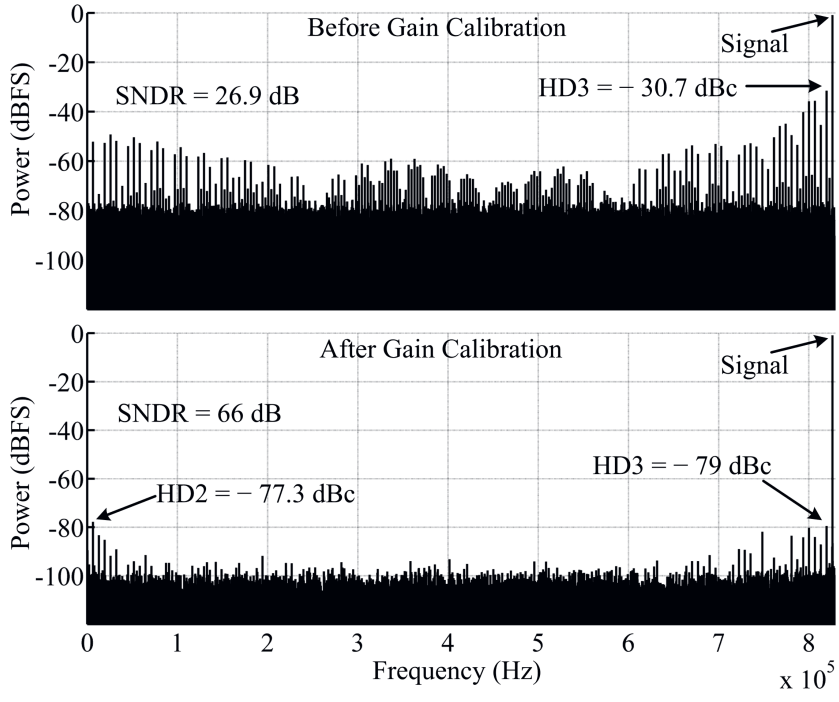

Figure 4.11: Measured 32x decimated ADC output spectra for F_{IN} = 25.7 MHz and F_S = 53 MS/s.

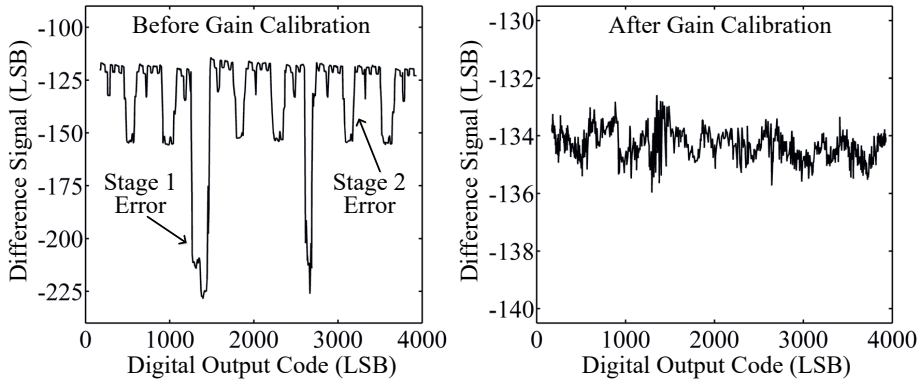

Figure 4.12: Split-ADC difference signal before and after the gain calibration.

4.5 Measurement Results

The prototype ADC was fabricated in a 40 nm CMOS process and occupied about 0.76 mm^2 of area, as shown in Figure 4.10. The ADC's full signal range is 1.5-$V_{pp\text{-}diff}$ with a 1-V supply. Figure 4.11 shows the measured spectra of 32× decimated ADC output data at F_S = 53 MS/s with a 25.7 MHz input signal, before and after gain calibration. The split-ADC difference signal is shown in Figure 4.12 with 12-bit resolution. Since the calibration of different stages is deterministic and orthogonal, convergence was reached in 12,000 clock cycles. As expected, the ADC's performance improves significantly after gain calibration, achieving a 66 dB SNDR and 77.3 dB SFDR.

Figure 4.13 shows the ADC's INL (–0.7/+0.6 LSB) and DNL (–0.24/+0.14 LSB) after gain calibration. Figure 4.14 shows the measured performance of the ADC at F_S = 53 MS/s as the frequency of the input signal was swept. Over the entire range, the ADC exhibits an SNDR of better than 65dB. Furthermore, the performance of the ADC at various clock frequencies is shown in Figure 4.15 for near-Nyquist input signals. The ADC achieves a better than 64 dB SNDR with near-Nyquist inputs up to a clock frequency of 106 MS/s.

The measured amplitude sweep for near-Nyquist input signals at F_S = 53 MS/s is shown in Figure 4.16. As expected, the ADC's SNR improves as the signal amplitude (V_{IN}) increases. Its SNDR also improves until the signal becomes large enough to degrade the linearity. Note that at smaller inputs (< -9dBFS), linearity reduces with V_{IN} due to ResAmp

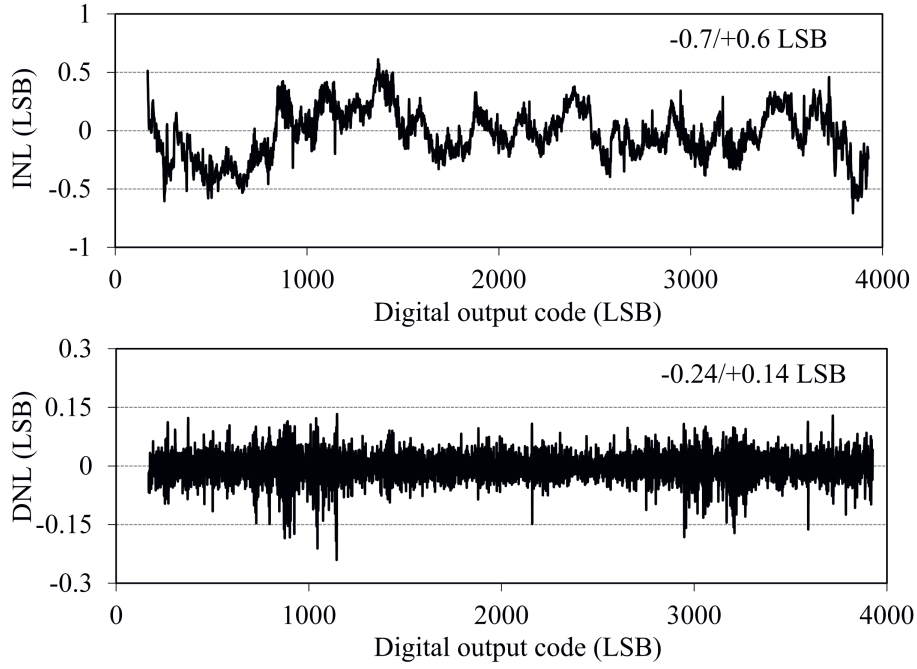

Figure 4.13: INL and DNL after the gain calibration.

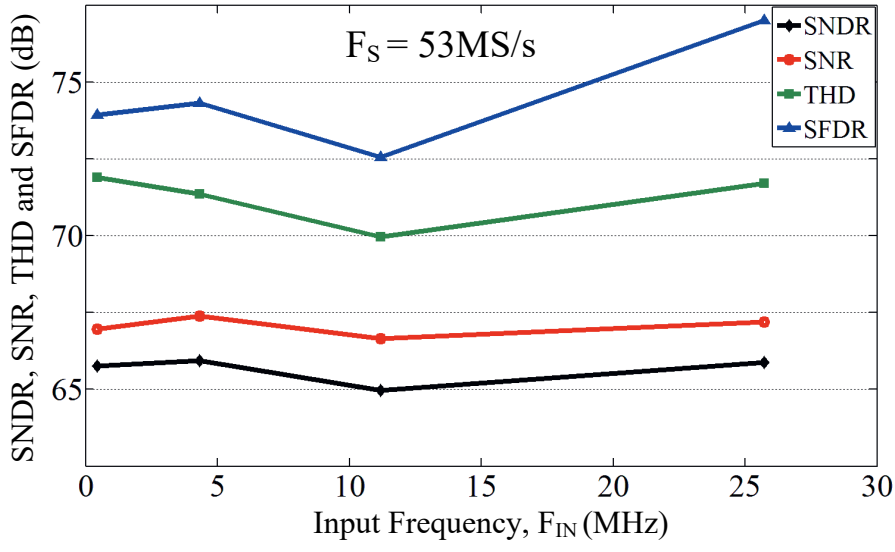

Figure 4.14: Measured ADC performance versus input frequency at a clock speed of 53 MS/s.

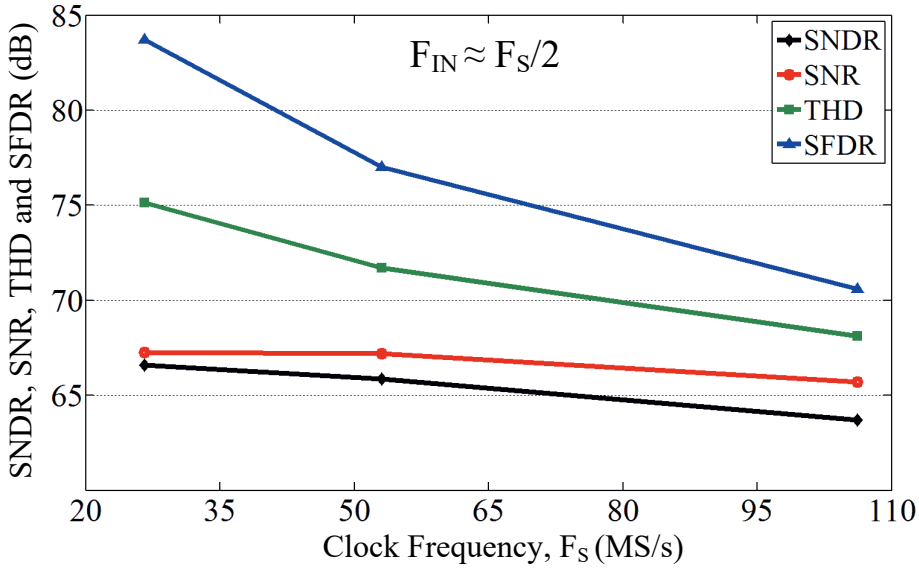

Figure 4.15: Measured ADC performance versus clock frequency with an input signal close to Nyquist.

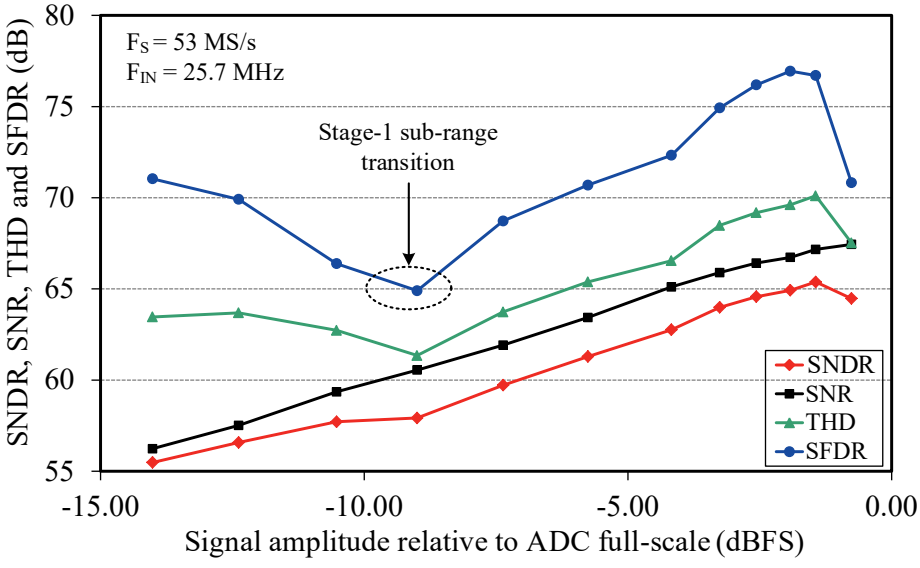

Figure 4.16: Measured performance of the ADC as a function of its input signal amplitude.

nonlinearity. A dip in the SFDR and THD curves can be observed around -9dBFS, which is caused by the residual gain-error of the stage-1 amplifier. This can be understood by realizing that for small input signals (V_{IN} < stage-1 comparator threshold $V_{C,th}$), the stage-1 residue signal is always in the mid-subrange. Therefore, no sub-range transitions take place, and hence the corresponding transition jumps do not occur. As V_{IN} becomes large, the residue signal of stage-1 spans across all three subranges, causing jumps at the sub-range transitions (due to gain error) and degraded linearity. However, when V_{IN} becomes even larger, these errors become relatively small, thus leading to improved linearity (i.e., SFDR and THD).

Excluding off-chip references, the ADC dissipates 9 mW: 2.8 mW analog power and 6.2 mW clock power. It should be noted that the ADC is based on [16] and modified to accommodate the proposed class-AB residue amplifier. Consequently, the reused clock generation, originally intended for operation at 1 GS/s [16], dissipates a relatively large amount of power. However, the proposed residue amplifiers dissipate only 0.83 mW, which is 30% of the analog power and 9% of the overall ADC power.

Table 4.1 gives the performance summary and a comparison with similar pipelined ADCs at the time of publication. Compared to [5], [14], [16], [29], the proposed design requires the least number of calibration clock cycles. This is because of the split-ADC technique and the fact that no nonlinearity correction is required. Mainly due to the high clock power, the ADC's overall power efficiency is only in line with the state-of-the-art. However, the proposed residue amplifier results in a significant reduction in its analog power. Compared to [16], which describes a similar ADC with a different residue amplifier, this work improves the analog power efficiency by 4×.

As might be expected, subsequent pipeline ADCs have achieved even better power efficiency [31]–[39]. Sometimes by employing even more efficient ResAmps, such as open-loop dynamic amplifiers. For instance, [31] reports a pipelined ADC with linearized dynamic amplifiers that achieves nearly 2× better power efficiency than the current design.

However, it is also fair to say that recent improvements in ADC power efficiency are also due to architectural level optimizations [33]–[39]. This includes favoring the use of power-efficient SAR-based architectures over conventional flash-based ones. The speed increase afforded by nanoscale CMOS technologies has also facilitated this change to a certain

Table 4.1: Performance summary and comparison table.

	Kim JSSC [5]	Oh JSSC [8]	Shin JSSC [9]	Boo JSSC [11]	Panigada JSSC [14]	Sehgal JSSC [16]	Miyahara JSSC [29]	This work
Technology	90nm	0.13µm	55nm	65nm	90nm	40nm	0.18µm	40nm
Number of calibration cycles	22×10^3	-	-	-	2×10^9	70×10^3	32×10^3	12×10^3
Clock frequency F_S (MS/s)	30	70	200	250	100	195	60	53
Supply voltage (V)	1.2	1.3	1.1	1.2	1.2 / 1	1	1.6	1
SNDR at Nyquist (dB)	64.5	65.2	63.2	65.7	68.8	64.8	73.3	66
Total power (mW) ➢ FoM at Nyquist (dB)	2.95 161.6	6.38 162.6	30.7 158.3	49.7 159.7	130 154.7	53 157.5	67.8 159.7	9 160.7
Clock power (mW) ➢ Clock power/Total power	0.54 18%	1.02 16%	-	7.2 14%	20 15%	18 34%	18 26%	6.2 69%
Analog power (mW) ➢ FoM at Nyquist (dB)	2.09 163.1	5.36 163.3	-	42.5 160.4	93 156.1	35 159.3	39 162.2	2.8 165.8

FoM = SNDR + 10 $\log_{10}$ (Bandwidth / Power)

extent. Moreover, employing fewer pipelined stages (hence fewer ResAmps) by resolving a higher number of bits per stage has gained popularity due to its power and area benefits. This is reflected by the numerous two-stage pipelined SAR ADC publications that have advanced the state-of-the-art [33]–[39]. A recent example of this is reported in [39], which describes a two-stage SAR-assisted Pipelined ADC with a dynamic ResAmp that achieves a 179.6dB Schreier FoM. It is interesting to note that while both [31] and [39] use dynamic ResAmps, [39] achieves 34× better power efficiency than [31], mainly due to architectural level enhancements. These architectural optimizations can be combined with the proposed ResAmps of this thesis to further improve ADC performance.

4.6 Conclusion

The proof-of-concept pipelined split-ADC, fabricated in 40-nm CMOS, utilizes four main techniques to achieve both excellent analog power efficiency and negligible calibration power.

1) A class-AB residue amplifier with a split-capacitor biasing technique is proposed. It enables independent biasing of the NMOS and PMOS transistors, eliminating additional level-shifting capacitors as well as their power penalty.

2) Linearity is ensured by biasing the amplifier's transistors in the strong-inversion saturation region and applying some feedback.
3) Incomplete settling is used to improve the amplifier's power efficiency.
4) Amplifier gain error is corrected by tuning its bias current, thus significantly reducing the calibration power.

The ADC achieves an SNDR and SFDR of 66 dB and 77.3 dB, respectively, with a near-Nyquist input signal at a 53 MS/s clock speed. It dissipates 9-mW power, of which the residue amplifiers consume only 0.83 mW.

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5

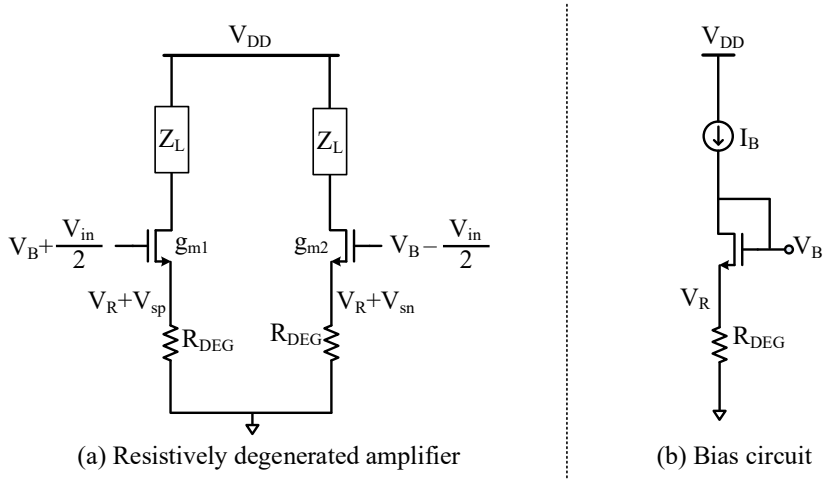
Implementation II – A Resistively Degenerated Open-Loop Amplifier

5.1 Introduction

Recent analog-to-digital converters (ADCs) are collectively moving towards the use of simpler and more power-efficient residue amplifier topologies [1]–[6]. Open-loop amplifiers or integrators [2]–[3] exhibit optimal power efficiency for a given noise performance but are more nonlinear, thus requiring analog [4]–[6] or digital [7]–[8] nonlinearity correction as discussed in Chapter 2.

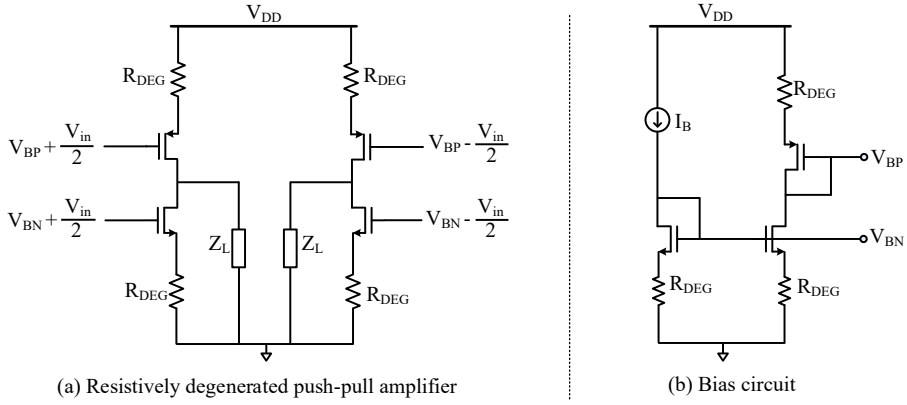
This chapter describes an analog linearization technique for open-loop amplifiers. As discussed in Section 3.4, it uses resistive degeneration and relies on the exponential voltage to current (*V–I*) characteristics of transistors. Hence, it is viable for both MOSFETs in weak-inversion and BJTs. This technique was first introduced some two decades ago [9], when it was shown that a bipolar transistor could be linearized by mildly degenerating it with a resistor. However, the usefulness of this technique was limited by its sensitivity to PVT spread. Nowadays, this drawback can be mitigated by the use of calibration techniques.

This chapter is based on the following publication by the authors M. S. Akter, R. Sehgal and K. Bult, "A Resistive Degeneration Technique for Linearizing Open-Loop Amplifiers," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 11, pp. 2322-2326, Nov. 2020.



(a) Resistively degenerated amplifier (b) Bias circuit

Figure 5.1: (a) Resistively degenerated amplifier with an NMOS differential pair and its (b) bias circuit.



(a) Resistively degenerated push-pull amplifier (b) Bias circuit

Figure 5.2: (a) Resistively degenerated push-pull amplifier and its (b) bias circuit.

In this chapter, the combination of foreground nonlinearity detection and resistive degenerated linearization (RDL) in a differential amplifier will be discussed. The accuracy of the nonlinearity correction is tuned by simply adjusting the amplifier's bias current. To experimentally validate the RDL technique, a prototype amplifier was constructed on a stripboard. It achieves a measured HD3 of –105dB with a 50m$V_{pp\text{-}diff}$ input signal, which corresponds well with the theoretical predictions shown in Figure 3.22.

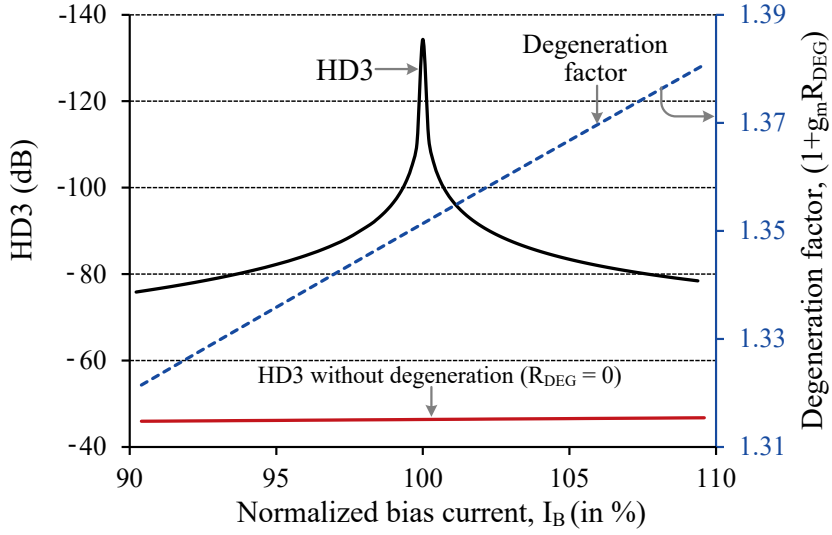


Figure 5.3: Simulated nonlinearity and degeneration factor ($1+g_mR_{DEG}$) of the PDD amplifier as a function of its bias current I_B, for $70mV_{p\text{-}p,diff}$ input signal.

5.2 Amplifier Design

The proposed RDL technique can be used in various amplifier topologies. Figure 5.1(a) shows a resistively degenerated amplifier identical to that in Figure 3.8(a), which is based on an NMOS differential pair. Figure 5.1(b) shows the amplifier's bias circuit, where I_B is the bias current. R_{DEG} is the degeneration resistor, and Z_L is the load impedance, which can either be a resistor or a switched capacitor for continuous- or discrete-time operation, respectively. Note that the amplifier can employ both NMOS and PMOS differential pairs to double its effective transconductance, as shown in Figure 5.2.

Figure 5.3 shows the simulated amplifier nonlinearity versus its bias current I_B for a $70mV_{pp\text{-}diff}$ input signal. The figure shows the input (or g_m) nonlinearity and ignores the effect of the amplifier's signal-dependent output impedance. According to Equation (3.30), the amplifier should exhibit optimal third-order nonlinearity if it is degenerated by 1.35× (i.e. $1+g_mR_{DEG} = 1.35$). This can be validated by plotting the amplifier's degeneration factor ($1+g_mR_{DEG}$) versus its bias current I_B (on the right-hand y-axis of Figure 5.3). As can be seen, the amplifier exhibits an HD3 of better than –100dB when the degeneration factor is

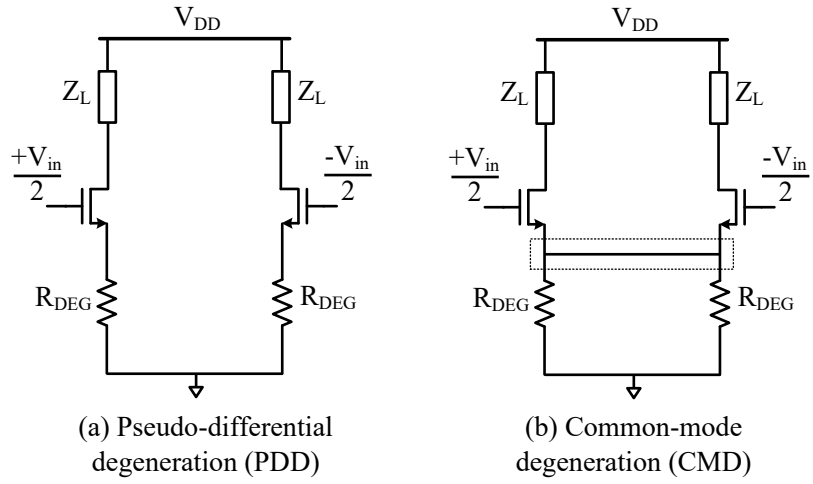


Figure 5.4: Amplifiers with (a) both differential and common-mode degeneration and (b) only common-mode degeneration.

around 1.35, which agrees with the calculated value. Furthermore, it achieves more than 75dB linearity even as the bias current varies by ±10%, corresponding to a 30dB improvement in linearity compared to a grounded differential pair ($R_{DEG} = 0$) in weak-inversion, as can be seen from Figure 3.22 and Figure 5.3.

It should be noted that the presented RDL technique differs considerably from traditional resistive degeneration [10]–[11]. In the latter, linearity is improved by employing a large degeneration factor ($1+g_mR_{DEG}$), which reduces the amplifier's efficiency (or g_m). However, the RDL technique practically eliminates this trade-off between linearity and power efficiency. It allows the amplifier to achieve high linearity (>80dB) with a small degeneration factor ($1+g_mR_{DEG} = 1.35$), thus requiring only 35% extra power. In comparison, it can be shown that a similar amplifier with traditional degeneration would require an approximately 4× larger degeneration factor ($1+g_mR_{DEG}$) to achieve 80dB linearity. In other words, the RDL technique improves amplifier power efficiency by approximately 4× compared to traditional degeneration.

In both Figure 5.1(a) and Figure 5.2(a), the amplifiers are degenerated in a pseudo-differential manner, causing both the common-mode (CM) and differential-mode (DM) signals to experience the same degeneration. We can also choose to degenerate only the

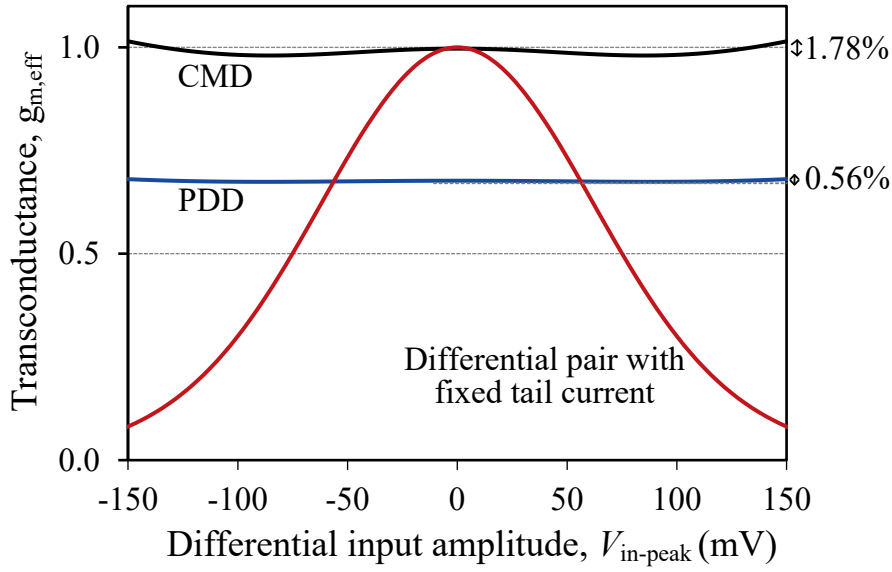


Figure 5.5: Simulated transconductance versus input signal of the PDD and CMD amplifiers along with that of a conventional differential pair with a fixed tail current source.

common-mode signal by connecting the source nodes of the input transistors. Figure 5.4 shows amplifiers with both (a) pseudo-differential degeneration (PDD) and (b) common-mode degeneration (CMD). The advantage of the CMD topology is that it does not reduce g_m, thus requiring about 35% less power than the PDD topology. However, it exhibits ~10dB worse linearity than PDD, as can be shown with simulations.

Figure 5.5 shows the simulated transconductance $g_{m,eff}$ versus input signal for the PDD and CMD amplifiers along with that of a conventional differential pair with a fixed tail current source (Figure 3.2). As can be observed, both the PDD and CMD amplifiers exhibit significantly less g_m variation than the conventional differential pair. Although the PDD amplifier's $g_{m,eff}$ is reduced by 35%, it varies 3× (or ~10dB) less than the CMD amplifier.

Similar to other pseudo-differential amplifiers [6], [12]–[14], the proposed amplifiers exhibit low common-mode rejection (0dB for PDD and 2.6dB for CMD). To mitigate this, techniques such as differential sampling [13] or a dedicated common-mode control loop [6], [12], [14], [15] can be implemented to suppress common-mode signals.

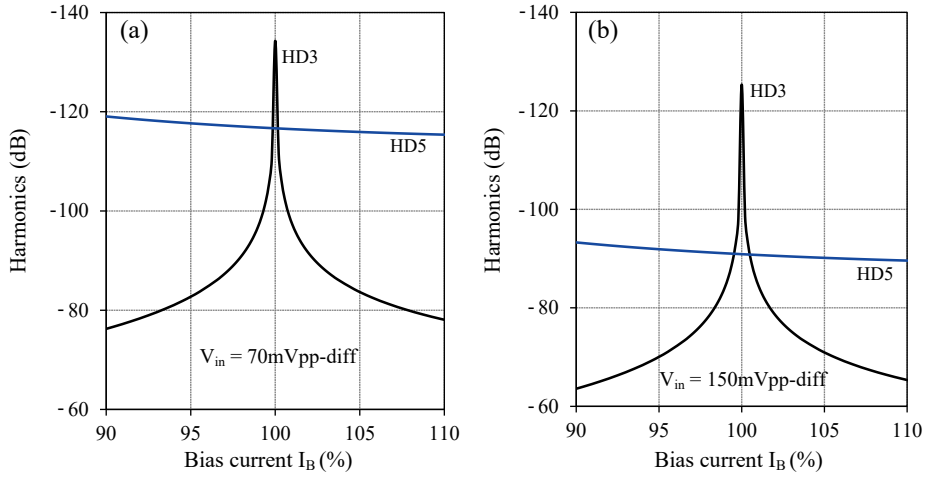


Figure 5.6: Simulated nonlinearities of the amplifier versus its bias current (in percentage) for (a) $70mV_{p\text{-}p,diff}$ and (b) $150mV_{p\text{-}p,diff}$ input signals.

5.3 Design Considerations

This section addresses various design aspects of the resistively degenerated linearization (RDL) technique. In the following discussions, an amplifier with pseudo-differential degeneration (Figure 5.1) is considered.

5.3.1 Dependence on Bias Current

We have seen in Section 3.4 that the amplifier exhibits optimal linearity when the following condition, as shown in (3.29), is met:

$$V_R = I_B R_{\mathrm{DEG}} \approx 0.5 U_T \tag{5.1}$$

The bias current I_B of the amplifier can be programmed to ensure this condition. The optimal bias current $I_{B,\mathrm{opt}}$ is given by:

$$I_{B,\mathrm{opt}} \approx \frac{0.5 U_T}{R_{\mathrm{DEG}}} \tag{5.2}$$

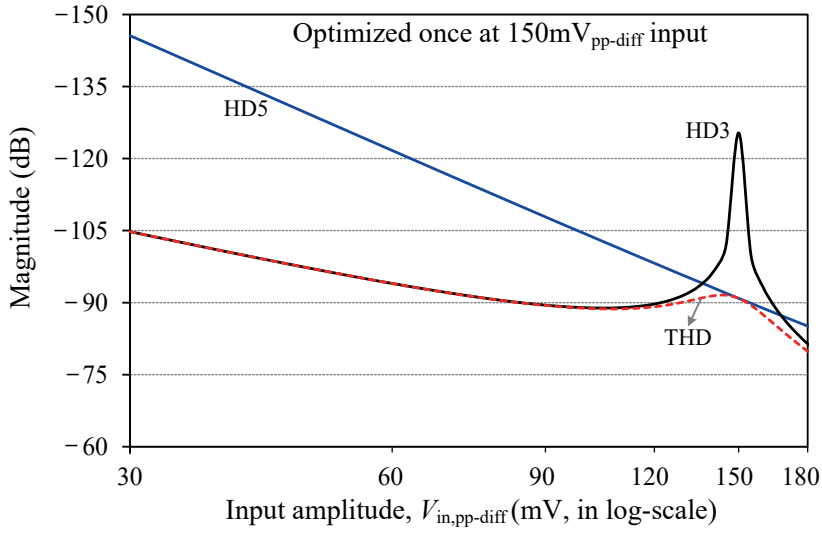


Figure 5.7: Simulated harmonic distortions of the amplifier as its input signal amplitude is varied.

The linearity of the amplifier will drop if its bias current I_B deviates from $I_{B,opt}$. Figure 5.6 shows the simulated nonlinearity versus bias current I_B for two different input amplitudes, 70mV$_{pp-diff}$ and 150mV$_{pp-diff.}$ For the 70mV$_{pp-diff}$ input (Figure 5.6(a)), the amplifier achieves an optimal HD3 of better than –100dB. Moreover, it maintains an HD3 of at least –75dB even though the bias current I_B varies by ±10%. When the input amplitude is increased to 150mV$_{pp-diff}$ (Figure 5.6(b)), both the optimal linearity and its tolerance to bias current inaccuracy decrease as expected. Nevertheless, the amplifier exhibits at least –64dB of HD3 with ±10% variation in the bias current.

5.3.2 Dependence on Signal Amplitude

It is important to confirm that the RDL technique is not limited to a specific input signal amplitude. To validate this, the amplifier's nonlinearity is simulated across an input amplitude range of 30-180mV$_{pp-diff}$, as shown in Figure 5.7. The amplifier is calibrated once during this sweep, for a 150mV$_{pp-diff}$ input signal. For smaller input amplitudes, the amplifier exhibits at least –89dB of HD3 or THD, confirming that the RDL technique can be used for a broad amplitude range. When the input amplitude exceeds 150mV$_{pp-diff}$, the amplifier's linearity gradually degrades, as expected.

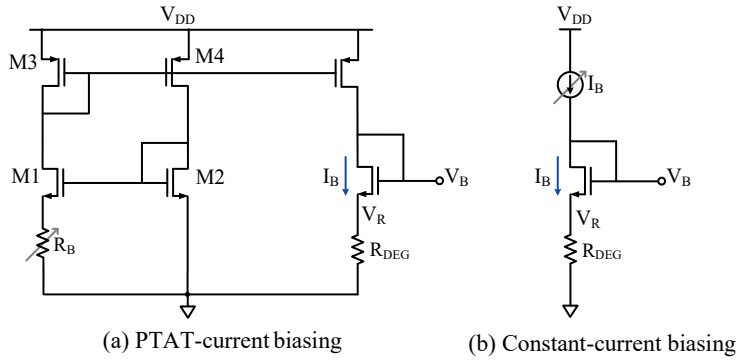


Figure 5.8: Biasing circuits of the amplifier: (a) PTAT-current and (b) constant-current biasing.

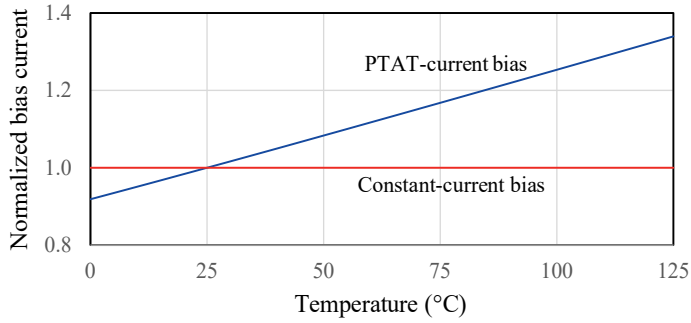


Figure 5.9: Normalized currents of PTAT- and constant-current bias circuit over a temperature range of 0°C to 125°C.

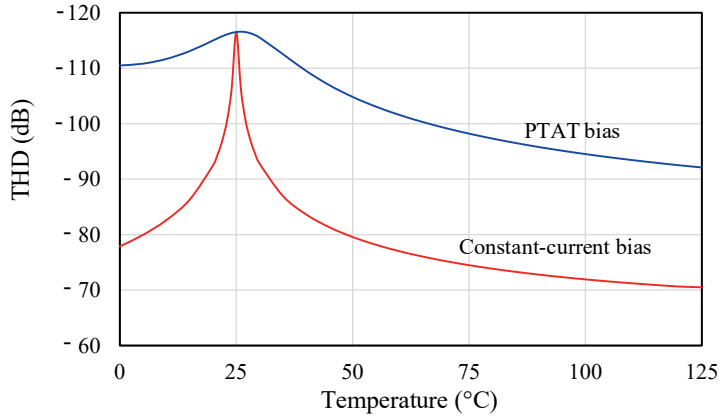


Figure 5.10: Simulated nonlinearity with temperature variation when using a constant-current or a PTAT-current biasing circuit.

5.3.3 Temperature Dependence

It is evident from (5.2) that the optimal linearity condition depends strongly on temperature. Hence, in order to reduce the influence of temperature on linearity, the bias current I_B needs to be proportional to temperature. This can be realized by using proportional to absolute temperature (PTAT) current biasing [15]–[19].

A PTAT current source based on MOS transistors is shown in Figure 5.8(a). The MOS transistors M1 and M2 operate in the weak-inversion region, with M1 having a larger aspect ratio (W/L) than M2. The transistors M3 and M4 are of equal size and act as a current mirror. They can be biased either in the strong-inversion or in the weak-inversion region.

The nonlinearity of the amplifier is simulated over a temperature range of 0°C to 125°C, with an input signal amplitude of $70\text{mV}_{\text{pp-diff}}$. For this test, the amplifier is calibrated once at room temperature (25°C). For comparison, the amplifier is also simulated with a constant-current bias circuit, as shown in Figure 5.8(b). The normalized current profiles versus temperature for both of these bias circuits are shown in Figure 5.9. Figure 5.10 depicts the resulting harmonics and THD of the amplifier with temperature variations. When a constant-current is used to bias the amplifier, the voltage drop V_R across the R_{DEG} resistor is fixed. It does not change with temperature according to (5.1), degrading the linearity. Thus, the amplifier exhibits a worst-case HD3 or THD of –70dB when the temperature increases to 125°C (Figure 5.10). When a PTAT-current bias is used instead, the voltage drop V_R increases linearly with temperature, thus improving the linearity by more than 20dB compared to the constant-current bias. As a result, the amplifier exhibits an HD3 or THD of at least -93dB over the entire temperature range.

5.3.4 Mismatch

The proposed linearization technique can only improve the odd-order distortion components of the amplifier (Section 3.5.2.2). However, any mismatch between the differential circuit components will give rise to even-order harmonics, which the RDL technique cannot correct. Simulations show that with a ±10% β_n mismatch, the amplifier exhibits better than -75dB THD for $100\text{mV}_{\text{pp-diff}}$ input signal. Note that $\beta_n = \mu_n C_{\text{ox}}(W/L)$, as shown in (3.2). With careful layout, however, 1% mismatch can be readily achieved in deep-submicron technologies. Furthermore, offset calibration [5]–[6] can be used to

improve linearity by mitigating the second-order harmonic distortion, noting that the higher even-order components will generally be much smaller.

5.3.5 Biasing and Signal Swing

The proposed linearization principle relies on the weak-inversion operation of MOS transistors. If the input signal swing is too large with respect to its biasing voltage ($V_{GS} - V_{th}$), it can drive the input transistors towards the moderate- and eventually strong-inversion saturation region. At that point, the V–I transfer will no longer be exponential, and the linearization principle will not be effective. Hence, the amplifier needs to be designed so that it remains in weak-inversion with the maximum input signal.

5.3.6 Adjusting the Transconductance

The transconductance (g_m) of the amplifier can be adjusted by tuning its biasing current. However, to maintain optimal linearity, the degeneration resistance R_{DEG} also needs to be adjusted according to (5.1). This can be achieved by making R_{DEG} programmable by placing, for instance, multiple resistors in series with parallel switches to ground. Alternatively, a MOS transistor in the triode region can be used to implement a voltage-controlled tunable resistor R_{DEG}.

5.3.7 Effect of Output Impedance

As shown in Figure 5.3 and Equation (3.30), the amplifier exhibits optimal third-order nonlinearity when it is degenerated by about 1.35× (i.e. $1+g_m R_{DEG} = 1.35$). This assumes that the nonlinearity is predominantly caused by the input g_m. However, for large output signals, the amplifier's output impedance varies with the signal amplitude, typically resulting in a compressing nonlinearity. Thus, an expanding nonlinearity from the input g_m is required to mitigate this effect. The amplifier, therefore, achieves optimal linearity with a somewhat smaller degeneration. Note that this would cause the circuit's linearity to be more susceptive to supply variations, which can be relaxed by backing off the signal swing without losing much SNR.

5.3.8 Noise Performance

In traditional degeneration, the amplifier's transconductance $g_{m,\text{eff}}$ and noise are predominantly dictated by the degeneration resistance R_{DEG}. This is because R_{DEG} is significantly larger than the $1/g_m$ of the MOS transistor. However, for the RDL technique, the R_{DEG} resistor only amounts to about one-third of the transistor's $1/g_m$. Thus, both the transistor and the degeneration resistor contribute to the noise. As for the transistor, its input-referred noise power density can be approximated as follows, assuming $\gamma = 1$ and ignoring the flicker noise component:

$$V_{n,\text{gm}}^2(f) = 4kT(1/g_m) \tag{5.3}$$

The input-referred noise contribution from the degeneration resistor is given by:

$$V_{n,\text{Rdeg}}^2(f) = 4kTR_{\text{DEG}} \tag{5.4}$$

The total input-referred noise power density can be obtained by summing (5.3) and (5.4) as follows:

$$\begin{aligned} V_{n,\text{tot}}^2(f) &= 4kT(1/g_m + R_{\text{DEG}}) \\ &= 4kT\left(\frac{1+ g_m R_{\text{DEG}}}{g_m}\right) \\ &= 4kT\left(\frac{1}{g_{m,\text{eff}}}\right) \end{aligned} \tag{5.5}$$

Equation (5.5) shows that the total noise power density of a resistively degenerated amplifier is similar to that of a non-degenerated amplifier (Equation (5.3)). The difference being that the intrinsic g_m of the transistor is replaced by the effective transconductance $g_{m,\text{eff}}$ of the degenerated amplifier. Since $(1+g_m R_{\text{DEG}}) \approx 1.35$ for the RDL technique, the transconductance $g_{m,\text{eff}}$ is reduced by 1.35× compared to that of a non-degenerated amplifier for the same power dissipation. However, if the transconductance of the degenerated amplifier is made equal to that of the non-degenerated amplifier (by increasing I_B and reducing R_{DEG} by 1.35×), then both will exhibit the same noise power density. Hence, the cost of the RDL technique is 1.35× extra power. However, degeneration will reduce the transistor's flicker noise contribution.

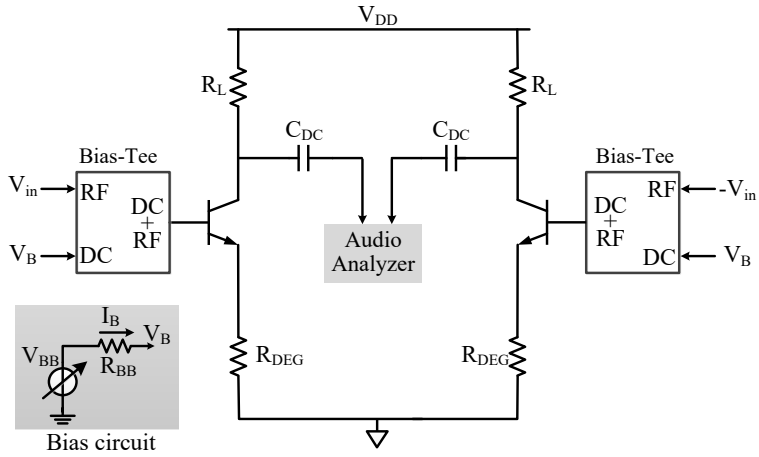


Figure 5.11: Test structure to verify the proposed linearization technique.

5.4 Implementation Details

5.4.1 Test Structure

Figure 5.11 shows the test setup used to demonstrate the proposed linearization technique. As a proof-of-concept, the pseudo-differential amplifier of Figure 5.4(a) was implemented with discrete BJTs, degeneration resistors R_{DEG}, and load resistors R_L on a stripboard. The bias circuit comprises of a voltage source V_{BB} in series with a high ohmic resistor to bias the base of the transistors. A bias-tee is used to combine the bias voltage V_B and the input signal V_{in}. To optimize the linearity, the bias voltage V_{BB} is adjusted, which tunes the amplifier's bias current I_B and base voltage V_B.

Since the amplifier under test can achieve high linearity (<−100dB), measuring it with spectrum analyzers is quite challenging. This is because most cannot support measurements over a 100dB dynamic range. Also, most use 50Ω input termination, which is difficult to drive without an additional buffer. Hence, an audio analyzer (APx555) with a dynamic range of over 120dB was used to measure the nonlinearity of the amplifier. Unlike typical spectrum analyzers, its inputs employ 100kΩ termination rather than 50Ω termination, making it relatively easy to drive without incurring much signal attenuation. The drawback, however, is the limited range of input frequencies that can be measured.

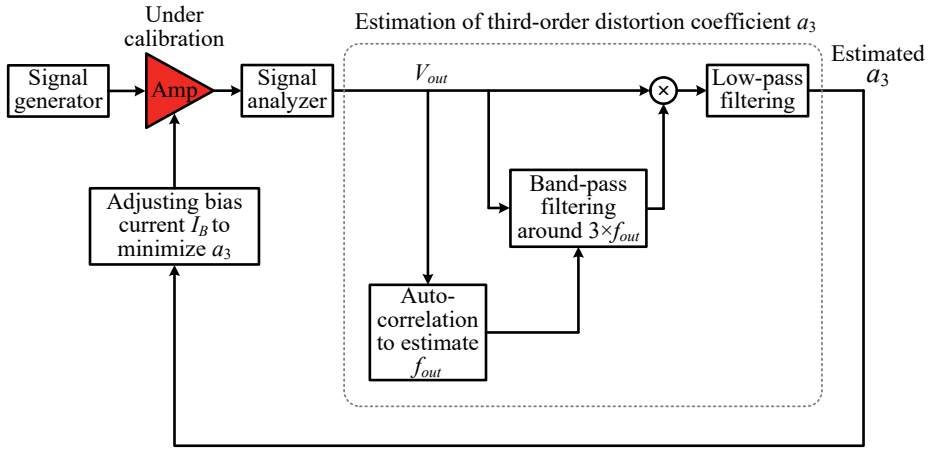


Figure 5.12: Foreground calibration scheme to detect the third-order distortion coefficient a_3 of the amplifier.

5.4.2 Nonlinearity Calibration

It should be noted that there are two ways of using the proposed RDL technique: either with or without calibration. Without calibration, the amplifier can still achieve –76dB HD3 for a 70mV$_{pp\text{-}diff}$ input signal as long as the product $I_B \times R_{DEG}$ can be maintained within ±10% accuracy (Figure 5.3). Here a calibration method will be discussed to achieve even lower distortion by mitigating the effect of process variation, mismatch, and any parasitic resistance in series with R_{DEG}.

In this design, a foreground detection scheme is used (Figure 5.12) to estimate the third-order distortion coefficient a_3 of the amplifier. The detection is done off-chip in Matlab. First, the amplifier output signal V_{out} from the audio analyzer is processed to detect its fundamental frequency f_{out}. This is done by using the autocorrelation method, i.e. correlating V_{out} with its shifted copy, as shown in [20]. Next, the output signal V_{out} is band-pass filtered around $3\times f_{out}$ and subsequently multiplied with the V_{out} signal. The resulting signal is then low-pass filtered to estimate the a_3 coefficient. Once the nonlinearity is detected, the amplifier's bias current I_B is tuned so that a_3 is minimized. Note that if the amplifier is part of an ADC (e.g., a residue amplifier), then background calibration [6]–[8] can be used to track a_3 over PVT. It can also calibrate the gain either digitally or by adjusting the load resistor R_L.

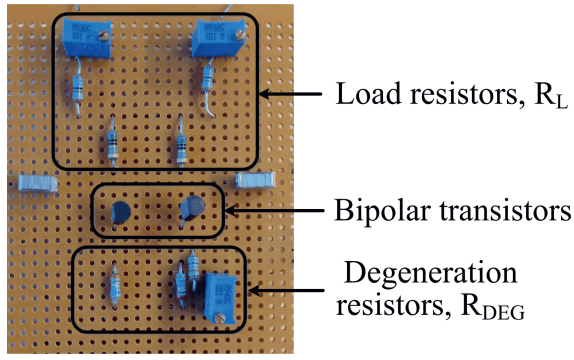


Figure 5.13: Picture of the implemented circuit.

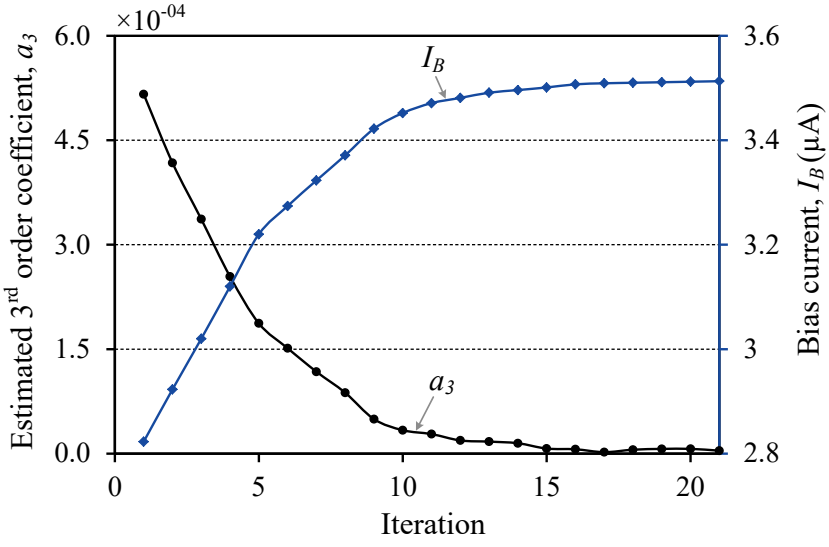


Figure 5.14: Convergence of a_3 coefficient and bias current I_B.

5.5 Measurement Results

The prototype amplifier of Figure 5.11 was implemented on a stripboard using discrete BJTs and resistors, as shown in Figure 5.13. An input signal frequency of 73KHz was used for measurements. Note that the audio analyzer (APx555) that was used can measure up to 1MHz frequency. Unless otherwise stated, all measurements were performed with a $50mV_{pp\text{-}diff}$ input signal and around $200mV_{pp\text{-}diff}$ output signal (gain ≈ 4).

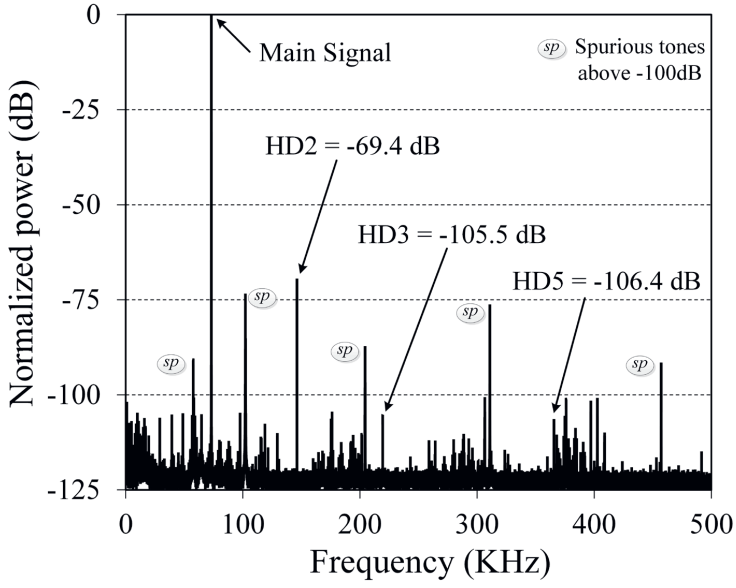


Figure 5.15: Measured output spectrum of the amplifier with a 50mV$_{pp\text{-}diff}$ input signal and ~4× gain.

Figure 5.14 shows the convergence of the measured third-order distortion coefficient a_3 of the amplifier along with its bias current I_B. First, the a_3 coefficient was detected in MATLAB using the foreground calibration scheme discussed in Section 5.4.2. Subsequently, the bias voltage V_{BB} (Figure 5.11) was tuned to adjust I_B such that a_3 was minimized. The measured output spectrum after the nonlinearity calibration is shown in Figure 5.15. The amplifier exhibits an excellent HD3 of –105dB. However, the HD2 component is still relatively high (–69.4dB) due to the mismatch between the discrete BJTs, which was not calibrated in this work. In an on-chip implementation, much better matching can be achieved, and thus HD2 can be reduced significantly. Note that the spurious tones above –100dB, indicated in Figure 5.15, are not coming from the circuit but rather from the measurement set-up.

Figure 5.16 shows the measured amplitude sweep when the amplifier was optimized once with a 50mV$_{pp\text{-}diff}$ input signal. Over the input amplitude range of 25-70mV$_{pp\text{-}diff}$, it exhibits better than –80dB HD3 without any re-calibration. The measured nonlinearity of the amplifier with bias current I_B variation is shown in Figure 5.17. For this measurement, two

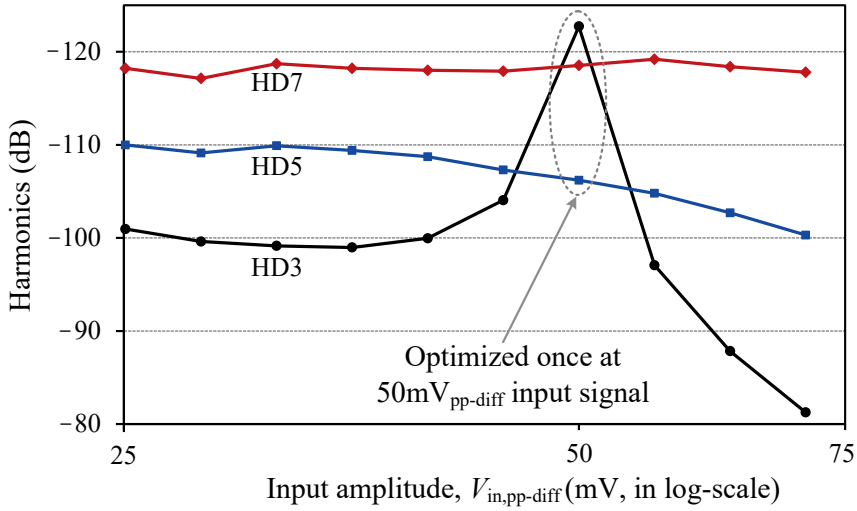


Figure 5.16: Harmonic distortions of the amplifier as a function of its input signal amplitude when calibrated once at a $50mV_{pp\text{-}diff}$ input amplitude.

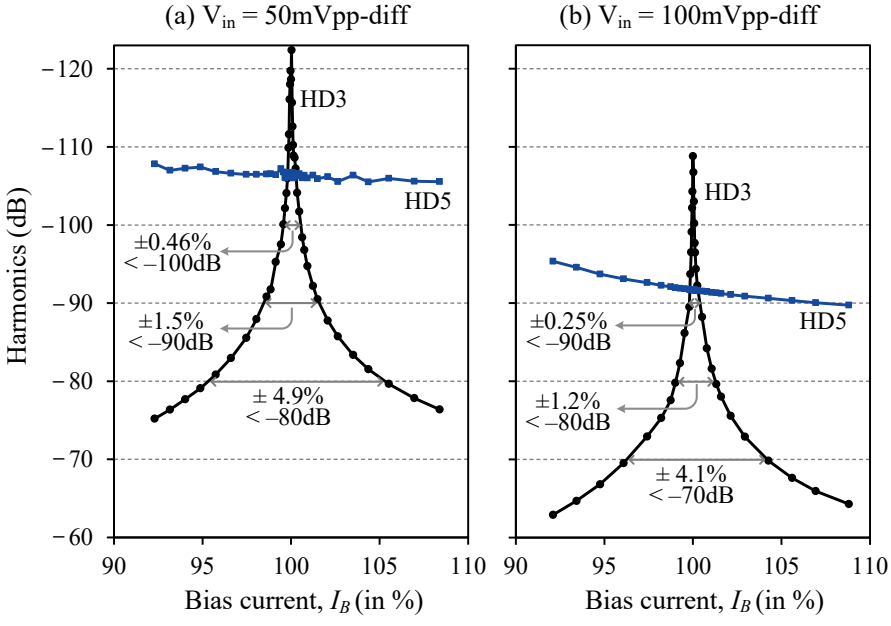


Figure 5.17: Measured harmonics of the amplifier with bias current variation for (a) $50mV_{pp\text{-}diff}$ and (b) $100mV_{pp\text{-}diff}$ input signals.

different input signal amplitudes were used: (i) $50mV_{pp\text{-}diff}$ and (ii) $100mV_{pp\text{-}diff}$. The amplifier demonstrates an optimal HD3 of better than –100dB and –90dB for $50mV_{pp\text{-}diff}$ and $100mV_{pp\text{-}diff}$ input signals, respectively. This linearity performance is similar to that reported in [5]–[6], [15] but significantly better than other state-of-the-art open-loop amplifiers [2]–[4]. The proposed amplifier also exhibits a wide linear range and maintains a –80dB HD3 even when the bias current I_B deviates from the optimum value by ±4.9% for $V_{in} = 50mV_{pp\text{-}diff}$, or ±1.2% for $V_{in} = 100mV_{pp\text{-}diff}$.

It is noteworthy to state that the presented RDL technique is reported in [15] with a MOSFET-based chip implementation. It uses a push-pull CMD amplifier, achieving 40× better linearity than a conventional differential pair. It also employs a PTAT bias circuit to maintain high linearity over process and temperature variations.

5.6 Conclusion

This chapter describes a power-efficient linearization technique for open-loop amplifiers [9]. It employs weak degeneration to counteract the expanding nonlinearity arising from the exponential *V*–*I* characteristic of a transistor. Based on this technique, a power-efficient amplifier topology is presented that leverages calibration to achieve excellent linearity. The prototype amplifier was implemented on a stripboard to validate the proposed linearization technique. It exhibits a measured HD3 of –105dB with a $50mV_{pp\text{-}diff}$ input signal. Due to the relatively simple nature of resistive degeneration, this technique is suitable for both continuous- and discrete-time amplifiers. It can be used together with a digital error detection loop to achieve accurate linearization over PVT.

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6

Implementation III– A Capacitively Degenerated Amplifier with a Floating Supply

6.1 Introduction

This chapter presents the design and performance of a switched-capacitor amplifier for discrete-time systems. It embodies two novel circuit techniques: (i) the capacitively degenerated linearization (CDL) technique (Section 3.5) and (ii) the floating supply technique. The CDL technique ensures excellent linearity in open-loop amplifiers [1]–[9], thus making them attractive for wide dynamic range applications [10]–[13]. It presents a viable alternative to traditional closed-loop amplifiers [14]–[18], which sacrifice power-efficiency to achieve high linearity. Next, the proposed amplifier employs a floating supply technique that uses a switched-capacitor circuit as the amplifier's local supply. This technique significantly improves the amplifier's common-mode rejection and eliminates any additional CMFB circuits, thus saving power and area. Moreover, the proposed amplifier

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This chapter is based on the journal publication by the authors: M. S. Akter, K. A. A. Makinwa and K. Bult, "A Capacitively Degenerated 100-dB Linear 20–150 MS/s Dynamic Amplifier," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1115-1126, April 2018.

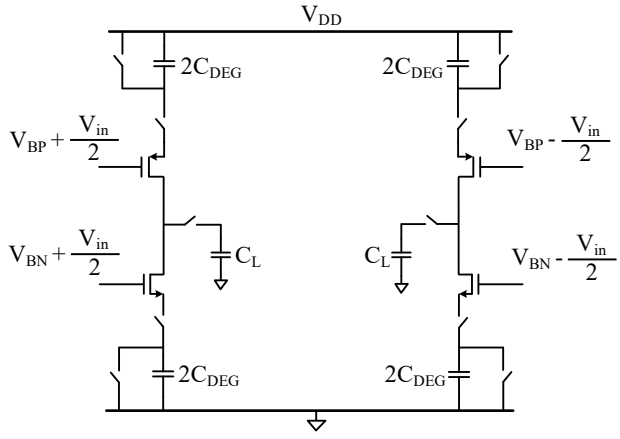

Figure 6.1: Push-pull dynamic amplifier using capacitive degeneration.

uses a simple analog control knob to minimize nonlinearity, thus reducing the calibration power overhead [1], [4], [19]–[22].

The proof-of-concept amplifier was fabricated in a 28 nm CMOS process. With 4× gain and a 100m$V_{pp\text{-}diff}$ input signal, it achieves −100dB THD. It dissipates 87µW of power at a clock speed of 43MS/s, thereby improving the energy per cycle by 10× compared to that of state-of-the-art high-linearity amplifiers [16]–[18], [20], [23].

6.2 Amplifier Design

6.2.1 Pseudo-Differential Dynamic Amplifier

Figure 3.14 illustrates the principle of capacitive degeneration by using a dynamic amplifier that consists of an NMOS differential pair. We can reuse the current to double the amplifier's transconductance by employing both NMOS and PMOS differential pairs (Figure 6.1). However, both these amplifiers are pseudo-differential, thus exhibit equal common-mode (CM) and differential-mode (DM) gain. In other words, they have no common-mode rejection capability. When used in a pipelined ADC, any CM signals will be amplified while propagating through the pipelined stages, which may overload the ADC. This drawback can be alleviated by using a floating supply technique as described in the following section.

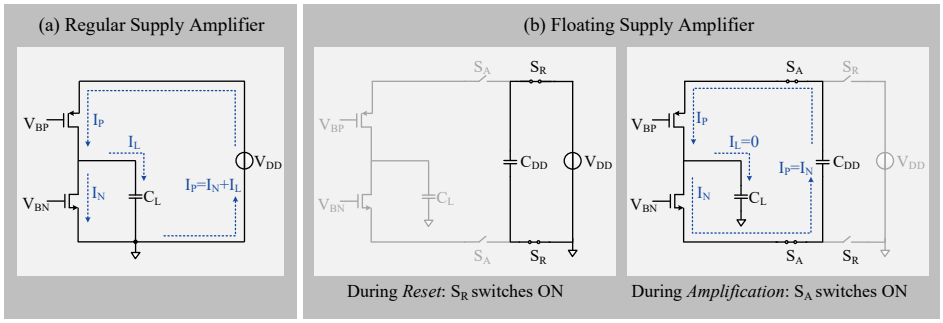

Figure 6.2: Amplifier with a (a) typical supply and (b) floating supply.

6.2.2 Floating Supply Technique

Figure 6.2 illustrates the concept of the floating supply technique with common-mode equivalent circuits. First, let us consider the traditional supply case as shown in Figure 6.2(a). If the PMOS (I_P) and NMOS (I_N) bias currents are unequal, the difference current (I_L) will flow through the load capacitor C_L. Thus, the output bias voltage will change based on the mismatch between I_P and I_N, necessitating a CM control loop. This issue is alleviated in the floating supply amplifier, as shown in Figure 6.2(b). It uses a capacitor C_{DD} as a local supply, which is pre-charged to the supply voltage V_{DD} during reset. During amplification, this C_{DD} capacitor acts as the amplifier's supply; hence, no other circuit components are tied to the ground apart from C_L (ignoring parasitics). This forces the PMOS and NMOS currents to be equal ($I_P = I_N$), resulting in zero CM load current ($I_L = 0$). Hence, the need for a dedicated CMFB circuit is eliminated, and the amplifier exhibits an excellent CM signal rejection capability.

6.2.3 Proposed Differential Amplifier

Figure 6.3 shows the proposed differential amplifier. It combines the floating supply and capacitive linearization techniques (Section 3.5) by employing a cross-coupled capacitor (C_{DEG}) topology. Due to this structure, the C_{DEG} capacitors can serve as both the degeneration element and the floating supply, as will be shown later. Furthermore, since the C_{DEG} capacitors are differentially connected, their overall size is reduced by 4× compared to that used in the pseudo-differential amplifier of Figure 6.1. Figure 6.4 shows the bias circuit of the amplifier. The symbols V_{BN} and V_{BP} represent the bias voltages at the NMOS

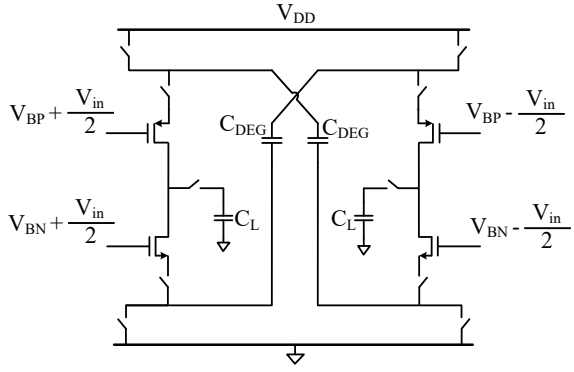

Figure 6.3: Proposed dynamic amplifier topology using a differential cross-coupled capacitors.

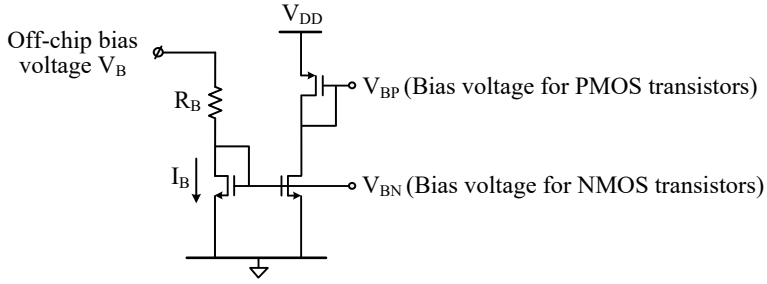

Figure 6.4: Biasing circuit of the proposed dynamic amplifier.

and PMOS gates, respectively. The bias current I_B, which acts as the amplifier's calibration "knob", can be programmed via an off-chip bias voltage V_B. Note that the bias voltages V_{BN} and V_{BP} combine with the input signal through sampling capacitors and switches (not shown in Figure 6.3). These will be shown in the detailed circuit topology in Figure 6.9.

The operating principle of the proposed amplifier is illustrated in Figure 6.5. It operates in two phases: reset and amplification. During the reset phase, the degeneration capacitors C_{DEG} are connected between the supply and ground to pre-charge it (Figure 6.5(a)). At the same time, the load capacitors C_L are reset to their common-mode voltage. Furthermore, the amplifier is switched off by opening the series switches at the NMOS and PMOS sources, thus reducing its power consumption by nearly half. After the reset, the amplifier enters the amplification phase and connects to the cross-coupled C_{DEG} capacitors. During this phase, the amplifier is completely floating with the C_{DEG} capacitors acting simultaneously as a local supply and degeneration capacitors, as shown in Figure 6.5(b).

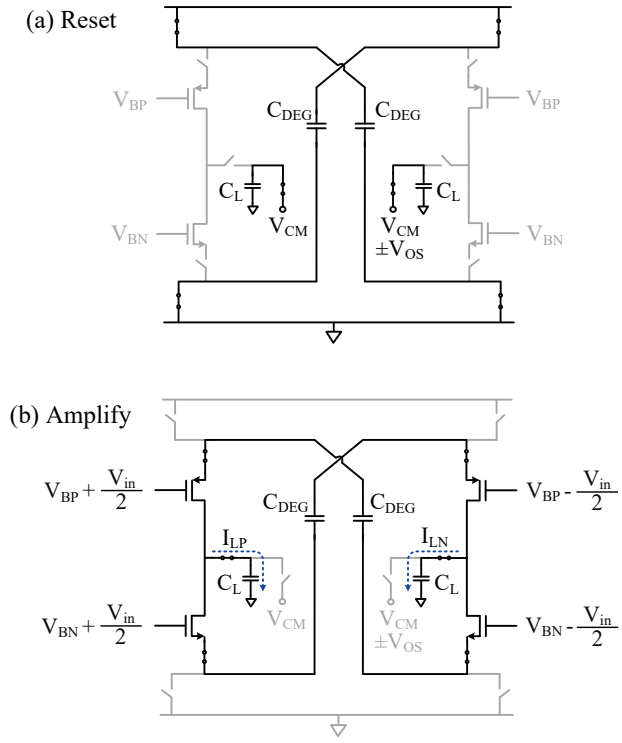

Figure 6.5: Operation of the proposed dynamic amplifier during the (a) reset and (b) amplification phases.

6.3 Design Considerations

6.3.1 Impact on Noise Performance

The impact of the proposed linearization technique on the amplifier's overall noise performance is analyzed in this section, using the half-circuit shown in Figure 3.13. At the end of the reset phase, the noise sampled across the degeneration capacitor C_{DEG} due to the switching action is kT/C_{DEG}. During the amplification phase, this noise on the C_{DEG} capacitor is transferred to the amplifier's output. Note that since the body of the transistor is connected to the ground, the amplifier's gain from the source to the output is n (= weak-inversion slope factor) times larger than that from the gate to the output. Assuming that the amplification period t_{amp} is equal to the optimum linearity time t_{opt}, the output noise power due to switched capacitor C_{DEG} can be expressed as:

$$P_{n,\mathrm{cdeg}} = \left(\frac{kT}{C_{\mathrm{DEG}}}\right) (n{\times}A(t_{\mathrm{opt}}))^2. \tag{6.1}$$

Of course, the amplifier's transistors also contribute noise. Since the amplifier behaves like an integrator, as discussed in Section 3.5.2, its integrated output noise power $P_{n,\mathrm{gm}}$ at the end of the amplification period can be approximated [3] as:

$$P_{n,\mathrm{gm}} = \gamma \left(\frac{2kT}{C_L}\right) A(t_{\mathrm{opt}}), \tag{6.2}$$

where γ is the noise factor of the MOS transistor ($\approx 2/3$). Dividing (6.1) by (6.2) gives:

$$\frac{P_{n,\mathrm{cdeg}}}{P_{n,\mathrm{gm}}} = \left(\frac{n^2 C_L}{2\gamma C_{\mathrm{DEG}}}\right) A(t_{\mathrm{opt}}). \tag{6.3}$$

Using the optimal gain $A(t_{\mathrm{opt}})$ expression of (3.46) in (6.3) results in the following:

$$P_{n,\mathrm{cdeg}} = \left(\frac{n}{4\gamma}\right) P_{n,\mathrm{gm}} \tag{6.4}$$

It can be concluded from (6.4) that the noise power associated with the degeneration capacitor C_{DEG} is approximately two times smaller than the amplifier's inherent noise. In reality, this contribution will be even smaller because there are other noise sources in the circuit such as the input sampling noise (kT/C_S), and the reset noise associated with C_L.

6.3.2 Common-Mode Behavior

The proposed amplifier embodies the floating supply technique (Section 6.2.2) and hence exhibits excellent common-mode rejection capability. This becomes evident by observing that in the amplification phase (Figure 6.5(b)), there is no connection to the supply voltages, i.e., the circuit is completely floating. Only parasitic capacitances between the source nodes and supply or ground can cause a finite CM transfer function. As a result, the amplifier exhibits high CM rejection and does not require a common-mode feedback circuit. This is a significant advantage over most amplifiers [7], [15] and directly leads to power savings as a result.

6.3.3 Calibration "Knob"

The intended goal is to use the proposed amplifier as a residue amplifier in a pipelined ADC. As discussed in Section 3.5.2, the amplifier's output needs to be sampled at a particular time t_{opt} to ensure optimal linearity. This means the amplification time t_{amp} must be equal to the optimal linearity time, i.e., $t_{amp} = t_{opt}$. This condition can be satisfied by adjusting the clock period ($T_S = 1/F_S$) of the ADC since t_{amp} is usually proportional to T_S. However, varying the clock speed could affect other circuits; hence it might not be viable.

Instead of tuning the amplification time t_{amp}, we can adjust the optimal linearity time t_{opt} to ensure that $t_{opt} = t_{amp}$. As can be seen in (3.48), the optimal time t_{opt} is inversely proportional to the bias current I_B. Hence, I_B is used as the calibration "knob" to adjust t_{opt} so that it is equal to t_{amp}. In this implementation, the nonlinearity that occurs when $t_{opt} \neq t_{amp}$ is detected off-chip. In an ADC, this could be detected by processing its digital output using various background techniques [1], [19]–[22]. The presence of nonlinearity indicates that $t_{opt} \neq t_{amp}$, assuming it is primarily caused by the residue amplifier. Subsequently, the bias current is adjusted to ensure $t_{opt} = t_{amp}$ and optimize linearity over PVT.

6.3.4 Mismatch

Symmetry in differential amplifiers is essential to avoid offset and even-order distortion. However, the mismatch between the transistors and capacitors of the two half-circuits will limit this symmetry. The proposed linearization technique only addresses the odd-order distortion components and hence cannot correct for these effects, as discussed in Section 3.5.2. To overcome this problem, an adjustable offset voltage V_{OS} is stored on the load capacitors C_L during the reset phase, as shown earlier in Figure 6.5(a). This offset voltage can tune the MOSFETs' initial drain-to-source voltages and mitigate even-order distortion caused by the mismatch. Note that in an ADC, a background calibration technique [7] for second-order nonlinearity detection can be used to adjust this V_{OS} voltage over PVT.

6.3.5 Effect of Series Resistance

This section explains that the parasitic resistance $R_{S,par}$ in series with the C_{DEG} capacitor has a minor effect on the proposed linearization technique. This $R_{S,par}$ resistance can be a transistor parasitic or an ON-resistance of a series switch. It tends to degenerate the exponential V–I characteristic of MOSFETs, causing its transconductance $g_{m,eff}$ to expand

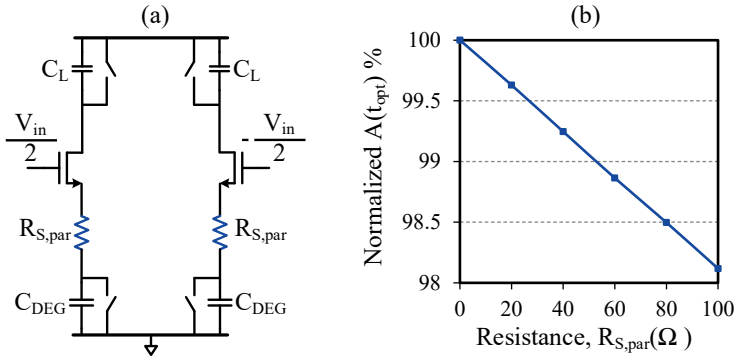

Figure 6.6: Effect of series resistance $R_{S,par}$ on the amplifier's optimum gain $A(t_{opt})$.

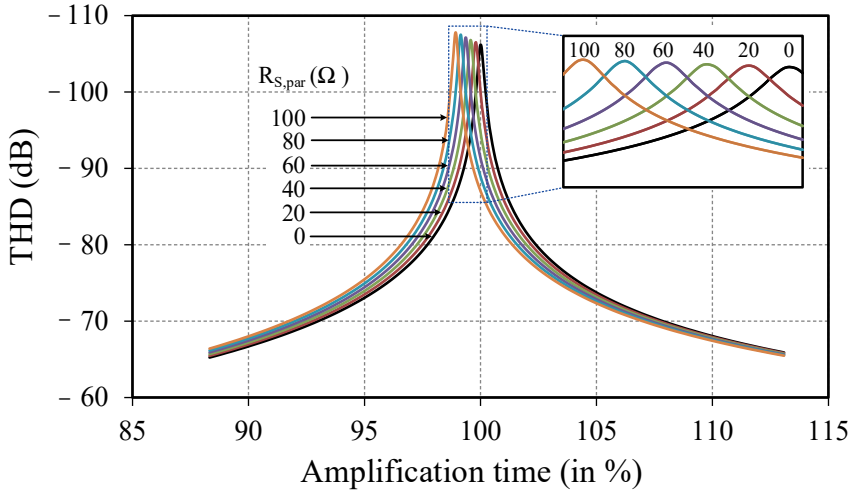

Figure 6.7: Effect of series resistance $R_{S,par}$ on the amplifier's linearity performance.

less with the input signal. We can model this $R_{S,par}$ as a lumped resistance shown in Figure 6.6(a). It is varied from 0 to 100Ω to observe its impact on the amplifier's gain and linearity. The input transistors have a quiescent $g_m \approx 110\mu S$ in this simulation.

As expected, the optimal gain $A(t_{opt})$ of the amplifier is slightly reduced due to the parasitic resistance $R_{S,par}$ (Figure 6.6(b)). This loss of gain can be compensated by increasing the capacitor ratio C_{DEG}/C_L. Figure 6.7 shows the effect of parasitic resistance $R_{S,par}$ on linearity. As can be seen, the optimal THD remains alike for different $R_{S,par}$ values. It is important to note that the parasitic source resistance of MOSFETs is typically not this large.

Furthermore, the series switches of the proposed amplifier in Figure 6.3 operate close to the supply or ground. Hence, they can be designed with a low enough ON-resistance ($R_{S,\text{par}} << 1/g_m$), making their effect negligible.

The above discussion can be extended to include short channel effects like velocity saturation, which can be characterized by a resistor (R_{vsat}) in the source. This R_{vsat} will eventually cause an inherent zero distortion point [24] for the MOSFET even though no external degeneration element is added. However, it is essential to note that the proposed linearization techniques are weak-inversion based with an inversion coefficient [25] below 0.1. Therefore, the effect of velocity saturation is considerably weaker than that observed in the strong-inversion region, as explained in detail in [25]. This means R_{vsat} is significantly smaller than the separately added degeneration impedance, causing only a mild shift in the optimal linearity point and gain (Figure 6.7). Hence, the proposed linearization techniques are less impacted by velocity saturation.

6.3.6 Bias Considerations

The amplifier experiences a large gate-source voltage V_{GS} due to the initial input step at the beginning of integration. If V_{GS} is too large and pushes the device into the strong-inversion regime, then the *V–I* characteristic is no longer exponential, gradually degrading the proposed CDL technique. Note that this V_{GS} voltage decreases during the integration as the source voltage V_S is increased, bringing the amplifier towards the weak-inversion region. However, the moment when the amplifier starts to exhibit an exponential *V–I* characteristic will vary with the signal amplitude because the amplification starts in strong-inversion for large signals and in weak-inversion for small signals. To eliminate this issue, the amplifier must be biased such that it operates in the weak-inversion region for the maximum input signal. If, for example, the input signal range of the amplifier is $100\text{mV}_{\text{pp-diff}}$, then each MOSFET sees a maximum of 25mV peak signal, which it needs to handle while still operating in the weak-inversion saturation region.

6.4 Implementation Details

The proposed amplifier with the CDL technique can achieve excellent linearity (<−100dB THD) at high input frequencies. However, measuring this is quite challenging because any measurement circuitry added to the signal path must itself be more than 100dB

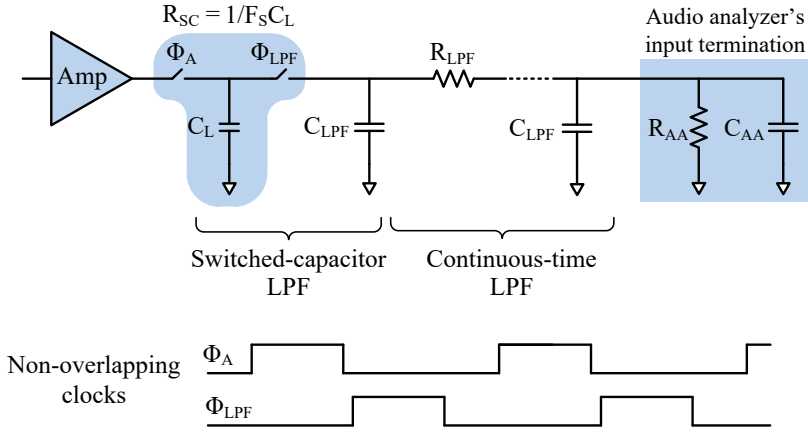

Figure 6.8: Low-pass filter (LPF) design.

linear. Spectrum analyzers are suitable for high-frequency signal measurements but introduce two issues. Firstly, most cannot support measurements over a 100dB dynamic range. Secondly, most use 50Ω input termination, which in this case would require an additional buffer, and hence introduce extra nonlinearity.

The use of an audio analyzer (APx555) eliminates both of these issues since it facilitates high-linearity measurements (<−120dB THD) and employs 100kΩ input termination which is relatively easy to drive. However, it can only measure audio-frequency signals. Therefore, to measure the amplifier's performance with high-frequency inputs, an output chopper is implemented to down-convert higher frequency signals to the audio-band, as will be described later in this section. Moreover, a low-pass filter (LPF) is used to remove high-frequency spurs before taking the output off-chip to measure it with the audio analyzer.

6.4.1 Low-Pass Filter (LPF) Design

At the end of the amplification phase Φ_A, the amplifier's output voltage is sampled on the load capacitors C_L (Figure 6.8). Subsequently, the output signal needs to be taken off-chip for measurement. To facilitate this, the voltages on C_L are re-sampled onto larger capacitors C_{LPF} during an additional clock phase Φ_{LPF}, as shown in Figure 6.8. The circuit effectively behaves like a switched capacitor (SC) low-pass filter with a cut-off frequency given by:

$$f_{\mathrm{SC,-3dB}} = \left(\frac{1}{2\pi}\right) F_S \left(\frac{C_L}{C_{\mathrm{LPF}}}\right), \tag{6.5}$$

where F_S is the operating speed of the clock. For example, if $C_{\mathrm{LPF}} = 125C_L$ and $F_S = 50$MS/s, then the cut-off frequency of the filter becomes $f_{\mathrm{SC,-3dB}} \approx 64$KHz.

The input impedance of the audio analyzer consists of a 100KΩ input termination resistor (R_{AA}) in parallel with a 100pF capacitor (C_{AA}). Due to the resistive part R_{AA} of the termination, there could be considerable signal attenuation if the design being tested is not sized appropriately to drive the audio analyzer. This becomes evident by recognizing that the switched capacitor C_L is equivalent to a resistor $R_{\mathrm{SC}} = 1/(F_S C_L)$. This SC resistor R_{SC} together with the audio analyzer's termination resistor R_{AA} gives a signal attenuation β as follows:

$$\beta = \frac{R_{\mathrm{SC}}}{R_{\mathrm{AA}} + R_{\mathrm{SC}}}. \tag{6.6}$$

If we assume that $C_L = 500$fF and $F_S = 50$MS/s, the equivalent switched capacitor resistor R_{SC} is 40KΩ. Given $R_{\mathrm{AA}} = 100$KΩ, this would lead to a signal loss of approximately 30%. Therefore, the whole design on-chip is sized up ($C_L = 7.6$pF and $C_{\mathrm{DEG}} = 30$pF) to keep the signal attenuation below 5% while maintaining the same amplifier gain and filter bandwidth.

Due to sampling action, the switched capacitor LPF generates images around multiples of the clock frequencies. Any spurs around those frequencies will not be filtered out before going to the audio analyzer. Hence, a continuous-time LPF is used after the switched capacitor LPF (Figure 6.8), resulting in an overall cut-off frequency $f_{\mathrm{-3dB}}$ of 45KHz. It allows measurement up to the 17th harmonic of a 2.5KHz input signal. However, any unwanted signals including noise beyond the $f_{\mathrm{-3dB}}$ frequency are suppressed by the low-pass filter. Although it limits the amplifier's noise measurement, it plays a crucial role in measuring –120dB distortion tones relative to the main signal.

6.4.2 Implemented Circuit Topology

Figure 6.9 shows the half-circuit of the implemented topology along with its timing diagram. All the switches in the signal path are bootstrapped to ensure sufficient linearity. During the sampling phase Φ_S, the input signal is sampled on the sampling capacitor C_S. An

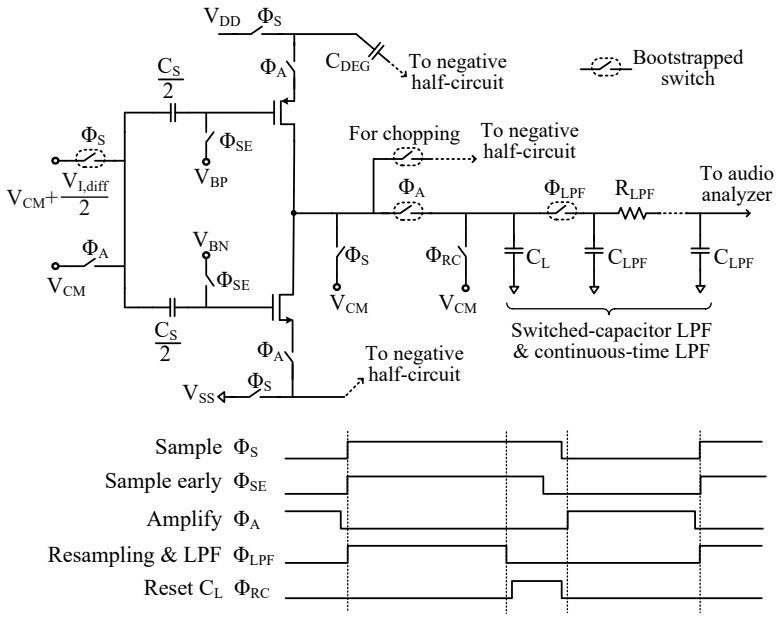

Figure 6.9: Half-circuit of the implemented topology to test the amplifier.

early sampling clock Φ_{SE} is used for bottom plate sampling. Furthermore, the degeneration capacitors C_{DEG} are pre-charged to the supply voltage. The split-capacitor level shifting technique discussed in Section 4.2.1 is also used, which splits the sampling capacitor C_S into two parts to bias the amplifier's NMOS and PMOS transistors independently. As a result, no additional capacitive level shifters are required [21], thus reducing power dissipation and chip area. The amplifier is switched off to save power since it is not used during Φ_S.

During the amplification phase Φ_A, the amplifier is connected to the cross-coupled capacitors C_{DEG}. Simultaneously, the top plates of the input sampling capacitors are tied to the common-mode voltage to pass the signal to the bottom plate side, thus giving an input step to the amplifier. At the end of the amplification, the output signal is captured on the load capacitor C_L. While the input network captures the next data sample, two events occur at the output. First, during Φ_{LPF} the output signal is resampled onto the filter capacitors C_{LPF} and also low-pass filtered. After that, the load capacitors C_L are reset (Φ_{RC}) to their common-mode voltages to remove any inter-symbol interference. During this time, a tunable offset voltage is also added to the C_L capacitors to mitigate circuit imbalance, as described in Section 6.3.4.

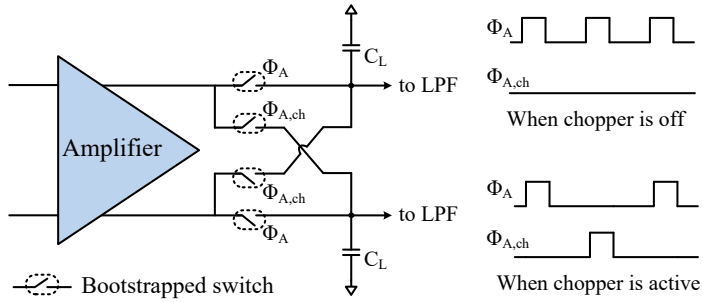

Figure 6.10: Output chopper to measure with near-Nyquist frequency input.

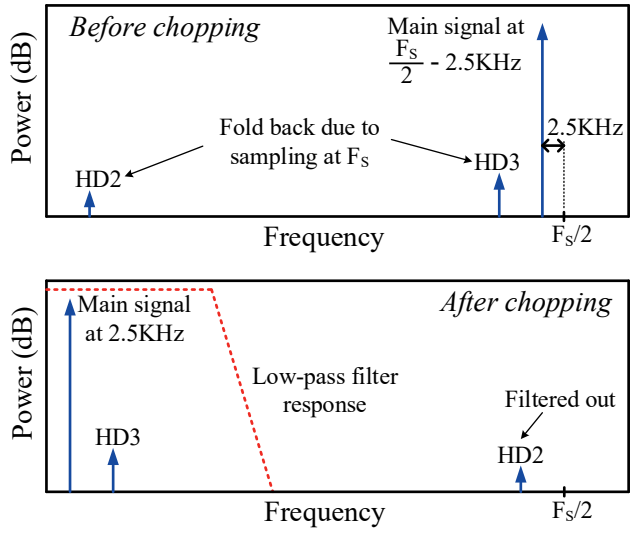

Figure 6.11: Conceptual spectra before and after the output chopping for an input signal close to the Nyquist frequency.

6.4.3 Output Chopper Design

A chopper is implemented at the amplifier's output to facilitate its high-frequency signal measurement, as shown in Figure 6.10. It can be programmed to be either ON or OFF. When the chopper is off, the Φ_A clock runs at the full sampling speed, and the other clock $\Phi_{A,\text{ch}}$ becomes inactive to disable the chopping switches. However, when the chopper turns on, both the clocks Φ_A and $\Phi_{A,\text{ch}}$ operate at half the sampling speed. The input signal is applied close to the Nyquist frequency ($F_S/2 - 2.5\text{KHz}$). Since there is no chopping at the input, the

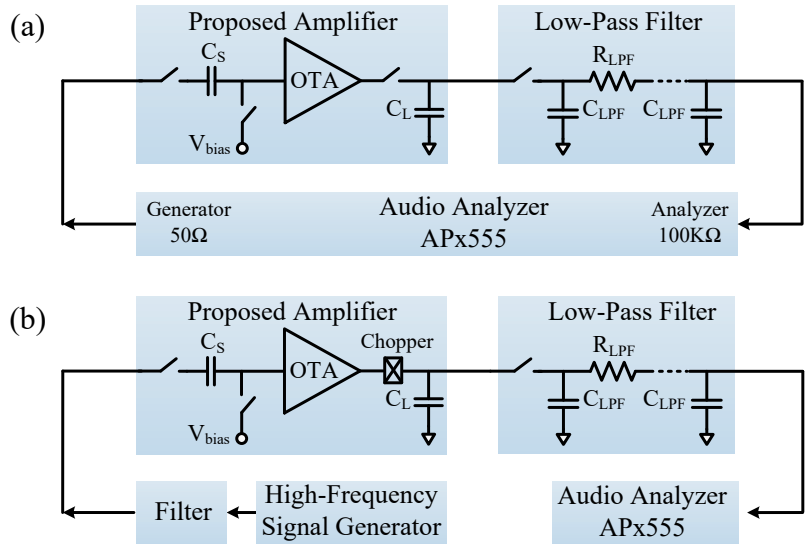

Figure 6.12: Measurement setups for (a) low-frequency and (b) near-Nyquist frequency input.

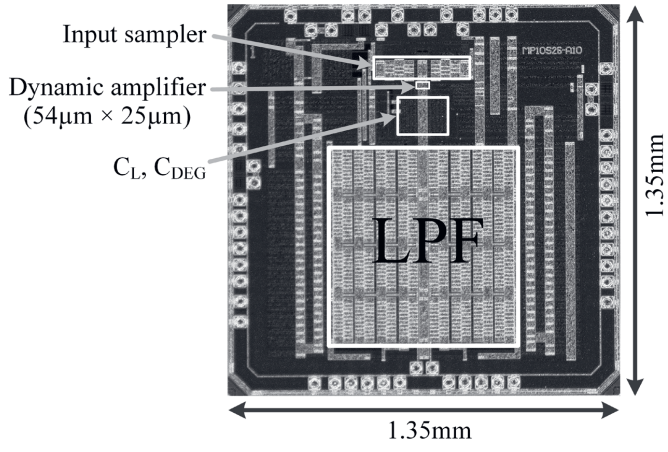

Figure 6.13: Chip photograph.

amplifier's high-frequency signal performance is truly captured. The signal is only down-sampled to the audio band (2.5KHz) after the output chopping. As a result, it can pass through the filter and be measured by the audio analyzer. The drawback, however, is that the even-order harmonic distortion tones will be near the Nyquist frequency after the chopping (Figure 6.11). Hence, they are filtered out by the LPF and cannot be measured.

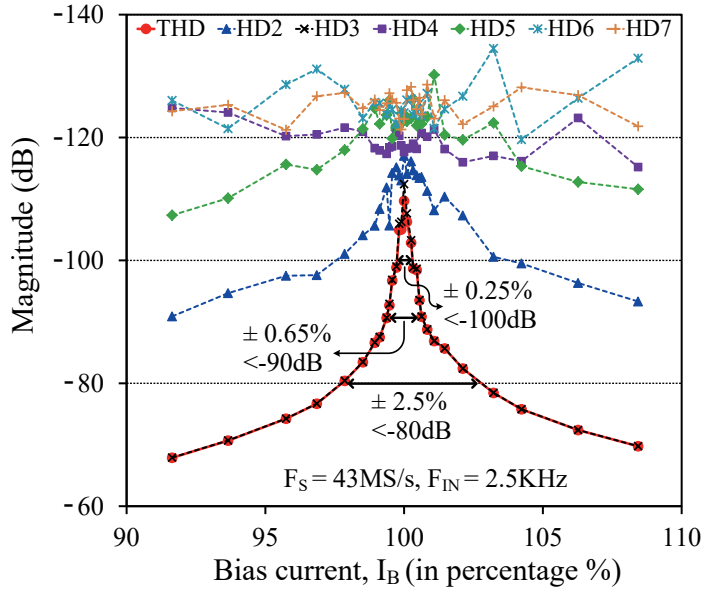

Figure 6.14: Measured THD and harmonics as a function of bias current (as a percentage).

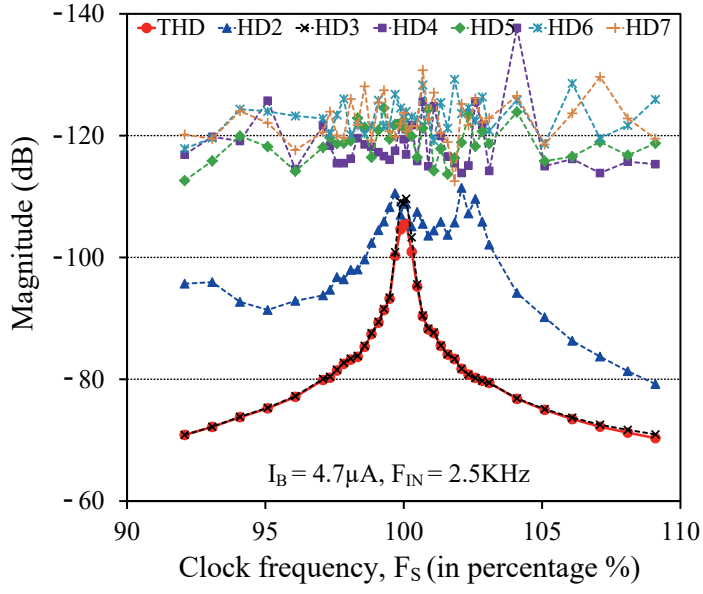

Figure 6.15: Measured THD and harmonics as a function of clock frequency (as a percentage).

6.5 Measurement Results

Figure 6.12 shows the setup used for low-frequency and near-Nyquist frequency signal measurements. The high-precision signal generator of the audio analyzer was used for measurements with audio frequency input signals. To measure with near-Nyquist input frequencies, a high-frequency signal generator was used. It was followed by an off-chip band-pass filter to remove harmonic tones. For this measurement, the chopper was enabled to bring the signal in the audio band, as explained in Section 6.4.3. The prototype design was fabricated in a 28nm digital CMOS process. The area occupied by the proposed amplifier is approximately 0.0014mm^2. A die photo of the chip is shown in Figure 6.13.

Unless otherwise stated, all the measurements were performed at a clock speed of 43MS/s with a 100mV$_{pp\text{-}diff}$ input signal and ~4× gain. Figure 6.14 shows the amplifier's linearity when its bias current I_B, i.e. the calibration knob, was varied. The THD was limited by HD3, as expected, with an optimum of −108dB. Note that the shape, as well as the measured THD, is very close to the simulated curve (Figure 3.18). Even with ±2.5% bias current I_B variation, the THD remained better than −80dB, showing the wide linear range of the proposed amplifier.

Although the bias current was used as the calibration knob in this design, the clock frequency F_S could also be adjusted to calibrate the amplifier's nonlinearity (if allowed by the system), as shown in Figure 6.15. Figure 6.16 shows the linearity measurements for five chips. For both low (Figure 6.16(a)) and near-Nyquist (Figure 6.16(b)) frequency input signals, the amplifier achieves around −100dB HD3. The measured output spectra corresponding to the optimum linearity settings are shown in Figure 6.17. Intermodulation tones between the desired signal and the supply (50Hz) appear around the main tone at multiples of the supply frequency. The proof-of-concept amplifier consumes 87µA from a 1V supply. This low power is partly attributed to the fact that the proposed amplifier does not require any additional CMFB circuits, verified through measuring a well-performing amplifier. The clock circuitry consumes 230µW while the rest dissipates 39µW.

The sampling speed F_S of the amplifier was varied from 20MS/s to 150MS/s with an input amplitude of 100mV$_{pp\text{-}diff}$. For each of these F_S, the bias current was adjusted to calibrate the linearity, as shown in Figure 6.18. Over the entire clock frequency range, the amplifier achieved an HD3 of better than −100dB.

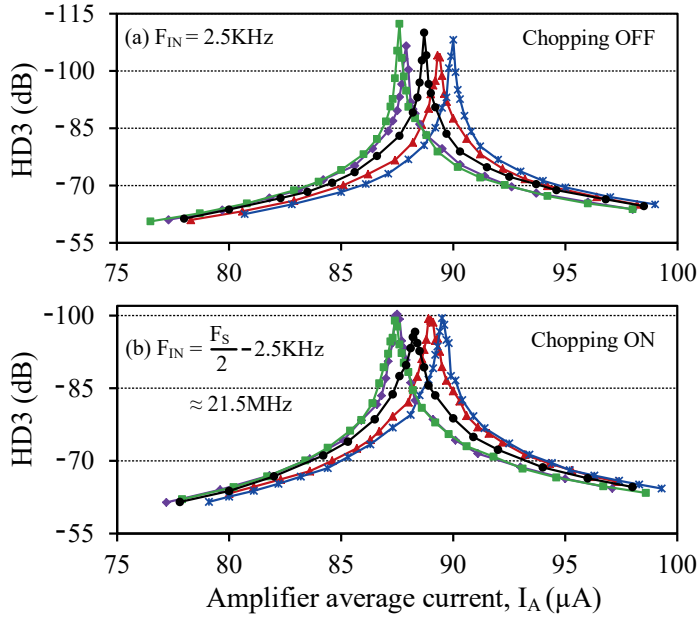

Figure 6.16: Measured HD3 for five chips with (a) low and (b) near-Nyquist frequency input signals.

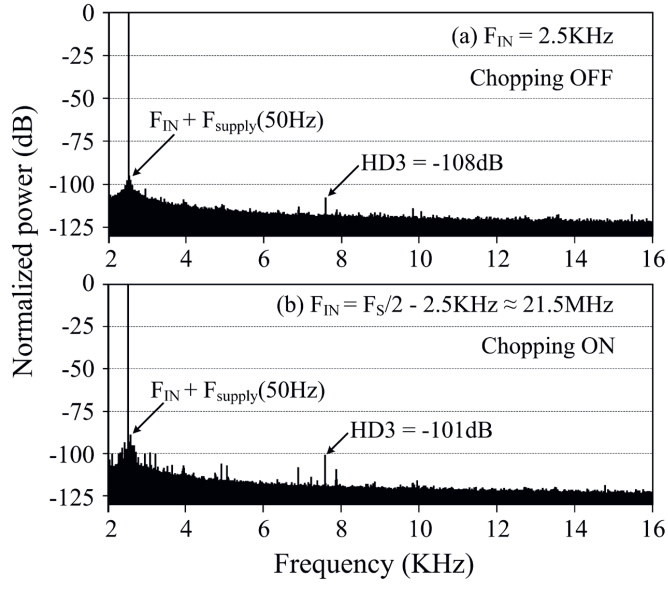

Figure 6.17: Measured output spectra with (a) low and (b) near-Nyquist frequency input signals.

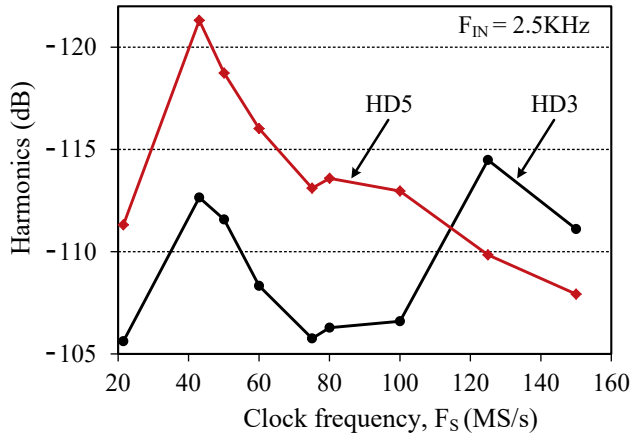

Figure 6.18: Measured linearity performance at clock frequencies between 20MS/s and 150MS/s.

Figure 6.19 shows the measurement over temperatures from −40°C to 125°C with a near-Nyquist input signal. For this measurement, the amplifier was calibrated once at room temperature of 25°C. Over the entire temperature range, it maintained an HD3 of better than −77dB. Recalibrating the amplifier at different temperatures improved the HD3 to about −100dB. Note that the linearity spread over temperature can be reduced if the amplifier uses a PTAT bias circuit.

The amplifier's input amplitude was swept from 50-200$mV_{pp\text{-}diff}$ with a ~4× gain at both low and near-Nyquist input frequencies, as shown in Figure 6.20(a). With a one-time calibration at the 100$mV_{pp\text{-}diff}$ input, the amplifier exhibited better than −86dB HD3 over the entire amplitude range. The degradation in linearity at higher signal amplitudes was due to the amplifier's nonlinear output impedance. It should be noted that the amplifier's performance remains almost the same irrespective of the signal amplitude chosen for calibration.

To show this, a higher input amplitude, 200$mV_{pp\text{-}diff}$, is chosen to calibrate the amplifier (Figure 6.20(b)). Optimizing for linearity at a higher signal amplitude means that the *expanding input-nonlinearity* has to compensate for the *compressing output-nonlinearity*. Consequently, the HD3 improved to −97dB at 200$mV_{pp\text{-}diff}$. However, since the amplifier was not re-optimized at smaller amplitudes, its HD3 was degraded to −92dB at 125$mV_{pp\text{-}diff}$ input. Hence, the worst-case linearity over the entire amplitude range stays similar to the previous case.

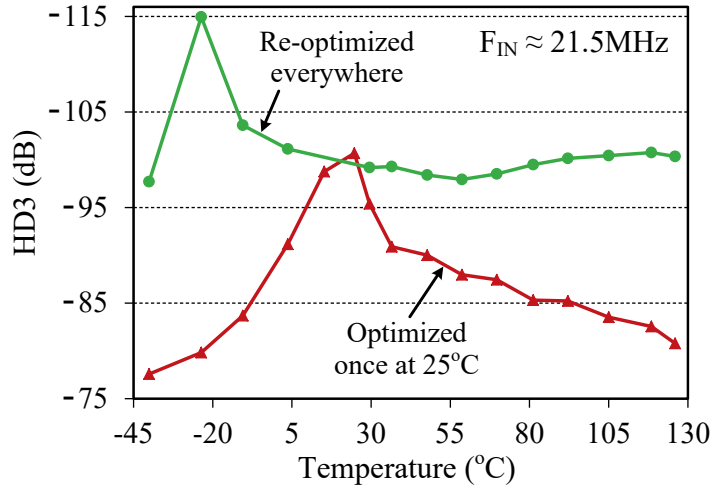

Figure 6.19: Measured amplifier linearity over the temperature range -40°C to 125°C.

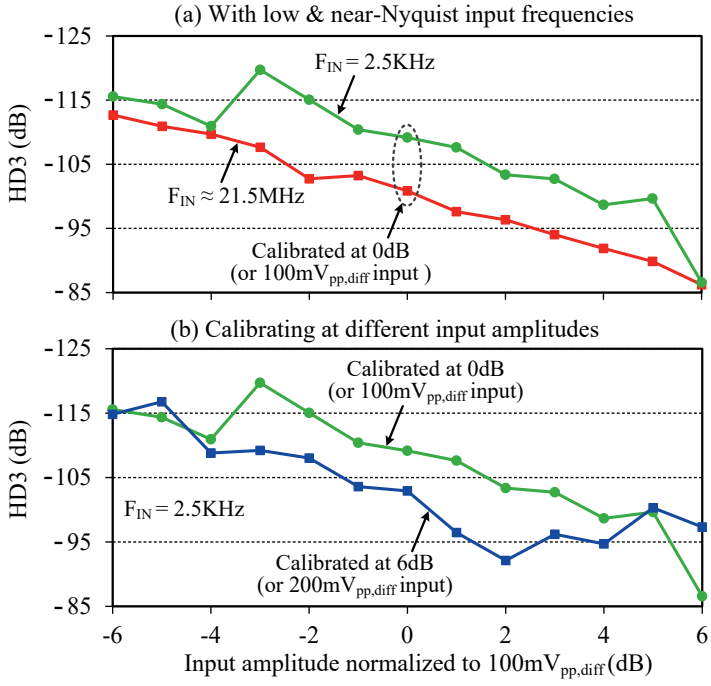

Figure 6.20: Measured amplitude sweeps (a) at two input frequencies, and (b) while calibrating at two different signal amplitudes.

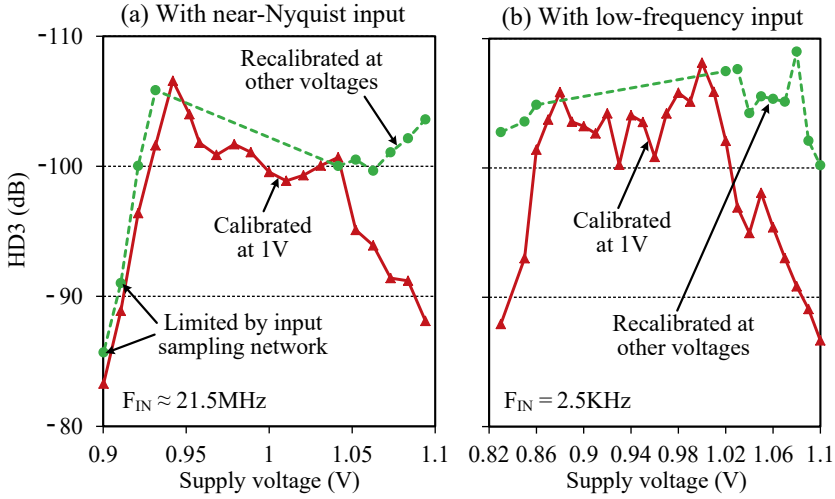

Figure 6.21: Supply sweep measurements at (a) near-Nyquist and (b) low-frequency input signals.

The supply voltage of the amplifier was varied from 0.9V to 1.1V with a near-Nyquist input, as shown in Figure 6.21(a). With a single calibration at a 1V supply, the amplifier exhibited better than −83dB HD3 over the entire supply range. Calibrating the amplifier at different supply voltages improved the HD3 to −100dB except when the supply voltage dropped below 0.93V. This degradation was due to the nonlinearity of the input sampling network since the signal acquisition occurred at near-Nyquist frequencies. However, when the supply sweep (0.83V to 1.1V) was performed with a low-frequency input signal, as shown in Figure 6.21(b), the sampling network was no longer limiting the linearity. Consequently, the amplifier exhibited better than −100dB of HD3, even with a supply voltage of 0.83V after recalibration.

Table 6.1 shows a comparison of this design with other high-linearity amplifiers. Compared to [16]–[18], [20], [23], the proposed amplifier requires at least 10× less energy per cycle to drive per unit capacitor. It achieves either similar or better SFDR than the rest despite supporting the largest relative output signal swing (V_{out}/V_{DD}). Moreover, even without continuous calibration, the amplifier is quite robust to supply voltage and temperature variations (THD < −77dB). Compared to previously published open-loop amplifiers [2]–[5], the proposed amplifier with the CDL technique demonstrates 25dB better linearity while supporting two times larger output signal swing.

Table 6.1: Performance summary and comparison table.

	[16]	[17]	[18]	[20]	[23]	This design	
Technology	0.25µm	0.18µm	65nm	90nm	28nm	28nm	
Clock speed F_S (MS/s)	100	60	90	100	16	43	
Load capacitor C_L (pF)	4	6**	7.5	2	0.913	7.6	
Amplifier power P_{Amp} (µW)	12500	27400	14700	5760†	41	87	96
Normalized power $P_{Amp\text{-}N} = P_{Amp}/C_L$ (µW/pF)	3125	4566	1960	2880	45	11.5	12.6
Supply voltage V_{DD} (V)	2.5	1.6	-	1.2	1.8	1	
Output signal V_{out} ($V_{pp,diff}$)	1.8	1	1.6	0.6	0.45	0.4	0.8
Relative signal swing V_{out}/V_{DD}	0.72	0.63	-	0.5	0.25	0.4	0.8
SFDR at Nyquist (dB)	80	84*	63	85*	99.2	101	86
Energy per cycle P_{Amp}/F_S (pJ)	125	456	163	57.6	2.6	2	2.2
Normalized energy per cycle $P_{Amp\text{-}N}/F_S$ (J/F)	31.2	76	21.7	28.8	2.8	0.27	0.29

*ADC SFDR **ADC input capacitance †Estimated from simulation
Note that P_{Amp} is the power of a single amplifier.

Note that the proposed CDL and floating supply techniques have recently been adopted in various publications [26]–[35]. For instance, [26], [34] described pipelined-SAR ADCs with floating supply based residue amplifiers, demonstrating excellent power efficiency. In fact, [34] achieved the best Walden figure-of-merits for over 12-bit ENOB ADCs and exhibited a consistent performance and power scaling over 100× clock speed range. [26], [27] presented techniques to enhance the robustness of the capacitive linearization technique. Amplifiers with floating supply are also used in residue integrators of noise-shaping SAR ADCs [30], [33], [35] to enhance performance. Moreover, these are being used as pre-amplifiers in comparator circuits, demonstrating 7× better energy efficiency compared to a typical strong-arm latch [28], [31], [35].

6.6 Conclusion

A switched-capacitor amplifier topology is presented utilizing two novel circuit concepts. First is the use of capacitive degeneration technique to ensure excellent linearity for integrating amplifiers. Second is the floating supply technique that can boost the amplifier's CM performance. The proposed dynamic amplifier combines these techniques by implementing a cross-coupled capacitor structure. It exhibits high CM rejection capability and requires no dedicated CMFB circuits, thus saving power and area. Nonlinearity is minimized by adjusting the amplifier's bias current to the appropriate level, with negligible power overhead. Fabricated in a 28nm CMOS process, the proof-of-concept amplifier demonstrates 100dB linearity up to a 150MS/s sampling speed. It achieves 25dB better linearity than previously published open-loop amplifiers. Despite exhibiting linearity similar to state-of-the-art high-linearity amplifiers, the proposed amplifier improves the energy per cycle by a factor of 10.

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7

Conclusion

This work primarily focuses on the development of power-efficient discrete-time amplifiers for data converters. This chapter summarizes its main contributions and provides an outlook for possible future work.

7.1 Primary Contributions

The main contributions of this research are summarized as follows:

- An efficient technique for actively driving a push-pull amplifier is presented [1]–[2] (Section 4.2.1). This typically requires a dedicated switched-capacitor level shifter to drive its NMOS and PMOS inputs. However, this can also be done with the existing sampling and feedback capacitors. This is accomplished by splitting these capacitors in half and then using them to store the level-shifting voltages required for the NMOS and PMOS inputs. Due to its simplicity and power efficiency, this technique is used in both the closed-loop inverter amplifier of Chapter 4 and the open-loop dynamic amplifier of Chapter 6.
- The benefits of the proposed level shifter over a typical level shifter (with additional switched capacitors C_{LS}) are quantitatively analyzed in Section 4.2.1 and Appendix A. It is shown that the proposed solution eliminates the drawbacks of extra noise, signal attenuation, and bandwidth reduction due to additional level shifting capacitors C_{LS}. This results in considerable power (~ 60%) and area reduction.

- The use of incomplete settling to reduce amplifier power dissipation is analyzed (Section 2.3). To maintain the same gain, it can be combined with a larger steady-state closed-loop gain, which also improves the ADC's noise performance.
- An efficient calibration scheme is used for the proposed push-pull inverter amplifier [1]–[2] (Sections 2.4 and 4.4). It employs a simple analog knob to adjust amplifier gain by tuning its bias current. In this way, only the error detection needs to be performed in the digital domain (using the split-ADC technique). Thus, the power required for calibration is minimized.
- A resistive linearization technique [3] is presented for open-loop amplifiers in Section 3.4 and Chapter 5. It employs mild resistive degeneration to counteract the exponential *V–I* characteristic of a transistor. It is shown that by using a specific relationship between the input transconductance and the source degeneration resistance, a significant reduction (~50×) in the amplifier's third-order distortion can be achieved. This technique is used in tandem with foreground calibration to enhance robustness over process spread and mismatch. It is experimentally validated in a prototype amplifier exhibiting < -80dB HD3 [4], a significant linearity improvement compared to most open-loop amplifiers.
- In this research, the concept of a "floating supply" is introduced for discrete-time amplifiers [5]–[7] (Section 6.2). Instead of using a standard supply voltage V_{DD}, the amplifier uses a precharged capacitor as a local supply. Since this capacitor is floating during the amplification period (i.e. not connected to the supply or ground), common-mode currents could not flow to the output. Hence, the amplifier exhibits high CM rejection and does not require a CMFB circuit, saving considerable power and area. Due to these benefits, this technique has already been adopted in numerous works in the literature [8]–[18].
- A novel linearization principle is proposed in this work for open-loop or integrating amplifiers [5]–[7] (Section 3.5). It utilizes capacitive degeneration and the exponential *V–I* characteristic of MOSFETs in the weak-inversion saturation region. It enables open-loop amplifiers to exhibit high linearity (>60dB) without any digital assistance. However, using it with a digital error detection loop can significantly improve linearity (>100dB).
- A detailed mathematical analysis is conducted to validate this capacitively degenerated linearization (CDL) technique (Section 3.5.2). It confirms that the

amplifier can, in theory, achieve perfect linearity by merely adjusting its biasing current. In practical circuits, the proposed technique can eliminate all odd-order harmonics, while the even-order ones can be mitigated by differential operation.

- A power-efficient dynamic amplifier topology is proposed in Chapter 6 (Figure 6.3). It combines the CDL and floating supply techniques by configuring the supply capacitors C_{DEG} in a differentially cross-coupled manner [5]–[7], as shown in Section 6.2.3. Doing so allows these capacitors to serve as a local supply as well as degeneration elements. It also reduces the capacitor size by 4×, saving considerable area. The proof-of-concept amplifier [5]–[7], implemented in a 28nm CMOS process, exhibits better than –100dB THD, the first-ever dynamic amplifier to achieve such low distortion. It also demonstrates excellent power efficiency, requiring 10× less energy per cycle than the state-of-the-art high-linearity amplifier [12].

7.2 Future Recommendations

Below are some recommendations for possible future work:

- The prototype amplifier of Chapter 6 used metal-oxide-metal (MOM) capacitors as its floating supply. This ensures that the degeneration is not signal-dependent because MOM capacitors do not depend on the voltage across it. However, they occupy a significant portion of the amplifier's area. As an alternative, MOS capacitors can be employed to reduce this area. Since these capacitors operate near the supply voltage, MOS capacitors will exhibit a higher capacitor density than MOM capacitors and occupy considerably less area. Moreover, the nonlinearity incurred by MOS capacitors should be low because the voltage across these does not vary significantly during amplification. Further investigation is needed to validate this point.
- The proposed dynamic amplifier with the CDL technique (Figure 6.3) degenerates the transconductance g_m by around 1.5× to optimize linearity. To remove this drawback, the dynamic amplifier topology of Figure 7.1 can be considered. It employs degeneration for only common-mode signals, hence does not degenerate the transconductance g_m. However, this amplifier would exhibit

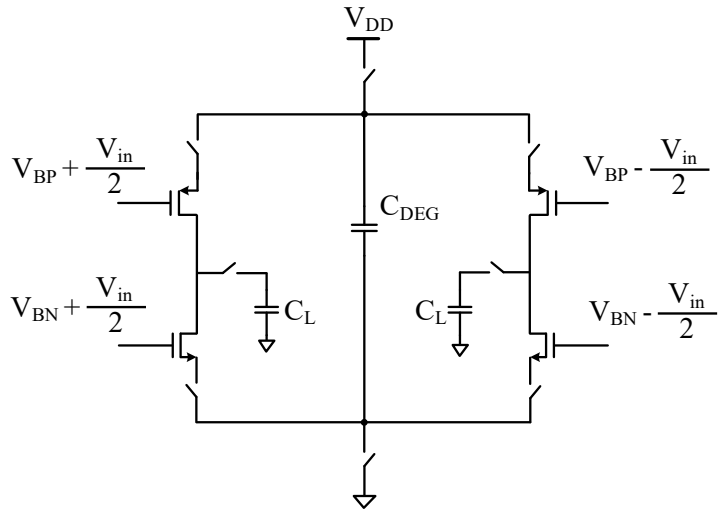

Figure 7.1: Push-pull dynamic amplifier with only common-mode degeneration.

more nonlinearity than the proposed amplifier. Further research should provide more insight into this amplifier topology.

- The resistively degenerated amplifier of Chapter 5 employs load resistors and operates as a continuous-time amplifier. These load resistors could be replaced with switched-capacitors to use this amplifier as a ResAmp in an ADC. Other possibilities should also be explored to utilize this RDL technique for circuits such as filters, programmable gain amplifiers, and LNAs.
- To accommodate higher operating speeds, care should be taken to minimize the mismatch between the two sampling paths of the split-capacitor network (Figure 4.3). This will ensure that the signals captured on the two sampling capacitors are as similar as possible. Furthermore, clock paths should be optimized to reduce timing jitter, which would impact noise performance at higher speeds. Additionally, implementing an on-chip reference buffer could be beneficial because delivering charge at high rates from off-chip circuits is challenging due to the presence of bond wire inductances and large parasitic capacitances.
- Further research is required to improve the supply noise immunity of the proposed amplifiers, which may become essential for higher resolution systems. The supply ripple can be reduced either by employing an on-chip LDO or a large supply

capacitor, costing power and area. The floating supply technique can help mitigate this drawback because the amplifier is not connected to the supply during amplification. The only supply connection is when the capacitor is pre-charged during the reset phase. Hence, circuit topologies such as a zero-crossing detector [19] or a fast source follower should be investigated that can charge a capacitor with high supply immunity.

7.3 Concluding Remarks

This thesis has discussed the design and implementation of power-efficient amplifiers for data converter systems. Some general analog design techniques are developed during this research, e.g., the split-capacitor level shifter, capacitive linearization, floating supply based amplification, which alleviate significant circuit limitations. The resulted open-loop amplifier combining these techniques has shown 25dB better linearity than prior state-of-the-art dynamic amplifiers. It also demonstrated excellent energy efficiency, requiring 10× less energy per cycle than state-of-the-art high linearity amplifiers.

However, with further research, developments can still be made to improve the power efficiency, robustness, and area consumption of the proposed amplifiers and circuit techniques. Moreover, although the presented techniques in this thesis are mainly developed for residue amplifiers of a pipelined ADC, they can improve the performance of other circuits such as delta-sigma loop integrator, pre-amplifier of a comparator.

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Appendix A

This Appendix discusses the drawbacks of using additional capacitors C_{LS} as level shifters (Figure 4.1(b)). As mentioned in Section 4.2.1, the use of these level-shifting capacitors C_{LS} (i) introduces kT/C noise, (ii) attenuates the input signal, and (iii) reduces the amplifier's feedback factor β. Here, each of these effects will be analyzed and compared with the proposed split-capacitor level shifter (Figure 4.3).

Let us begin by analyzing noise. The level-shifting capacitors C_{LS} sample kT/C noise at the end of the sampling phase Φ_1, similar to the sampling C_S and feedback C_F capacitors (Figure A.1). During the amplification phase Φ_2, these noise sources transfer to the amplifier output. The integrated output noise power, considering sufficient amplifier bandwidth and loop-gain, can be expressed as follows:

$$P_{\text{noise}} = \frac{kT}{C_S}\left(\frac{C_S}{C_F}\right)^2 + \frac{kT}{C_F} + \gamma\frac{kT}{C_L}\left(\frac{1}{\beta}\right) + 2\frac{kT}{C_{\text{LS}}}\left(\frac{1}{2\beta}\right)^2 \tag{A.1}$$

where γ is the noise factor of the MOSFET. The last term in Equation (A.1) is the noise contribution due to the two level-shifting capacitors C_{LS}, where $(1/2\beta)$ represents the gain of each kT/C_{LS} noise source from the NMOS or PMOS gate to the amplifier output. To reduce this noise contribution, the C_{LS} capacitor size must be increased. The proposed split-capacitor technique, however, completely removes this additional noise contribution by eliminating these C_{LS} capacitors (Section 4.2.1).

Next, the input signal must pass through the C_{LS} capacitors to drive the NMOS and PMOS gates. Note that even if an ideal level shifter is used, there is always signal attenuation from the amplifier input (V_{IN}) to the transistor gate (V_G) due to finite C_{GS} capacitance. Therefore, to analyze the effect of additional C_{LS} capacitors, the signal attenuation (α) is

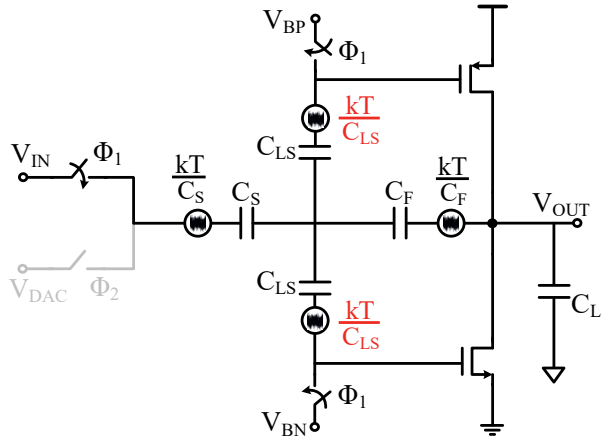


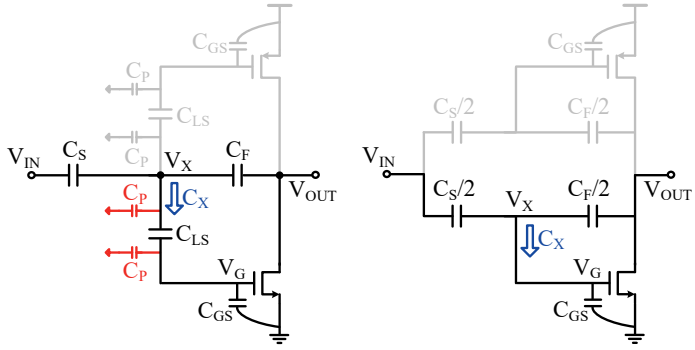
Figure A.1: Additional noise sources due to level-shifting capacitors C_{LS}.

calculated from the virtual ground node (V_X) of the amplifier (Figure A.2(a)) to the transistor gate (V_G) as follows:

$$\alpha = 1 - \frac{V_G}{V_X} = \frac{C_P + C_{GS}}{C_{LS} + C_P + C_{GS}}. \tag{A.2}$$

Here, C_P represents the parasitic capacitance of the level-shifting capacitor C_{LS}. Note that a capacitor C_{LS} cannot be realized on-chip without parasitic capacitors C_P that are a fixed percentage of the value of C_{LS}. Equation (A.2) shows that the signal attenuation α increases for a smaller C_{LS} capacitor because it is in series with the gate-source capacitance C_{GS}. Consequently, the level-shifting capacitor C_{LS} needs to be significantly larger than the gate capacitance C_{GS} to reduce this signal attenuation. It should be noted that there is always a minimum attenuation of $C_P/(C_{LS}+C_P)$ because of the level-shifting capacitors C_{LS}. In contrast, the proposed level shifter (Figure A.2(b)) does not lose signal from the virtual ground node to the transistor gate ($V_G = V_X$) since there is no extra C_{LS} capacitor.

Although increasing the C_{LS} capacitor size reduces noise and signal attenuation, it adds more parasitic capacitance C_P at the virtual ground node (Figure A.2(a)). Thus, the amplifier's feedback factor reduces, degrading its bandwidth and loop-gain. The feedback factor β of the amplifier is given by:



(a) Capacitor level-shifter (b) Proposed solution

Figure A.2: Input signal and feedback factor attenuation for (a) additional capacitor level-shifters C_{LS} and (b) the proposed level-shifting solution.

$$\beta = \frac{C_F}{C_S+C_F+2C_X}, \tag{A.3}$$

where C_X is the equivalent capacitance looking into the level shifters, as shown in Figure A.2. Note that parasitic capacitances from the sampling and feedback capacitors are not considered as they are similar in both cases. For the class-AB amplifier with capacitor level-shifters (Figure A.2(a)), C_X is considerably larger due to the added parasitic capacitance C_P as follows:

$$C_X = \frac{C_{LS}(C_P+C_{GS})}{C_{LS}+C_P+C_{GS}} + C_P. \tag{A.4}$$

The proposed class-AB amplifier, however, exhibits a higher feedback factor β because the capacitance C_X is the same as the amplifier's gate-source capacitance C_{GS}, i.e. $C_X = C_{GS}$ (Figure A.2(b)).

Summary

This thesis describes the design and implementation of power-efficient discrete-time amplifiers for data converter systems.

Chapter 1 presents an introduction to this thesis. It briefly discusses the pipelined ADC architecture and explains the importance of residue amplifiers to its overall power efficiency. While the primary reason for using a residue amplifier is to improve ADC noise performance, a significant power overhead is imposed to meet other design specifications such as gain accuracy and linearity. Hence, the amplifier design ends up far from being noise-limited, which would be the ultimate goal of this research. This chapter presents a design strategy to achieve that goal by (i) innovating analog techniques to mitigate circuit limitations, (ii) developing noise-optimized amplifier topologies, and (iii) leveraging power-efficient calibration schemes.

Chapter 2 discusses the power efficiency in the context of a discrete-time amplifier. It presents guidelines on how different design choices and circuit parameters can influence the amplifier's power dissipation. It is analytically shown that an amplifier becomes more power-efficient with a reduced setting, indicating the high power efficiency of integrating amplifiers. The resulting non-idealities can be addressed by leveraging digital calibration techniques, as discussed in this chapter. Moreover, a mixed-mode calibration approach is proposed to minimize power by combining *digital error-detection* and *analog error-correction* methods.

Chapter 3 provides an overview of amplifier linearization techniques. It describes existing methods to linearize amplifiers that are biased in the strong-inversion saturation region. It is shown that a considerable linearity improvement can be achieved by connecting the common source node of a differential pair to the ground instead of a fixed tail current source. Next, to optimize power efficiency or g_m/I_d, two linearization techniques are

presented based on the MOSFET's weak-inversion operating region. These methods use the exponential *V–I* device-characteristic and some form of degeneration (resistive or capacitive) to ensure high linearity in open-loop or integrating amplifiers. In fact, it is confirmed with detailed mathematical analysis that an integrating amplifier employing this capacitive degeneration technique can, in principle, achieve perfect linearity by merely adjusting its bias current. This is validated with transistor-level simulations, showing the amplifier can indeed achieve extremely high linearity (< –100dB THD). Finally, the viability of this technique is discussed by considering various practical design issues.

Chapter 4 describes the design and implementation of a closed-loop class-AB residue amplifier in a pipelined split-ADC. It consists of a push-pull structure with split-capacitor level shifting to enhance power efficiency. Since the amplifier is inherently quite linear, incomplete settling can be used to save power while still maintaining sufficient linearity. This also allows the amplifier's gain to be corrected by adjusting its bias current. When combined with digital gain-error detection, in this case the split-ADC technique, the result is a power-efficient gain calibration scheme. The prototype pipelined ADC in 40nm CMOS, using this class-AB amplifier, achieves a 66-dB SNDR and 77.3-dB SFDR at 53MS/s. It dissipates 9mW, of which only 0.83mW is consumed in the residue amplifiers.

In Chapter 5, the implementation of an open-loop amplifier using the resistively degenerated linearization technique (RDL) is discussed. It utilizes an exponential *V–I* transistor characteristic together with a weak form of resistive degeneration. This allows the amplifier to achieve high linearity (>80 dB) at the cost of 35% g_m (or power efficiency). This g_m reduction can be traded with more nonlinearity by using the common-mode degeneration technique, which does not degrade g_m but exhibits ~10dB worse linearity. To ensure an optimal linearity over process variation, a foreground calibration scheme is used to detect the nonlinearity. The nonlinearity correction is done by merely adjusting the amplifier's bias current. The proof-of-concept amplifier exhibits an optimal HD3 < –100dB at 50m$V_{pp\text{-}diff}$ input signal. It maintains –80dB HD3 over an input amplitude range of 25-70m$V_{pp\text{-}diff}$, thus exhibiting significantly better linearity than most open-loop amplifiers.

Chapter 6 presents a power-efficient dynamic amplifier for discrete-time systems. It employs the capacitively degenerated linearization (CDL) technique to ensure high linearity performance. This CDL technique is combined with the floating supply technique by configuring the supply capacitors in a differentially cross-coupled manner. As a result, these

capacitors degenerate the amplifier and also serve as its local supply. This configuration also reduces the capacitor area by 4×. Thanks to the floating supply technique, the amplifier exhibits high CM rejection and requires no CMFB circuit, saving power and area. The proof-of-concept amplifier, fabricated in a 28nm CMOS process, demonstrates 100dB linearity up to a 150MS/s sampling speed. It achieves 25dB better linearity than previously published dynamic amplifiers while supporting 2× larger output swing. It dissipates 87μW of power at a clock speed of 43MS/s, thereby improving the energy per cycle by at least 10× compared with that of state-of-the-art high-linearity amplifiers.

Chapter 7 concludes this thesis by summarizing the primary contributions of this research and providing few recommendations for possible future work.

Samenvatting

Dit proefschrift beschrijft het ontwerp en de implementatie van energiezuinige tijd discrete versterkers voor data converter systemen.

Hoofdstuk 1 geeft een inleiding op dit proefschrift. Het bespreekt kort de pipelined ADC-architectuur en legt het belang uit van residu-versterkers voor de algehele energie-efficiëntie. Hoewel de belangrijkste reden voor het gebruik van een residu-versterker het verbeteren van de ADC-ruisprestaties is, wordt er een aanzienlijke vermogensoverhead opgelegd om te voldoen aan andere ontwerpspecificaties zoals versterkings nauwkeurigheid en lineariteit. Het ontwerp van de versterker voldoet niet aan de ruis beperkende eis, wat het uiteindelijke doel van dit onderzoek zou zijn. Dit hoofdstuk presenteert een ontwerpstrategie om dat doel te bereiken door (i) analoge technieken te innoveren om circuit beperkingen te verminderen, (ii) voor ruis geoptimaliseerde versterker topologieën te ontwikkelen, en (iii) gebruik te maken van energie-efficiënte kalibratie schema's.

Hoofdstuk 2 bespreekt de energie-efficiëntie in de context van een discrete-time versterker. Het geeft richtlijnen over hoe verschillende ontwerpkeuzes en circuitparameters de vermogensdissipatie van de versterker kunnen beïnvloeden. Het is analytisch aangetoond dat een versterker energiezuiniger wordt met een lagere instelling, wat wijst op het hoge energierendement van de integrerende versterkers. De resulterende niet-idealiteiten kunnen worden aangepakt door gebruik te maken van digitale kalibratietechnieken, zoals besproken in dit hoofdstuk. Bovendien wordt een mixed-mode kalibratie benadering voorgesteld om het vermogen te minimaliseren door digitale foutdetectie- en analoge foutcorrectie methoden te combineren.

Hoofdstuk 3 geeft een overzicht van versterker linearisatie technieken. Het beschrijft bestaande methoden om versterkers te lineariseren die van invloed zijn in het sterk-inversie-verzadigingsgebied. Het is aangetoond dat een aanzienlijke verbetering van de lineariteit

kan worden bereikt door het gemeenschappelijke bron knooppunt van een differentieel paar met aarde te verbinden, in plaats van een fixed-tail stroombron. Vervolgens worden, om de energie-efficiëntie of gm/Id te optimaliseren, twee linearisatie technieken gepresenteerd op basis van het zwakke-inversie-werkgebied van de MOSFET. Deze methoden gebruiken het exponentiële V–I-apparaatkenmerk en een vorm van degeneratie (resistief of capacitief) om een hoge lineariteit te garanderen in open-lus- of integrerende versterkers. In feite wordt met gedetailleerde wiskundige analyse bevestigd dat een integrerende versterker die deze capacitieve degeneratietechniek toepast, in principe perfecte lineariteit kan bereiken door alleen de biasstroom aan te passen. Dit wordt gevalideerd met simulaties op transistor niveau, waaruit blijkt dat de versterker inderdaad een extreem hoge lineariteit kan bereiken (< –100dB THD). Ten slotte wordt de uitvoerbaarheid van deze techniek besproken aan de hand van verschillende praktische ontwerp scenario's.

Hoofdstuk 4 beschrijft het ontwerp en de implementatie van een klasse-AB residu-versterker met gesloten lus in een pipelined split-ADC. Het bestaat uit een push-pull-structuur met gesplitste condensator niveau verschuiving om de energie-efficiëntie te verbeteren. Aangezien de versterker inherent vrij lineair is, kan onvolledige afwikkeling worden gebruikt om stroom te besparen terwijl toch voldoende lineariteit behouden blijft. Hierdoor kan ook de versterking van de versterker worden gecorrigeerd door de biasstroom aan te passen. In combinatie met digitale gain-error-detectie, in dit geval de split-ADC-techniek, is het resultaat een energiezuinig kalibratieschema. Het prototype pipelined split-ADC in 40nm CMOS bereikt, met behulp van deze klasse-AB-versterker, een 66-dB SNDR en 77,3-dB SFDR bij 53MS/s. Het dissipeert 9 mW, waarvan slechts 0,83 mW wordt verbruikt in de residu-versterkers.

In Hoofdstuk 5 wordt de implementatie van een open-loop versterker met behulp van de resistief-gedegenereerde-linearisatie techniek besproken. Het maakt gebruik van een exponentiële V-I-transistor karakteristiek samen met een zwakke vorm van resistieve degeneratie. Hierdoor kan de versterker een hoge lineariteit (>80 dB) bereiken ten koste van 35% gm (ofwel energie-efficiëntie). Deze gm-reductie kan met meer niet-lineariteit worden veranderd door gebruik te maken van de common-mode degeneratietechniek, die gm niet degradeert maar een ~10dB slechtere lineariteit vertoont. Om een optimale lineariteit ten opzichte van procesvariatie te garanderen, wordt een voorgrond kalibratieschema gebruikt om de niet-lineariteit te detecteren. De niet-lineariteits correctie wordt gedaan door alleen de biasstroom van de versterker aan te passen. De proof-of-concept versterker vertoont een

optimaal HD3 < –100dB bij 50mVpp-diff ingangssignaal. Het handhaaft -80dB HD3 over een ingangsamplitudebereik van 25-70mVpp-diff, waardoor het een aanzienlijk betere lineariteit vertoont dan de meeste open-lus versterkers.

Hoofdstuk 6 presenteert een energiezuinige dynamische versterker voor tijd discrete systemen. Het maakt gebruik van de capacitief-gedegenereerde-linearisatie techniek om hoge lineariteit prestaties te garanderen. Deze techniek wordt gecombineerd met de floating supply-techniek door de voedingscondensatoren differentieel kruis-gekoppeld te configureren. Als gevolg hiervan degenereren deze condensatoren de versterker en dienen ze ook als lokale voeding. Deze configuratie verkleint ook het condensator oppervlak met 4×. Dankzij de floating-supply techniek vertoont de versterker een hoge CM-onderdrukking en vereist geen CMFB-circuit, wat stroom en ruimte bespaart. De proof-of-concept versterker, vervaardigd in een 28nm CMOS-proces, demonstreert 100dB lineariteit tot een bemonsteringssnelheid van 150MS/s. Het bereikt een 25dB betere lineariteit dan eerder gepubliceerde dynamische versterkers, terwijl het ook een 2x grotere output swing ondersteunt. Het dissipeert 87µW aan vermogen bij een kloksnelheid van 43MS/s, waardoor de energie per cyclus met minstens 10× wordt verbeterd in vergelijking met die van de modernste versterkers met hoge lineariteit.

Hoofdstuk 7 besluit dit proefschrift door de belangrijkste bijdragen van dit onderzoek samen te vatten en een paar aanbevelingen te doen voor mogelijk toekomstig werk.

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Shakil
Utrecht, June 2021

List of Publications

Journal papers:

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